

Clock and Timing ICs for Wireline Applications



In Networks and Beyond

Analog Devices, Inc. (ADI), is a global leader in high performance semiconductors for signal processing applications and a leader in integrated circuits for the telecommunications market. ADI offers a wide portfolio to address the needs of integrated clock solutions targeted at critical timing functions. By combining world leadership in data converters and years of expertise in frequency/phase synthesis techniques, ADI's clock generation, synchronization, and distribution ICs offer industry-leading performance and enhanced value to our customers.

- Flexible, integrated designs with critical clocking functions
- Innovative clock ICs that can be used in wired and wireless networks, providing cost efficient solutions for high performance clock generation and distribution
- Wide range of integrated clock products that provide designers with the flexibility needed to satisfy the most demanding clocking requirements

Distribution and Synchronization

Analog Devices leverages its leadership position in high performance wireless clocking applications to provide leading-edge solutions for the wired market. Performance and features found in our network clock products provide high reliability, flexibility, and ease of design to build a cutting edge solution for the next generation of network standards.

Phase synchronization occurs when the phases at the output and at the input are related with a fixed relative phase angle. The most common phase synchronization is when the edge of the output is aligned with the edge of the input clock. Zero-delay functionality allows such phase synchronization and is provided by some Analog Devices products.

Frequency clock synchronization is a basic requirement in the network space and is achieved when the output and the input clock frequencies are related to each other with a fixed translation ratio. If the input drifts, the output also drifts by that translation ratio.

Redundancy

To improve network reliability and stability, some of ADI's clocks support redundancy by managing multiple inputs with priority-based hitless switchover between inputs, as well as providing holdover functionality (maintaining an output clock signal when no input signal is present). These clock ICs support up to Stratum 3/3E applications.

An ADI clock featuring holdover mode is able to provide output signals even when the reference input disappears. This feature allows designers to build systems with greater up-time, alleviating fears of intermittent or unreliable reference signals crashing the system. Holdover can be initiated either as directed by controller/processor elements in a system or via a provided monitoring function that activates the holdover mode when the reference input goes quiet.

An ADI clock featuring switchover capability has multiple reference input ports. If the active references fails, the device uses one of the alternate references instead. An important aspect of all the switchover functions provided in ADI clock devices is that no runt pulses or any extra long pulses result from this change. Downstream PLLs do not lose lock as a result of a clock switchover, even when no predefined relationship exists between the frequencies or phases of the various reference input signals.

Frequency Translation

Analog Devices fractional-N clock ICs can translate between any two standard frequencies with 0 ppm error. Input and output frequencies ranging from 1 pps to >1 GHz are supported. As many as 14 different clock frequencies can be synthesized from a single device, each supporting any of four output logic standards.

ADI clocks support the generation of precise frequency signals required across the full spectrum of network standards. In all cases, the absolute accuracy of the output frequency depends entirely upon the absolute accuracy of the reference frequency. ADI's clock generation devices are essentially a programmable, variable factor (Y) in a multiplication equation, where the reference frequency is the other factor: $F_{OUT} = F_{IN} \times Y$. The key element that differentiates the various levels to which ADI products support frequency translation is how finely the designer can program that variable.

Jitter Cleanup

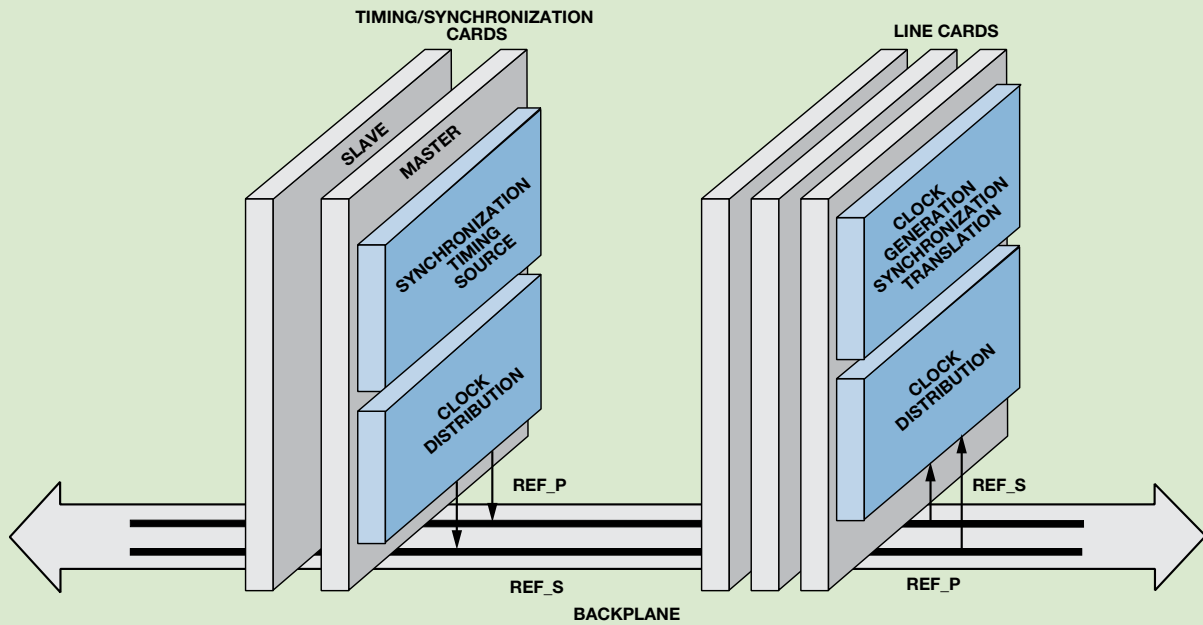
Whether relying on a clock signal routed off a backplane or one accompanying data transmissions, a network reference signal often acquires a substantial amount of noise on its journey through the system. Many ADI clocks are capable of filtering off much of the noise/jitter that exists on the reference input so that the signals are sufficiently clean to meet the jitter levels required by network standards.

Clock generation products are available with jitter generation exceeding the requirements for OC-12 to OC-768, with performance as good as <200 fs rms (integrated from 12 kHz to 20 MHz). For clock distribution, our fanout buffers provide additive jitter as low as 25 fs (12 kHz to 20 MHz). In addition, with programmable loop bandwidths as low as 1 mHz, many of our network clocks provide extreme jitter cleanup.

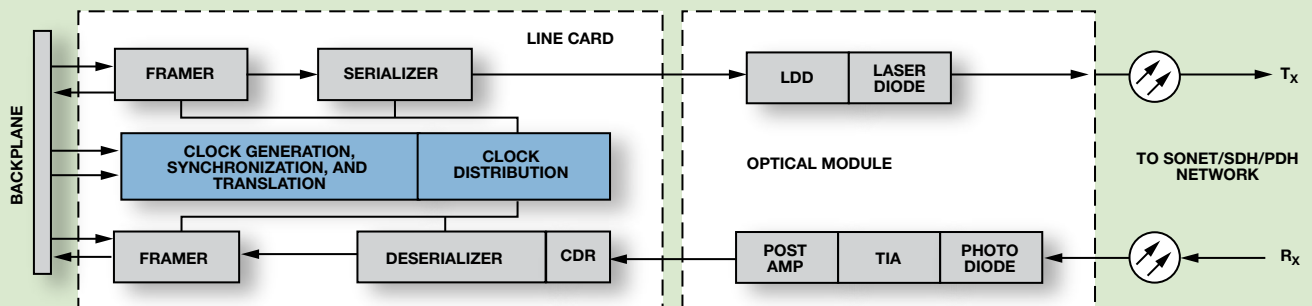
Ease of Use

ADI clock products support the most common standard frequency combinations for SONET/SDH, Gb Ethernet, synchronous Ethernet, GPON/EPON, Fibre Channel, and DOCSIS through pin programming modes. In addition, most of our clock generators include an SPI/I²C port to enhance flexibility. Many of our products include an integrated EEPROM to store customized configurations.

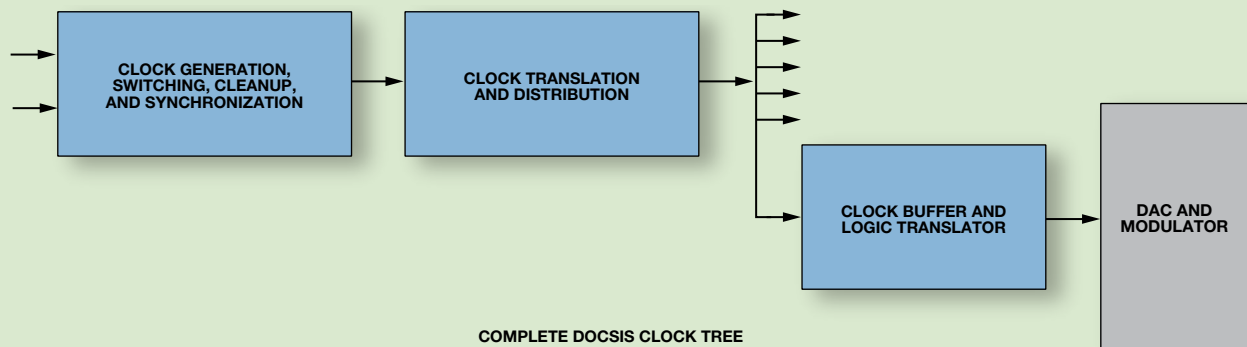
Because clocking requirements vary across wired and wireless networks, ADI offers the appropriate device architectures to support the critical timing functions necessary throughout multiple stages of the clock tree. From network backplane synchronization to localized distribution for clocking data converters, ADI has created flexible, integrated timing solutions targeted for communications systems using industry-leading technology.



ADI CLOCKS ARE USED ON TIMING/SYNCHRONIZATION CARDS AND LINE CARDS.



ADI CLOCKING SOLUTIONS TRANSLATE FREQUENCIES AND CLEAN UP CLOCK SIGNALS THAT HAVE BEEN SENT ACROSS NOISY BACKPLANES. ADI CLOCKS ALSO SUPPORT PRECISE FREQUENCY TRANSLATIONS BETWEEN STANDARDS, INCLUDING STANDARD FEC RATIOS.

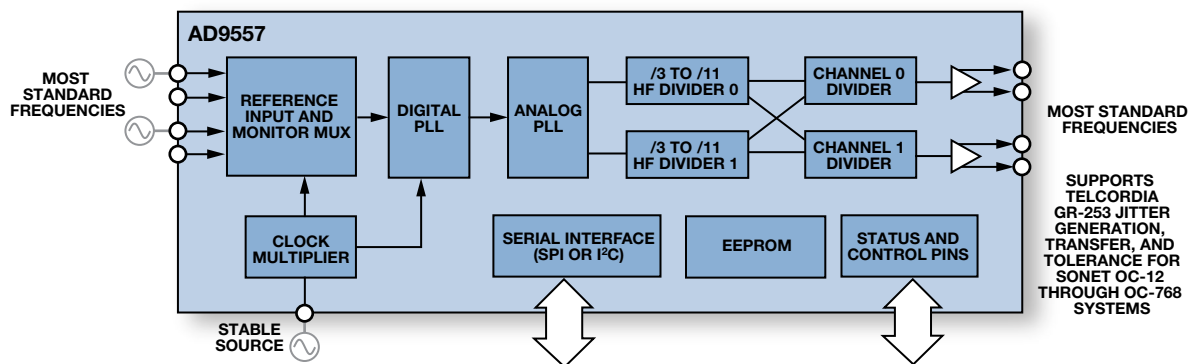


ADI PROVIDES ALL THE NECESSARY CLOCK DEVICES FOR DEVELOPING COMPLETE NETWORK CLOCK TREES.

Network Clock Product Highlights

AD9557/AD9558

The [AD9557/AD9558](#) (the most recent additions to ADI's network clock family) provide jitter cleanup with jitter generation of <0.4 ps rms. They support all major network frequency translations (2 kHz to 1.25 GHz input and 360 kHz to 1.25 GHz output) including those using FEC. The user can fully program either device via its SPI port or select from a group of predefined configurations via pin strapping. The performance and versatility of the [AD9557/AD9558](#) provide a cost competitive solution to traditional PLLs that rely on expensive voltage controlled crystal oscillators (VCXOs). The [AD9557/AD9558](#) satisfy a wide range of high performance wired communications applications, SONET/SDH clocks up to 100 Gbps, synchronous Ethernet, cable infrastructure, wireless base stations, and instrumentation.

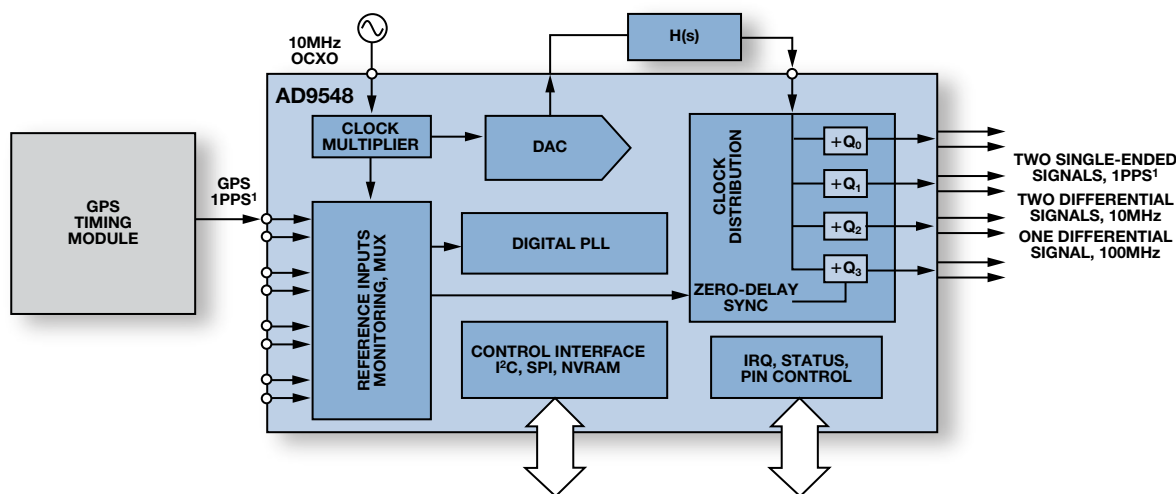


The [AD9557](#) (available in a 6 mm × 6 mm, 40-lead LFCSP package) provides two outputs and two inputs along with switchover and holdover functionality. It includes an integrated EEPROM and a digital loop filter with programmable loop bandwidth from 0.1 Hz to 2 kHz. The [AD9557](#) maps different standards (for example, SDH to OTN or OTN to SDH) by supporting adaptive clock functionality. This feature is vital for applications such as TDM over Ethernet because it allows the user to dynamically vary the output frequency over a ± 100 ppm range in sub 0.1 Hz steps.

The [AD9558](#) (available in a 9 mm × 9 mm, 64-lead LFCSP package) includes the same core features as the [AD9557](#) but with four inputs and six differential outputs (one capable of providing a 2 kHz or 8 kHz frame sync signal).

AD9548

Most 2G, 3G, WiMAX, and LTE base transceiver stations are synchronized to an absolute time reference. In CDMA, for example, synchronization establishes a time offset between base stations, enabling a mobile unit to experience a soft handoff from tower to tower. In many cases, base station time synchronization is achieved by phase locking to a 1 pulse per second signal provided by a GPS receiver. The [AD9548](#) offers an integrated high performance GPS-based synchronization solution by means of its ability to lock to the 1 pulse per second signal from a GPS receiver and generate a stable output signal from 1 Hz to 400 MHz.

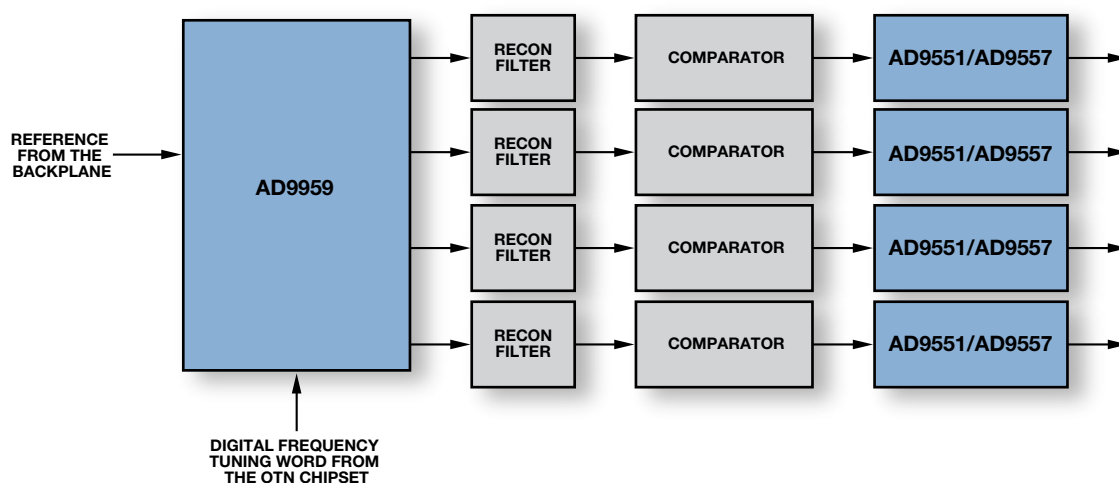


¹EXAMPLE OF A SPECIFIC APPLICATION, BUT THE FREQUENCIES AND THE FORMAT AT THE INPUTS/OUTPUTS ARE FLEXIBLE.

The architecture of the [AD9548](#) all-digital PLL offers unparalleled flexibility and high performance with virtually no part-to-part variation. The device internally samples the time difference between the feedback and reference clock edges. The time samples pass through a digital loop filter that relies on programmable numeric coefficients to establish the loop bandwidth of the digital PLL (from 0.001 Hz to 100 kHz). The numeric output of the digital loop filter is a sequence of frequency tuning words that drives a 48-bit direct digital synthesizer (DDS), which provides frequency resolution that is 3.6×10^{-15} of the internal system clock frequency (that is, 3.6 μ Hz for a 1 GHz system clock). The DAC at the output of the DDS produces a sinusoidal analog signal at a frequency dictated by the frequency tuning words delivered to the DDS from the digital loop filter. The output of the digital PLL drives a clock distribution section to produce the desired outputs. Each of the four output channels is configurable as a single differential (LVDS/LVPECL) or a pair of single-ended (CMOS) outputs, and each channel includes a dedicated programmable frequency divider.

AD9959

The [AD9959](#) (available in a 56-lead LFCSP package) is a 4-channel DDS. It contains four fully integrated 32-bit DDS channels, each supporting independent control of frequency, phase, and amplitude. Because all four DDS channels share a common system clock, they are inherently synchronized, which effectively eliminates mismatches in the output signal that would otherwise appear in a design employing four separate DDS devices. For those applications requiring more than four independent DDS channels, the [AD9959](#) provides the ability to synchronize multiple devices, enabling applications that require many synchronized channels.

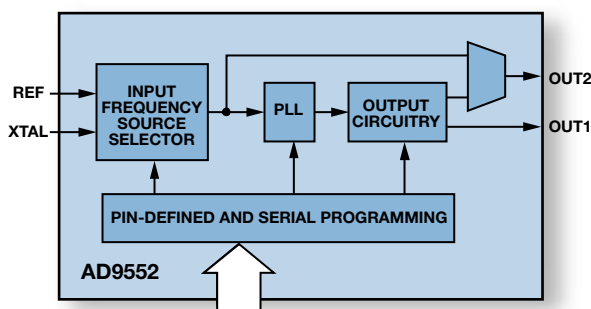


One specific application of the [AD9959](#) is the generation of four independently programmable clock frequencies, all phases related to one another by using comparators to square up the sinusoidal output of the DDS channels. The 32-bit DDS architecture of the [AD9959](#) provides frequency resolution that is 2.3×10^{10} ppm of the internal system clock frequency (that is, 0.023 Hz for a 100 MHz system clock).

AD9552/AD9553

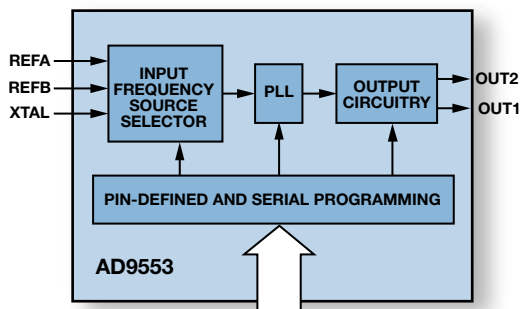
Oscillators are used in a wide variety of applications but can be expensive, especially at high frequencies and for applications requiring temperature stability. They also tend to be among the least reliable components in a system. Furthermore, oscillators that provide nonstandard frequencies usually come at a premium and typically have long lead times. Few alternatives exist for generating nonstandard clock frequencies with low noise and high stability.

The AD9552 fractional-N PLL is one alternative that supports frequency translations of up to 800 MHz with very fine tuning resolution and allows system designers to use a standard low frequency crystal to produce a high frequency output clock signal. Users can program the output frequency via an SPI port or select a predefined frequency translation via pin strapping. The AD9552 can also provide a buffered copy of the applied reference input clock, enabling multiple AD9552 devices to generate multiple frequencies from a single oscillator.



AD9552

- Fractional-N PLL
- High performance
- VCXO replacement



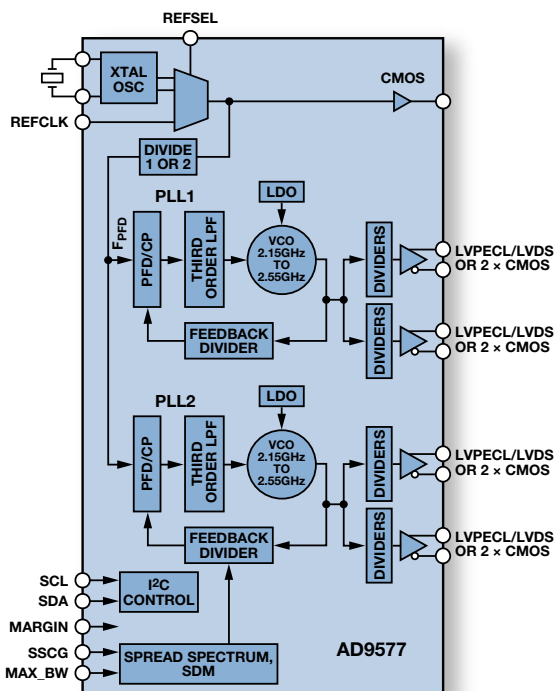
AD9553

- Integer-N PLL
- Cost-effective solution
- GPON and base station applications

The AD9553 integer-N PLL is another cost-effective alternative supporting input frequencies as low as 8 kHz. It is a viable solution for many network applications, especially GPON. Users can program the output frequency via an SPI port or select a predefined frequency translation via pin strapping.

AD9577

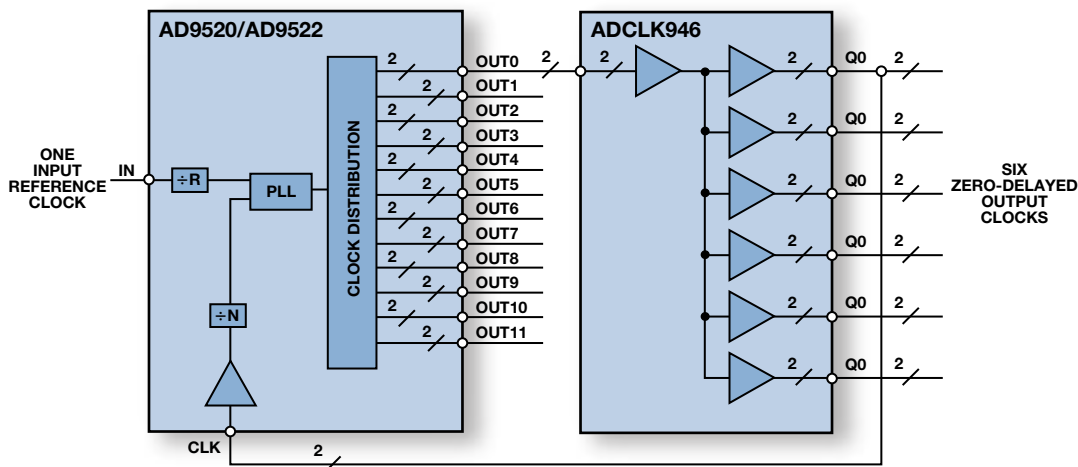
The AD9577 (available in a 6 mm × 6 mm, 40-lead LFCSP package) is a multioutput clock generator with two parallel PLL cores. The first PLL is an integer-N design optimized for extremely low jitter (0.4 ps rms, 12 kHz to 20 MHz), while the second PLL is configurable as either integer-N with 0.4 ps rms jitter (12 kHz to 20 MHz) or fractional-N with 0.9 ps rms jitter (12 kHz to 20 MHz). The second PLL also features spread spectrum capability for PCIe applications, and both PLLs provide a clock frequency margining pin.



Each PLL provides two differential output drivers with each driver configurable as a pair of single-ended CMOS outputs. Furthermore, a dedicated CMOS output provides a buffered copy of the input reference clock. The [AD9577](#) reference clock input operates from 19.44 MHz to 27 MHz and supports either a single-ended CMOS driver or direct connection of a crystal resonator. The [AD9577](#) is fuse programmable, making it an attractive candidate for high volume applications. The [AD9577](#) complements the [AD9557/AD9558](#) in line card designs requiring clock cleanup and frequency plans for both SONET/SDH and synchronous Ethernet.

AD9520/AD9522

Some applications require edge timing alignment between the input and output clock signals. The [AD9520/AD9522](#) family of clock generators has a PLL with a zero-delay architecture, which is the solution for such applications (an explanation of zero delay appears in the AN-0983 Application Note). The output channels of these clock generators have a programmable delay stage, making it possible to generate multiple zero-delay clocks that are edge aligned to within ± 60 ps. Applications requiring more than the 12 differential (24 single-ended) outputs from the [AD9520/AD9522](#) are possible by using fanout buffers from ADI's ADCLK buffer family.



ADCLK9xx

Analog Devices provides the industry's best performing buffers in terms of phase noise, jitter and timing skew, frequency range, and power efficiency. The buffer family includes 4.8 GHz LVPECL and 1.2 GHz LVDS/CMOS drivers targeting high speed, low jitter, low power applications. Broadband additive jitter is as low as 75 fs for the fanout buffers with LVPECL drivers and 100 fs for those with LVDS/CMOS drivers. The excellent jitter performance makes ADI clock buffers the perfect choice in ADC and/or DAC clock signal chains to maximize SNR performance. The [ADCLK9xx](#) clock buffer family exhibits only 9 ps of edge timing skew between output channels. These buffers accept a wide variety of single-ended and differential logic levels, including LVPECL, LVDS, HSTL, CML, and CMOS. Power consumption is as low as 12 mW per LVDS channel at 100 MHz operation and 34 mW per LVPECL channel. With up to 12 output channels, ADI clock buffers are not only cost-effective but also simplify the design of high speed signal chains.

Clock Fanout Buffers and Dividers

Part Number	Number of Inputs/ Outputs	Input/Output Logics		Toggle Rate (GHz)	RMS Jitter (ps)	Typ Output to Output Skew (ps)	Division
		Input	Output				
AD9512/AD9513/ AD9514/AD9515	1 to 2 ¹ /3 ¹ /5 ¹	Differential	LVDS/CMOS	800 MHz LVDS/250 MHz CMOS	0.3	—	Yes (32 bits)
ADCLK905/ADCLK907	1 to 1, Dual 1 to 1	Differential	LVPECL	7.5	0.06	—	No
ADCLK925	1 to 2	Differential	LVPECL	7.5	0.06	9	No
ADCLK944	1 to 4	Differential	LVPECL	7	0.05	9	No
ADCLK946/ADCLK948/ ADCLK950/ADCLK954	1 or 2 to 6/8/10/12	LVPECL/CML/ CMOS/LVDS	LVPECL	4.8	0.075	9	No
ADCLK914	1 to 1	LVPECL/CML/ CMOS/LVTTL/LVDS	HVDS	7.5	0.11	—	No
ADCLK846/ADCLK854	1 or 2 to 6 ¹ /8 ¹	LVPECL/LVDS/ HSTL/CML/CMOS	LVDS/CMOS	1.2 GHz LVDS/250 MHz CMOS	0.1	65	No
ADN4670	1 or 2 to 10	Differential	LVDS	1.1	0.1	30	No

¹ Some differential channels can be configured as single-ended CMOS outputs, increasing the total number of output channels.

Network Clock Products Supported by ADI

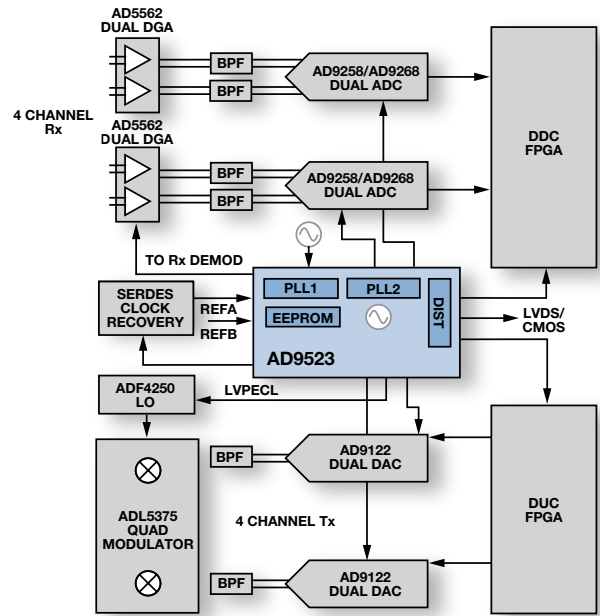
Part Number	Control	Redundancy		Input Frequency (MHz)	Output Frequency (MHz)	Loop Bandwidth for Jitter Cleanup	Typical RMS Jitter (12 kHz to 20 MHz)	Distribution			Comments
		Holdover	Switchover					# of Inputs	# of Outputs	Output Format	
AD9510/AD9511	SPI	None	None	0.008 to 250	1600	Adjustable (external loop filter)	Depends on external VCXO	2	8/5	LVPECL/LVDS/CMOS	
AD9516/AD9517/AD9518	SPI	Yes	Hitless	0.008 to 250	1600	Adjustable (external loop filter)	0.4 ps to 0.7 ps	2	10 ¹ /8 ¹ /6	LVPECL/LVDS/CMOS	10G Ethernet, FC, SONET line cards
AD9520/AD9522	I ² C or SPI	Yes	Hitless	0.008 to 250	1600/800	Adjustable (external loop filter)	0.36 ps to 0.7 ps	2	12/12 ¹	LVPECL/LVDS/CMOS	10G Ethernet, FC, SONET line cards
AD9523/AD9524	I ² C or SPI	Yes	Hitless	0.3 to 400	<1 to 1000	10 Hz to 100 kHz	0.169 ps	2	14/6	LVPECL/LVDS/CMOS	
AD9548	SPI, I ² C, or pin	Yes, Stratum 2	Hitless and build out	1 pps to 750	1 pps to 450	0.001 Hz to 100 kHz	0.35 ps to 0.7 ps	2 ¹ /4 ¹	2 ¹ /4 ¹	LVPECL/LVDS/CMOS	GPS synchronization, BITS/timing cards
AD9549	SPI or pin	Yes	Hitless and build out	1 pps to 750	1 pps to 450	0.001 Hz to 100 kHz	0.35 ps to 0.7 ps	2 ¹ /4 ¹	2 ¹ /4 ¹	HSTL/CMOS	
AD9550	Pin	None	None	0.008 to 200	0.008 to 200	400 Hz	1 ps to 1.3 ps	2	2	LVPECL/LVDS/CMOS	
AD9551	SPI or pin	Yes	Build out	104 to 806	10 to 900	180 Hz	0.8 ps	2	2 ¹	LVPECL/LVDS/CMOS	Low power fractional-N, 10G Ethernet, FC, SONET line cards
AD9552	SPI or pin	None	None	6.6 to 112.5	10 to 900	None	0.64 ps	2	2 ¹	LVPECL/LVDS/CMOS	Low power fractional-N, 5 mm × 5 mm package
AD9553	SPI or pin	Yes, Stratum 4	Yes	0.008 to 200	0.008 to 810	170 Hz/75 kHz	1 ps to 1.3 ps	2	2 ¹	LVPECL/LVDS/CMOS	
AD9557/AD9558	SPI, I ² C, or pin	Yes, Stratum 3	Phase build out	0.002 to 1250	0.002 to 1250	0.1 Hz/2 kHz	0.4 ps	2/4	2 ¹ /6 ¹	HSTL/LVDS/CMOS	G.812; GR253; G.8262; OC-48 to 768 OTN mapping/demapping
AD9571/AD9572	Pin	None	Phase build out	25	Multiple fixed (including 106.25 MHz, 156.25 MHz, 33.33 MHz, 100 MHz, and 125 MHz)	None	0.4 ps	1	7	LVPECL/LVDS/CMOS	G.812; GR253; G.8262; OC-48 to 768 OTN mapping/demapping
AD9573/AD9575	Pin	None	Phase build out	25	Multiple fixed (including 100 MHz, 125 MHz, 155.25 MHz, 159.375 MHz, 161.13 MHz, and 312.5 MHz)	None	0.4 ps	1	2	LVPECL/LVDS/CMOS	G.812; GR253; G.8262; OC-48 to 768 OTN mapping/demapping
AD9577	I ² C or preset	None	None	19 to 26	13 to 650	None	0.4 ps integer/0.9 ps fractional	1	7/3	LVPECL/LVDS/CMOS	Gigabit Ethernet, FC, four independent frequencies in the 11.2 MHz to 637.5 MHz range, factory preset or I ² C controlled, speed spectrum
AD9599	SPI	None	None	1 to 500	<1 to 200	None	Comparator dependent	1	4	Reconstructed sine wave (DAC)	Used for nondocking applications, too

¹Some differential channels can be configured as single-ended CMOS outputs, increasing the total number of output channels.

ADI's Clock Portfolio—More Than Just Wired Networks

The highly integrated dual PLL architecture of the [AD9523](#) provides a jitter cleaner with 14 channels of clock generation and distribution to meet all the needs of a wireless base station transceiver (the [AD9524](#) is a six output version). The PLL1 relies on an external VCXO to provide jitter cleanup of the remote radio unit reference clock. PLL2 has an integrated VCO that translates the low jitter output of PLL1 to ~3.7 GHz. The output buffer stage adds less than 200 fs (femtoseconds) rms jitter. These integrated blocks enable a complete system clock solution by performing jitter cleanup of the input clock while generating all necessary clocks to drive two dual, 14-bit, 125 MSPS/150 MSPS ADCs ([AD9258](#) or [AD6655](#)), four channels of 14-/16-bit, 1 GSPS DACs ([AD9122](#) or [AD9779](#)), and a pair of FPGAs.

The [AD9523](#) also has the flexibility to provide multiple buffered outputs of PLL1, which can be used as low noise reference sources to other ADI local oscillator PLL devices. The extremely low jitter dividers and buffers in the [AD9523](#) make the device an excellent solution for a variety of 3G/4G base station designs, including LTE, MCGSM, W-CDMA, CDMA2000, and TD-SCDMA. In addition to its superb performance, the [AD9523](#) provides programmable output logic, an integrated EEPROM, and a feature-rich architecture packaged in a small 72-lead LFCSP.



Converter clocks.

State-of-the-Art Power Management Products

Enhance your system's clock performance by using low noise power supplies. ADI offers a broad portfolio of state-of-the-art power management products.

ADP1874/ADP1875

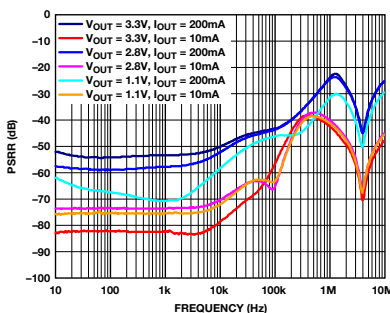
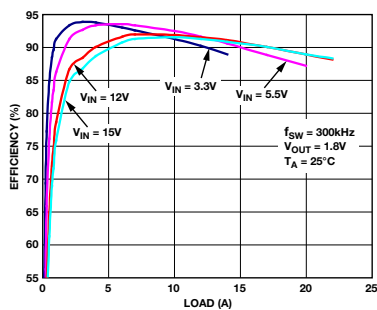
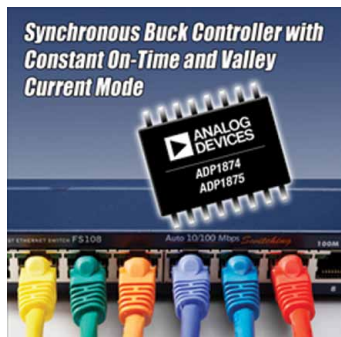
The [ADP1874](#) and [ADP1875](#) synchronous dc-to-dc switching controllers offer versatility, performance, and integration. They provide a simple approach to generating an output as low as 0.6 V from input of 2.75 V to 20 V, along with reliable system power-up sequencing and accurate voltage tracking. Available in the small 6 mm × 5 mm QSOP package, the [ADP1874/ADP1875](#) include an on-board start-up linear regulator and a boot-strap diode for the high-side drive, which are ideal for high density designs. The [ADP1875](#) offers a power-saving mode by skipping pulses and reducing switching losses to improve light load efficiency. Both controllers are suited to operate over a range of output currents, thus allowing system designers to leverage their performance and flexibility over a number of different platforms and designs without requalifying new devices.

ADP1828

The [ADP1828](#) is a synchronous step-down dc-to-dc switching controller offering performance and flexibility. This controller handles a wide input range from 3.0 V to 20 V and is capable of supplying a stable output voltage down to 0.6 V. Available in both 4 mm × 4 mm LFCSP and 20-lead QSOP, the user can program the [ADP1828](#)'s switching frequency via an external resistor from 300 kHz to 600 kHz. Additional features include soft start, voltage tracking, and over- and undervoltage power-good indicators. Users can also configure the [ADP1828](#) for a range of output currents to leverage its performance over a number of different design platforms without requalifying new devices.

ADP151

The [ADP151](#) is a 200 mA low dropout regulator featuring 9 μ V rms output noise at low frequency (10 Hz to 100 kHz). Designed for ultrasensitive noise and micropower applications, the [ADP151](#) operates from 2.2 V to 5.5 V and provides output voltages ranging from 1.2 V to 3.3 V, providing low noise 1.8 V and 3.3 V for the clock products' power supplies. The [ADP151](#) also consumes less than 40 μ A of quiescent current and is available in a 2 mm × 2 mm LFCSP package (DFN). Other packages include an industry-standard SOT-23-5 and a 0.76 mm × 0.76 mm WLCSP.

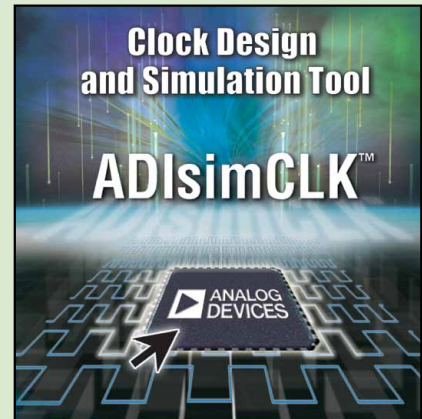


Support Tools and Design Assistance

ADIsimCLK Clock Circuit Design and Simulation Tool

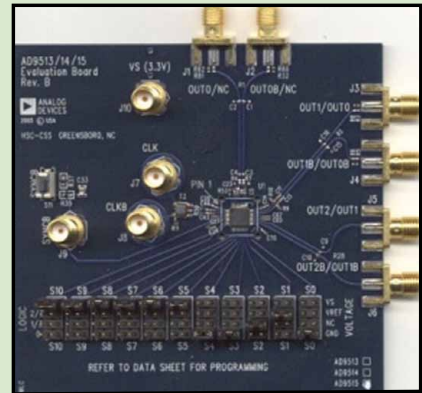
ADIsimCLK™ is the design tool developed specifically for Analog Devices' range of ultralow jitter clock distribution and clock generation products. The ADIsimCLK tool enables designers to observe detailed performance data for a simulated clock distribution design within minutes. Optimization of the clock circuit can be accomplished in this interactive environment with spreadsheet-like simplicity and interactivity.

For a free download of the complete software package, please visit www.analog.com/ADIsimCLK.



Evaluation Board Kits

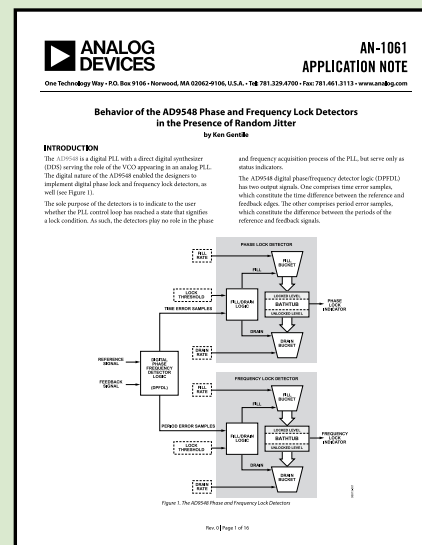
Analog Devices provides a complete range of evaluation boards for its portfolio of clock products. User-friendly software allows our customers to rapidly evaluate the actual performance of our clock ICs and, when the software is used in conjunction with ADIsimCLK, a customer can quickly and accurately design, optimize, and bread-board a new clock, thereby reducing design cycle time and improving time to market. Associated documentation, including schematics, bill of materials, and instruction guides, is available online at www.analog.com/ClockEval.



Application Notes and Technical Papers

- AN-0983 Application Note, *Introduction to Zero-Delay Clock Timing Techniques*. Analog Devices, Inc. (December 2008).
- "Analog-to-Digital Converter Clock Optimization: A Test Engineering Perspective." *Analog Dialogue* (February 2008).

Available at www.analog.com/clocks.



Online Webinars

- Network Clocks: How to Achieve Maximum System Up Time
- Performance Clocks: Demystifying Jitter

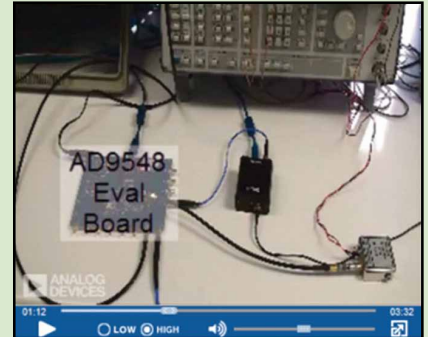
Available at www.analog.com/webcasts.



Online Videos

- [AD9548](#): GPS Clock Synchronization
- [AD9548](#): Evaluation Board Setup
- [AD9548](#): Evaluation Board SW Overview
- [AD9548](#): Profile Designer SW
- [AD9520/AD9522](#) Evaluation Board and SW Setup

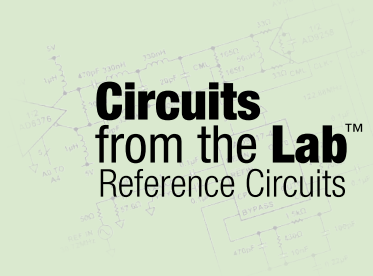
Available at videos.analog.com.



Circuits from the Lab

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. They are modular subsystem designs designed for quick and easy integration into the customer design, are thoroughly documented, and have been built and tested to ensure function and performance. New reference circuits include schematics, bill of materials, and layout files. Evaluation hardware is also available for most new circuits.

Please visit www.analog.com/circuits.



Analog Devices EngineerZone

EngineerZone™ is an online support community for engineers who are using Analog Devices products to ask questions, share knowledge, and search for answers to their design questions. Collaborate with Analog Devices engineers and other designers in this open forum at ez.analog.com.



PC refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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