

# ADSP-2191 16-Bit Fixed-Point DSP

ADSP-218x Code-Compatible,  
Enhanced Peripheral Ports, For Telecommunications

## KEY FEATURES:

- 160 MIPS sustained 16-bit fixed-point DSP performance
- 160 Kbytes of on-chip RAM, configured as 32K words 24-bit RAM and 32K words 16-bit RAM
- User selectable low-power operating modes
- External memory interface configured for 8-bit or 16-bit data bus interface to external SRAM, FLASH, or EPROMs
- Host port with DMA capability for efficient, glueless Host Interface that supports 8- and 16-bit microcontrollers and microprocessors
- Three full-duplex multichannel Serial Ports support H.100 standards, A-law or  $\mu$ -law companding, and T1/E1 compatible devices
- One UART Port with DMA capability
- Two SPI-compatible Ports with DMA capability
- Sixteen general-purpose I/O pins
- Three programmable 32-bit Interval Timers with pulse width counter, PWM generator, and externally clocked timer capability
- Up to 11 DMA channels can be active at any given time for high I/O bandwidth
- IEEE JTAG standard 1149.1 Test Access Port supports in-circuit emulation and system debugging
- 2.5 V internal operation with 3.3 V I/O
- 144-lead LQFP (20 x 20mm) or 144-lead BGA (10 x 10mm) packages

## OVERVIEW

Designed for Telecommunications applications, the ADSP-2191 DSP's on-chip system interfaces support T1, E1, and H.100-based telephony systems. In these systems, the processing power of the ADSP-2191 DSP enables the voice processing needed for high Quality of Service (QoS). At 160 MIPS, the ADSP-2191 doubles the performance of current ADSP-218x models and can double the channel capacity

within an existing PBX or voice gateway chassis. For a complete solution, ITU compliant high-quality speech codecs and robust echo cancellation software algorithms are available for the ADSP-219x series directly through ADI. This allows service providers to rapidly deploy high-quality, cost-effective and scalable next-generation voice convergent platforms.



ADSP-2191 FUNCTIONAL BLOCK DIAGRAM

## ALGORITHMS

Vocoders	Description	Peak MIPS
Voice Coders – (Choice of speech compression algorithms)	G.723.1	18.9
	G.729/A	19.9/10.8
	G.728	29
	G.726	9.7
	G.722	12.9
G.711	0.2	
Auxiliary		
Jitter Buffer	Adaptive	1
Tone Detection System	Voice/Fax/Data	2.5
Echo Cancellation	G.165/G.168	4.5
VAD	Voice Activity Detection	CS
Signal Detection & Generation	Call Progress	CS
	Caller ID	CS
	DTMF	<1
	E&M Signalling	<0.5

CS: Customer specific (Provided on request)

## MEMORY

### Internal Memory

- 32K x 24 words of Program Memory and 32K x 16 words of Data Memory
- Unified Program and Data Memory space for high efficiency compiler
- Dual-purpose Program Memory for dual operand fetches in a single cycle

### External Memory Interface

- Configurable data bus provides an 8- or 16-bit interface to External Memory
- Address translation and data word packing provided to support an 8- or 16-bit External Data Bus
- Adjustable external clock rate allows interface to low cost memory devices

## PERIPHERALS

### Host Port Interface

- 16-bit Host Port that lets External Hosts read from or write to the entire DSP's memory space, boot space, or internal I/O space
- Configurable for 8-bits to provide a glueless interface to low cost microcontrollers

## Serial Ports

- Support for T1/E1/H.100 standards. Support for up to 24-, 32- and 128-channel Time Division Multiplexing
- A-law or  $\mu$ -law companding in accordance with ITU recommendation G.711
- Synchronous serial communications with peripheral devices and other DSPs/MCUs
- Configurable for 3- to 16-bit word lengths

## Serial Peripheral Interface (SPI)

- Two full-duplex SPI ports for communication with multiple SPI-compatible devices
- Integrated DMA master, configurable to support both transmit and receive data streams

## UART

- Full-duplex asynchronous serial data transfer bit rates from 9.5M to 6.25M bits per second

## Timers

- Three 32-bit general-purpose timers
- Individually programmable for generating periodic interrupts
- Pulse Waveform Generation
- Pulse Width Count/Capture
- External Event Watchdog mode

## System Clock Generator and Power Management

- Optional crystal oscillator or clock source inputs
- Programmable PLL supports 1X to 32X frequency multiplication. Enables full-speed operation from low-speed input clocks or crystals
- User selectable idle modes significantly reduces the power dissipation for power constrained applications

## DEVELOPMENT TOOLS

- ADSP-2191 is supported by a complete set of software and hardware development tools including VisualDSP++™, evaluation boards and JTAG emulators.
- VisualDSP++ integrated development and debug environment (IDDE) features a C/C++ compiler, statistical profiling and the new VisualDSP® Kernel (VDK). All designed to make software development faster.
- ADI makes it easier to evaluate the ADSP-2191 for a specific application with the ADSP2191-22 EZ-KIT Lite™ evaluation system. The EZ-KIT Lite includes an ADSP-2191 DSP evaluation board and software.
- JTAG emulators available for PCI, USB and Ethernet host platforms provide easier and more cost-effective methods for engineers to develop and optimize DSP systems, shortening product development cycles for faster time-to-market.

## DSP SUPPORT:

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