

AD927x/AD967x Octal Ultrasound Analog Front End (AFE) Product Family for High Performance Cart-Based and Portable Ultrasound Systems

Ultrasound designs and the associated requirements have evolved over the years to meet increasingly complex diagnostic needs, ranging from routine prenatal care to advanced cardiac imaging. To meet new and varied demands, Analog Devices' AD927x/AD967x family of octal ultrasound receivers offers a range of features and functionality that maximize image quality and performance, while minimizing power dissipation and system cost.

Features and Functionality

CW I/Q Demodulator

Used to measure the speed and direction of blood flow, CW Doppler processing provides physicians and sonographers with a measurement technique to diagnose vascular conditions, such as faulty valves and arteries in the heart. The AD927x/AD967x family offers models that provide CW I/Q demodulation and individual programmable phase rotation supporting exceptional levels of performance while reducing the need for filter components. A CW I/Q demodulator reduces system cost, complexity, and power consumption.

Digital I/Q Demodulator and FIR Decimation Filter

An on-chip digital demodulator and decimator conditions eight channels of data from RF to a baseband frequency, reducing the processing load on the system FPGA (field-programmable gate array).

RF Decimator

An on-chip RF decimator enables the ADC to be oversampled, providing an increased signal-to-noise ratio (SNR) for improved image quality while maintaining a lower data I/O rate to system processors.

JESD204B Serial Interface

Several models in the product family have a 5 Gbps JESD204B data conversion serial interface to support higher data rates and channel counts, while reducing ultrasound system I/O data routing by as much as 80% compared to other data interface standards. The resultant savings addresses the design needs of small, high performance ultrasound systems. The ultrasound equipment board design is simplified while better meeting the industry's demands for higher data rates, larger channel counts, and greater image resolution.



Product Highlights

Low Noise

Excellent input- and output-referred noise enables improved system sensitivity for high performance applications.

Low Power

The power dissipation enables compact designs with a long battery life and low heat dissipation. The portfolio offers several models that support high end systems with small form factors at 130 mW per channel at 12 bits, 40 MSPS, and 50 mW per channel in CW Doppler mode; several models are optimized for portable systems at 85 mW per channel at 12 bits, 40 MSPS, and 25 mW per channel in CW Doppler mode.

Input Options

With active termination, the AD927x/AD967x product family offers the flexibility to design in several different probe types and maintain the dynamic range of the system.

Range of Sample Conversion Rates

The sample conversion rate is dependent on the specific model selected and the 12-bit or 14-bit ADC on chip. Sample conversion rates range from 10 MSPS to 125 MSPS. Several models offer an on-chip RF decimator, enabling oversampling for high frequency probe applications.

Digital Interface

Digital LVDS supports both IEEE and ANSI standards. Double termination allows the user to make longer trace runs supporting digital receivers off board. A data clock output (DCO) operates up to 480 MHz and supports double data rate (DDR) operation. On some models, CML outputs support JESD204B standards, and the embedded clock high speed serial link operates up to 5 Gbps.

User Flexibility

The serial port interface (SPI) allows designers to further customize the noise, gain, and bias for any given imaging mode, probe, or power requirement. By changing SPI registers, designers can optimize an ultrasound signal processing architecture for the best possible noise performance or longest battery life. An easy-to-use software tool simplifies each configuration.

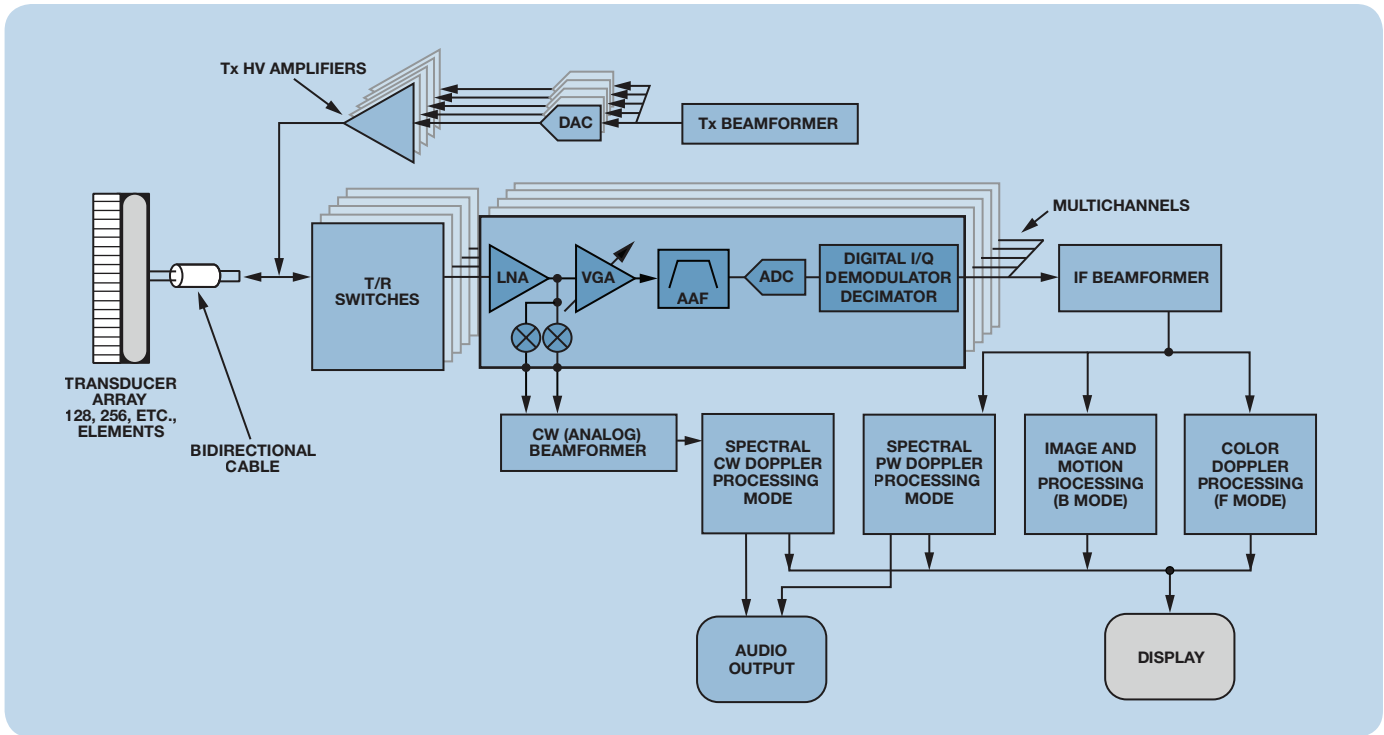
Small Form Factor

Eight channels of full TGC path, analog-to-digital converter, and crosspoint switch or I/Q demodulator are contained within a RoHS-compliant 10 mm × 10 mm, CSP_BGA or 16 mm × 16 mm, TQFP_EP package.

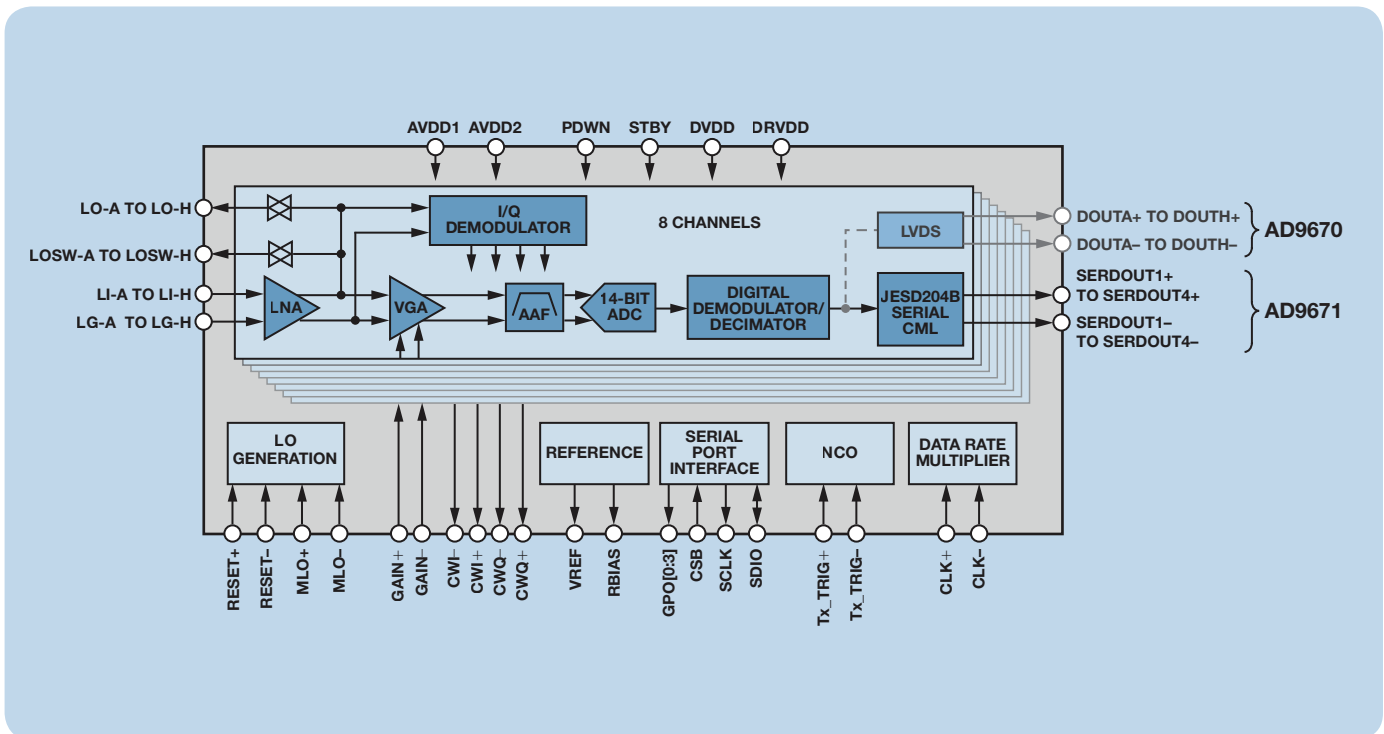
Octal Receivers

Part Number	ADC		Input Referred Noise			Dynamic Range (dBFS/√Hz)			Post-ADC Processing			Digital Serial Interface			Power @ 40 MSPS (mW)	Package ¹
	Number of Bits	MSPS (Max)	LNA (nV/√Hz)	LNA (pA/√Hz)	Total Channel R _s = 50 Ω (nV/√Hz)	TGC Mode Output	CW Mode Input	CW I/Q Demodulator	RF Decimator	Digital I/Q Demodulator	FIR Decimation Filter	JESD204B	IEEE LVDS	ANSI LVDS		
AD9671	14	125	0.75	2.6	0.8	143.6	160	•	•	•	•	•			150	CSP_BGA
AD9670	14	125	0.75	2.6	0.8	143.6	160	•	•	•	•		•	•	150	CSP_BGA
AD9675	14	125	0.75	2.6	0.8	143.6	160	•	•			•			150	CSP_BGA
AD9674	14	125	0.75	2.6	0.8	143.6	160	•	•				•	•	150	CSP_BGA
AD9277	14	50	0.75	1	0.85	140.5	160	•					•	•	193	TQFP_EP
AD9276	12	80	0.75	1	0.85	139.9	160	•					•	•	191	TQFP_EP
AD9279	12	80	0.75	2.5	0.8	141.6	160	•					•	•	130	CSP_BGA
AD9278	12	65	1.26	1.5	1.3	140.8	158	•					•	•	85	CSP_BGA
AD9272	12	80	0.75	1	0.85	139.9	160						•	•	191	TQFP_EP
AD9273	12	50	1.26	1	1.37	137.6	155						•	•	104	TQFP_EP, CSP_BGA

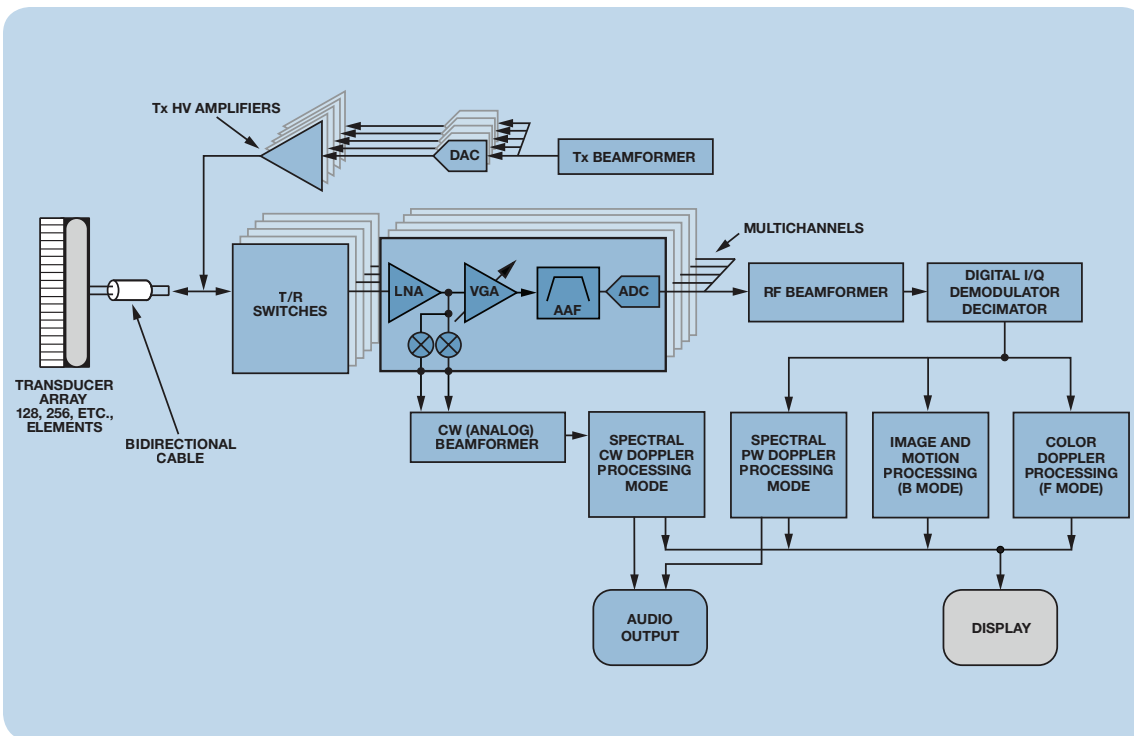
¹ 10 mm × 10 mm CSP_BGA; 16 mm × 16 mm TQFP_EP



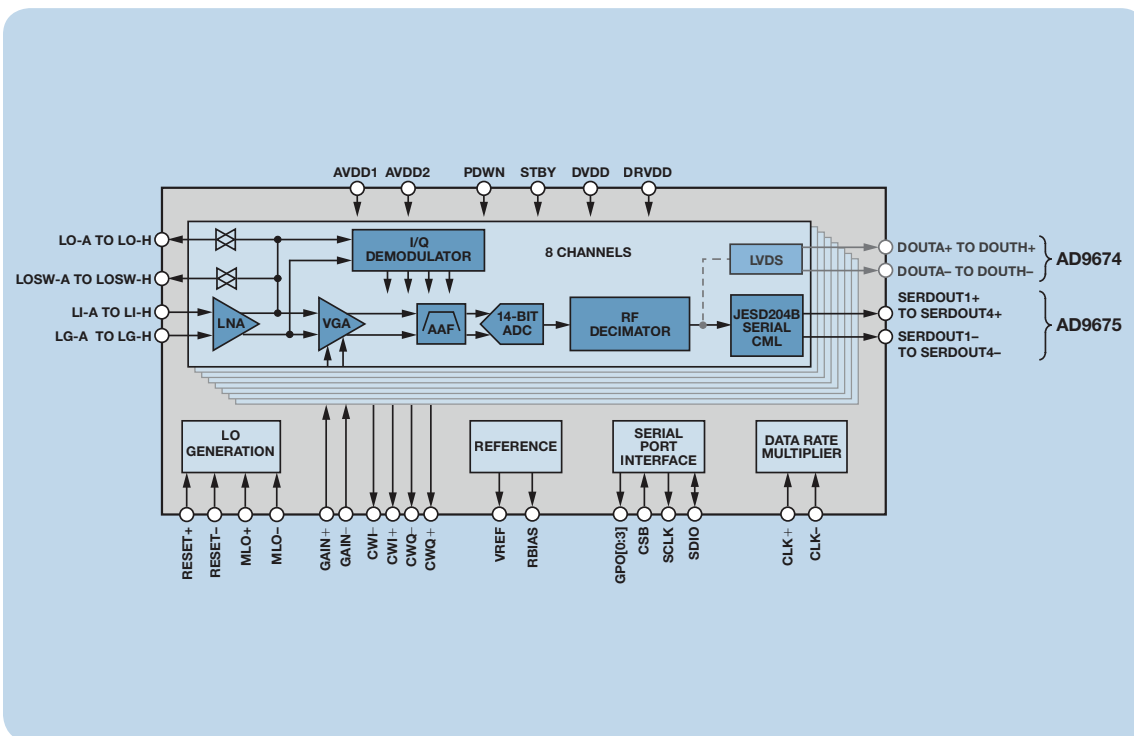
Simplified ultrasound system block diagram utilizing the AD9670/AD9671 offering per channel digital I/Q demodulation and decimation, reduced bandwidth, and IF beamforming.



On-chip CW I/Q demodulator, RF decimator, and FIR decimation filter is available on the AD9670 with LVDS digital serial interface and the AD9671 with JESD204B digital serial interface.



Simplified ultrasound system block diagram utilizing the AD927x and AD967x product family. All models in the family offer eight channels of LNA, VGA, AAF, and 12- or 14-bit ADC.



On-chip CW I/Q demodulator and RF decimator is available on the AD9674 with LVDS digital serial interface and the AD9675 with JESD204B digital serial interface.

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