

600 MHz TigerSHARC Processor: The Performance Density Leader

Key Features

Static Superscalar Architecture
Optimized for High Throughput, Fixed-Point, and Floating-Point Applications

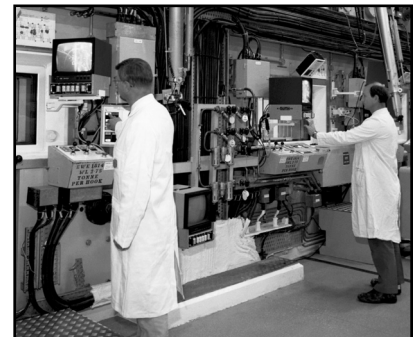
- Eight 16-bit MACs/cycle with 40-bit accumulation
- Two 32-bit MACs/cycle with 80-bit accumulation
- Specific support for Viterbi decoding through the implementation of add-compare-select (ACS) sequencing
- Add-subtract instruction and bit reversal in hardware for FFTs
- IEEE floating-point compatible

Highly Integrated

- Three variants offering 24-Mb, 12-Mb, and 4-Mb on-chip embedded DRAM
- Glueless multiprocessing
- Four link ports—1 GBps transfer rate each
- 64-bit external port, 125 MHz, 1 GBps
- 14 DMA channels

Flexible Programming in Assembly and C Languages

- User-defined partitioning between program and data memory
- 128 general-purpose registers
- Algebraic assembly language syntax
- Optimizing C compiler
- VisualDSP++® tools support
- Single-instruction, multiple-data (SIMD) instructions, or direct-issue capability
- Predicated execution
- Fully interruptible with full computation performance

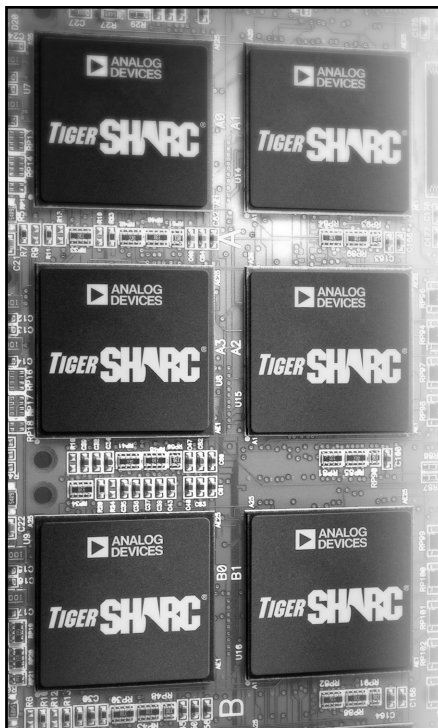


The TigerSHARC static superscalar architecture and instruction set is tailored for multiprocessing applications, especially continuous real-time processing for wireless network infrastructure, medical imaging, radar and sonar, and industrial instrumentation, all with high rate data flow and throughput.

A Breakthrough Architecture

The TigerSHARC® family continues with the ADSP-TS201S, ADSP-TS202S, and ADSP-TS203S. These processors target numerous signal processing applications requiring massive data throughput and provide the industry's highest fixed- and floating-point performance. Applications include, but are not limited to, wireless infrastructure equipment and power-sensitive embedded applications such as military hardware, medical equipment, industrial instrumentation, and software-defined radios.

On one piece of silicon, ADI has combined the 600 MHz TigerSHARC core, 24 Mb of on-chip embedded DRAM, a 14-channel zero-overhead DMA engine, and I/O processing capable of an aggregate throughput of 4 GB. With these features, TigerSHARC offers best-in-class MFLOPS delivered per watt, per dollar, and per square millimeter of silicon area. Equally important, two types of integrated multiprocessing support (link ports and a cluster bus) enable glueless scalability. This means the TigerSHARC Processor will gluelessly scale up to eight devices on the cluster parallel bus with global memory, while link ports will allow for scalability for up to thousands of processors. Furthermore, the link ports provide for a high bandwidth, point-to-point multiprocessing connection that is complementary to the cluster multiprocessing.



Integrated multiprocessing support—consisting of link ports and a cluster bus—provides high bandwidth and point-to-point connections, allowing up to eight TigerSHARC processors on the cluster without the need for bulky glue logic and scalability up to thousands of processors using link ports.

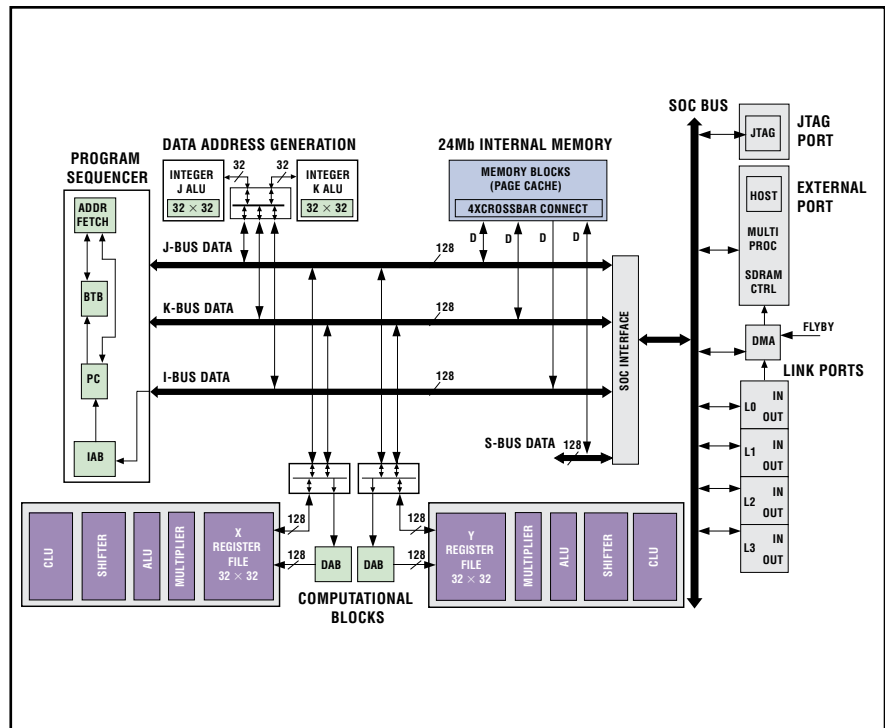
The ADSP-TS201S, ADSP-TS202S, and ADSP-TS203S are pin- and code-compatible and have 24-Mb, 12-Mb, and 4-Mb on-chip embedded DRAM respectively.

TigerSHARC Processors embody a breakthrough architecture that boasts native support of 1-bit, 8-bit, 16-bit, and 32-bit fixed-point and floating-point data types on a single chip. Each of these data types is critical in many of the various applications where TigerSHARC is used. One example of this is in 3G wireless applications. In this case, the support of multiple data types, as well as the enhanced instruction set, enables dynamic sharing of processor bandwidth. This means the chip-rate and symbol-rate tasks found within the 3G baseband signal processing can be accomplished in the TigerSHARC Processor. The soft-transceiver approach to baseband signal processing provides a level of flexibility unmatched by alternative approaches requiring costly external ASIC or FPGA devices. The end result is that OEM manufacturers can offer efficient and flexible solutions using a general-purpose processor while providing significant systems cost reduction.

The glueless scalability of TigerSHARC Processors enables common building blocks and even common design implementations to be used across programs. A complete set of TigerSHARC Processor documentation along with VisualDSP++ integrated development tools is available today, enabling all aspects of processor hardware and software development.

Static Superscalar Architecture

The TigerSHARC Processor architecture blends best practices in microprocessor design to enable the highest performance programmable processor for real-time systems.



The ADSP-TS201S high performance, static superscalar architecture includes an efficient, hierarchical three-level memory and enhanced I/O.

The TigerSHARC Processor employs a static superscalar architecture. It incorporates many aspects of conventional superscalar processors, including a load/store architecture, branch prediction, and a large interlocked register file. Up to four instructions can be executed in parallel in each cycle. The term “static superscalar” is applied because instruction-level parallelism is determined prior to run time and encoded in the program.

It is the instruction parallelism that allows the reduction in overall cycle count required to perform 3G-related functions such as channel decoding, despreading, and path search.

Additionally, the TigerSHARC Processor has the capability of supporting single-instruction, multiple-data (SIMD) operations through the use of both computational blocks in parallel and SIMD-specific computations. The programmer has the option of directing both computation blocks to operate on the same data (broadcast distribution) or different data (merged distribution).

All the registers are interlocked, supporting a simple programming model that is independent of the implementation latencies and is fully interruptible. Branch prediction is supported via a 128-bit entry branch target buffer (BTB) that reduces latency for loops and other types of nonsequential code execution.

Eight MACs/Cycle

There are two computation blocks (processing blocks X and Y) in the ADSP-TS201S architecture, each containing a multiplier, an ALU, and a 64-bit shifter. With the resources in these blocks, it is possible to execute, in a single cycle, eight 40-bit MACs on 16-bit data, two 40-bit MACs on 16-bit complex data, or two 80-bit MACs on 32-bit data. With 8-bit data types, the architecture executes 16 operations per cycle.



TigerSHARC Processor Benchmarks

Peak Rates at 600 MHz		
1-bit performance	153.6 billion MACs/second	
16-bit performance	4.8 billion MACs/second	
32-bit fixed-point performance	1.2 billion MACs/second	
32-bit floating-point performance	3.6 billion floating-point ops (GFLOPS)	
16-Bit Fixed-Point Algorithms	Execution Time at 600 MHz	Clock Cycles
256 point complex FFT (Radix 2)	0.975 μ s	585
FIR filter (per tap)	0.21 ns	0.125
Complex FIR (per tap)	0.83 ns	0.5
32-Bit Floating-Point Algorithms	Execution Time at 600 MHz	Clock Cycles
1024 point complex FFT (Radix 2)	15.64 μ s	9384
$[8 \times 8] \times [8 \times 8]$ matrix multiply	2.33 μ s	1399
FIR filter (per tap)	0.83 ns	0.5
Complex FIR (per tap)	3.33 ns	2

The benchmarks for the TigerSHARC Processor demonstrate its superior performance.

TigerSHARC Processor is a register-based load/store architecture, in which each computation block has access to a fully orthogonal 32-word register file.

Memory Architecture

The ADSP-TS201S features a short-vector memory architecture organized internally in six 128-bit wide banks. Quad (four words, 32 bits each), long (two words, 32 bits each), and normal word accesses move data from the memory banks to the register files for operations. In a given cycle, four 32-bit instruction words can be fetched, and 256 bits of data can be loaded to the register files or stored into memory. Data in 1-bit, 8-bit, 16-bit, and 32-bit words can be stored in contiguous, packed memory. Internal and external memories are organized in a unified memory map. The partition between program and data memory is completely user-determined. The internal memory bandwidth for data and instructions is 38.4 GBps. The arrangement of the memory blocks on the different variants is as follows:

- ADSP-TS201S—6 blocks, 4 Mb each
- ADSP-TS202S—6 blocks, 2 Mb each
- ADSP-TS203S—6 blocks, 1 Mb each

Integrated I/O Capabilities

The ADSP-TS201S integrates many features, including a 64-bit external port, a 14-channel direct memory access (DMA) controller, and four bidirectional link ports, all aimed at providing unparallelized interface capabilities without the use of any additional external glue logic. The 64-bit external port enables the establishment of a cluster bus configuration that may include a host processor, off-chip memory, and other memory-mapped peripherals.

The DMA controller found on the ADSP-TS201S operates independently and invisibly to the processor core, allowing DMA operations to occur while the processor core continues to execute program instructions. In the case of large-scale applications that require clusters of TigerSHARC Processors, the four patented bidirectional link ports permit direct chip-to-chip connections without the need for complex external circuitry.

Instruction Set Summary

The ADSP-TS201S instruction set directly supports all arithmetic types, including signed, unsigned, fractional, and integer data types, and there is optional saturation (clipping) arithmetic for all cases. Specific instructions have also been added to the TigerSHARC Processor core to enable software-based implementations of functions traditionally done in hardware. These include a special complex MAC operation for chip-rate processing and an add-compare-select (ACS) operation for channel decoding algorithms. With these instructions, the ADSP-TS201S provides the performance of an ASIC with the flexibility of a processor for both the symbol-rate and chip-rate processing found in 3G baseband signal processing applications.

CROSSCORE® Development Tools and Third-Party Developers

The TigerSHARC Processor is supported by CROSSCORE®, Analog Devices' wide range of processor software and hardware development tools. The CROSSCORE components include the VisualDSP++ software development environment, EZ-KIT Lite® evaluation systems, and emulators for rapid on-chip debugging.

The TigerSHARC Processor architecture is supported by ADI's third-party network, The Collaborative™. The Collaborative developers help shorten customer time to market by providing products and services such as completely populated TigerSHARC Processor design hardware, algorithms/source code, reference designs, and consultant services. To see a listing of TigerSHARC Processor third-party developers and their product offerings, visit www.analog.com/tigersharc.

Development Can Start Right Away

Accelerate the design and development cycle of wireless base station applications. Available today are processor code generation tools, 3G library software, multiprocessor development boards, and third-party products to help expedite wireless application development and reduce the time it takes to bring products to market.

CROSSCORE

Components include the VisualDSP++ integrated development and debugging environment (IDE), with code generation tools (C++ compiler, assembler, linker, simulator, and debugger), the VDK Real-Time Operating System kernel, statistical profiling, and much more. The EZ-KIT Lite provides developers with a cost-effective method for initial evaluation of ADI processors. Emulators are available for both PCI and USB host platforms.

TigerSHARC EZ-KIT Lite

The ADSP-TS201S EZ-KIT Lite provides developers with a cost-effective method for initial evaluation of the TigerSHARC processor family. The EZ-KIT Lite includes two ADSP-TS201S processors on the desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a USB-based, PC-hosted tool set. With this EZ-KIT Lite, users can learn more about ADI's ADSP-TS201S hardware

and software development and prototype applications. The ADDS-TS201S-EZLITE provides an evaluation suite of the VisualDSP++ development environment with the C/C++ compiler, assembler, and linker. All software tools are designed for use with the EZ-KIT Lite only.

3G Physical Layer Library Software

The TigerSHARC Processor 3G Library contains complete functionality for layer 1 base-band processing. The latest versions of WB-CDMA (3GPP), CDMA2000® (3GPP2), and TD-SCDMA standards are all supported. Functionality is programmed in both C and optimized TigerSHARC assembly with a C interface. Reference designs for IP-based functions are also included.

VHDL/Verilog Link Port Interface Model

The Link Port Interface Model is intended to simplify the FPGA design process when interfacing TigerSHARC link ports to XILINX® or Altera® FPGAs. The model is written in IEEE standard VHDL and is compatible with Virtex-E and Virtex-II family devices.

Multiprocessor System Analysis

A multiprocessor system analysis of TigerSHARC Processor's cluster bus loading and frequency of operation provides guidelines for system implementation. Details include maximum frequency of operation

for an eight TigerSHARC Processor system, including a host and memory along with design, termination, and layout recommendations.

Board Design Schematics

Example schematics illustrate the TigerSHARC Processor connectivity and system implementation for a multiprocessor board.

IBIS Models

I/O buffer information specification (IBIS) models are provided for the ADSP-TS201S as a behavioral model of I/O. This is useful for transmission line simulation of a TigerSHARC Processor digital system. It can be used with various commercially available system simulation packages for signal integrity analysis of TigerSHARC Processor system designs.

Third-Party Products

A number of third-party board-level products, software, and engineering services are available today from industry-leading companies, including

- Bittware
- Enea Embedded Technology
- EZ-DSP
- Navtel
- OSE
- PA Consulting
- SDL
- Transtech DSP Corp.
- Wind River

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str.6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Southeast Asia Headquarters
Analog Devices
22/F One Corporate Avenue
222 Hu Bin Road
Shanghai, 200021
China
Tel: 86.21.5150.3000
Fax: 86.21.5150.3222

Embedded Processing and DSP Support
U.S.A.:
processor.support@analog.com
Fax: 781.461.3010
Europe:
processor.europe@analog.com
Fax: 49.89.76903.157
www.analog.com/processors

