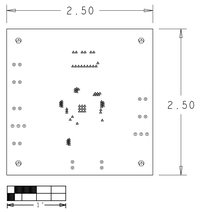
REVISIONS			
REV	DESCRIPTION	APPROVED	DATE
A	INITIAL RELEASE	DM	01/12/15



LAMINATION DIAGRAM

LAYER NUMBER	LAYER NAME	COPPER THICKNESS (OZ./INCH)	DIELECTRIC THICKNESS (in.)	DIELECTRIC MATERIAL
1	TOP	2 OZ./0.0028" MIN		FOIL
			TBD	ISOLA 370HR/EQUIVALENT
2	L2_GND	1 OZ./0.0014"		
			TBD	ISOLA 370HR/EQUIVALENT
3	L3_PWR	1 OZ./0.0014"		
			TBD	ISOLA 370HR/EQUIVALENT
4	BOTTOM	2 OZ./0.0028" MIN		FOIL

THE FINISHED PCB THICKNESS TO BE: 0.062" +/- 0.010"

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY	NOTES
△	12.0	+3.0/-10.0	PLATED	67	
▽	39.37	+3.0/-3.0	PLATED	16	
▽	43.31	+3.0/-3.0	PLATED	6	
▽▽	125.0	+3.0/-3.0	PLATED	4	

NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES (EXCEPT WHERE NOTED).

MATERIAL: (USE CHECKED ITEMS FOR MATERIAL)

2. BOARD MATERIAL:
   (X) ISOLA 370HR OR EQUIVALENT
   ( ) ISOLA-FR408HR OR EQUIVALENT
   ( ) NELCO-4000-13
   ( ) MEGTRON 6
   ( ) ROGERS 4350B
   ( ) ROGERS 4003C
   ( ) OTHER _____
3. THE PCB SHALL BE FABRICATED TO IPC-6012, TYPE X, CLASS 2. WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2, CURRENT REVISIONS.
4. BOARD MATERIAL & CONSTRUCTION SHALL MEET THE REQUIREMENTS OF UL796 WITH FLAMMABILITY RATING OF 94V-0.
5. OVERALL BOARD THICKNESS REFER TO LAMINATION DIAGRAM. TOLERANCE APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES. IT IS TO BE MEASURED FROM TOP PCB METAL TO BOTTOM PCB METAL UNLESS OTHERWISE SPECIFIED.
6. BOW & TWIST NOT TO EXCEED 0.0075 IN. (0.75%) PER LINEAR INCH. BOW & TWIST SHOULD BE MEASURED PER IPC-TM-650, METHOD 2.4.22.

TOOLING: (USE CHECKED ITEMS FOR TOOLING)

7. PHOTO ETCH CIRCUITRY PER ENCLOSED GERBER RS274X OR ODB++ FORMAT FILE. DRILL LOCATION AND SIZE CONTROLLED BY EXCELLON CNC DRILL FILE.
8. IF STATED IN THE LAMINATION DIAGRAM, THE DIELECTRIC THICKNESS OF ANY CONTROLLED IMPEDANCE LAYER IS FOR REFERENCE ONLY. FINAL ACCEPTANCE SHALL BE DETERMINED BY THESE LAYERS HAVING A CHARACTERISTIC IMPEDANCE OF +/-10% OHMS AS STATED IN THE LAMINATION DIAGRAM. THE VENDOR CAN MAKE ADJUSTMENTS AS LONG AS THE STATED IMPEDANCE AND OVERALL BOARD THICKNESS IS MAINTAINED. ANY ADJUSTMENT MADE TO TRACE WIDTH OR SPACING MUST HAVE PRIOR WRITTEN APPROVAL FROM MAXIM.
9. ALL TRACES FILLETED OPTION TO ENHANCE RELIABILITY AT PAD JUNCTIONS WHERE SPACING PERMITS, UNLESS OTHERWISE SPECIFIED:
   ( ) FILLETED
   (X) NOT FILLETED
10. LAYER TO LAYER REGISTRATIONS SHALL BE WITHIN .003 INCHES. LEGEND TO LEGEND +/- 0.007 INCHES

FINISH: (USE CHECKED ITEMS FOR PLATING)

11. FINISHED COPPER WEIGHT/THICKNESS:
   (X) REFER TO LAMINATION DIAGRAM FOR FINISHED COPPER WEIGHT/THICKNESS REQUIREMENTS. THE STARTING COPPER WEIGHT/THICKNESS CAN VARY AS LONG AS THE FINISHED COPPER WEIGHT/THICKNESS IS NOT LESS THAN THE SPECIFIED VALUE, UNLESS OTHERWISE SPECIFIED.
   ( ) OTHER _____
12. CHECK ALL THAT APPLY
   ( ) ELECTRODEPOSITED HARD GOLD PLATE, TYPE 1 (99.7% MIN GOLD), GRADE C (KNOOP HARDNESS 130-200), CLASS 1 (50-100 MICRO INCHES THICK) IN ACCORDANCE WITH MIL-G-45204C. GENERAL SURFACING REQUIREMENTS MUST MEET ANSI/IPC-A-600(CURRENT REV) SECTION 4.0, CLASS 3 (50-100 MICROINCHES THICK) OVER ELECTRODEPOSITED NICKEL PLATE IN ACCORDANCE WITH ANSI/IPC-A-600D, SECTION 4.0, CLASS 3 (200-600 MICROINCHES THICK).
   (X) FINISH CONDUCTOR SURFACES: IMMERSION GOLD, 3-8 MICRO INCHES OVER 100 MICRO INCHES MINIMUM OF ELECTROLESS NICKEL.
   ( ) FINISH CONDUCTOR SURFACES: IMMERSION GOLD, 2-5 MICRO INCHES OVER 118-236 MICRO INCHES MINIMUM OF ELECTROLESS NICKEL.
   ( ) FINGERS TO BE GOLD PLATED.
   ( ) LEAD FREE AND RoHS COMPLIANT PLATING.
   ( ) OTHER _____
13. DRILL SIZES ARE FINISHED HOLE SIZES. ALL HOLES SHALL BE LOCATED WITHIN .005 DTP. MINIMUM BARREL PLATING OF .001 IN. PLATED HOLES SHALL NOT BE ROUGH OR IRREGULAR SO AS TO HINDER PROPER SOLDER WICKING.
14. CHECK ALL THAT APPLY
   ( ) GREEN SOLDERMASK OVER BARE COPPER/BARE GOLD (BOTH SIDES) WITH LIQUID PHOTO IMAGEABLE INK (LPI) PER ARTWORK.
   (X) GREEN TAIYO PSR-4000
   ( ) OTHER _____
15. CHECK ALL THAT APPLY
   (X) APPLY SILKSCREEN USING A NON-CONDUCTIVE, WHITE EPOXY BASED INK PER ARTWORK.
   ( ) OTHER _____
16. VENDOR LOGO & DATE CODE REQUIRED IN INK ON BOTTOM SIDE ONLY. DATE CODE FORMAT MUST BE YYWW ONLY

TESTING:

17. FINAL ELECTRICAL TEST TO BE PERFORMED USING PROVIDED IPC-D-356A NETLIST OR ODB++ FORMAT FILE. (REQUIRED UNLESS OTHERWISE SPECIFIED IN QUOTE)
    THE PCB SHALL HAVE A VERIFICATION STAMP.
18. A TIME DOMAIN REFLECTOMETER REPORT FOR EACH IMPEDANCE CONTROLLED LAYER AND A CERTIFICATE OF COMPLIANCE SHALL BE PROVIDED BY VENDOR AT TIME OF SHIPMENT. INSTANCES WHERE TDR TESTING CAN'T BE PERFORMED BECAUSE THE TRACE LENGTH IS TOO SHORT ON THE OUTER LAYERS AT THE PIN ESCAPES IS ACCEPTABLE. ALL OTHER INSTANCES MUST BE REPORTED.

MISCELLANEOUS:

19. IF PRESENT, ALL BLIND/BURIED VIAS WITH AN ASPECT RATIO <1:1 TO BE PLATED SHUT WITH COPPER WHEN USED AS VIA-IN PAD OR AS A STACKED VIA. BLIND/BURIED VIAS WITH AN ASPECT RATIO >1:1 TO BE FILLED WITH NON-CONDUCTIVE EPOXY, UNLESS OTHERWISE SPECIFIED.
20. FOR ALL DRILL INFORMATION REFER TO DRILL CHART.
   ( ) NON-CONDUCTIVE EPOXY. FILL AND CAP ALL 0.XXXX INCH DRILLED VIAS.
   ( ) SILVER. FILL AND CAP ALL 0.XXXX INCH DRILLED VIAS.
21. FINISHED SURFACE CONTACTS AND FILLED VIAS TO BE FREE OF ANY PITS, SCRATCHES PROBE MARKS OR OTHER DEFORMITIES THAT COULD EFFECT THE APPERANCE AND PERFORMACE OF THE CONTACT SURFACE. CONTACTS ARE TO BE AS FLAT AS POSSIBLE. NOT TO EXCEED +/- 0.001" OF FLATNESS.
22. THIEVING:
   ( ) SUPPLIER MAY ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS ON THIS DESIGN.
   (X) SUPPLIER MAY NOT ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS ON THIS DESIGN.
23. PEMNUT
   ( ) PEMNUTS TO BE INSTALLED BY SUPPLIER.
   ( ) PEMNUTS NOT TO BE INSTALLED BY SUPPLIER.
   (X) NOT APPLICABLE

TOLERANCES UNLESS OTHERWISE SPECIFIED

FRACTIONS +/- 1/16 | DECIMALS .XX +/- .01, .XXX +/- .005 | ANGLES +/- 1/2°

MATERIAL: SEE NOTES

FINISH: SEE NOTES

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DRAWN BY: MS DATE: 01/04/2017

CHECKED BY: DATE:

APPR. BY: DATE:

APPR. BY: DATE:

maxim integrated™

HARDWARE NAME: MAX17536B_EVKIT_B

HARDWARE NUMBER: XX-XXXXX-XXX REV B

NOT TO SCALE | TEMPLATE REV: | SHEET 1 OF 1