


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	05DEC22	X
B	ECR-118394	11DEC23	X

HOLE TOLERANCE  
UNLESS SPECIFIED  
PLATED: +/- .003  
NON PLATED: +/- .002

FINISHED HOLES IN MILS				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
A	6.0	PLATED	2	
B	10.0	PLATED	365	
C	45.0	PLATED	5	
D	100.0	PLATED	5	
E	213.0	PLATED	4	
F	187.0	NON-PLATED	4	

PRIMARY SIDE								
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES  TOLERANCES  DECIMALS    FRACTIONS    ANGLES ..xx   ..,010    +-1/32    .. 2 XXX   ..,005 ,XXXX   ..,0050	APPROVAL	DATE	<div><div></div><div>ANALOG DEVICES</div></div> <div>WWM DIVISION 804 WOBURN STREET WILMINGTON, MA 01887</div>					
	TEMPLATE ENGINEER	X    ddMMMyy						
	HARDWARE SERVICES	X    ddMMMyy						
	HARDWARE SYSTEMS	X    ddMMMyy						
MATERIAL	TEST ENGINEER	X    ddMMMyy	TITLE  FABRICATION  EVAL-LTC7065-AZ					
	COMPONENT ENGINEER	X    ddMMMyy						
	TEST PROCESS	X    ddMMMyy						
	HARDWARE RELEASE	X    ddMMMyy						
FINISH	DESIGNER K. CHAN	ddMMMyy	SIZE C	FSCM NO 24355	DRAWING NUMBER 09-073689	REV B		
	PTD ENGINEER	X    ddMMMyy						
	CHECKER	X    ddMMMyy						
DO NOT SCALE DWG			SCALE	1 / 1		SHEET	1 OF 2	


TEST REQUIREMENTS, 100% NETLIST ELECTRICAL VERIFICATION USING CUSTOMER  
SUPPLIED IPC-D-356 NETLIST FOR OPENS AND SHORTS WHEN  
"GERBER DATA" IS PROVIDED. THIS VERIFICATION ALSO  
REQUIRED FOR "ODB++" DATA PER EMBEDDED NETLIST.

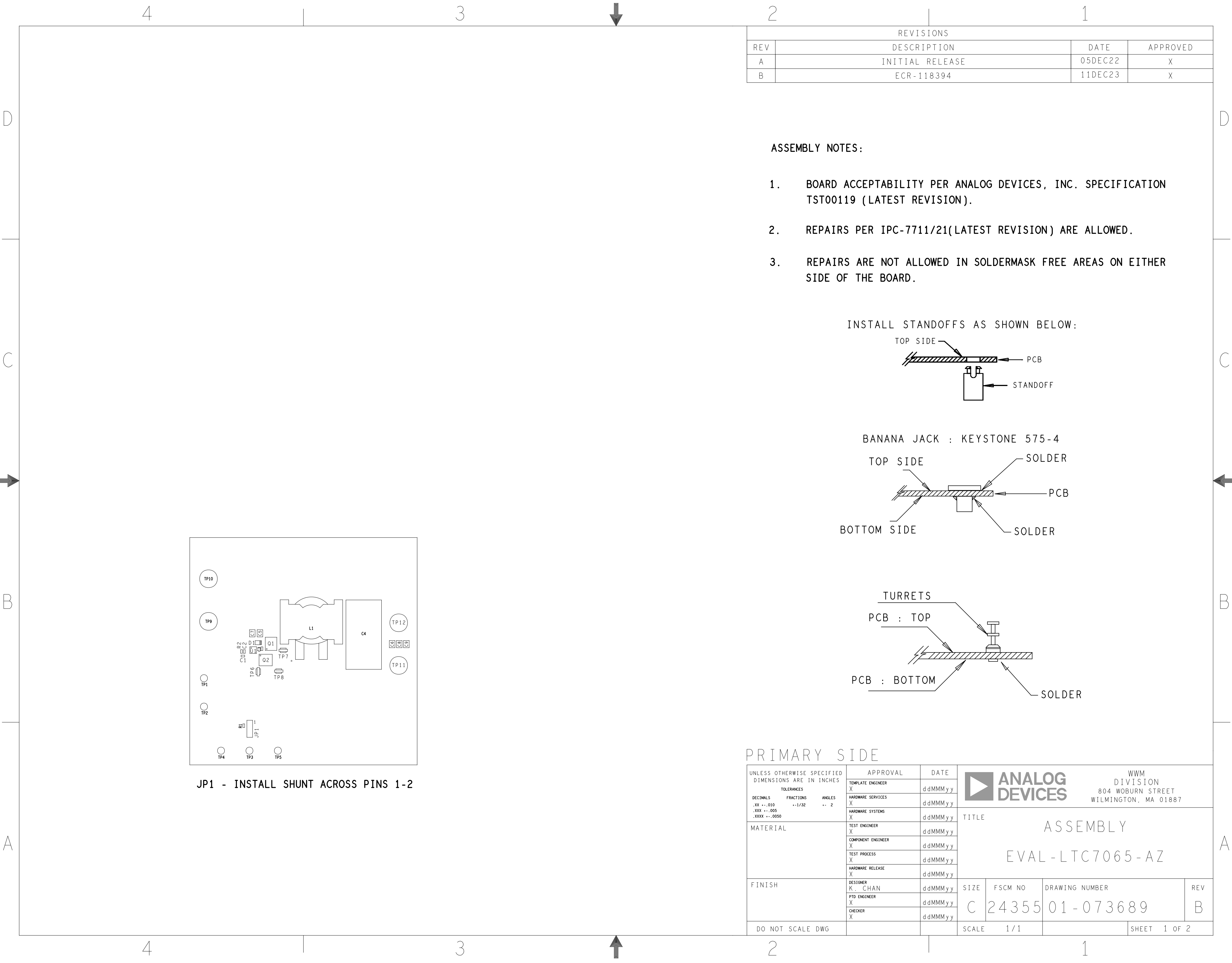
1. REFER TO IPC-6010 SERIES (LATEST REV.), CLASS 2 FOR FABRICATION UNLESS OTHERWISE SPECIFIED.
2. ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00115, (LATEST REVISION.)
3. MODIFICATIONS TO THE ARTWORK ARE NOT ALLOWED WITHOUT WRITTEN AUTHORIZATION.
4. HOLE PATTERN TOLERANCES FOR UNDIMENSIONED HOLES SHALL BE A DIAMETER OF 0.005 INCHES FROM THEIR TRUE POSITION.
5. PLATED HOLE WALL THICKNESS SHALL NOT BE LESS THAN 0.001 INCH MINIMUM AVERAGE, WITH NO READING LESS THAN .0008 BY CROSS SECTION.
6. HOLE DIAMETERS APPLY AFTER PLATING.
7. VIA SIZE LESS THAN OR EQUAL TO 0.012" SHALL BE PLUGGED AND COVERED WITH SOLDER MASK.
8. FINISHED CONDUCTOR WIDTHS SHALL NOT BE REDUCED FROM THE NOMINAL INDICATED ON THE MASTER PATTERN, BY MORE THAN THE CONDUCTOR THICKNESS.
9. MINIMUM DESIGN LINE WIDTH IS .XXX INCH.
10. MINIMUM DESIGN SPACING IS .XXX INCH.
11. NON-FUNCTIONAL PAD REMOVAL FROM INNER SIGNAL LAYERS MAY BE PERFORMED AFTER CUSTOMER APPROVAL.
12. IF PAD SIZES PROVIDED ARE NOT LARGE ENOUGH TO MAINTAIN ANNULAR RING REQUIREMENT, MFR. MAY REQUEST APPROVAL TO TEAR DROP PADS TO MAINTAIN ANNULAR RING. (AT PAD TO TRACE INTERSECTION ONLY AND ELECTRICAL INTEGRITY MUST BE MAINTAINED.)
13. THIEVING MAY BE ADDED TO COMPENSATE FOR LOW COPPER DENSITY AREAS ON THIS DESIGN ONLY AFTER REVIEW AND APPROVAL FROM THE CUSTOMER:
  - A. THIEVING TO CARD EDGE, FIDUCIALS, NON-PLATED THROUGH HOLES, ALL OTHER FEATURES TO BE 0.200 INCH MINIMUM.
  - B. THERE SHALL BE NO THIEVING IN ANY AREAS FREE OF SOLDER MASK OR INTERNAL COPPER PLANES.
14. MFR. TO LEGIBLY ETCH OR STAMP/SCREEN WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE IN A CLEAR AREA UNLESS OTHERWISE INDICATED;
  - A. U.L. CODE-FLAMMABILITY RATING
  - D. MFR LOGO
  - B. DATE CODE (STAMP).
  - E. SUCCESSFUL ELECTRICAL TEST.
  - C. LOT NUMBER
15. REPAIRS PER IPC-7711/21 (LATEST REV.) ARE ALLOWED. REPAIRS ARE NOT ALLOWED IN ANY AREA DEFINED ON GOLD\_PRM AND/OR GOLD SEC ARTWORK LAYERS WHEN PROVIDED IN GERBER OR ODB++ DATA.

Diagram illustrating the cross-section of a 4-layer PCB structure. The layers are labeled as follows:

- PRIMARY SILKSCREEN
- PRIMARY SOLDER MASK
- PRIMARY SIDE (LAYER 1)
- LAYER 2 (Thickness:  $\sim 3.9$  MIL)
- LAYER 3
- LAYER 4 (Thickness:  $\sim 3.9$  MIL)
- SECONDARY SIDE (LAYER 4)
- SECONDARY SOLDER MASK
- SECONDARY SILKSCREEN

NOMINAL FINISHED THICKNESS:  $0.062" \pm 10\%$

	<h1>ANALOG DEVICES</h1>		WWM DIVISION	
			804 WOBURN STREET WILMINGTON, MA 01887	
SIZE	FSCM NO	DRAWING NUMBER	REV	
C	24355	09-073689	B	
SCALE	1/1		SHEET 2 OF 2	

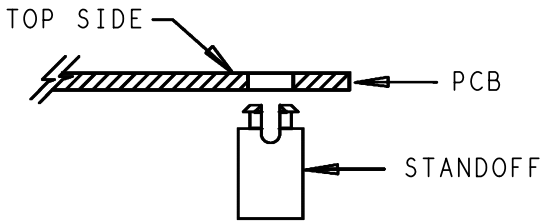


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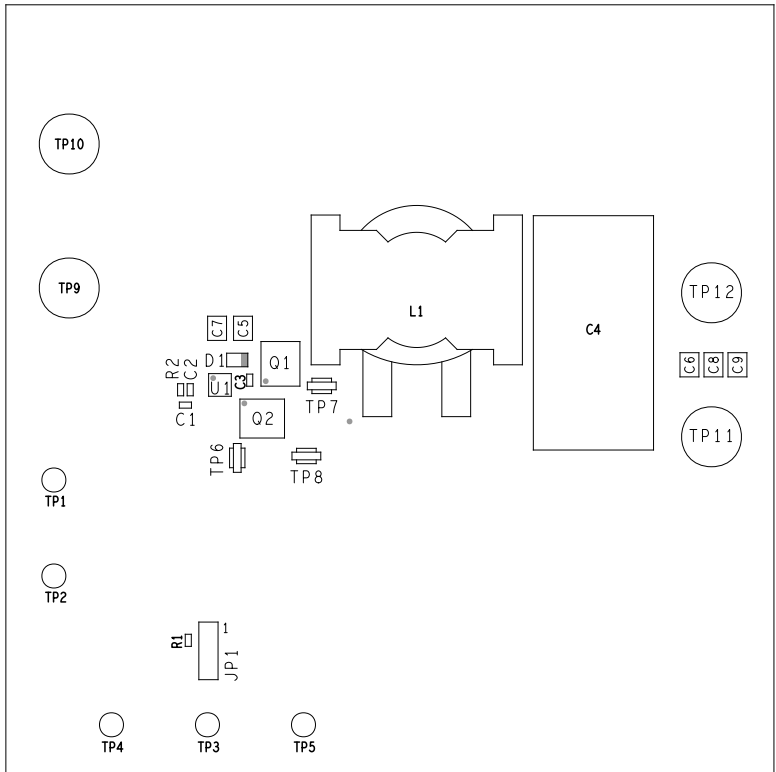
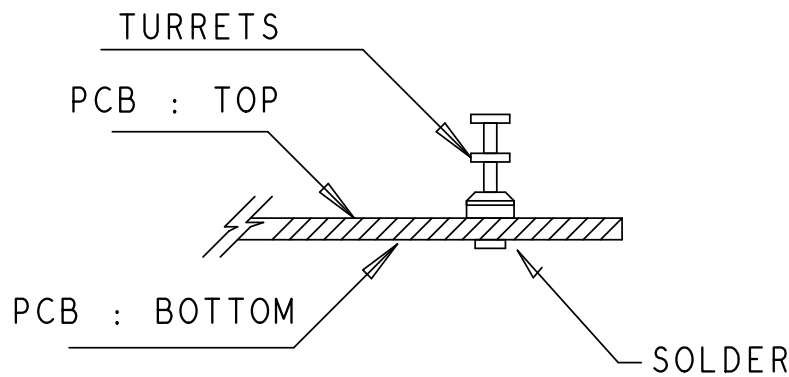
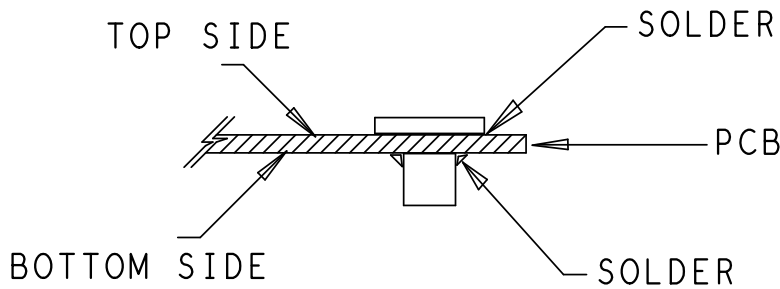
ASSEMBLY NOTES:

- BOARD ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00119 (LATEST REVISION).
- REPAIRS PER IPC-7711/21(LATEST REVISION) ARE ALLOWED.
- REPAIRS ARE NOT ALLOWED IN SOLDERMASK FREE AREAS ON EITHER SIDE OF THE BOARD.

INSTALL STANDOFFS AS SHOWN BELOW:




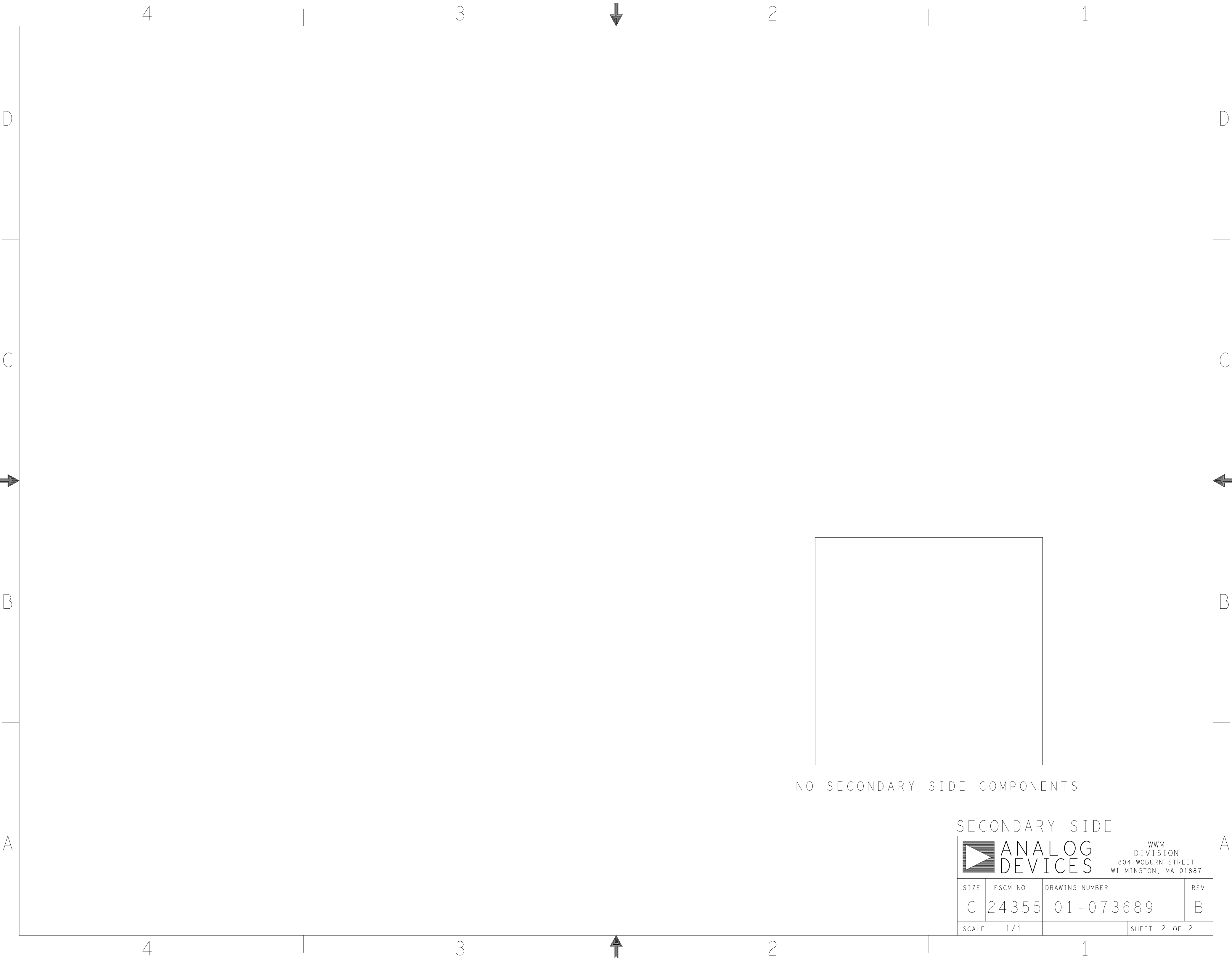
BANANA JACK : KEYSTONE 575-4



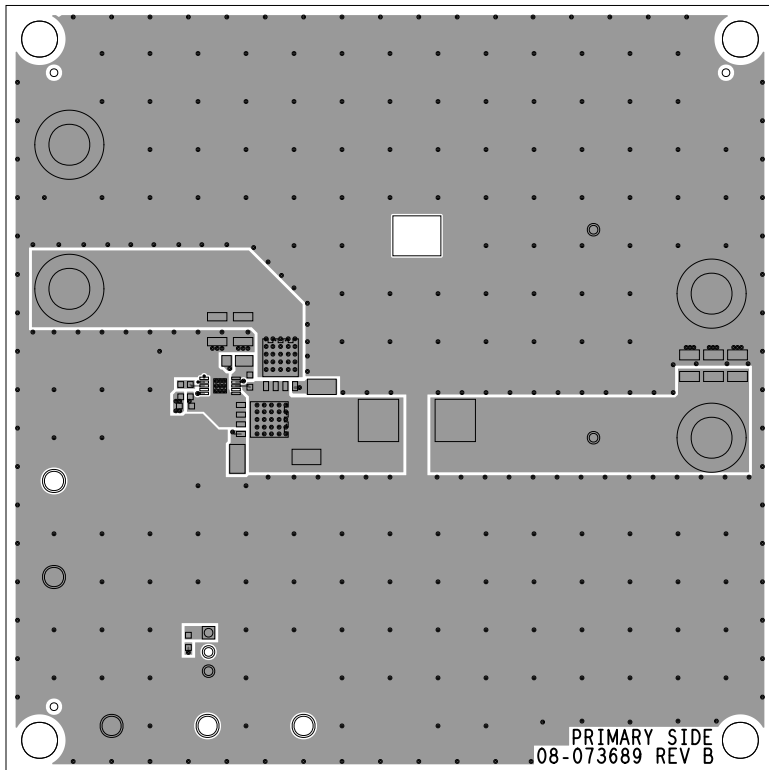
JP1 - INSTALL SHUNT ACROSS PINS 1-2

PRIMARY SIDE				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES  TOLERANCES  DECIMALS      FRACTIONS      ANGLES .XX    --.010      --1/32      -- 2 .XXX   --.005 .XXXX --.0050	APPROVAL		DATE	
	TEMPLATE ENGINEER X		d d M M y y	
	HARDWARE SERVICES X		d d M M y y	
	HARDWARE SYSTEMS X		d d M M y y	
MATERIAL	TEST ENGINEER X		d d M M y y	
	COMPONENT ENGINEER X		d d M M y y	
	TEST PROCESS X		d d M M y y	
	HARDWARE RELEASE X		d d M M y y	
FINISH	DESIGNER K. CHAN		d d M M y y	
	PTD ENGINEER X		d d M M y y	
	CHECKER X		d d M M y y	
DO NOT SCALE DWG				

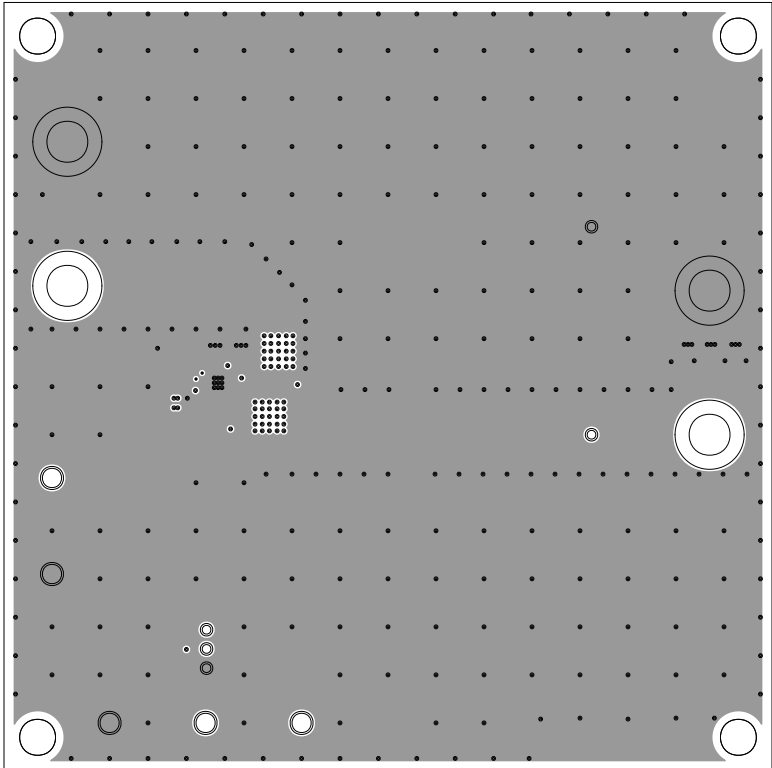
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TITLE				ASSEMBLY	
				EVAL-LTC7065-AZ	
SIZE	FSCM NO	DRAWING NUMBER		REV	
C	24355	01-073689		B	
SCALE 1 / 1				SHEET 1 OF 2	



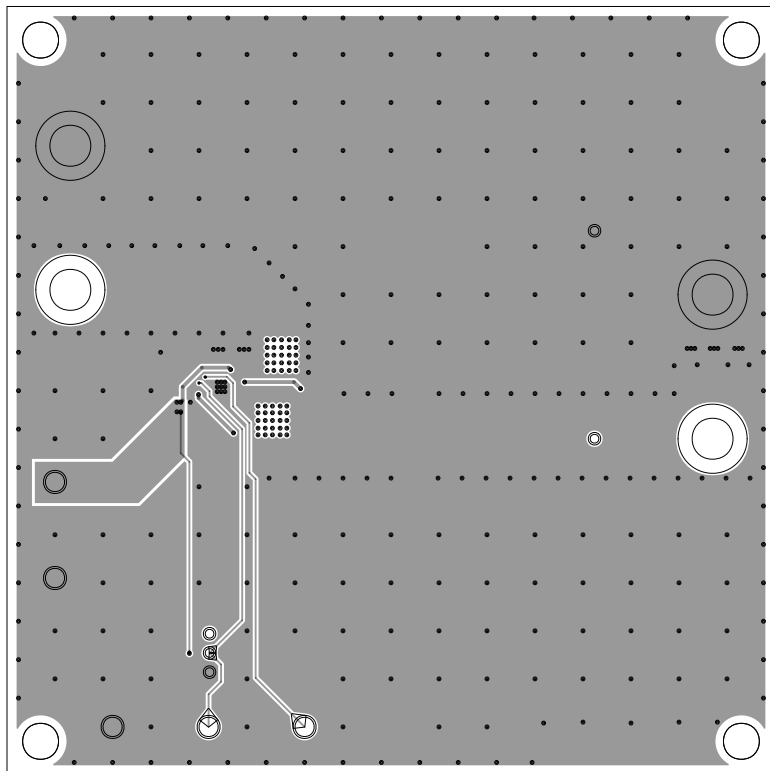
L1 PRIMARY  
08-073689-01  
REV B



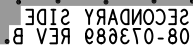
L2 GND  
08-073689-07  
REV B



L3 GND/SIGNAL  
08-073689-08  
REV B



08-073689 REV B SECONDARY SIDE

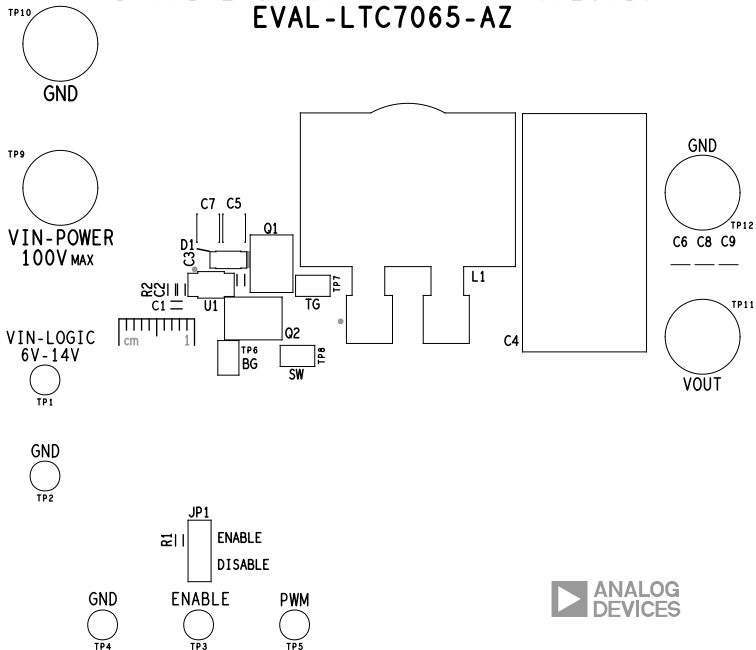




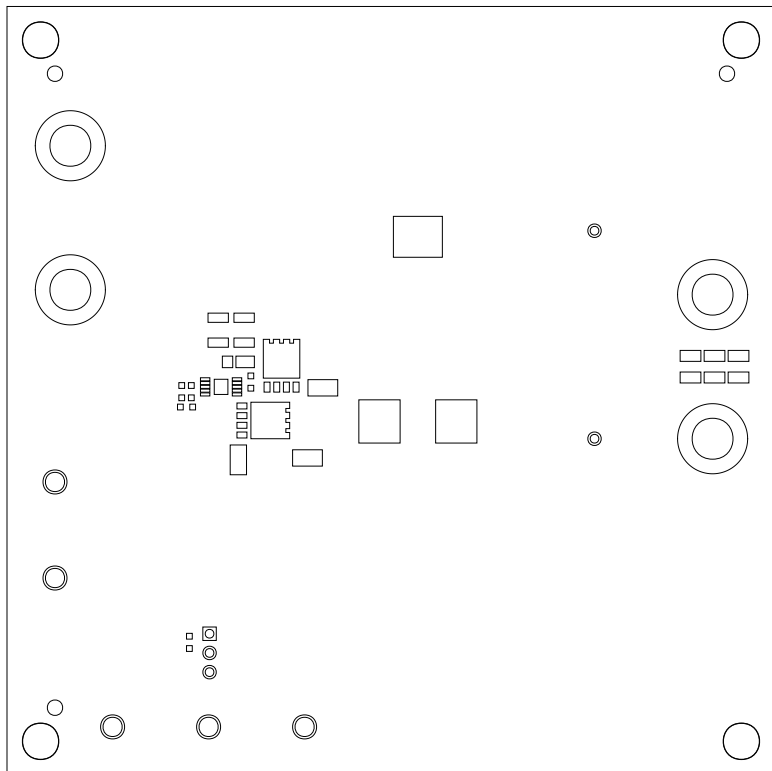
SILKSCREEN PRIMARY  
08-073689-03  
REV B

# LTC7065

## 100V HALF-BRIDGE DRIVER WITH ADAPTIVE SHOOT-THROUGH PROTECTION EVAL-LTC7065-AZ



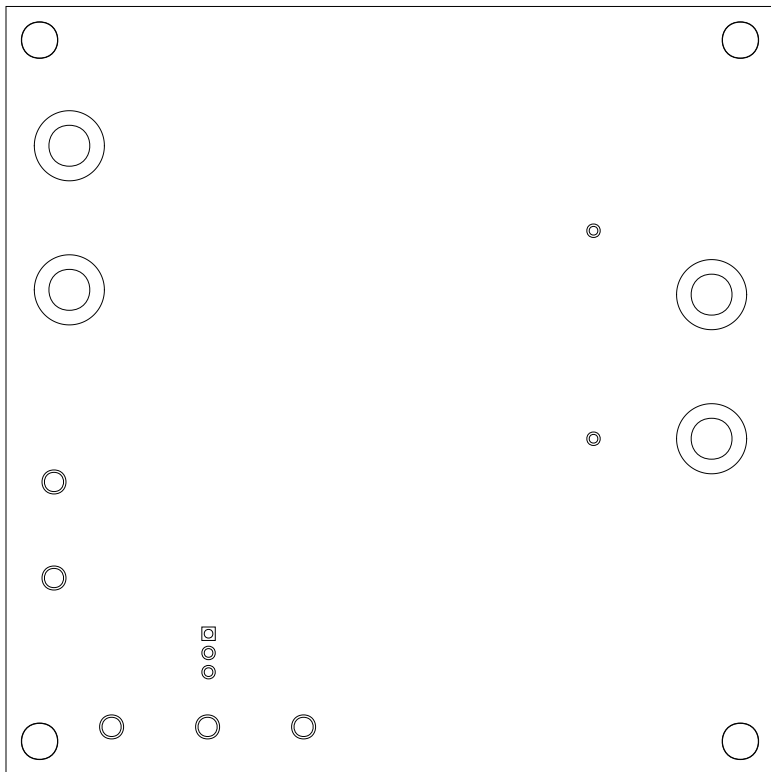
SOLDERMASK PRIMARY  
08-073689-04  
REV B



SILKSCREEN SECONDARY  
08-073689-05  
REV B



SOLDERMASK SECONDARY  
08-073689-06  
REV B



PASTEMASK PRIMARY  
08-073689-13  
REV B

