REVISION			
REV	DESCRIPTION	DATE	APPROVED
B	INITIAL RELEASE	13MAR26	S.OLSON

HOLE TOLERANCE

UNLESS SPECIFIED
PLATED: +/- .003
NON PLATED: +/- .002

DRILL CHART: TOP to BOTTOM					
ALL UNITS ARE IN MILS					
FIGURE	SIZE	TOLERANCE	PLATED	QTY	NOTES
A	6.0	+3.0/-3.0	PLATED	4	SEE FAB NOTE #20
B	10.0	+3.0/-3.0	PLATED	582	SEE FAB NOTE #20
R	31.5	+3.0/-3.0	PLATED	9	
EV	35.0	+3.0/-3.0	PLATED	6	
U	35.43	+3.0/-3.0	PLATED	10	
EX	40.0	+3.0/-3.0	PLATED	4	
FT	45.0	+3.0/-3.0	PLATED	2	
GB	100.0	+3.0/-3.0	PLATED	9	
FF	213.0	+3.0/-3.0	PLATED	4	
BW	118.11	+3.0/-3.0	NON-PLATED	4	
K	187.0	+3.0/-3.0	NON-PLATED	4	

ANALOG DEVICES

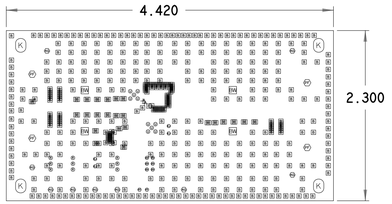
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:FAB_DWG1



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ANALOG DEVICES

TITLE

FABRICATION

EVAL-LT8419-AZ

APPROVAL	DATE
DESIGNER V.PONTIKES	1APR26
ENGINEER S.OLSON	1APR26
APPROVAL X	ddMMMyy
DO NOT SCALE DWG	

SIZE D

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
.XX +-.010 +-1/32 +-1°
.XXX +-.005
.XXXX +-.0050

DRAWING NUMBER 09-100210

REV B

SCALE 1/1

TEMPLATE REV:

SHEET 1 OF 2

CUSTOMER_EVALUATION_TEMPLATE

REVISION			
REV	DESCRIPTION	DATE	APPROVED
B	INITIAL RELEASE	13MAR26	S.OLSON

LAMINATION DIAGRAM				
LAYER NUMBER	LAYER NAME	COPPER THICKNESS (OZ,INCH)	DIELECTRIC THICKNESS (INCH)	MATERIALS
1	TOP	1.5 OZ, 0.0021"		FINAL CU (THICKNESS AFTER PLATING)
			0.006	ISOLA 370HR/EQUIVALENT
2	LAYER_2	2 OZ, 0.0028"		CU CLAD
			0.036	ISOLA 370HR/EQUIVALENT
3	LAYER_3	2 OZ, 0.0028"		CU CLAD
			0.006	ISOLA 370HR/EQUIVALENT
4	BOTTOM	1.5 OZ, 0.0021"		FINAL CU (THICKNESS AFTER PLATING)

THE FINISHED PCB THICKNESS TO BE: 0.062" +/-10%

ANALOG DEVICES

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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:FAB_DWG2

NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES (EXCEPT WHERE NOTED).
   ALL DOCUMENTS & SPECIFICATIONS REFERRED TO BELOW SHOULD BE THE LATEST REVISIONS.

MATERIAL: HOMOGENOUS MATERIALS IN THIS BOARD SHALL BE COMPLIANT WITH THE EU RoHS DIRECTIVE 2002/95/EC

2. BOARD MATERIAL:
   (X) ISOLA 370HR OR S1000-2 OR IT180 OR EQUIVALENT
   ( ) ISOLA-FR408HR OR EQUIVALENT
   ( ) ISOLA IS410
   ( ) MEGTRON 6
   ( ) NELCO-4000-13
   ( ) ROGERS 4350B
   ( ) ROGERS 3003
   ( ) OTHER _____

3. ALL LAMINATES & BONDING MATERIALS SHOULD BE SELECTED FROM IPC-4101 OR IPC-4103, (TG>170 DEGC TD>300 DEGC)
   UL FLAMMABILITY RATING 94V-0. BOARD MATERIAL & CONSTRUCTION SHALL MEET THE REQUIREMENTS OF UL796/UL796F.

4. REFER TO IPC-6010 SERIES, CLASS 2 FOR FABRICATION,WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2.

5. REFER TO LAMINATION DIAGRAM FOR OVERALL BOARD THICKNESS, TOLERANCE APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES. FINISHED THICKNESS MEASURED FROM TOP COPPER TO BOTTOM COPPER.

6. BOW & TWIST NOT TO EXCEED 0.0075 INCHES (0.75%) PER LINEAR INCH AND SHOULD BE MEASURED PER IPC-TM-650, METHOD 2.4.22.

7. ACCEPTABILITY PER ADI SPECIFICATION TST00115.

TOOLING:

8. IMPEDANCE REQUIREMENTS: IF NO STACKUP IS DEFINED, THE VENDOR IS ALLOWED TO ADJUST THE DIELECTRIC THICKNESS & TRACE WIDTHS TO MEET THE IMPEDANCE REQUIREMENT. IF SPECIFIED, THE VENDOR MUST MEET THE REQUIREMENTS LISTED IN THE IMPEDANCE TABLE. ANY ADJUSTMENT MADE TO THE DEFINED STACKUP, TRACE WIDTH & SPACING THAT IMPACT THE REQUIREMENTS MUST HAVE WRITTEN APPROVAL FROM ADI.

9. FILLET OPTIONS TO ENHANCE RELIABILITY AT PAD JUNCTIONS WHERE SPACING PERMITS.
   ( ) FILLETS ALLOWED
   (X) FILLETS NOT ALLOWED

10. THIEVING:
    ( ) VENDOR MAY ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS MAINTAINING A MINIMUM 0.100 INCH CLEARANCE FROM ALL COPPER FEATURES.
    (X) VENDOR MAY NOT ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS.

11. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.003 INCHES.

FINISH:

12. DRILL SIZES ARE FINISHED HOLE SIZES. ALL HOLES SHALL BE LOCATED WITHIN 0.005 INCHES DTP, UNLESS SPECIFIED. MINIMUM BARREL PLATING OF 0.001 INCHES. PLATED HOLES SHALL NOT BE ROUGH OR IRREGULAR SO AS TO HINDER PROPER SOLDER WICKING. BARREL RELIEF ON SOLDERMASK ALLOWED IN UNFILLED VIA IN PAD HOLES.

13. PLATING SPECIFICATION:
    (X) REFER TO LAMINATION DIAGRAM FOR FINISHED COPPER WEIGHT/THICKNESS REQUIREMENTS
    THE STARTING COPPER WEIGHT/THICKNESS CAN VARY AS LONG AS THE FINISHED COPPER WEIGHT/THICKNESS IS NOT LESS THAN THE SPECIFIED VALUE.

14. SURFACE FINISH:
    (X) IMMERSION GOLD (ENIG) 1.58-3.94 MICRO INCHES OVER 118-236 MICRO INCHES MIN. OF ELECTROLESS NICKEL PER IPC-4552
    ( ) OSP (ORGANIC SOLDERABILITY PRESERVATIVE)
    ( ) IMMERSION SILVER
    ( ) SOFT WIRE BONDABLE GOLD 30-50 MICRO INCHES OF SOFT WIRE BONDABLE GOLD OVER 100-150 MICRO INCHES OF NICKEL
    ( ) EDGE CONNECTOR FINGERS ARE TO BE PLATED WITH 100 MICRO-INCHES(.0001") OF LOW STRESS NICKEL UNDER 30 MICRO-INCHES (.00003") OF GOLD

15. SOLDERMASK:
    SOLDERMASK OVER BARE COPPER OR BARE GOLD (BOTH SIDES) TO MEET IPC-SM-840.
    IF PRESENT, DO NOT MODIFY SOLDERMASK DEFINED PADS (MASK OPENINGS LESS THAN COPPER PAD) WITHOUT APPROVAL.
    (X) LPI
    ( ) OTHER_____
    COLOR
    ( ) GREEN
    (X) OTHER: BLUE

16. APPLY SILKSCREEN TO BOTH SIDES USING A NON-CONDUCTIVE, EPOXY BASED INK PER ARTWORK.
    (X) WHITE
    ( ) OTHER_____

TESTING:

17. FINAL ELECTRICAL TEST TO BE PERFORMED USING PROVIDED IPC-D-356A NETLIST OR ODB++ FORMAT FILE. THE PCB SHALL HAVE A VERIFICATION STAMP.

18. A TIME DOMAIN REFLECTOMETER REPORT (TDR) FOR EACH IMPEDANCE CONTROLLED LAYER & A CERTIFICATE OF COMPLIANCE SHALL BE PROVIDED BY VENDOR AT TIME OF SHIPMENT. INSTANCES WHERE TDR TESTING CAN'T BE PERFORMED BECAUSE THE TRACE LENGTH IS TOO SHORT ON THE OUTER LAYERS AT THE PIN ESCAPES IS ACCEPTABLE. ALL OTHER INSTANCES MUST BE REPORTED.

MISCELLANEOUS:

19. IF PRESENT, ALL BLIND/BURIED VIAS WITH AN ASPECT RATIO <1:1 TO BE PLATED SHUT WITH COPPER WHEN USED AS VIA-IN-PAD OR AS A STACKED VIA. BLIND/BURIED VIAS WITH AN ASPECT RATIO >1:1 TO BE FILLED WITH NON-CONDUCTIVE EPOXY.

20. FOR VIA FILL INFORMATION REFER TO DRILL CHART:
    (X) NON-CONDUCTIVE EPOXY FILL ALL 0.006 AND 0.010 INCHES DRILLED VIAS
    ( ) COPPER FILL ALL 0.XXXX INCHES DRILLED VIAS

21. INTENTIONAL SHORTS:
    IF AN INTENTIONAL SHORT REPORT IS SUPPLIED AND DOES NOT MATCH THE FAB DATA THEN ADI APPROVAL IS REQUIRED.

22. PEMNUTS:
    ( ) PEMNUTS TO BE INSTALLED BY FABRICATOR.
    ( ) PEMNUTS NOT TO BE INSTALLED BY FABRICATOR.
    (X) NOT APPLICABLE.

23. MANUFACTURER TO ETCH/STAMP WITH PERMANENT NON-CONDUCTIVE INK ON BOTTOM LEGEND LAYER. CREATE BOTTOM LEGEND IF LAYER NOT PRESENT.
    A. UL CODE-FLAMMABILITY RATING FOR THOSE APPROVED MATERIALS (IF APPLICABLE)
    B. DATE CODE
    C. LOT NUMBER
    D. MANUFACTURER LOGO

24. PANELIZATION:
    BOARDS TO BE SHIPPED IN ARRAY AND KEPT INTACT
    PANEL TO BE SUBJECTED TO CUSTOMERS APPROVAL
    PANEL SOLDER PASTE STENCIL GERBER TO BE PROVIDED TO ANALOG

FAB NOTES REVISION: JULY 15 2025

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ANALOG DEVICES

TITLE: FABRICATION

EVAL-LT8419-AZ

APPROVAL	DATE
DESIGNER V.PONTIKES	1APR26
ENGINEER S.OLSON	1APR26
APPROVAL X	ddMMMyy

SIZE: D — UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES DECIMALS .XX +-.010 .XXX +-.005 .XXXX +-.0050 FRACTIONS +-1/32 ANGLES +-2

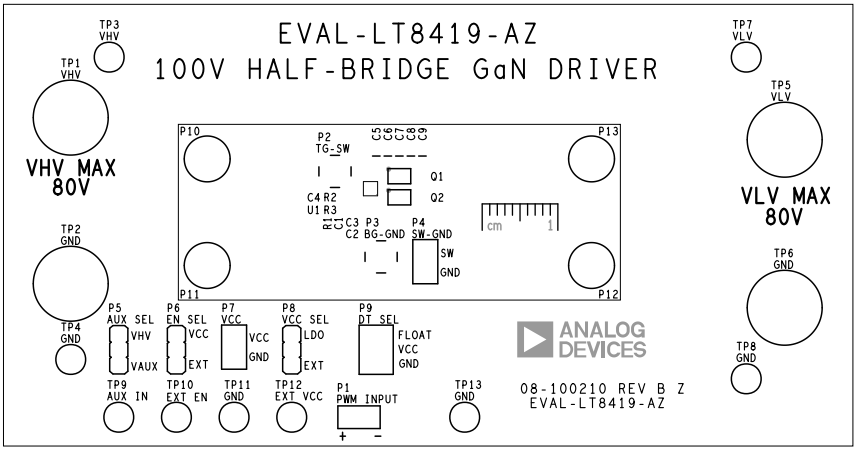
DRAWING NUMBER: 09-100210

REV: B

DO NOT SCALE DWG | SCALE 1/1 | TEMPLATE REV: | SHEET 1 OF 2

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HARDWARE NAME:EVAL-LT8419-AZ	
HARDWARE NUMBER:BR-100210 REV B	
ENGINEER:S.OLSON	DESIGNER:V.PONTIKES
DATE: 04/1/2026	ODB++/GERBER:SILK_TOP



ANALOG DEVICES

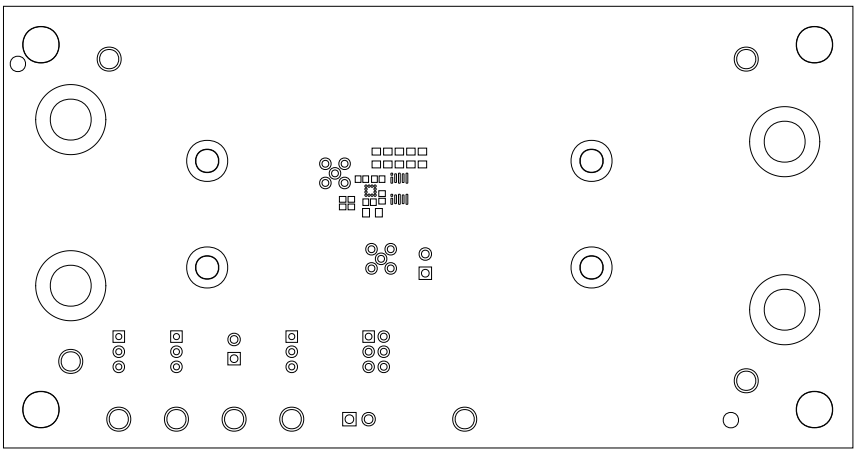
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:MASK_TOP



ANALOG DEVICES

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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:GOLD_TOP

REVISION			
REV	DESCRIPTION	DATE	APPROVED
B	INITIAL RELEASE	13MAR26	S.OLSON

ASSEMBLY NOTES:

1. BOARD ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00119 (LATEST REVISION).

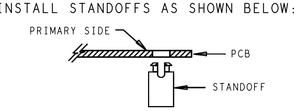
2. REPAIRS PER IPC-7711/21(LATEST REVISION) ARE ALLOWED.

3. REPAIRS ARE NOT ALLOWED IN SOLDERMASK FREE AREAS ON EITHER SIDE OF THE BOARD.

4. SHUNT JUMPERS P5-S, P6-S, P8-S, AND P9-S TO BE HAND-INSTALLED AFTER ASSEMBLY ONTO PINS P5, P6, P8, P9, RESPECTIVELY. SEE BELOW FOR SHUNT JUMPER POSITIONS.

P5 SHUNT POSITION: VHV
P6 SHUNT POSITION: VCC
P8 SHUNT POSITION: LDO
P9 SHUNT POSITION: VCC

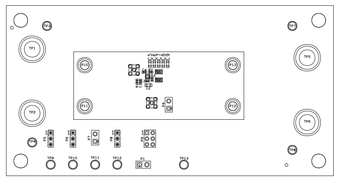
INSTALL STANDOFFS AS SHOWN BELOW:



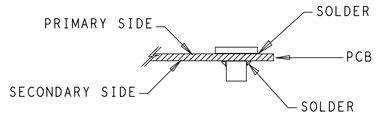
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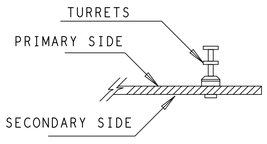
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HARDWARE NAME:EVAL-LT8419-AZ
HARDWARE NUMBER:BR-100210 REV B
ENGINEER:S.OLSON DESIGNER:V.PONTIKES
DATE: 04/1/2026 ODB++/GERBER:TOP_ASSY



BANANA JACK : KEYSTONE 575-4





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ANALOG DEVICES

TITLE
ASSEMBLY

EVAL-LT8419-AZ

APPROVAL	DATE
DESIGNER V.PONTIKES	1APR26
ENGINEER S.OLSON	1APR26
APPROVAL X	ddMMMyy

SIZE D | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: DECIMALS XX +-.010 XXX +-.005 XXXX +-.0050; FRACTIONS +-1/32; ANGLES +-2

DRAWING NUMBER 01-100210 | REV B

DO NOT SCALE DWG | SCALE 1/1 | TEMPLATE REV: | SHEET 1 OF 2

CUSTOMER_EVALUATION_TEMPLATE

ANALOG DEVICES

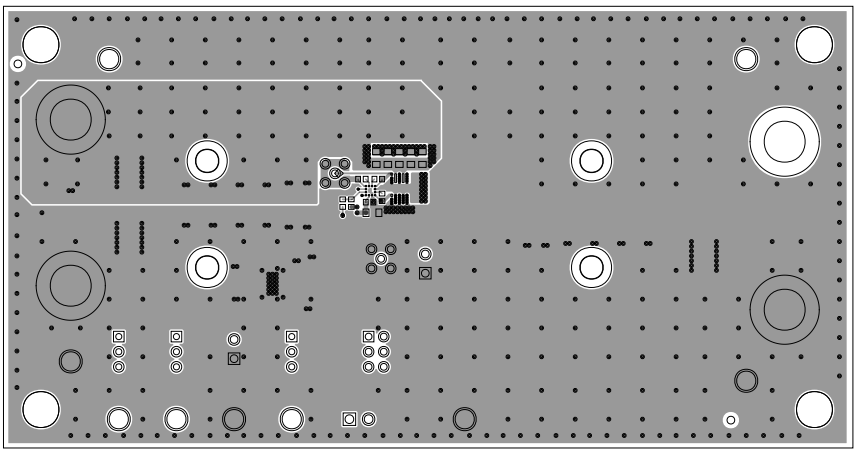
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:TOP



ANALOG DEVICES

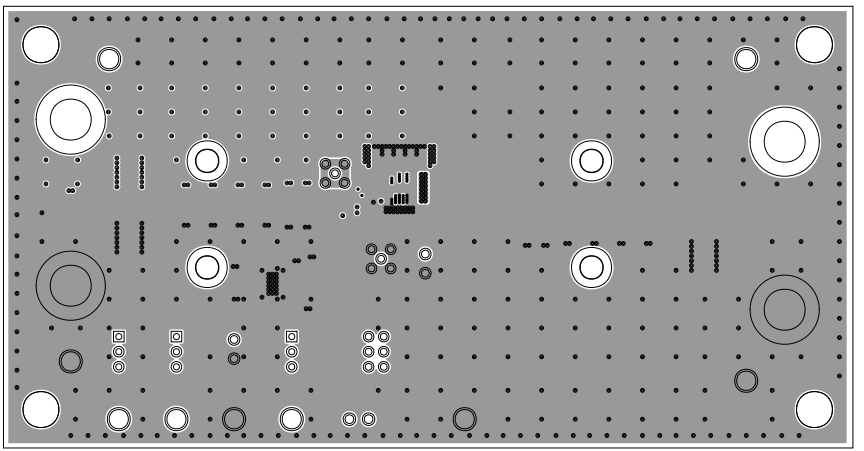
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:LAYER_2



ANALOG DEVICES

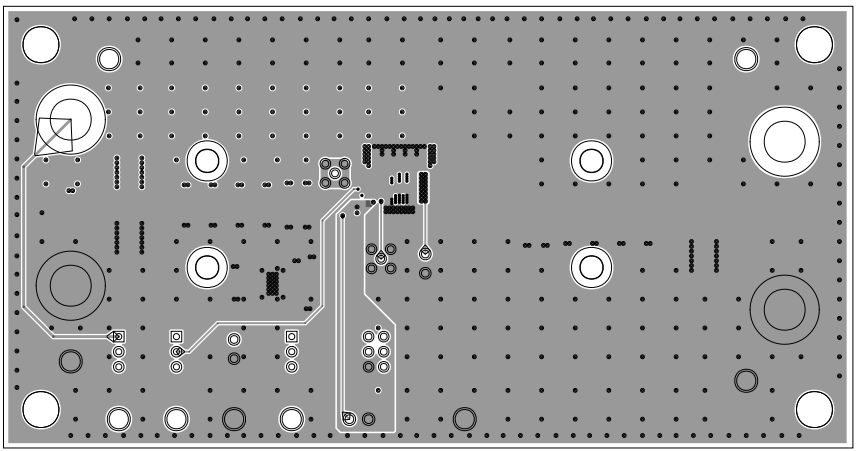
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:LAYER_3



ANALOG DEVICES

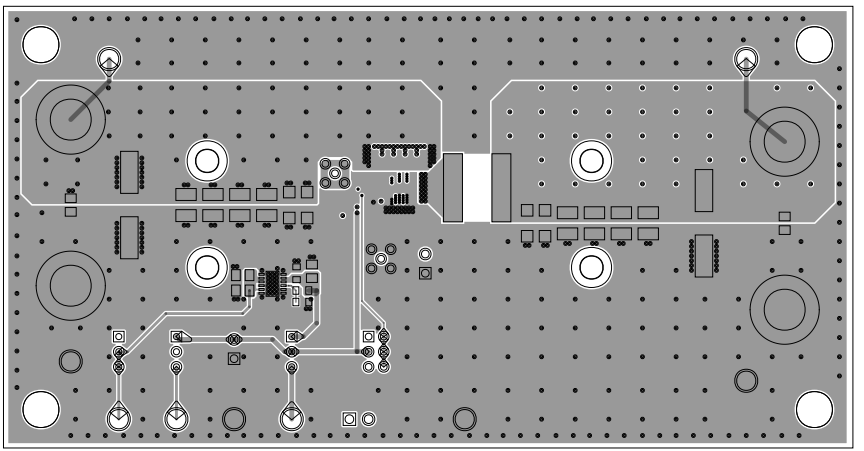
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:BOTTOM



ANALOG DEVICES

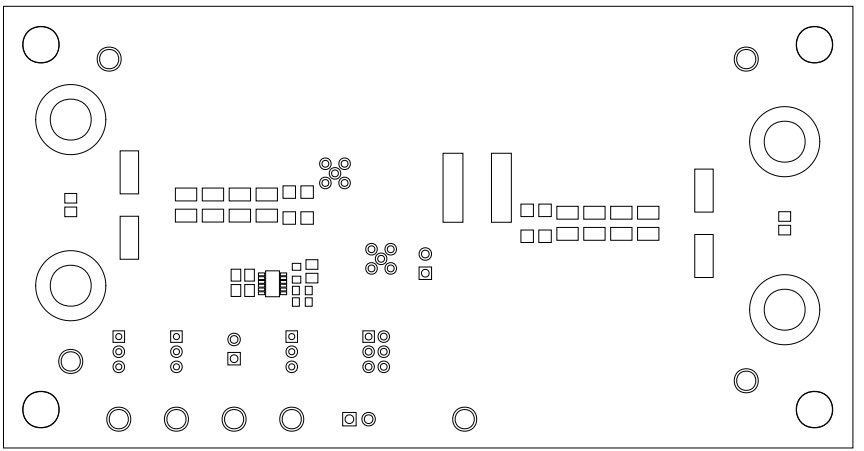
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:MASK_BOT



ANALOG DEVICES

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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:GOLD_BOT

REVISION			
REV	DESCRIPTION	DATE	APPROVED
B	INITIAL RELEASE	13MAR26	S.OLSON

ANALOG DEVICES

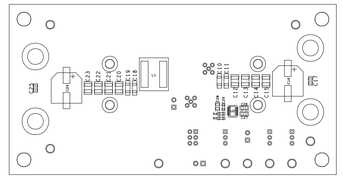
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON | DESIGNER:V.PONTIKES

DATE: 04/1/2026 | ODB++/GERBER:BOT_ASSY



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ANALOG DEVICES

TITLE

ASSEMBLY

EVAL-LT8419-AZ

APPROVAL	DATE
DESIGNER V.PONTIKES	1APR26
ENGINEER S.OLSON	1APR26
APPROVAL X	ddMMMyy

SIZE: D | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES | TOLERANCES: DECIMALS .XX +-.010 .XXX +-.005 .XXXX +-.0050; FRACTIONS +-1/32; ANGLES +-2

DRAWING NUMBER: 01-100210 | REV: B

DO NOT SCALE DWG | SCALE 1/1 | TEMPLATE REV: | SHEET 2 OF 2

CUSTOMER_EVALUATION_TEMPLATE

ANALOG DEVICES

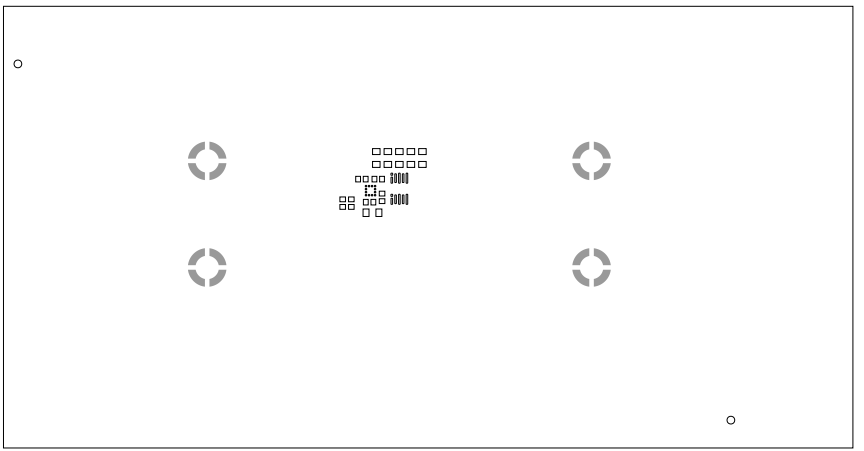
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:PASTE_TOP



ANALOG DEVICES

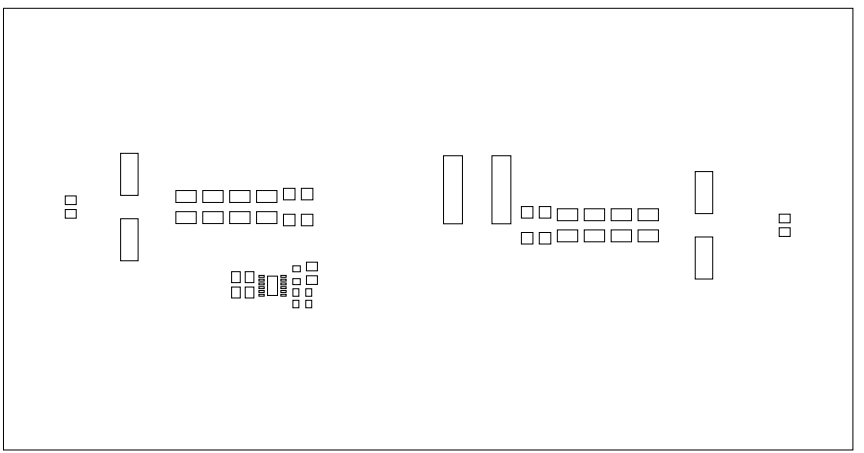
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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:PASTE_BOT



ANALOG DEVICES

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HARDWARE NAME:EVAL-LT8419-AZ

HARDWARE NUMBER:BR-100210 REV B

ENGINEER:S.OLSON DESIGNER:V.PONTIKES

DATE: 04/1/2026 ODB++/GERBER:SILK_BOT

