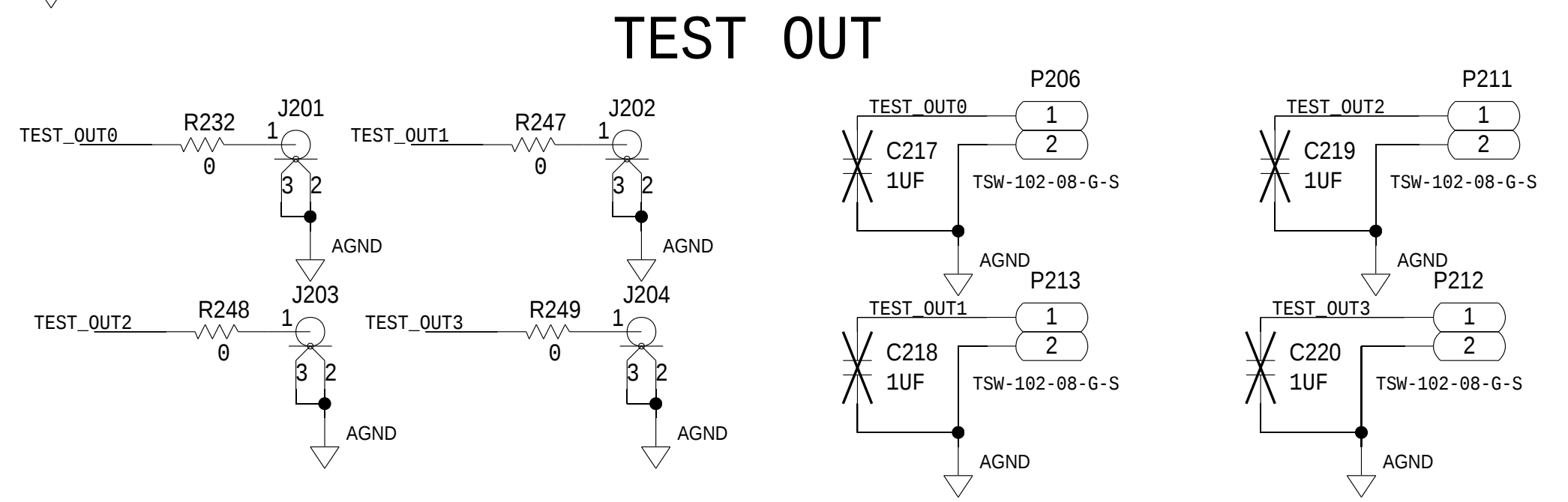
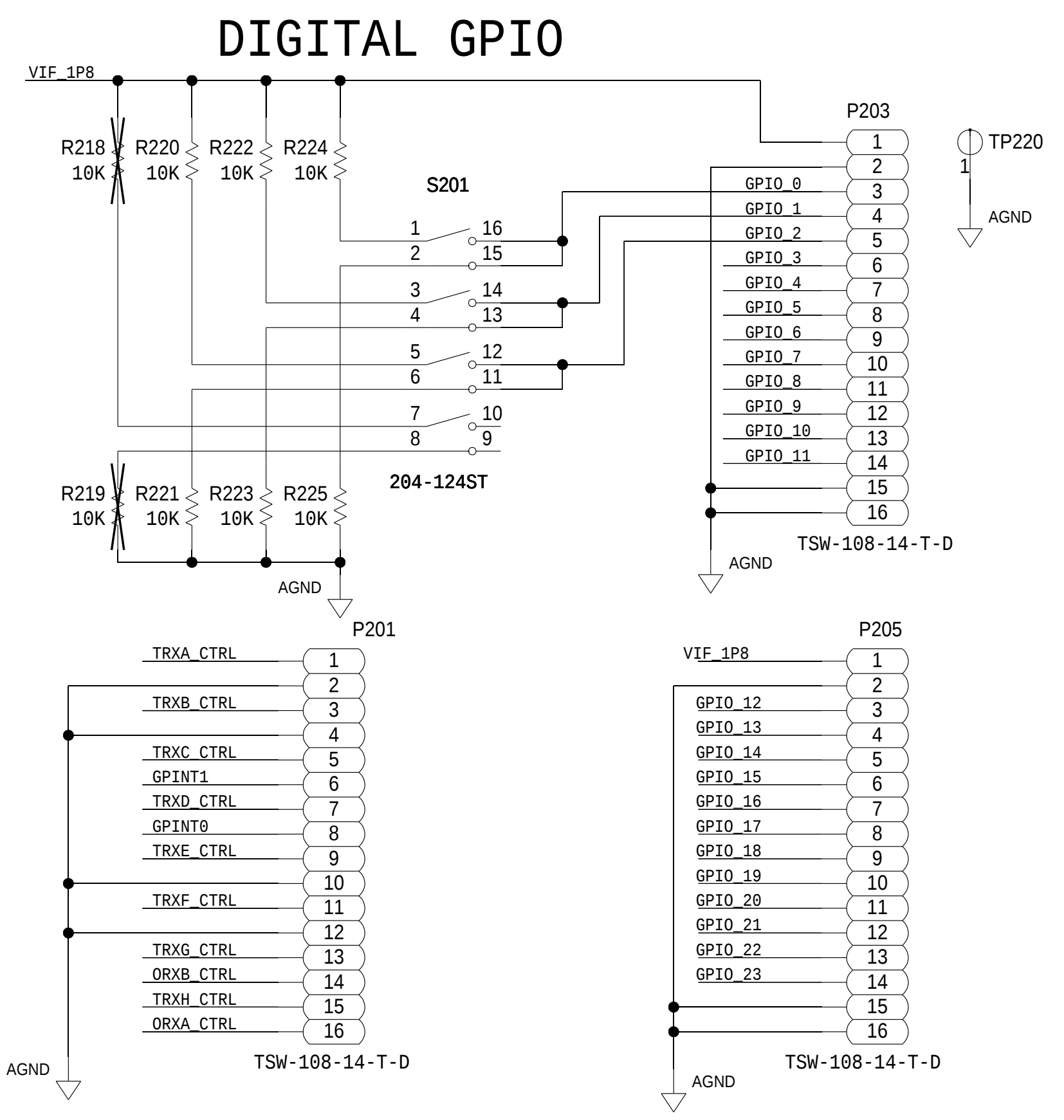
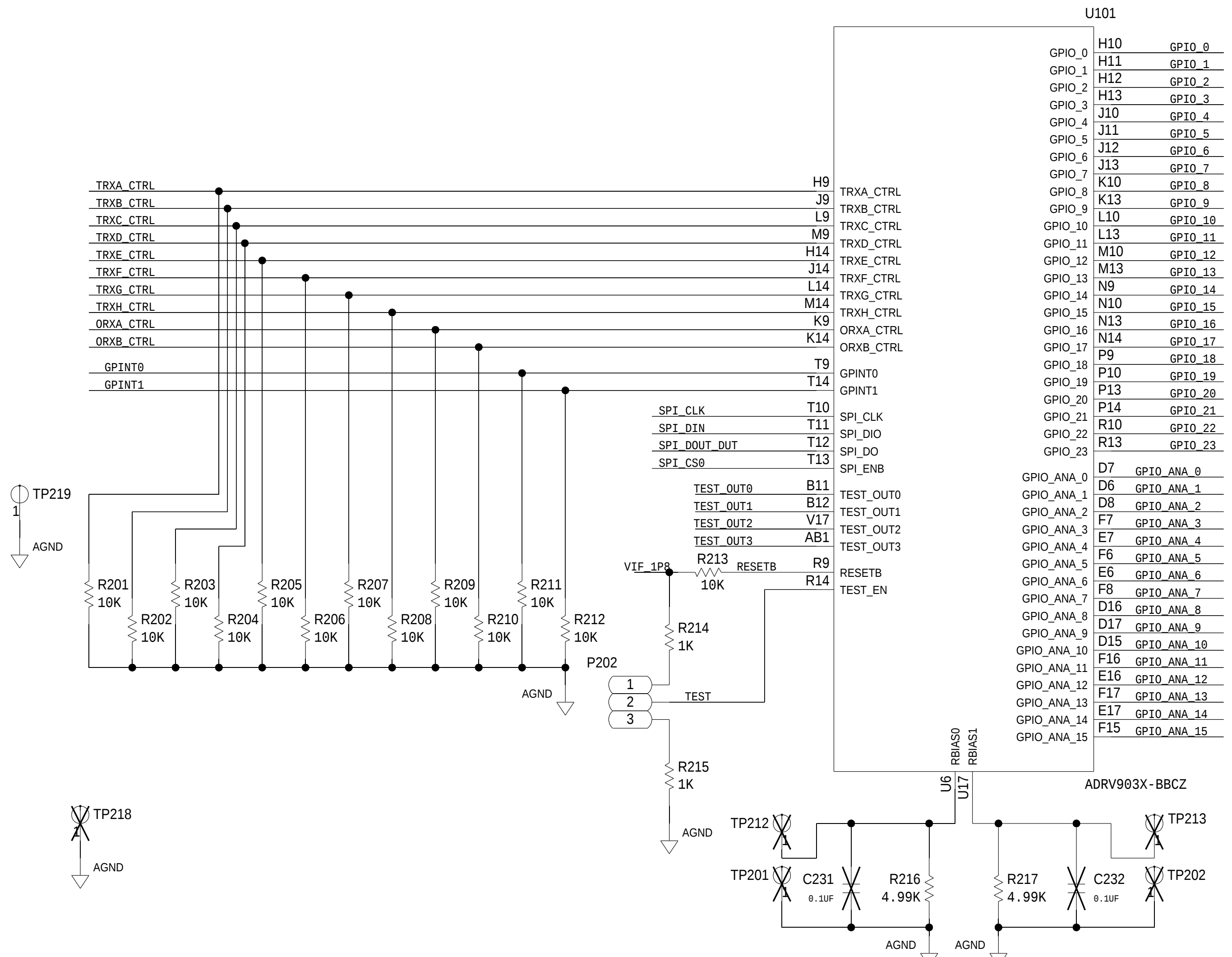


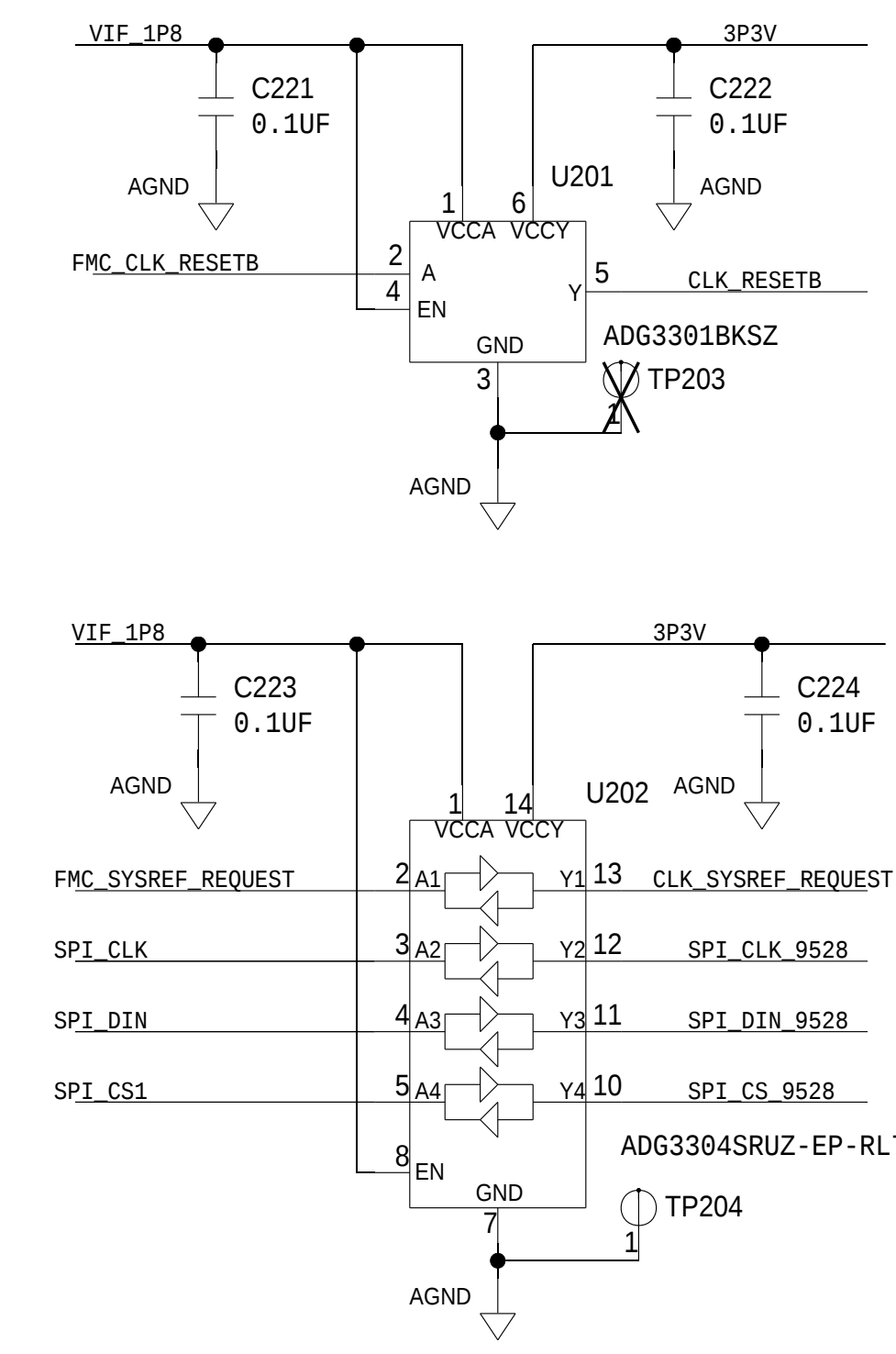
8		7		6		5		4		3		2		1																																																																																														
D	THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.					JUMPER TABLE			REVISIONS																																																																																																			
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A						<table><tr><td colspan="2">TEMPLATE ENGINEER</td><td>DATE</td><td colspan="2" rowspan="2">SCHEMATIC</td><td colspan="2" rowspan="2"></td></tr><tr><td colspan="2">-</td><td></td></tr><tr><td colspan="2">HARDWARE SERVICES</td><td></td><td colspan="2" rowspan="4">HW TYPE : Customer Evaluation Product(s): ADRV903x : N/A PACKAGE : LeadCount-lead BodySize PackageType-family : Pitch-pitch StyleVendor Style</td></tr><tr><td colspan="2">-</td><td></td></tr><tr><td colspan="2">HARDWARE SYSTEMS</td><td></td></tr><tr><td colspan="2">-</td><td></td></tr><tr><td colspan="2">TEST ENGINEER</td><td></td><td colspan="2" rowspan="4">Ultra High Band ADRV903X-UB/PCBZ 6000 MHz to 7500 MHz</td></tr><tr><td colspan="2">-</td><td></td></tr><tr><td colspan="2">COMPONENT ENGINEER</td><td></td></tr><tr><td colspan="2">-</td><td></td></tr><tr><td colspan="2">TEST PROCESS</td><td></td><td colspan="2" rowspan="2">MASTER PROJECT TEMPLATE TBD</td><td colspan="2" rowspan="2">TESTER TEMPLATE no_template</td><td colspan="2" rowspan="2">DRAWING NO. 02_064540-03</td><td colspan="2" rowspan="2">REV. C</td></tr><tr><td colspan="2">-</td><td></td></tr><tr><td colspan="2">HARDWARE RELEASE</td><td></td><td colspan="2" rowspan="3">UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES</td><td colspan="2" rowspan="3">TOLERANCES</td></tr><tr><td colspan="2">-</td><td></td></tr><tr><td colspan="2">DESIGNER</td><td></td></tr><tr><td colspan="2">-</td><td></td><td colspan="2" rowspan="2">DECIMALS X.XX +-0.010 X.XXX +-0.005</td><td colspan="2" rowspan="2">FRACTIONS +1/32</td><td colspan="2" rowspan="2">ANGLES +2</td></tr><tr><td colspan="2">PTD ENGINEER</td><td></td></tr><tr><td colspan="2">-</td><td></td><td colspan="2" rowspan="2">SIZE D</td><td colspan="2" rowspan="2">SCALE 1:1</td><td colspan="2" rowspan="2">CODE ID NO. CodeID</td><td colspan="2" rowspan="2">SHEET 1 OF 16</td></tr><tr><td colspan="2">CHECKER</td><td></td></tr><tr><td colspan="2">-</td><td></td></tr></table>									TEMPLATE ENGINEER		DATE	SCHEMATIC				-			HARDWARE SERVICES			HW TYPE : Customer Evaluation Product(s): ADRV903x : N/A PACKAGE : LeadCount-lead BodySize PackageType-family : Pitch-pitch StyleVendor Style		-			HARDWARE SYSTEMS			-			TEST ENGINEER			Ultra High Band ADRV903X-UB/PCBZ 6000 MHz to 7500 MHz		-			COMPONENT ENGINEER			-			TEST PROCESS			MASTER PROJECT TEMPLATE TBD		TESTER TEMPLATE no_template		DRAWING NO. 02_064540-03		REV. C		-			HARDWARE RELEASE			UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		TOLERANCES		-			DESIGNER			-			DECIMALS X.XX +-0.010 X.XXX +-0.005		FRACTIONS +1/32		ANGLES +2		PTD ENGINEER			-			SIZE D		SCALE 1:1		CODE ID NO. CodeID		SHEET 1 OF 16		CHECKER			-		
	TEMPLATE ENGINEER		DATE	SCHEMATIC																																																																																																								
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8		7		6		5		4		3		2		1																																																																																														

DIGITAL/ANALOG I/O

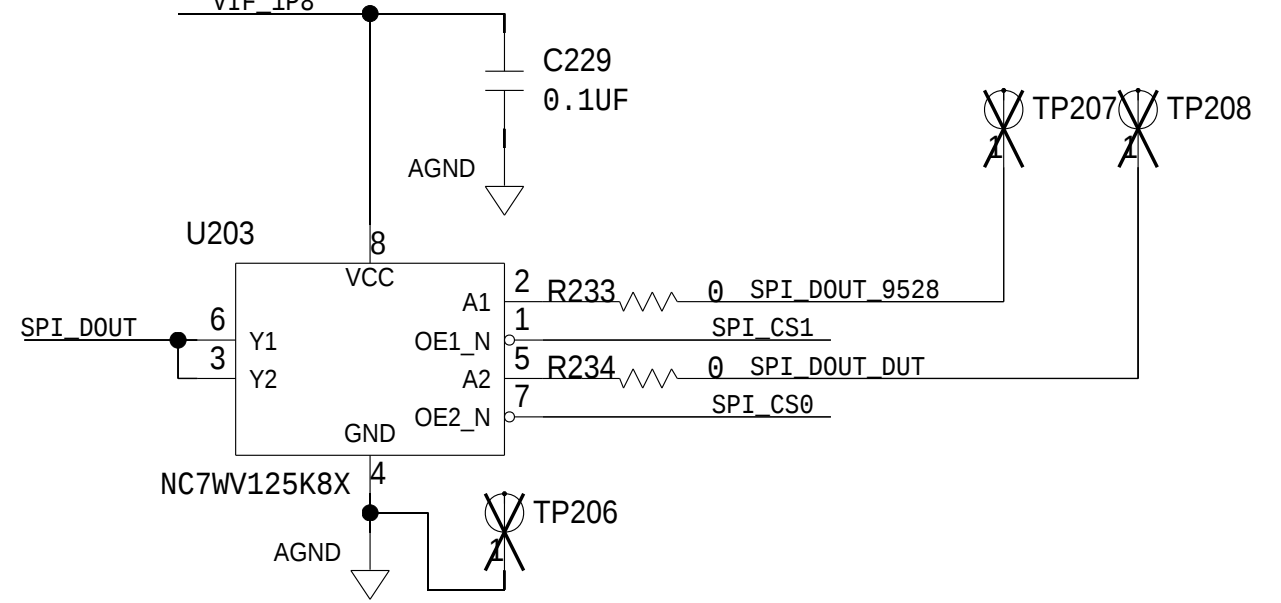
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



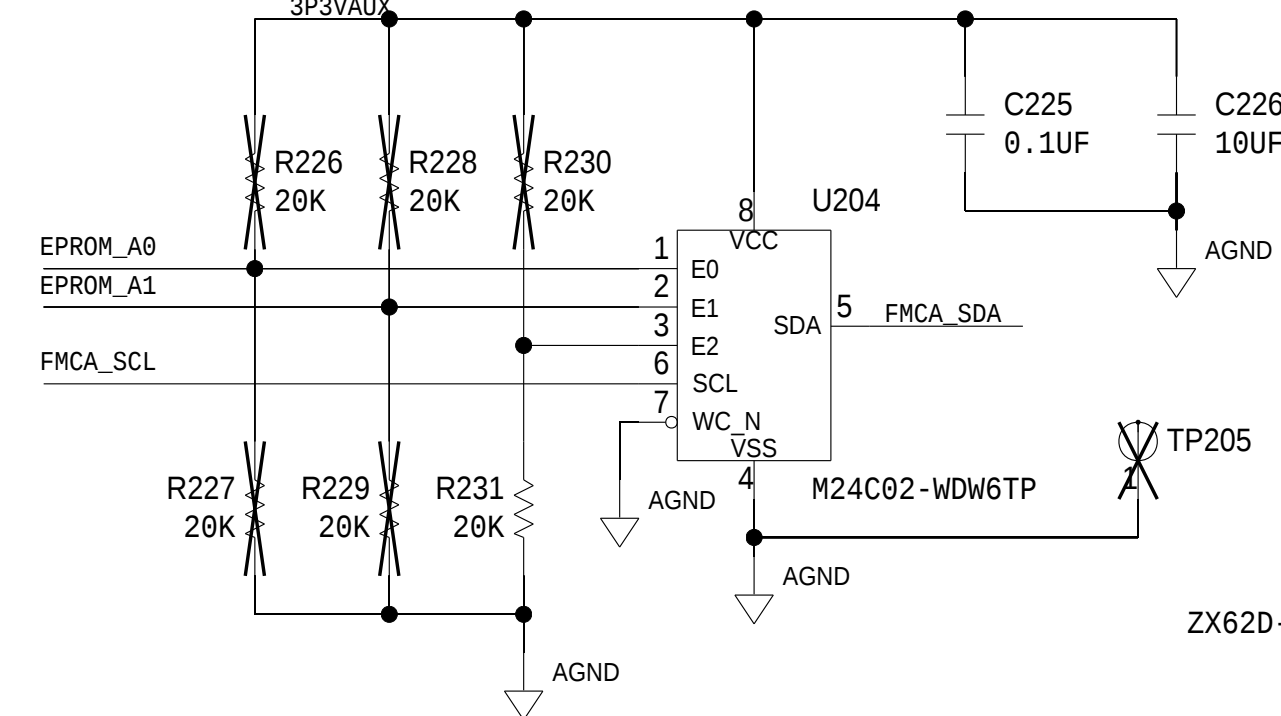
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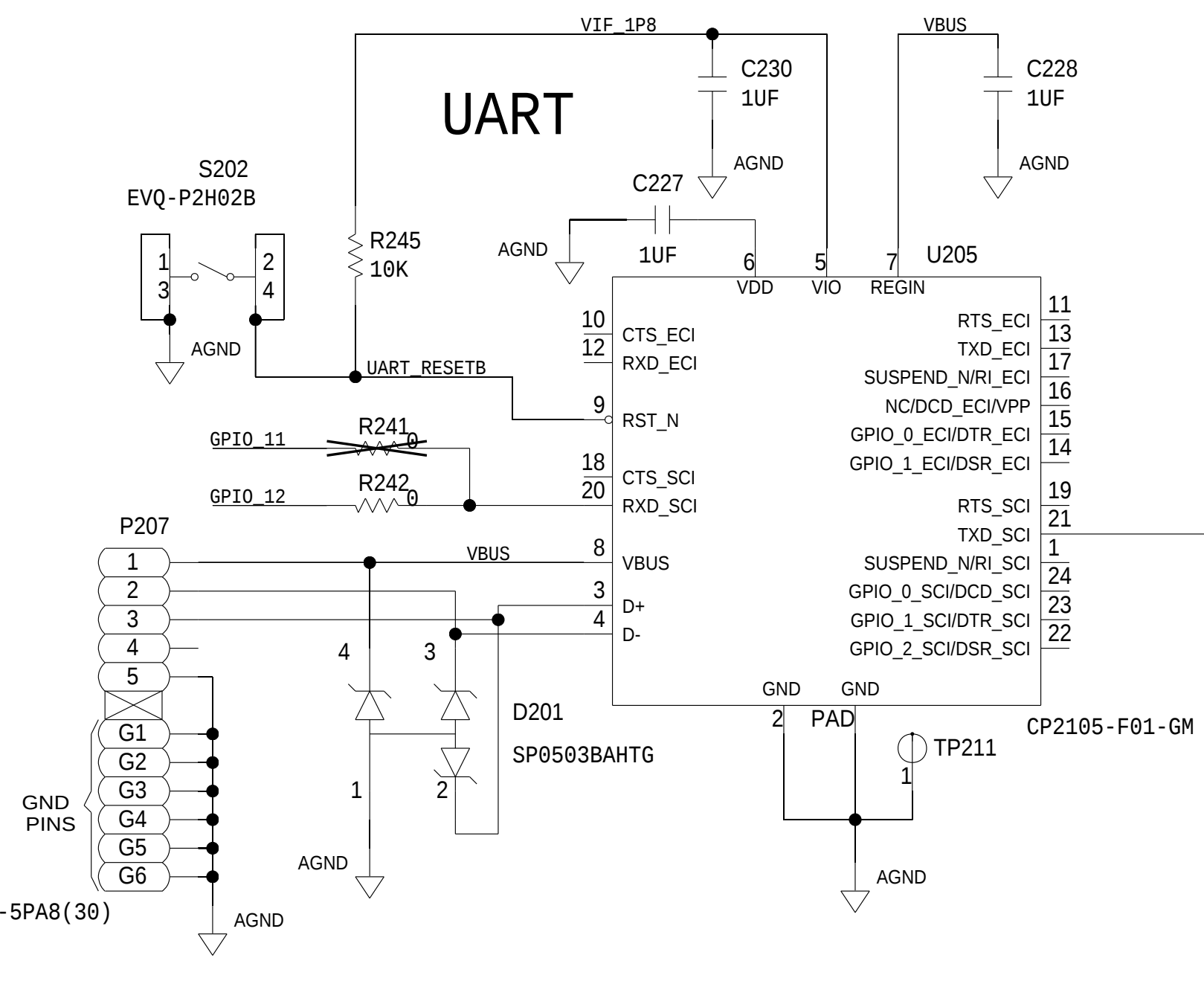
SPI INTERFACE BUFFER



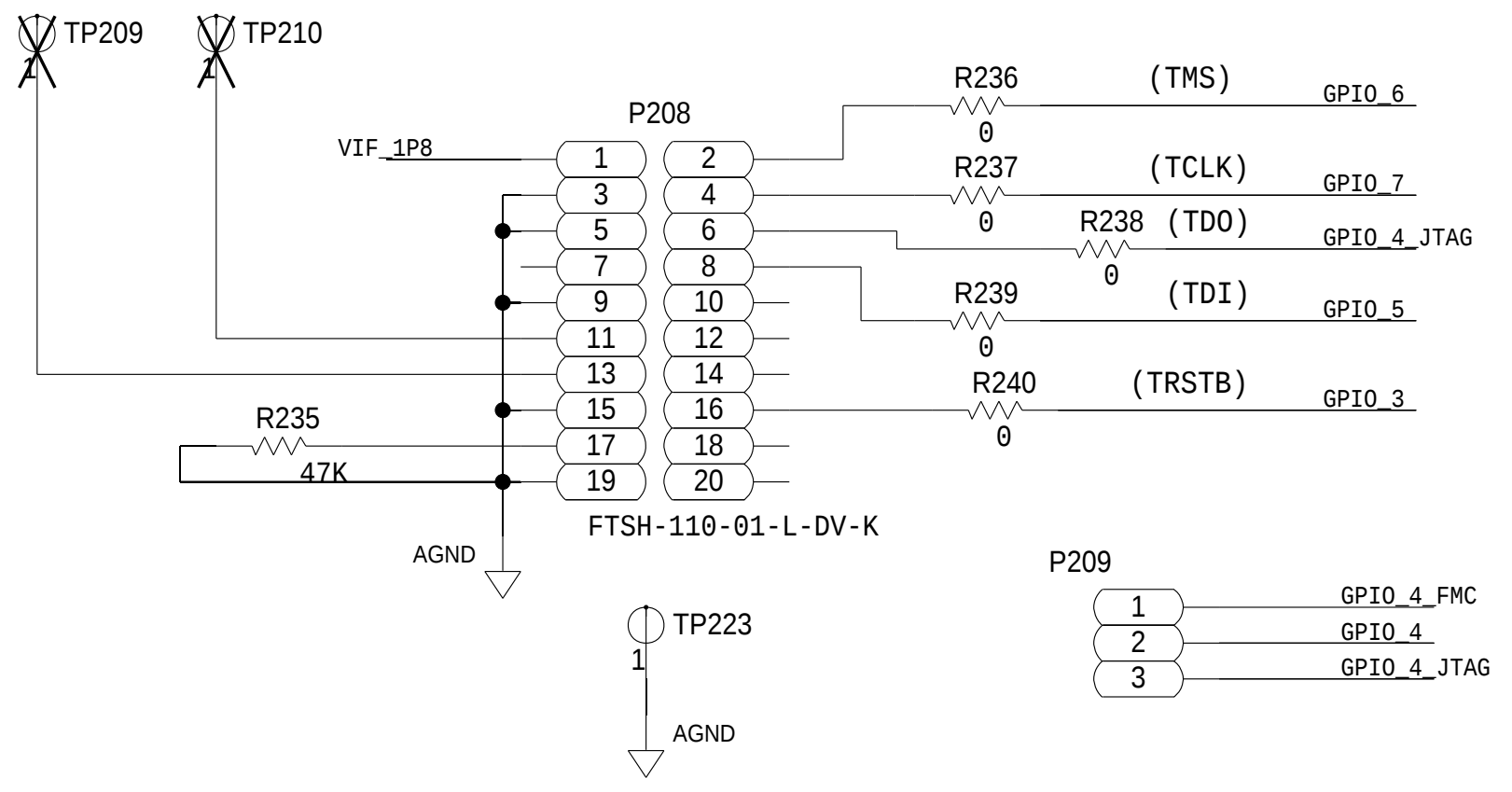
BOARD ID EEPROM



UART



JTAG INTERFACE

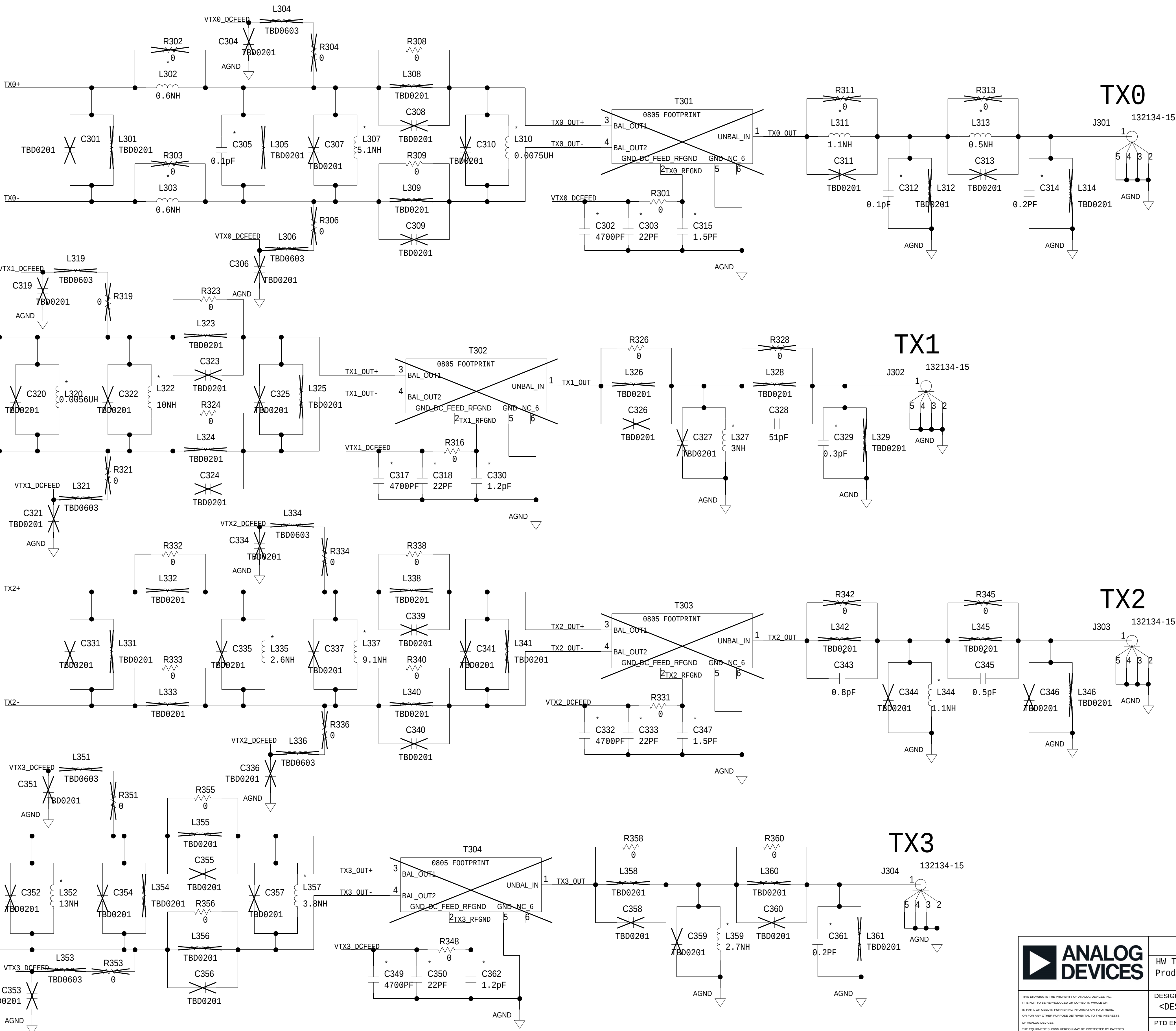


SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : ADRV903x : N/A			
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PTD ENGINEER -	SIZE D	SCALE 1:1	SHEET 2 OF 16

TRANSMITTER RF OUTPUT

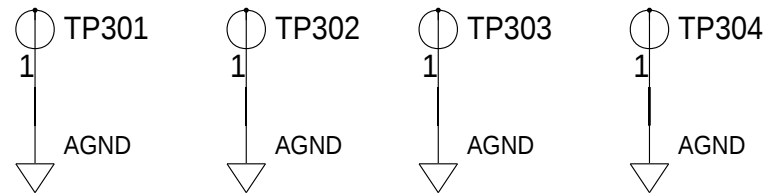
EVB MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

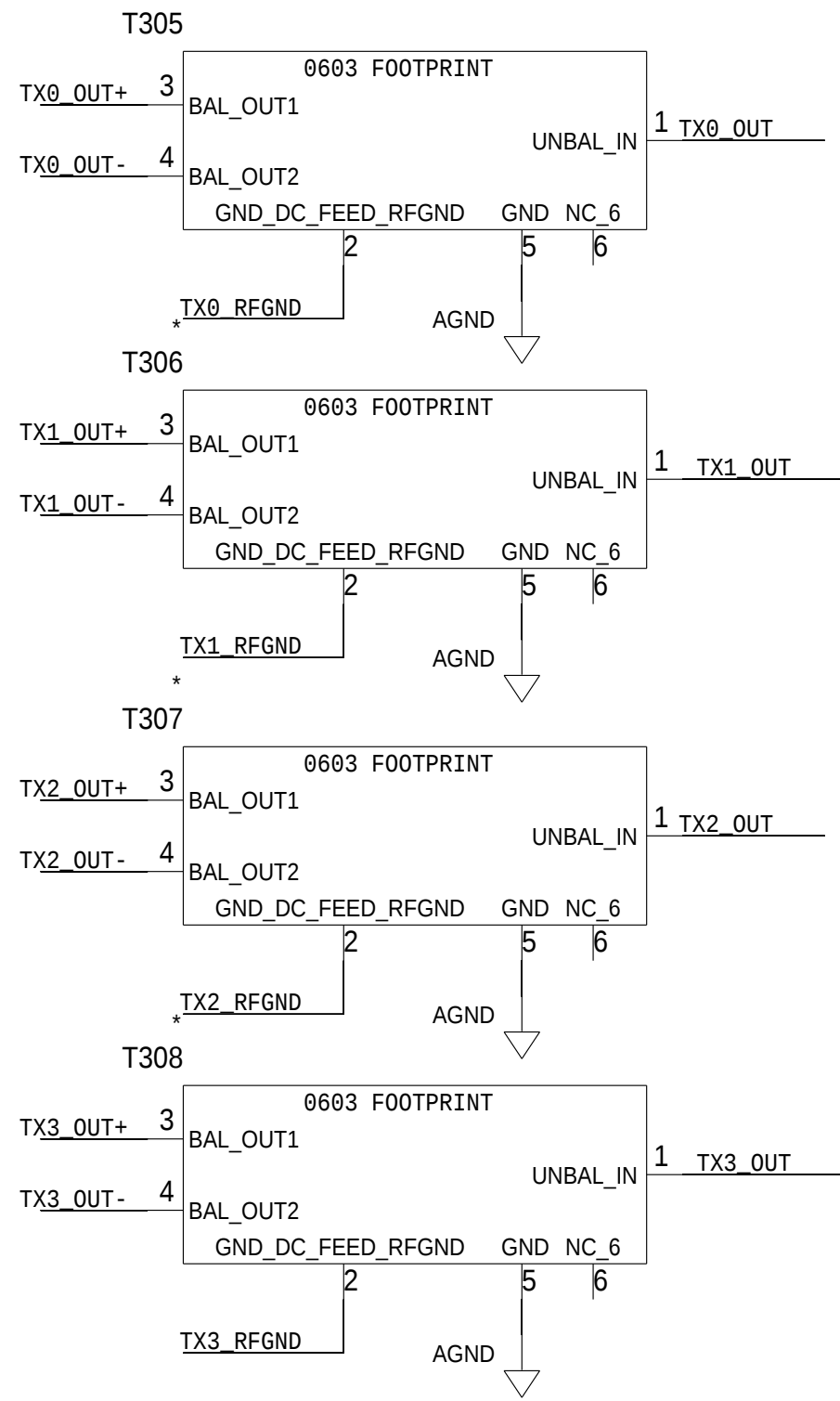


U101	
TX0P	C1 TX0+
TX0N	B1 TX0-
TX1P	G1 TX1+
TX1N	F1 TX1-
TX2P	R1 TX2+
TX2N	P1 TX2-
TX3P	W1 TX3+
TX3N	B22 TX4+
TX4P	C22 TX4-
TX5P	F22 TX5+
TX5N	G22 TX5-
TX6P	P22 TX6+
TX6N	R22 TX6-
TX7P	V22 TX7+
TX7N	W22 TX7-

ADRV903X-BBCZ



OVERLAP TX BALUNS



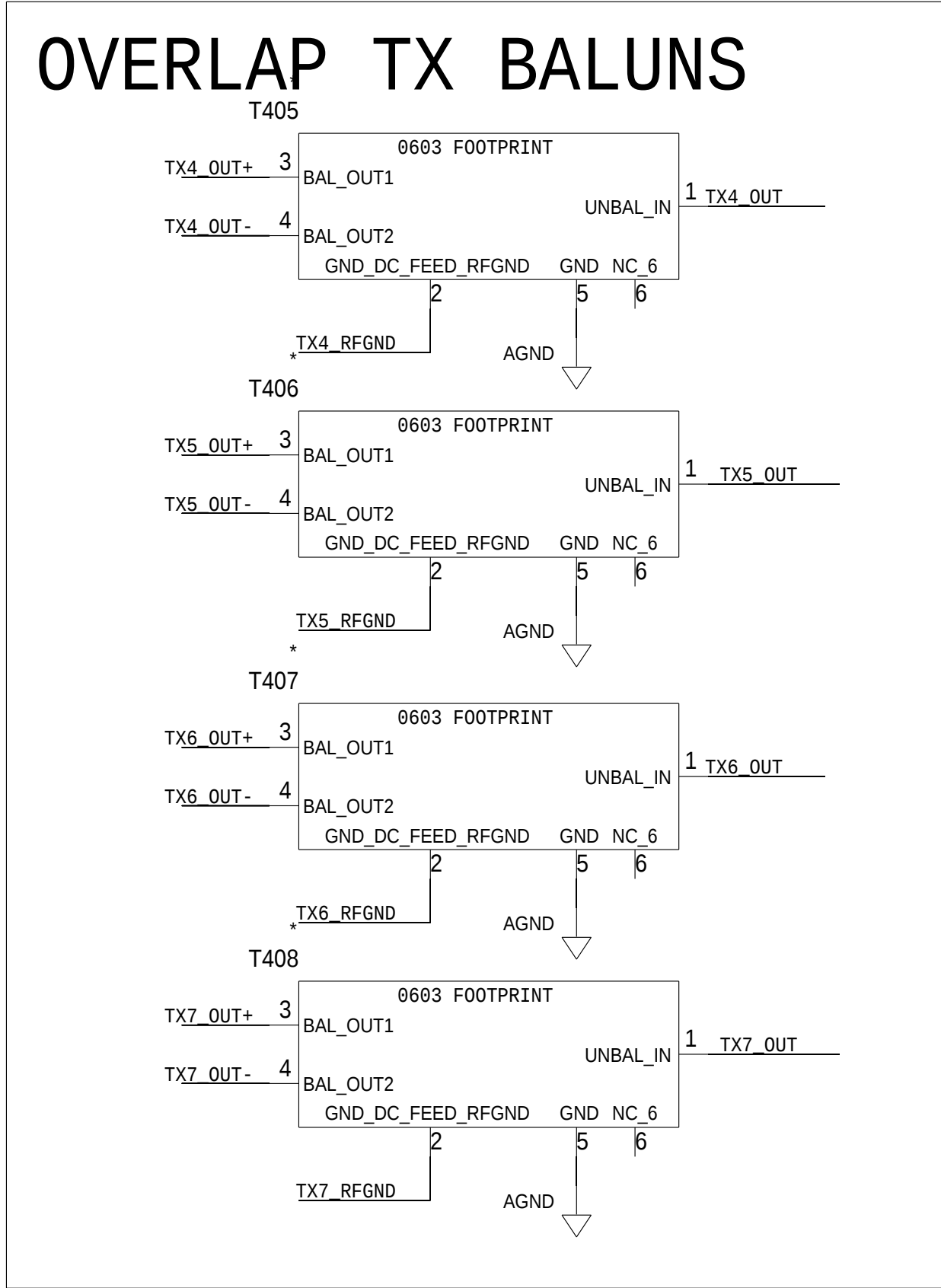
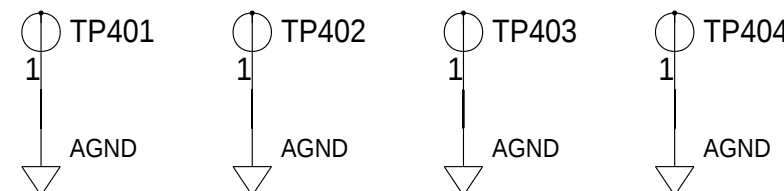
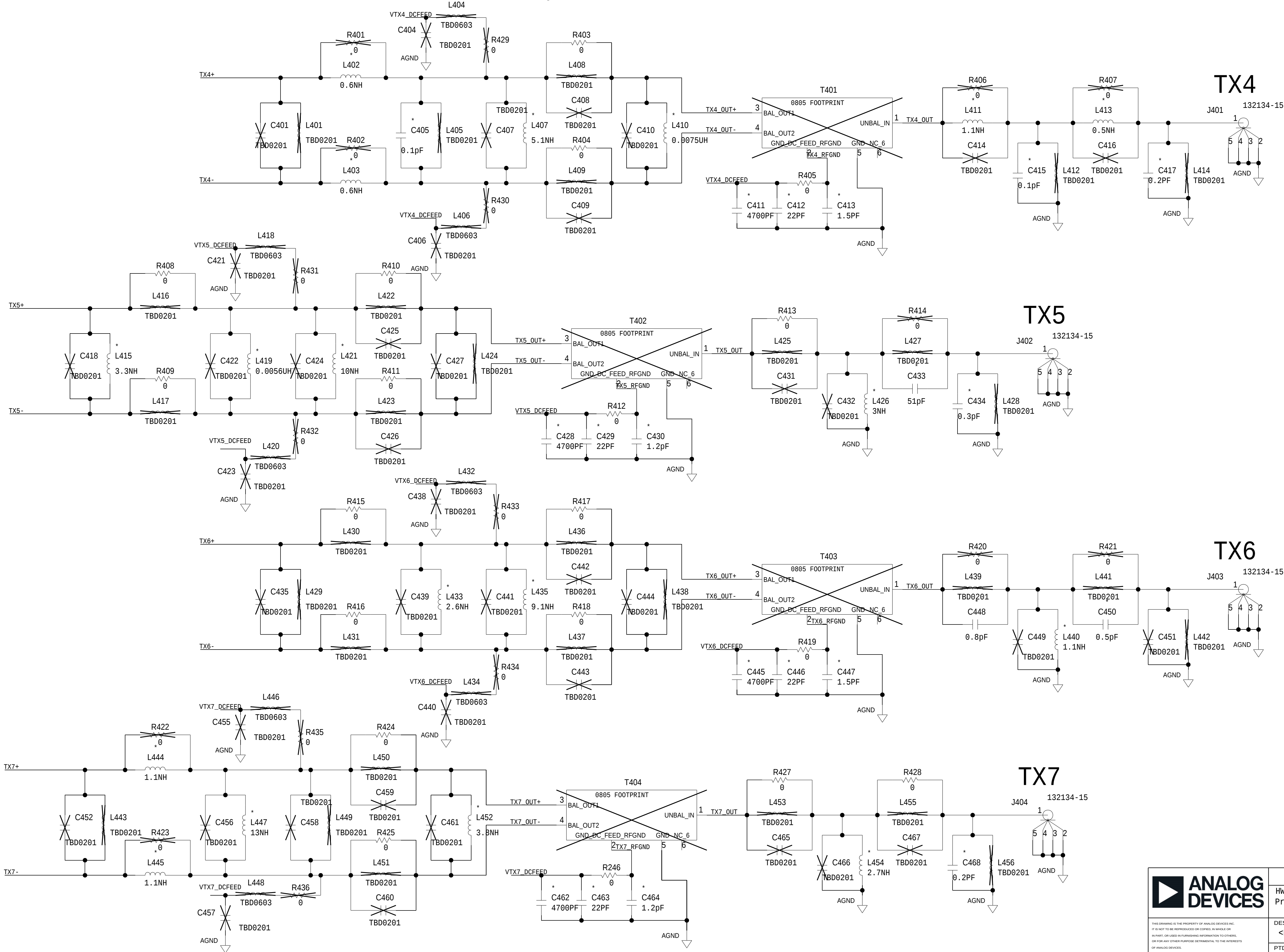
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SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : ADRV903x : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_064540-03	REV C	
PTD ENGINEER -	SIZE D	SCALE 1:1	SHEET 3 OF 16

TRANSMITTER RF OUTPUT

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
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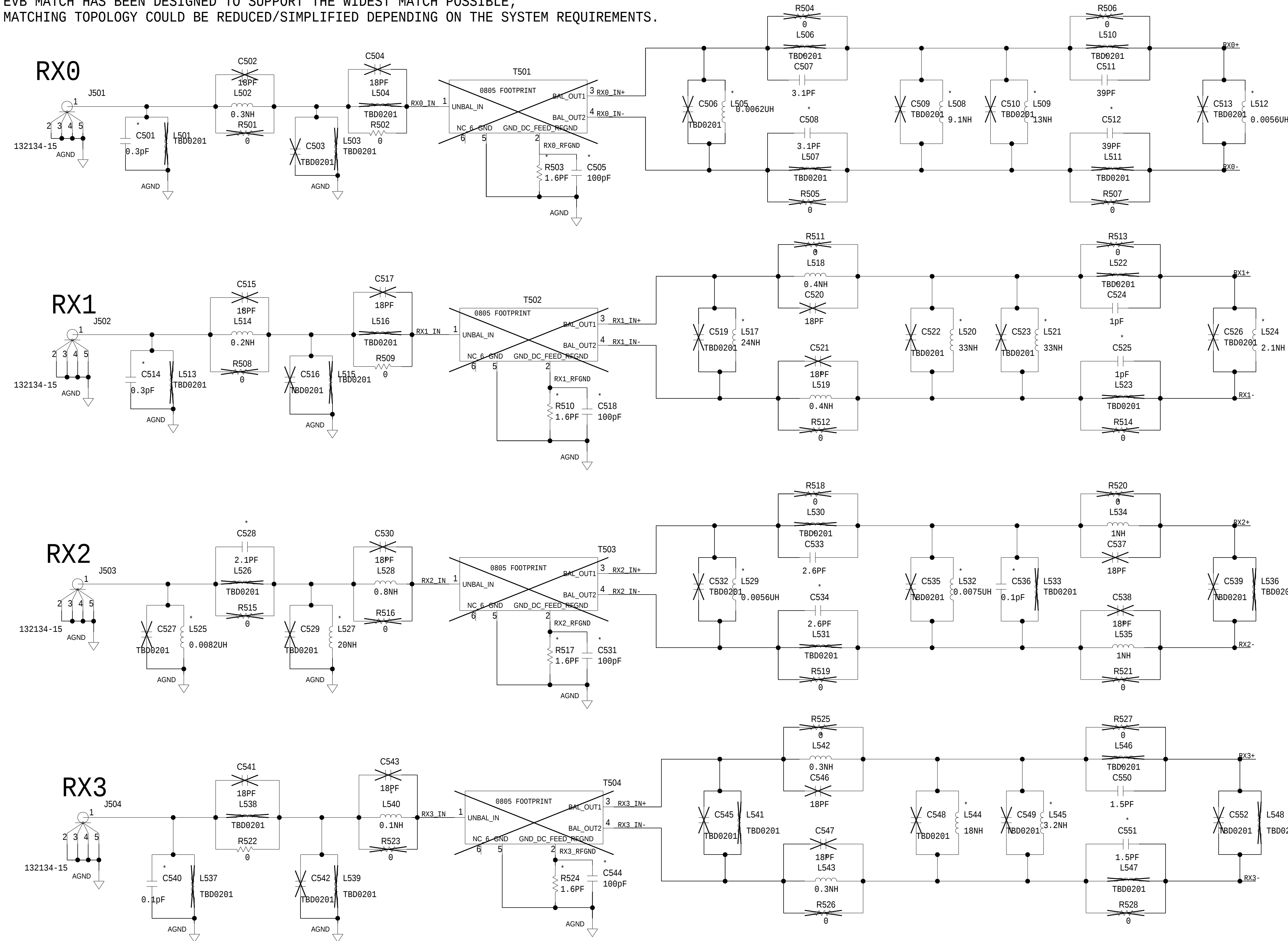
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REV	DESCRIPTION	DATE	APPROVED



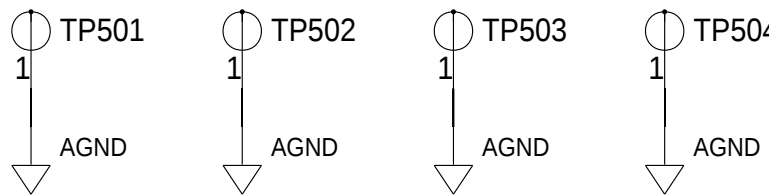
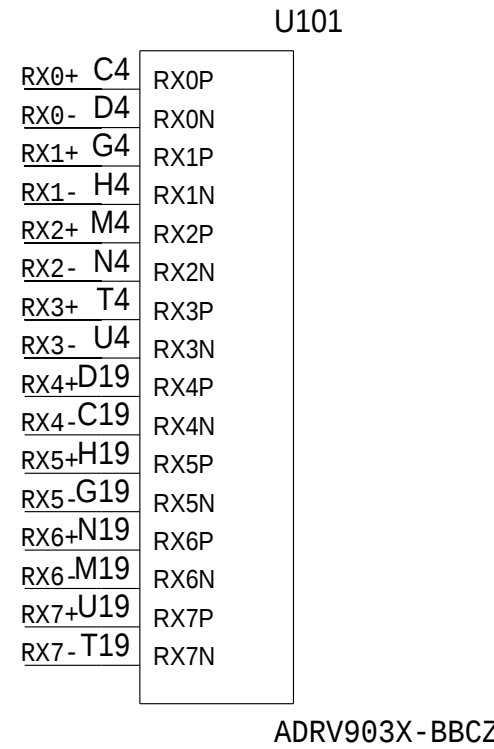
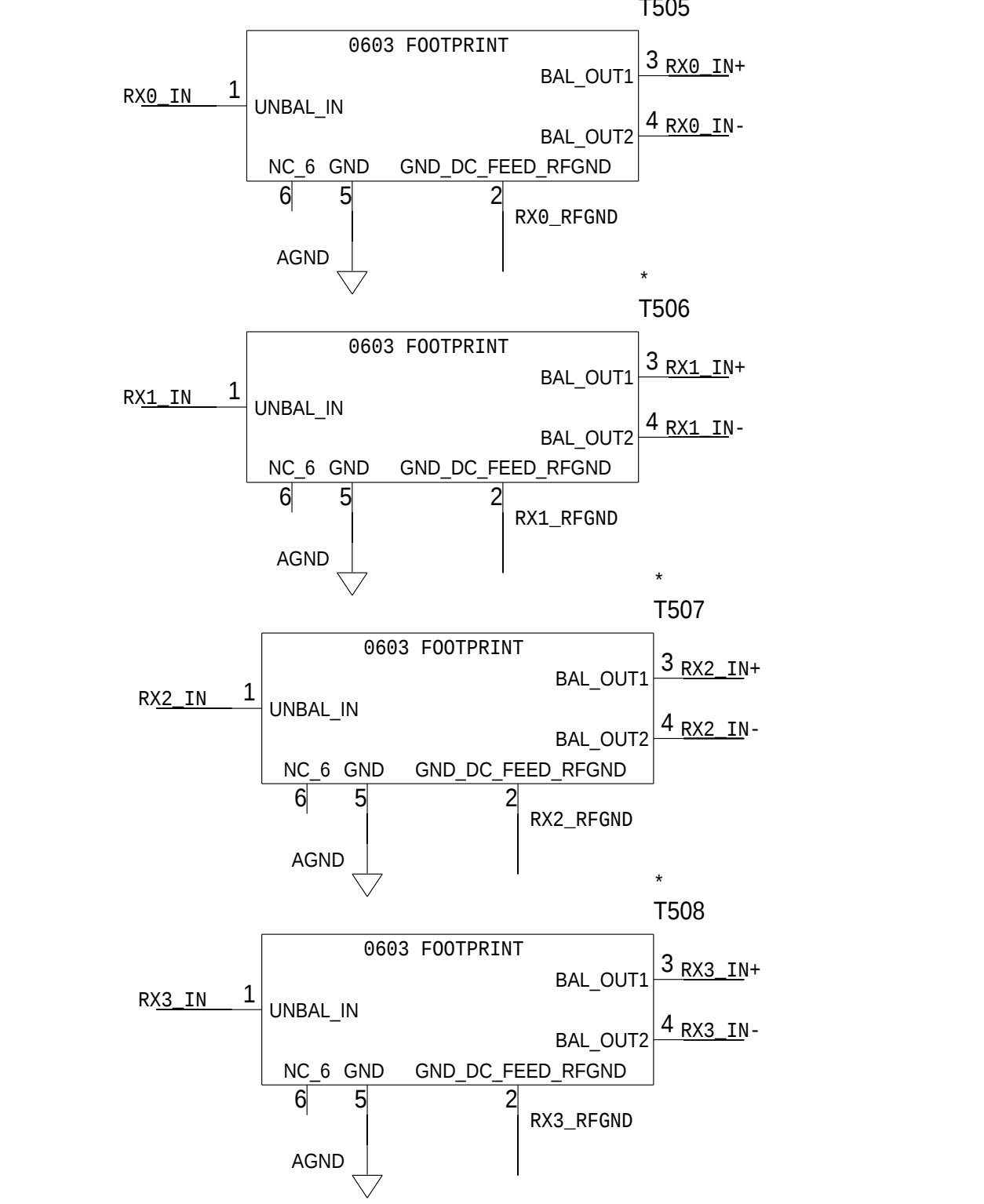
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HW TYPE : Customer Evaluation Product(s) : ADRV903x : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_064540-03	REV C	
PTD ENGINEER -	SIZE D	SCALE 1:1	SHEET 4 OF 16

RECEIVER RF INPUT

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.



OVERLAP RX BALUNS



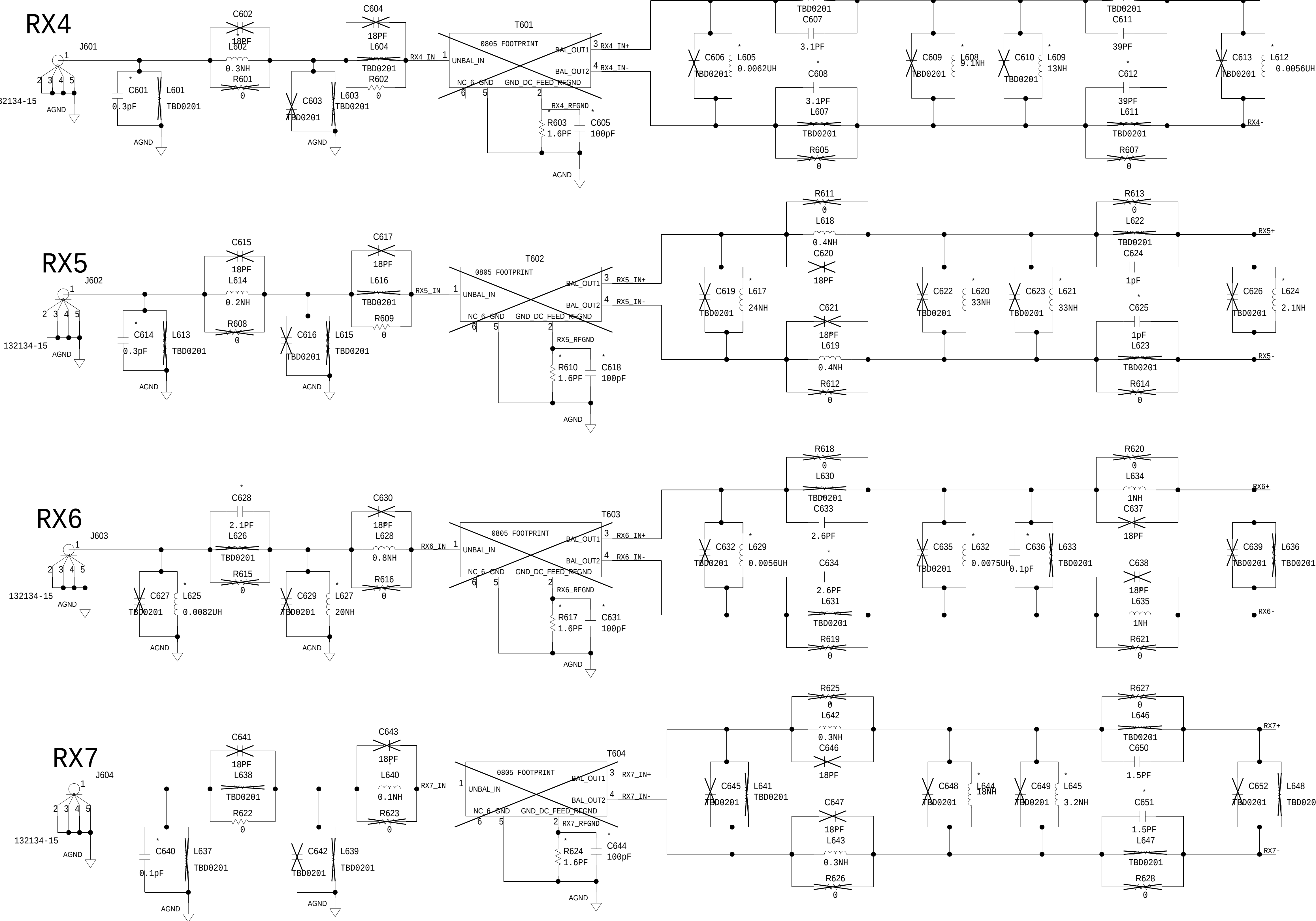
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SCHEMATIC			
HW TYPE : Customer Evaluation			
Product(s): ADRV903x			
: N/A			
DESIGN VIEW	DRAWING NO.		REV
<DESIGN_VIEW>	02_064540-03		C
PTD ENGINEER	SIZE	SCALE	SHEET 5 OF 16
-	D	1:1	

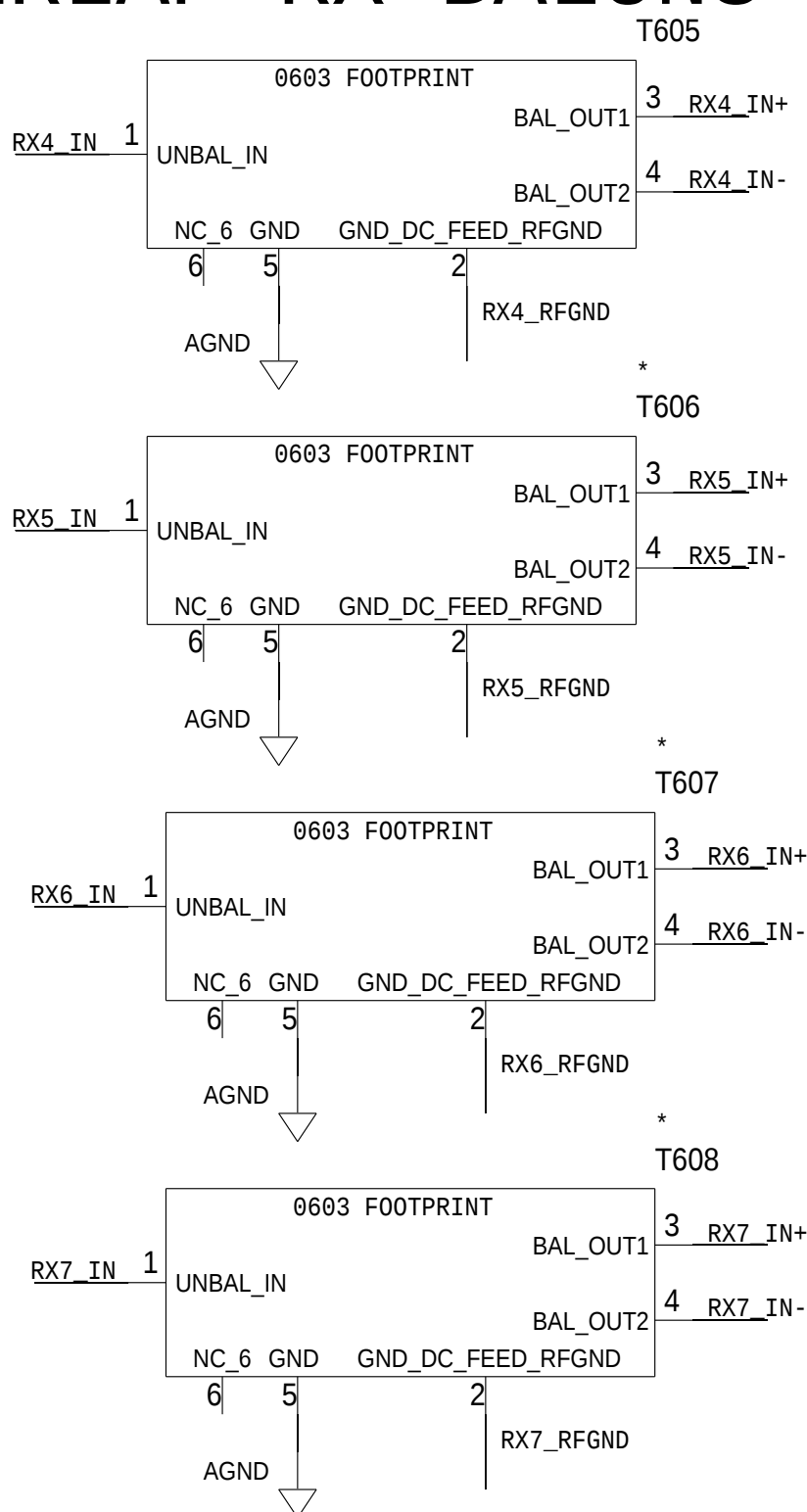
RECEIVER RF INPUT

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



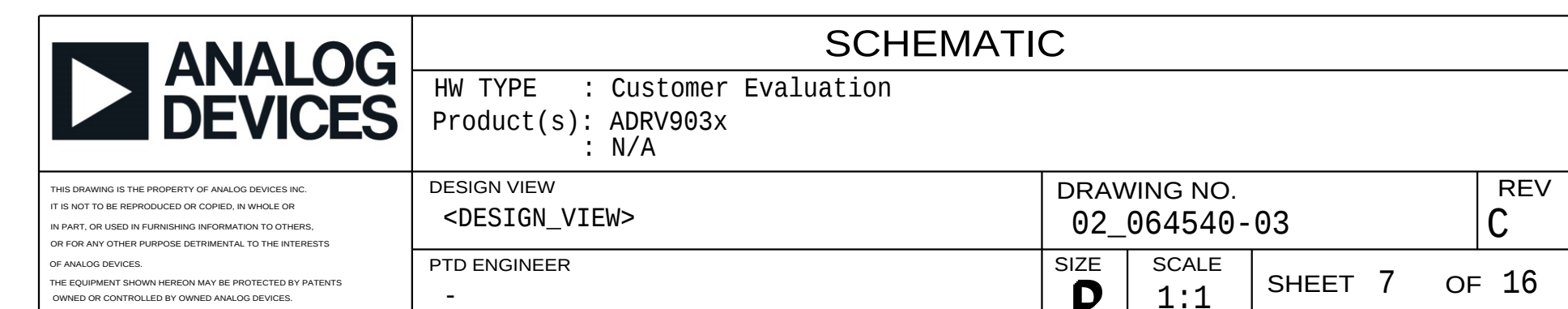
OVERLAP RX BALUNS



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SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): ADRV903x : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_064540-03	REV C	
PTD ENGINEER -	SIZE D	SCALE 1:1	SHEET 6 OF 16

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MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

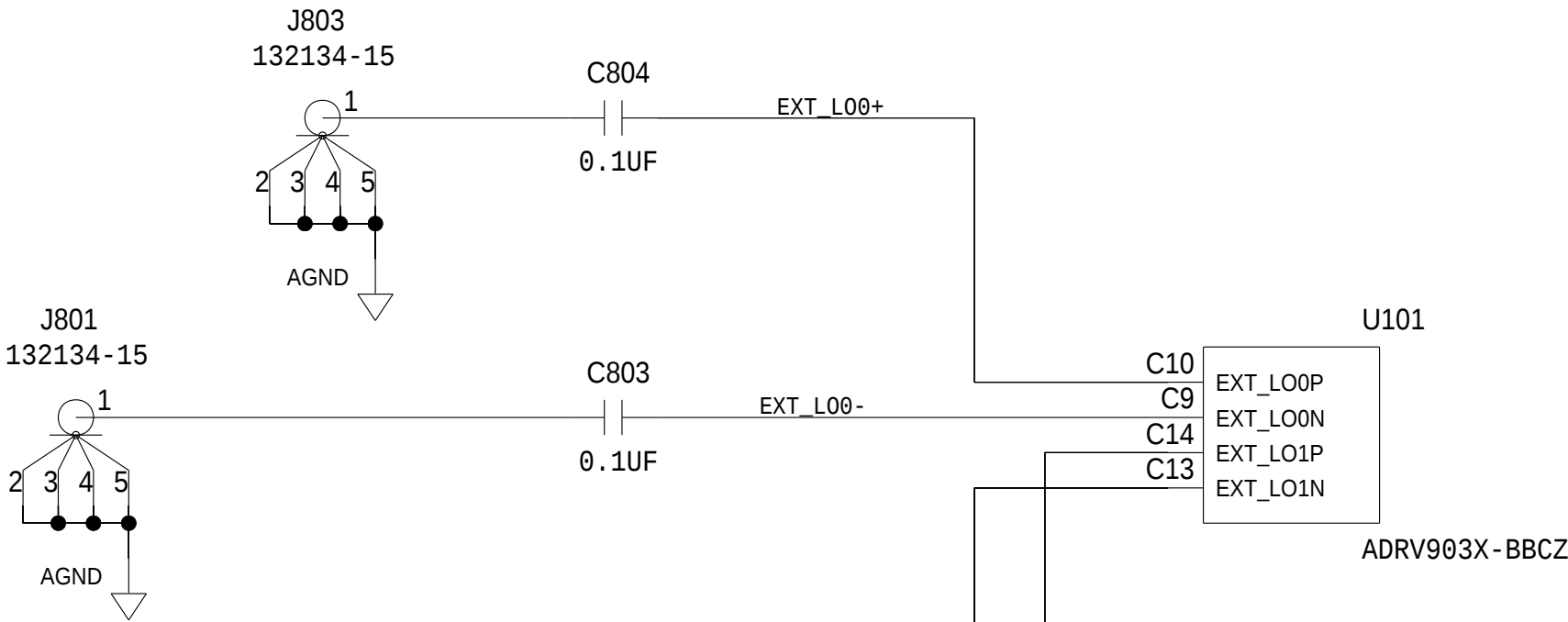


EXTERNAL L0 IN/OUT

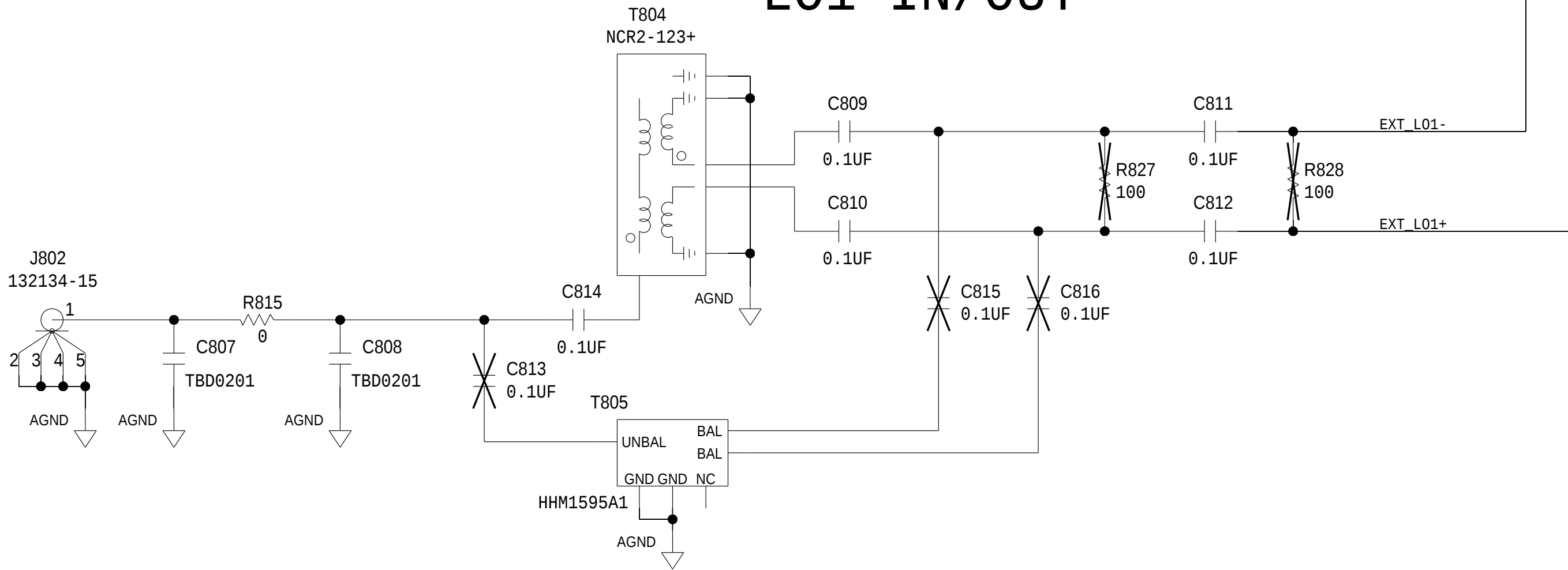
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

L00 IN/OUT



L01 IN/OUT



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SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): ADRV903x : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_064540-03	REV C	
PTD ENGINEER -	SIZE D	SCALE 1:1	SHEET 8 OF 16

CLOCK GENERATION/DISTRIBUTION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

D

D

EVB REF CLK

C

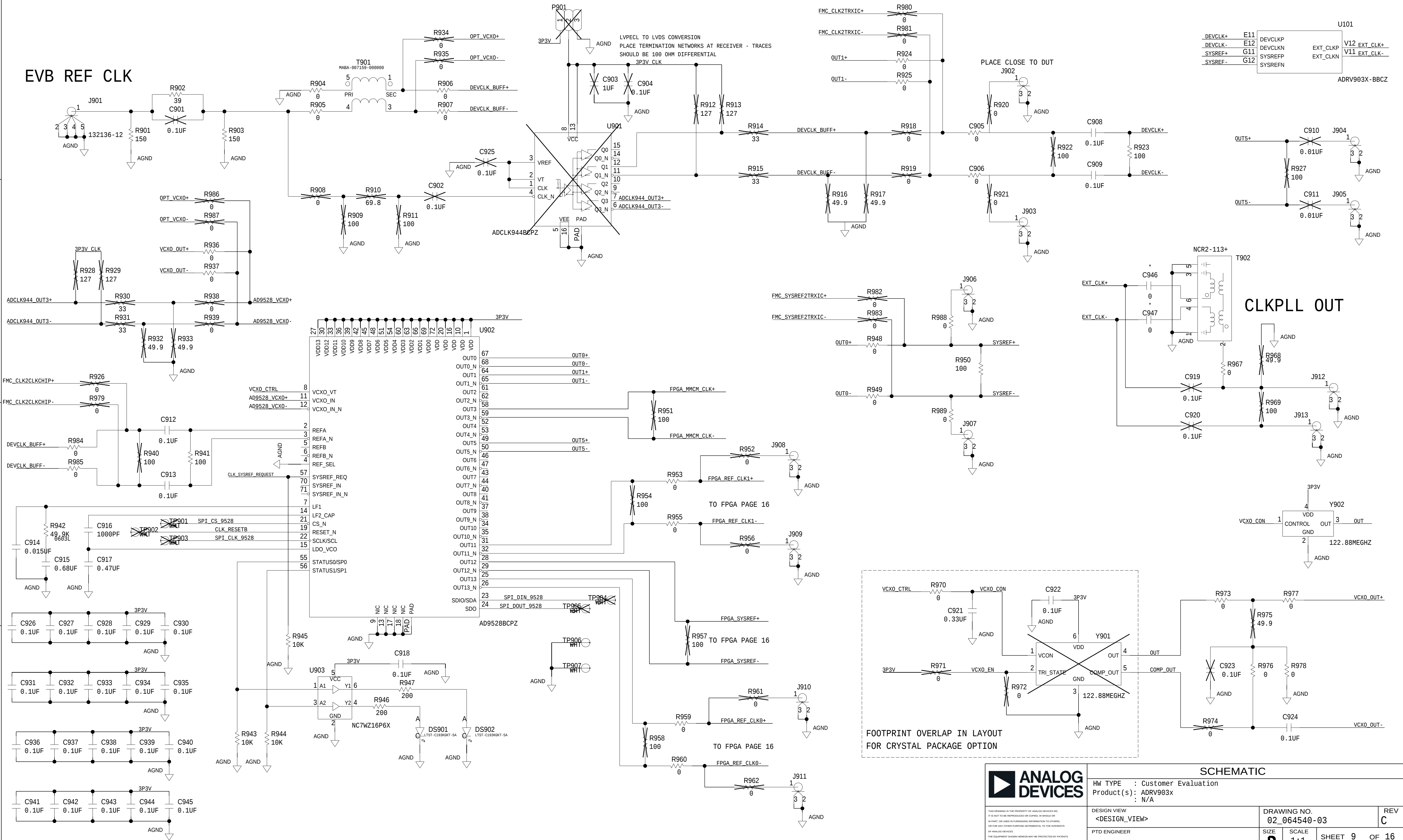
C

B

B

A

A



DEVCLK+	E11	DEVCLKP	EXT_CLKP	V12 EXT_CLK+
DEVCLK-	E12	DEVCLKN	EXT_CLKN	V11 EXT_CLK-
SYSREF+	G11	SYSREFP		
SYSREF-	G12	SYSREFN		

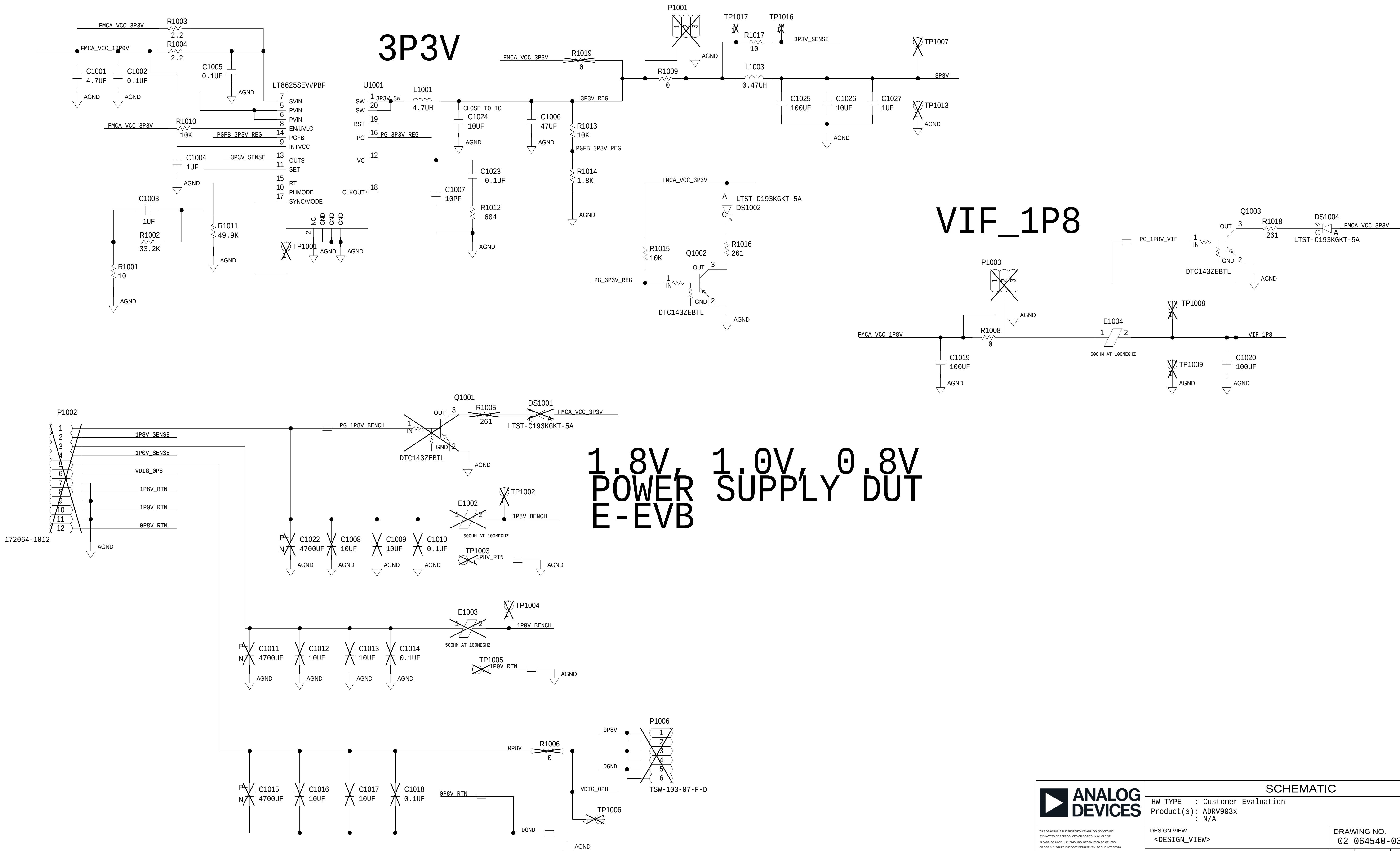
CLKPLL OUT

SCHMATIC
HW TYPE : Customer Evaluation
Product(s) : ADRV903x
: N/A

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_064540-03	REV C
PTD ENGINEER -	SIZE D	SCALE 1:1
	SHEET 9	OF 16

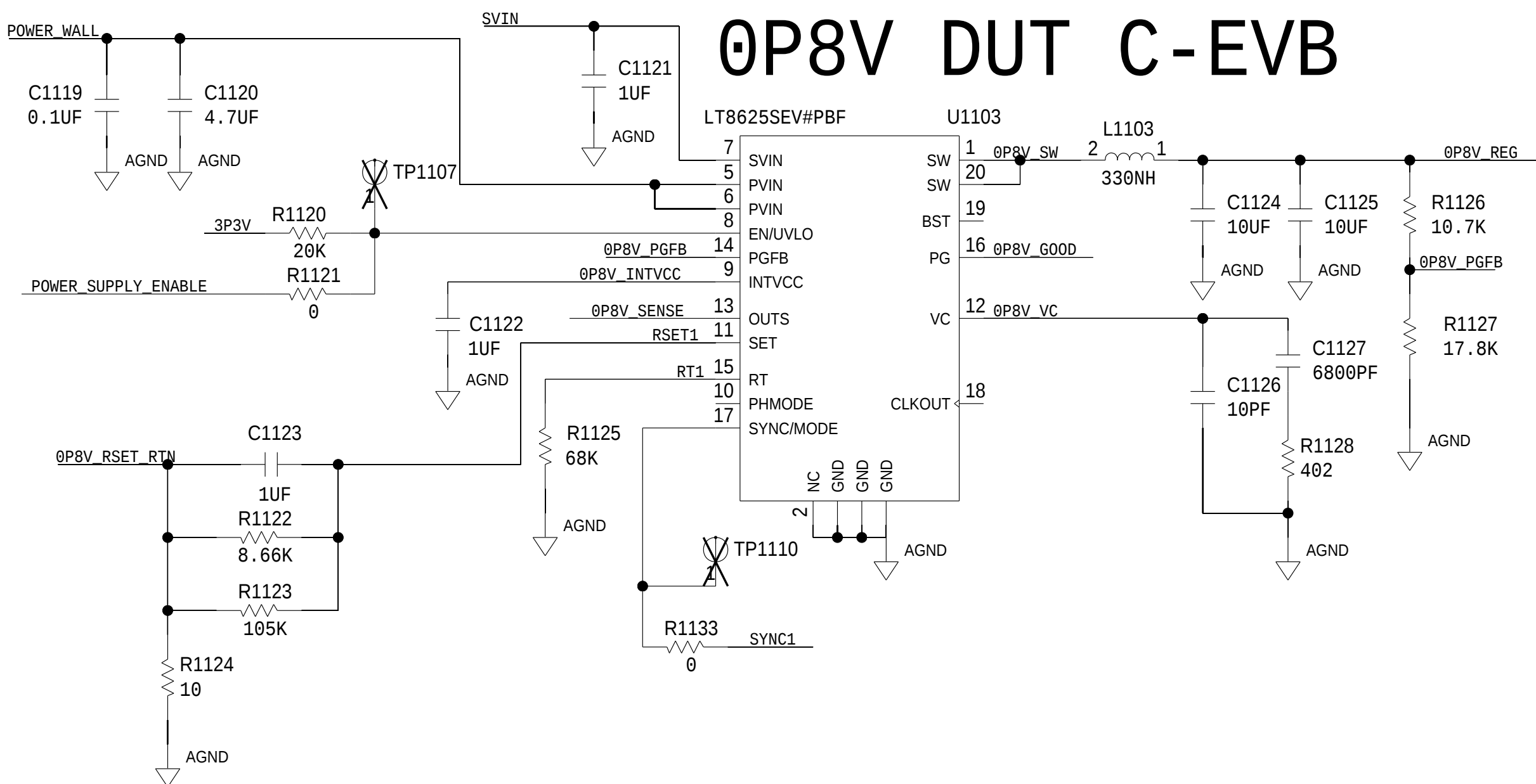
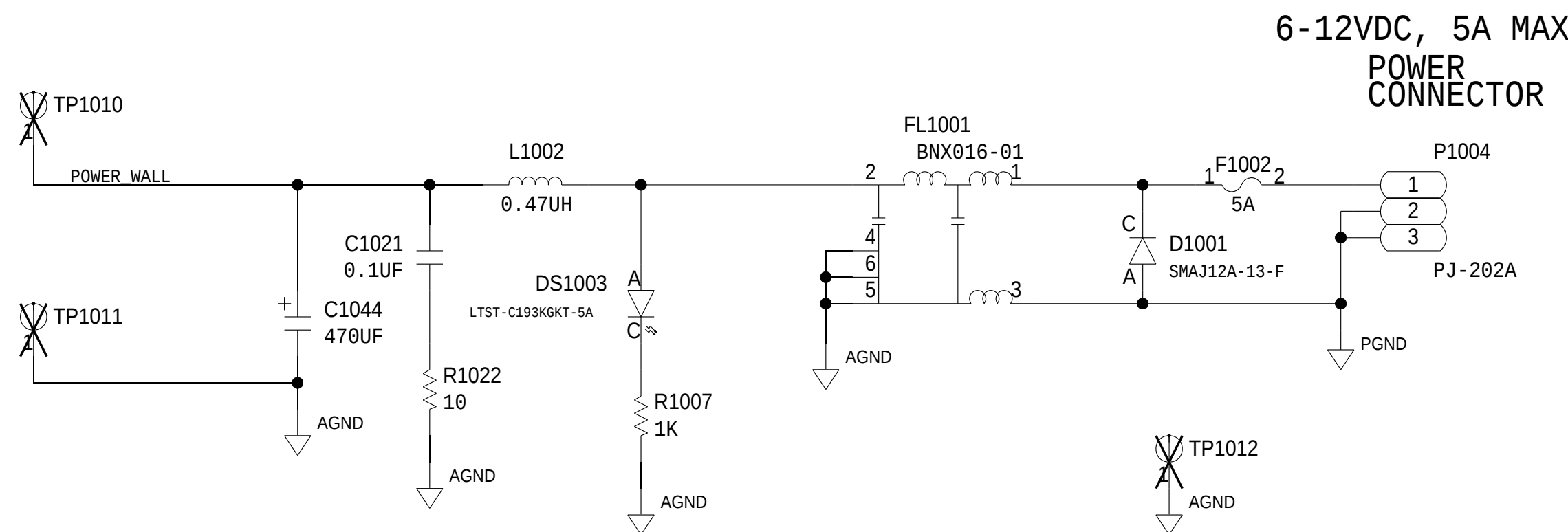
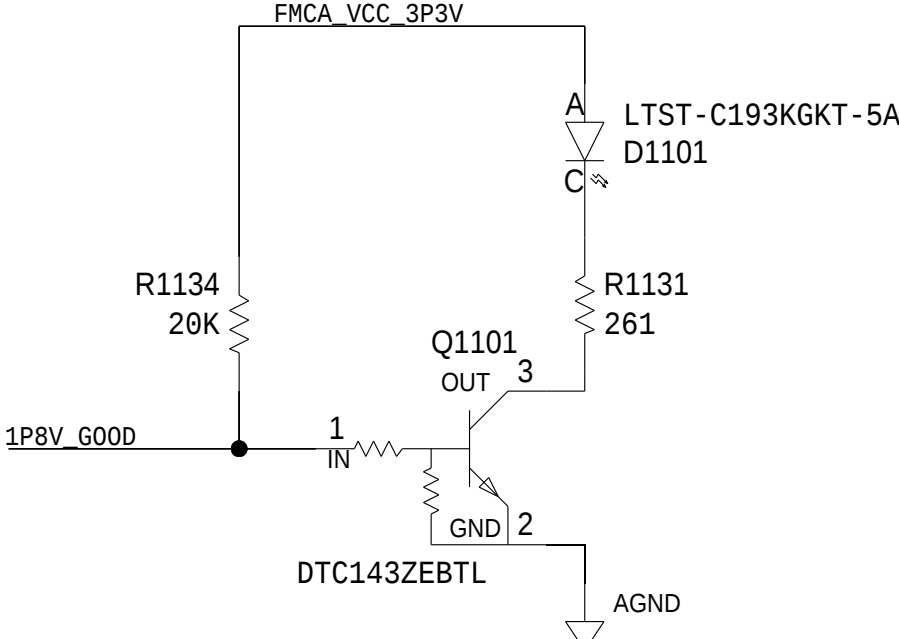
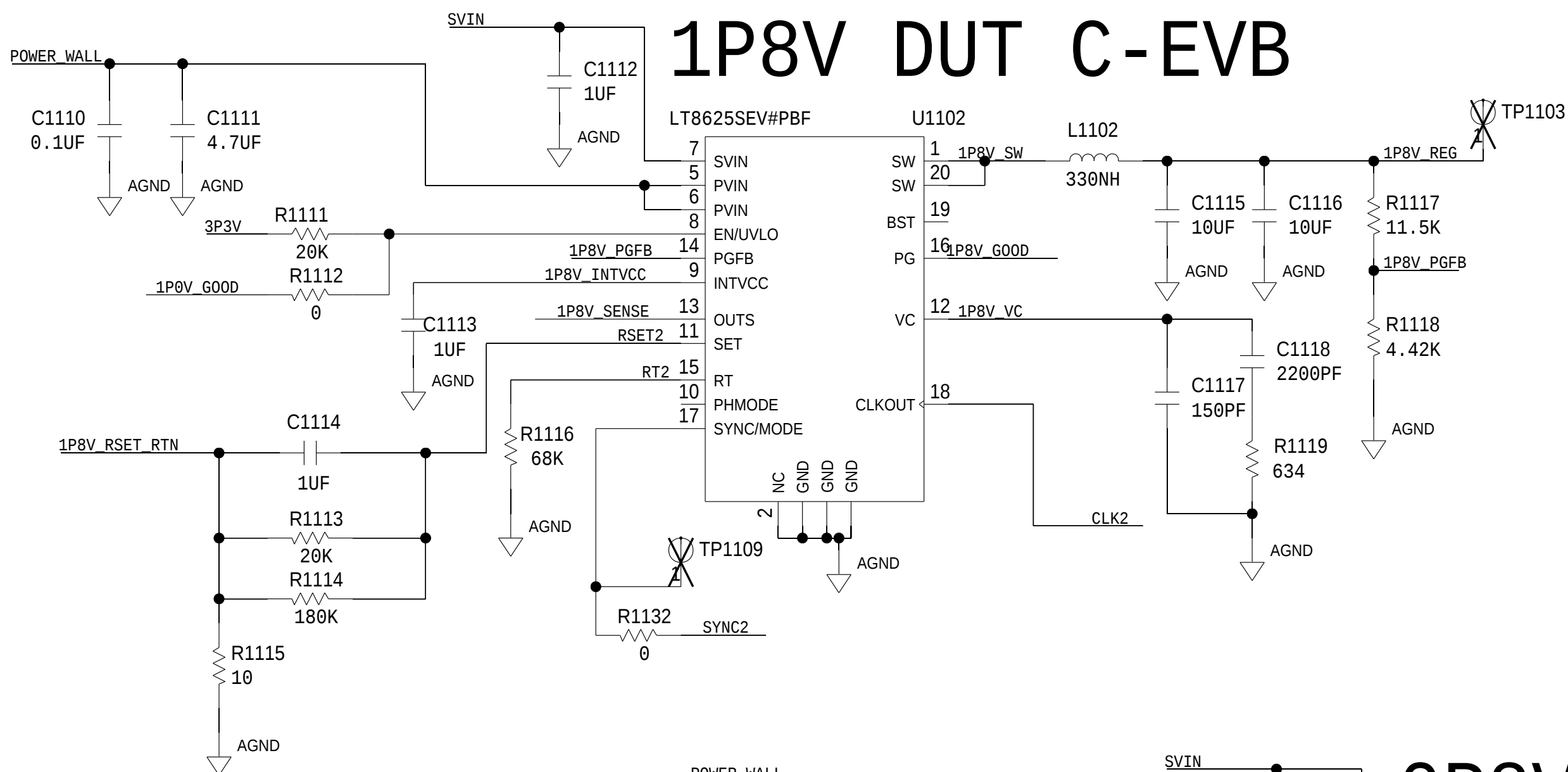
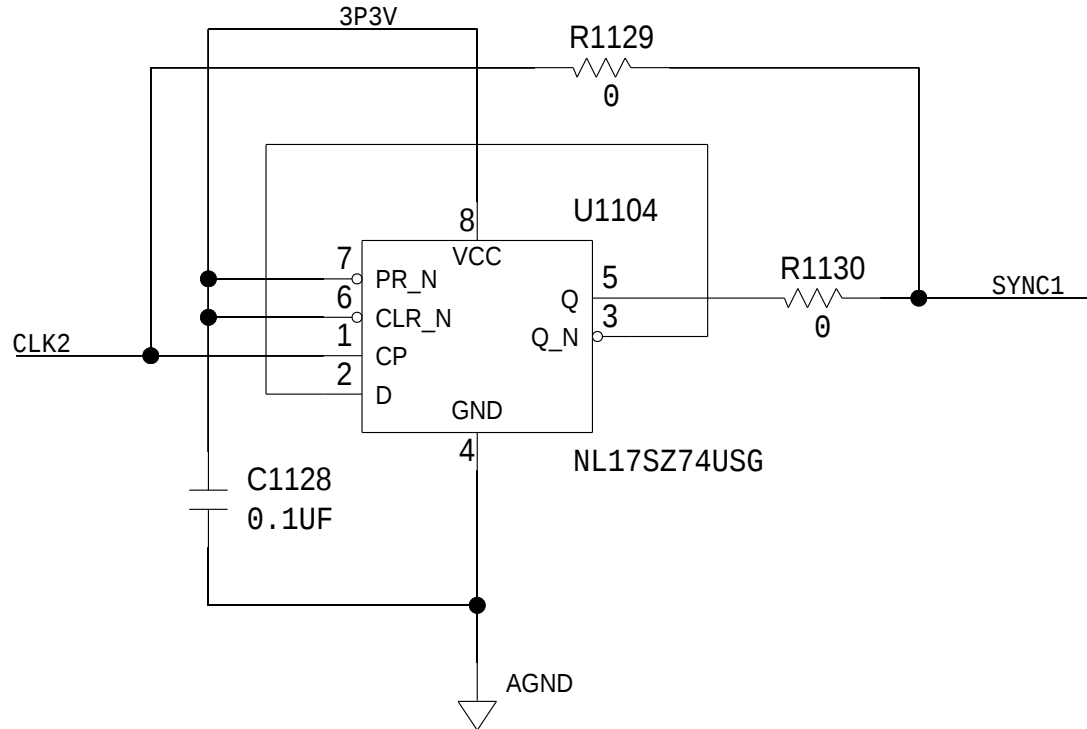
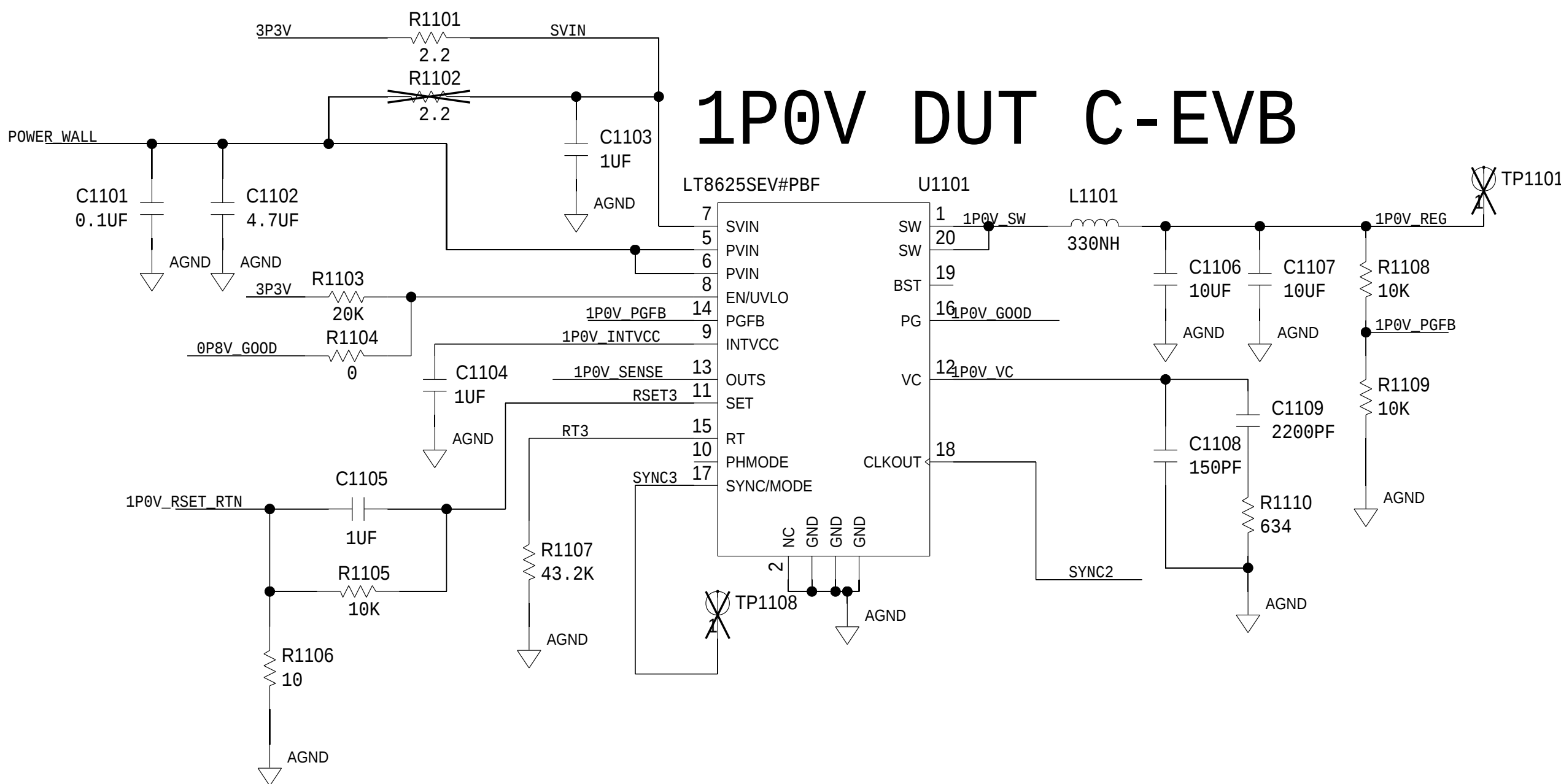
POWER SUPPLY

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



POWER SILENT SWITCHER

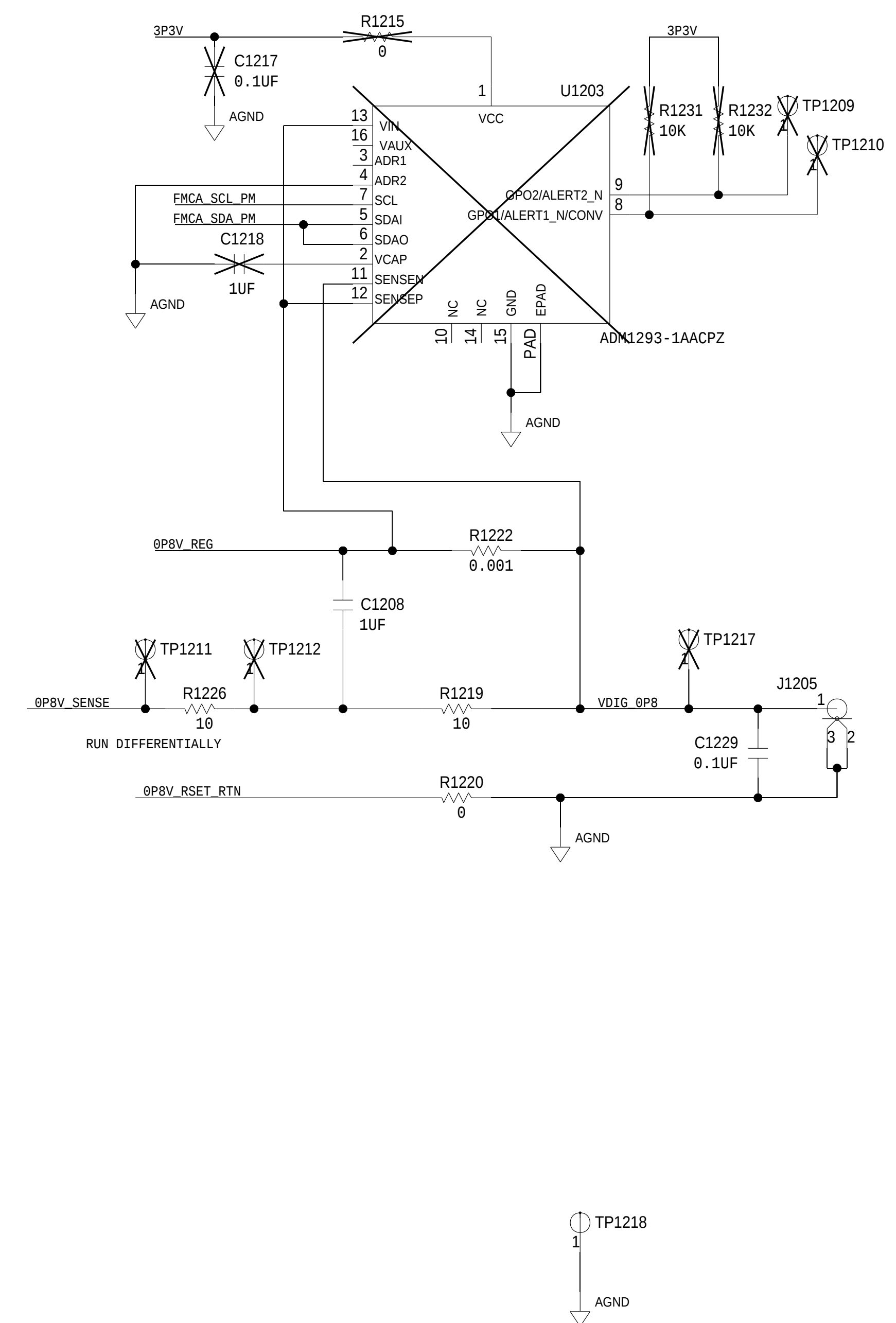
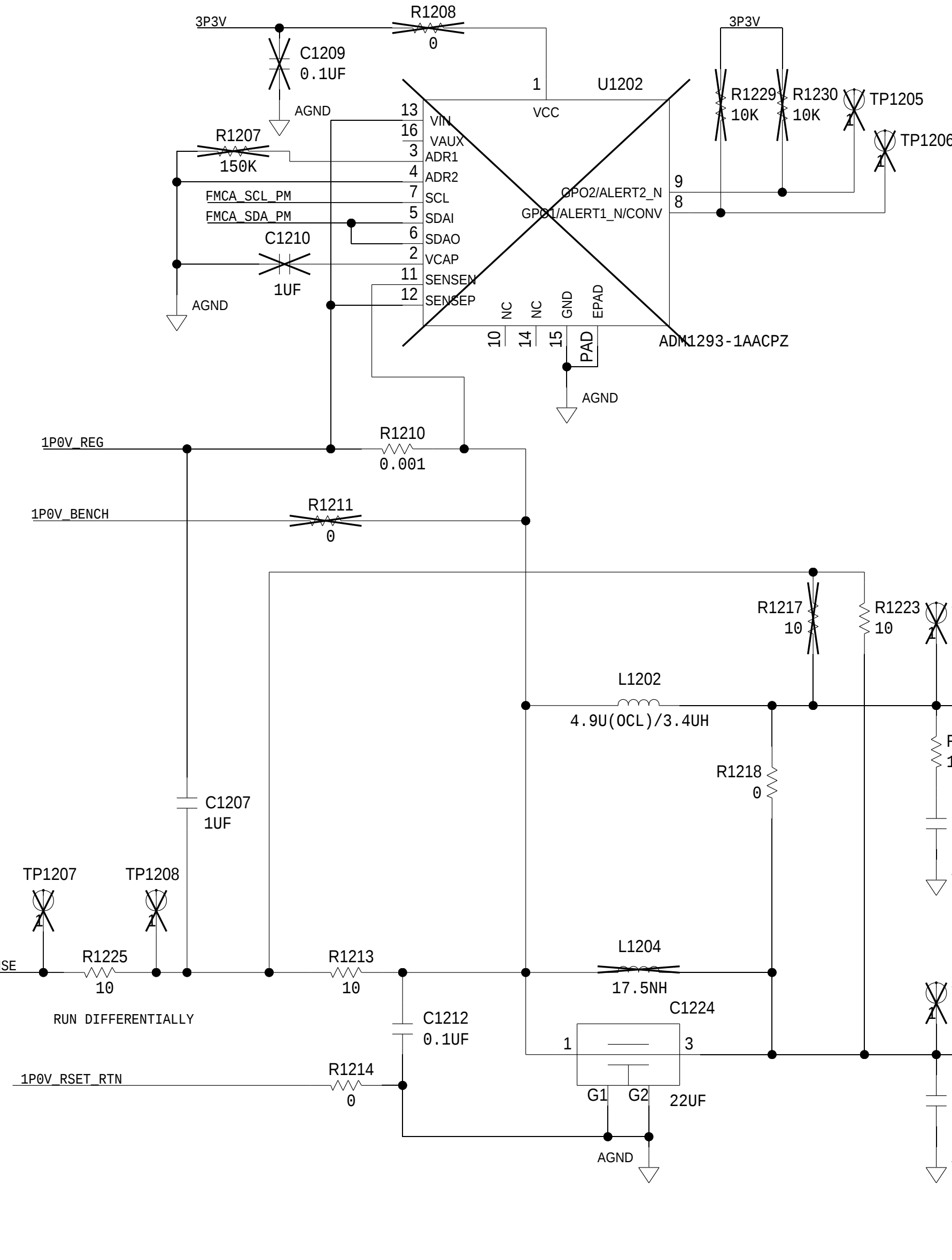
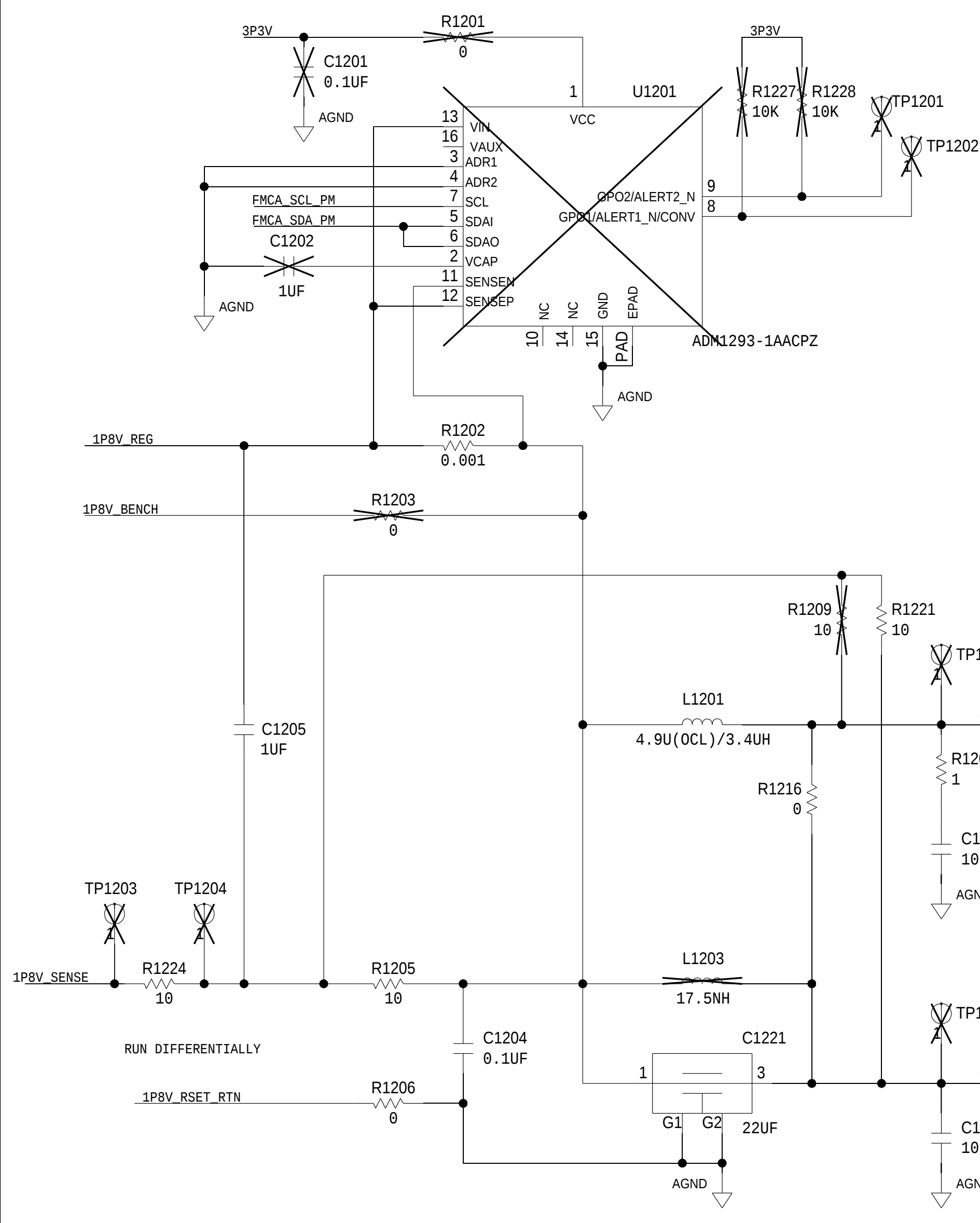
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): ADRV903x : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_064540-03	REV C	
PTD ENGINEER -	SIZE D	SCALE 1:1	SHEET 11 OF 16

POWER MEASUREMENT & FILTERING

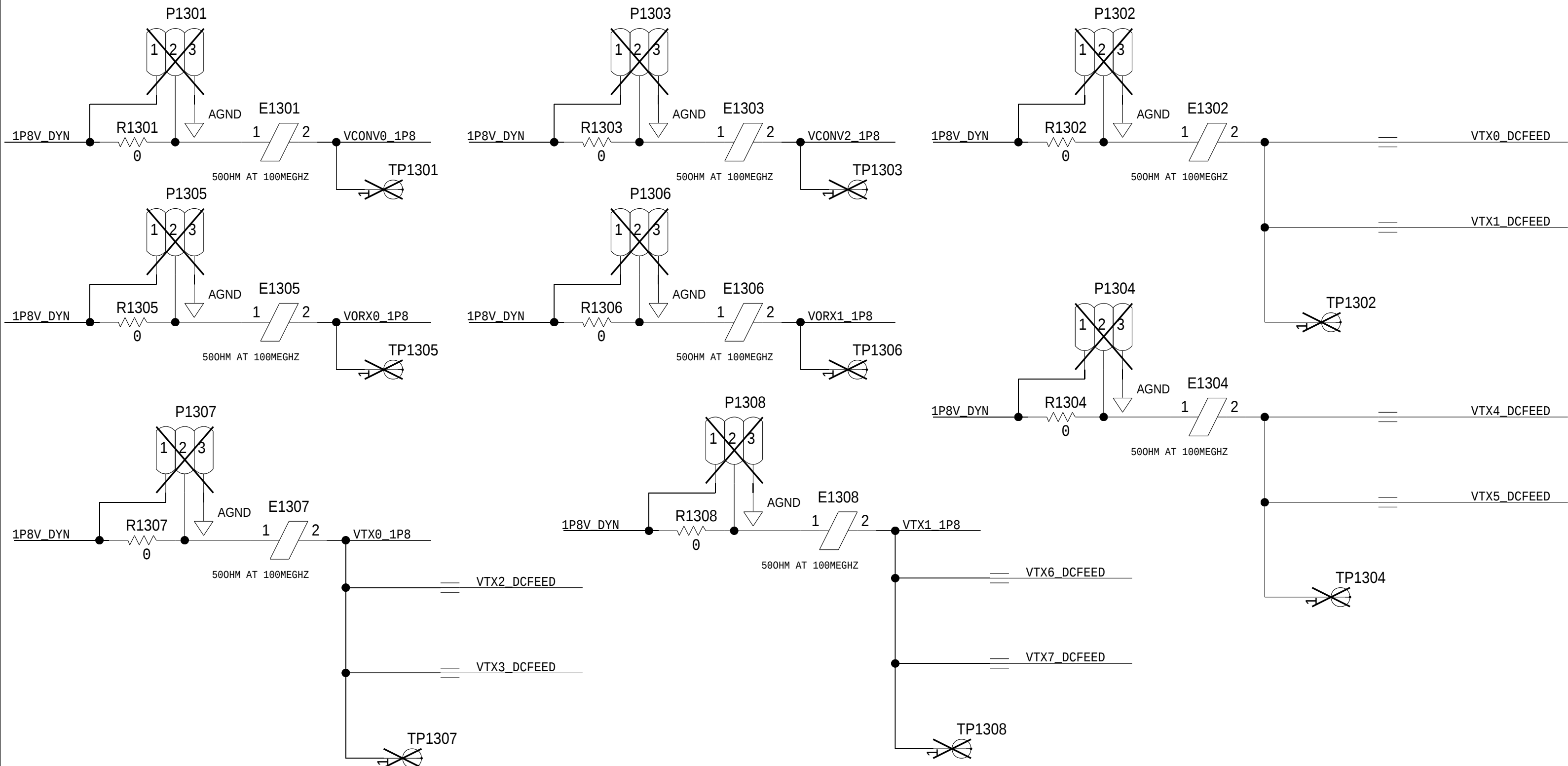
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REV	DESCRIPTION	DATE	APPROVED



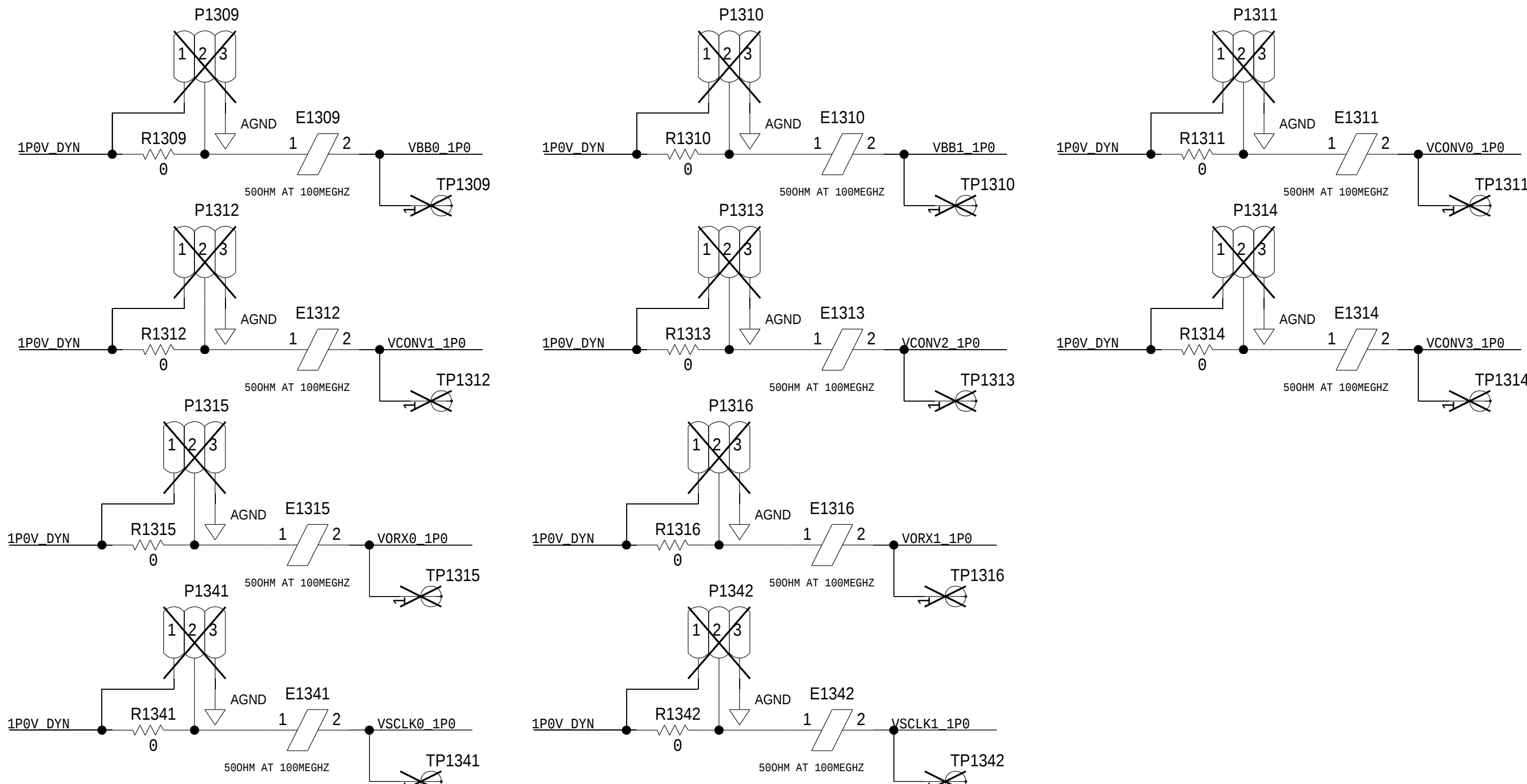
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	HW TYPE : Customer Evaluation Product(s) : ADRV903x : N/A			
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PTD ENGINEER _____		SIZE D	SCALE 1:1	SHEET 12 OF 16
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POWER DISTRIBUTION

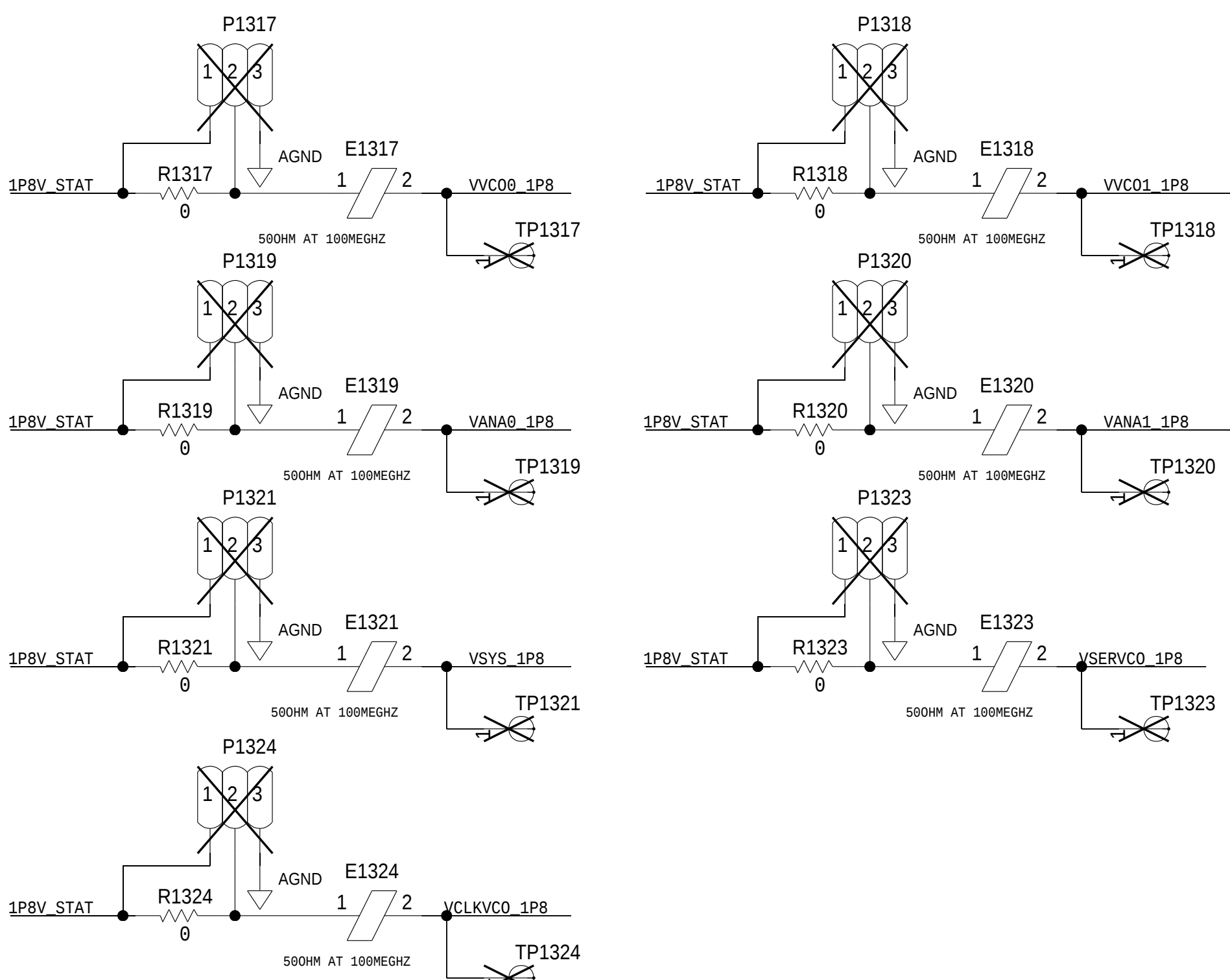
1.8V DYNAMIC SUPPLIES



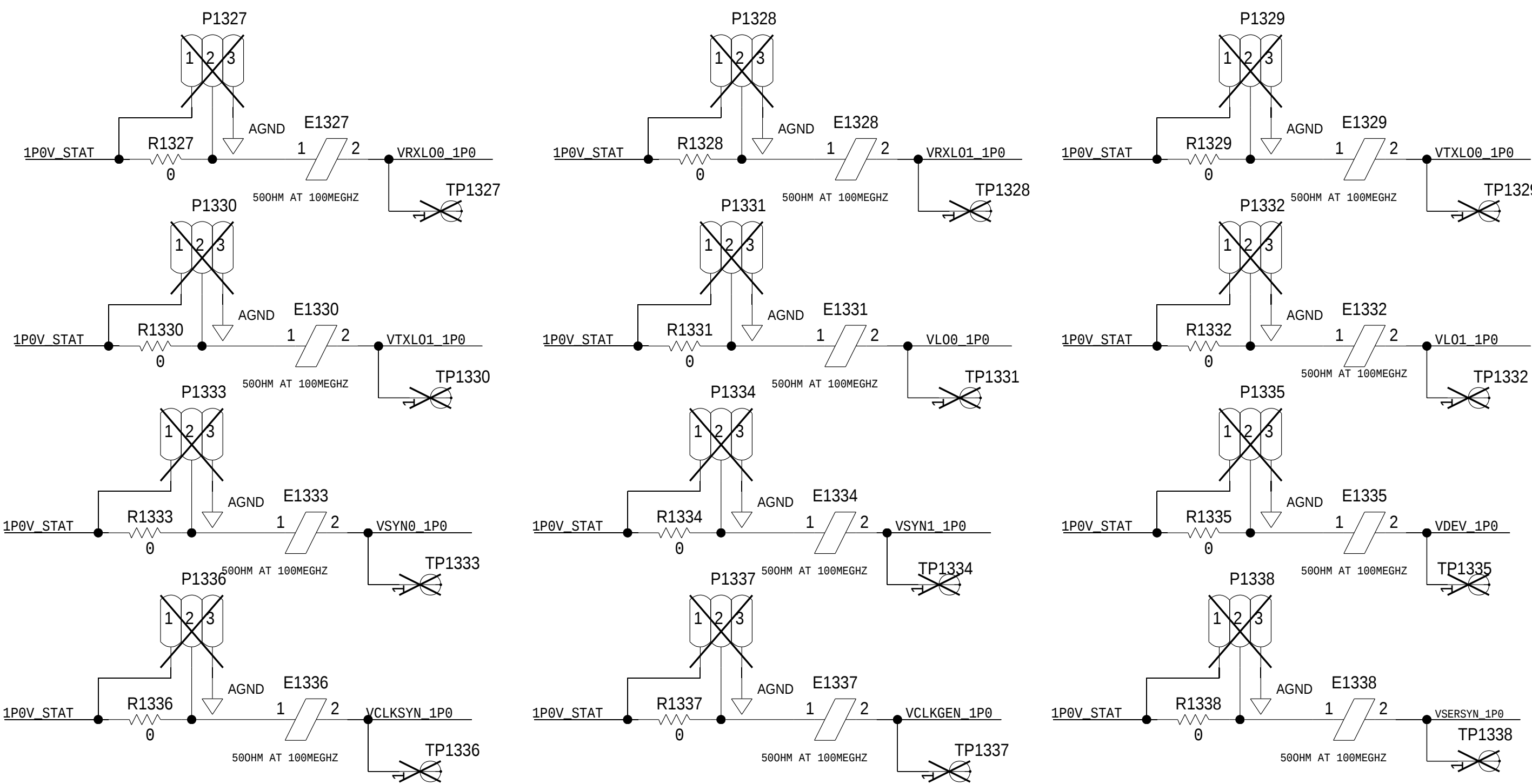
1.0V DYNAMIC SUPPLIES



1.8V STATIC SUPPLIES



1.0V STATIC SUPPLIES



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REV	DESCRIPTION	DATE	APPROVED

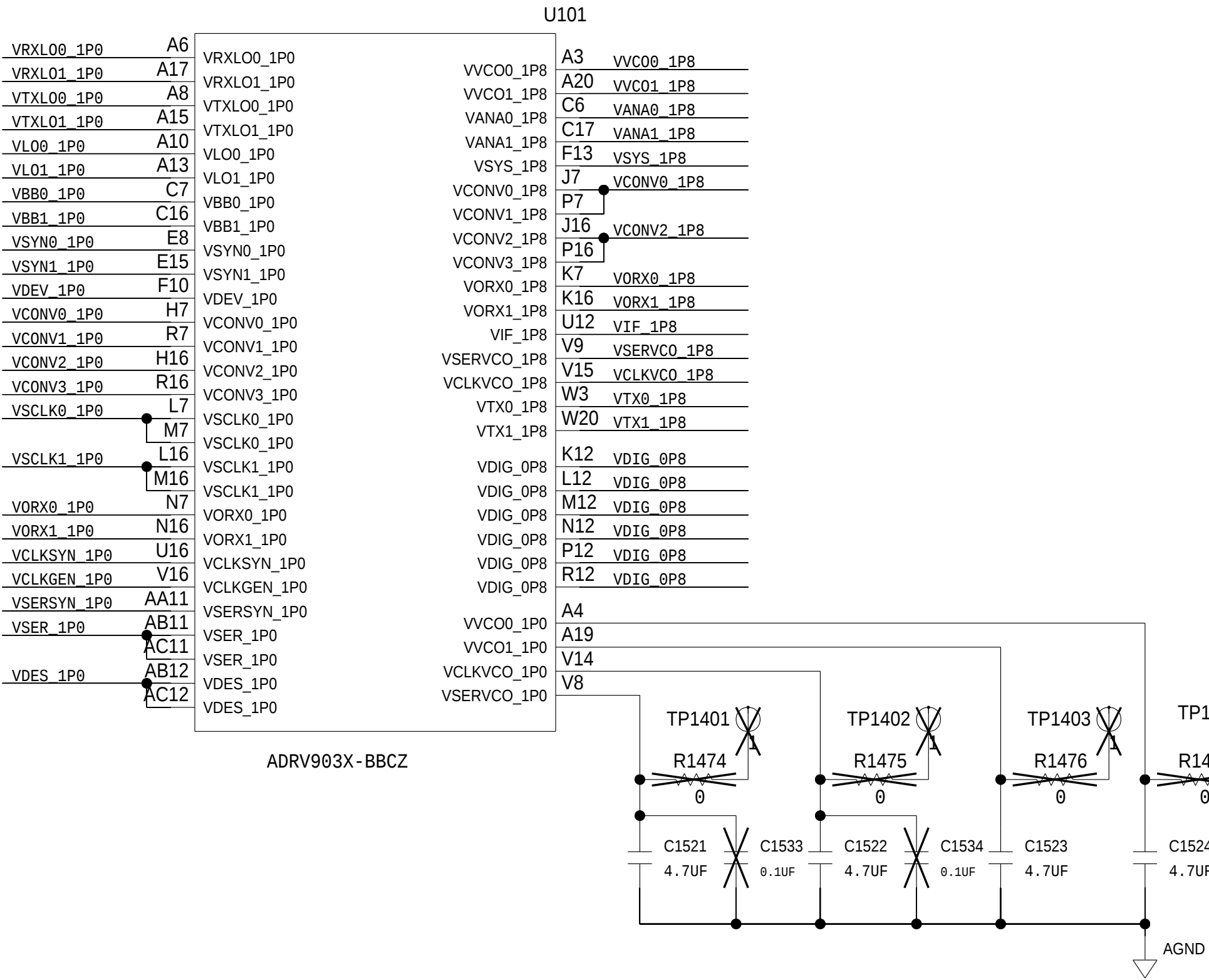
SCHEMATIC			
HW TYPE : Customer Evaluation			
Product(s): ADRV903x			
: N/A			
DESIGN VIEW	DRAWING NO.		REV
<DESIGN_VIEW>	02_064540-03		C
PTD ENGINEER	SIZE	SCALE	SHEET
-	D	1:1	13 OF 16

POWER INPUT

1.8V CAPS

0.8V CAPS

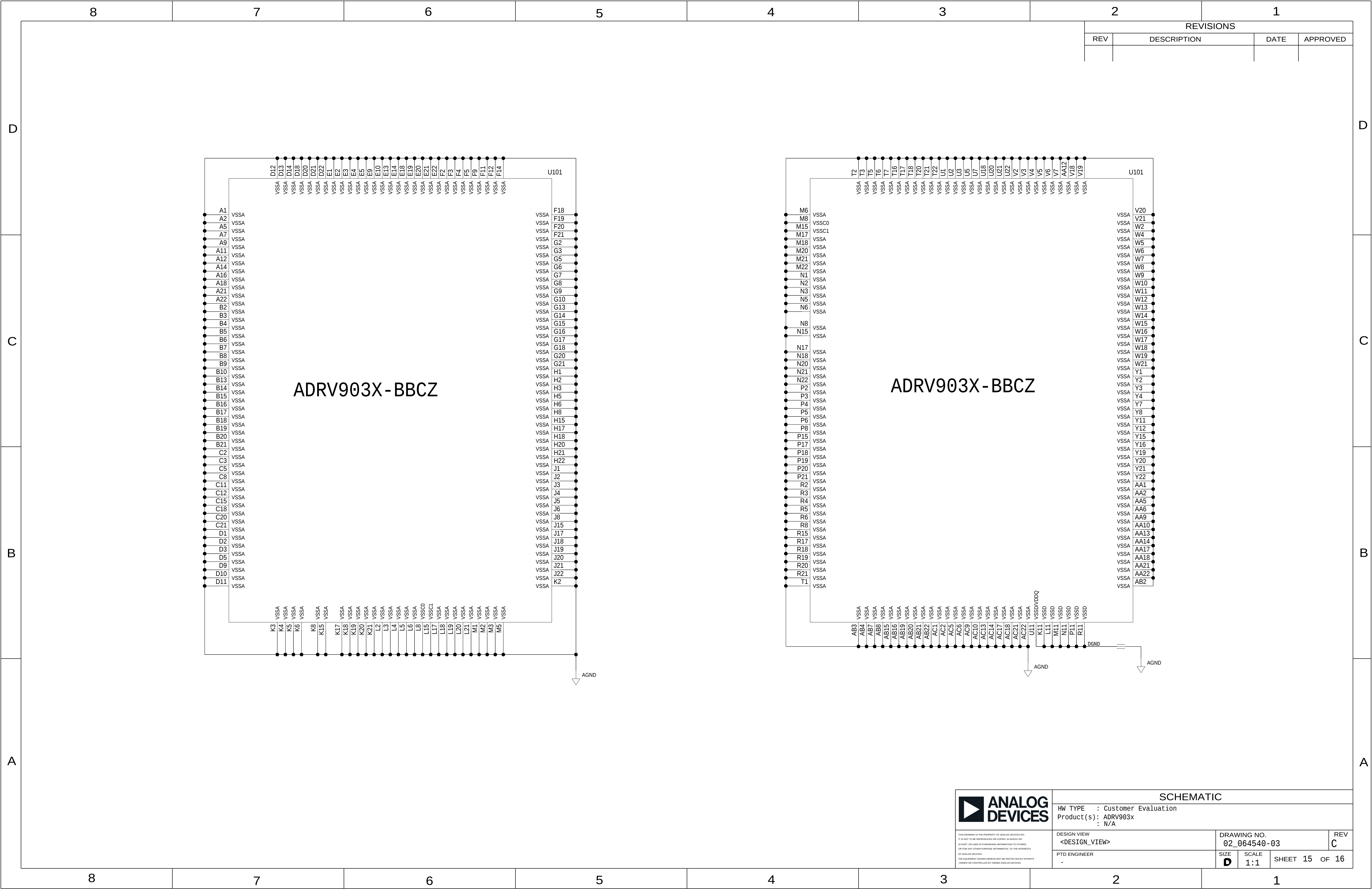
1.0V CAPS





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SCHEMATIC			
HW TYPE : Customer Evaluation			
Product(s) : ADRV903x			
: N/A			
DESIGN VIEW	DRAWING NO.		REV
<DESIGN_VIEW>	02_064540-03		C
PTD ENGINEER	SIZE	SCALE	SHEET
-	D	1:1	14 OF 16



D

C

B

A

D

C

B

A

FPGA CONNECTIONS

