

8

7

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1

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RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE		
JP#	ON	OFF
1		
2		
3		
4		
5		

\* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

TEMPLATE ENGINEER  
-

HARDWARE SERVICES  
M Madden

HARDWARE SYSTEMS  
-

TEST ENGINEER  
-

COMPONENT ENGINEER  
-

TEST PROCESS  
-

HARDWARE RELEASE  
-

DESIGNER  
-

PTD ENGINEER  
D Sloan

CHECKER  
-

DATE

JULY 2024

JULY 2024

SCHEMATIC

HW TYPE : Customer Evaluation

Product(s): AD4884

: AD4883,AD4884,AD4885,AD4886

PACKAGE : 196-lead 10X10\_MM BGA-family

: Pitch-pitch StyleVendor Style

<User Define>

<User Define>

<User Define>

MASTER PROJECT TEMPLATE  
TBD

TESTER TEMPLATE  
067706\_a

DRAWING NO.  
02\_083437-02

REV.  
C

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES

DECIMALS X.XX +0.010 X.XXX +0.005

FRACTIONS +1/32

ANGLES +2

SIZE D

SCALE 1:1

CODE ID NO. CodeID

SHEET 1 OF 12

8

7

6

5

4

3

2

1

8

7

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4

3

2

1

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CODE ID NO. CodeID

SHEET 1 OF 12

8

7

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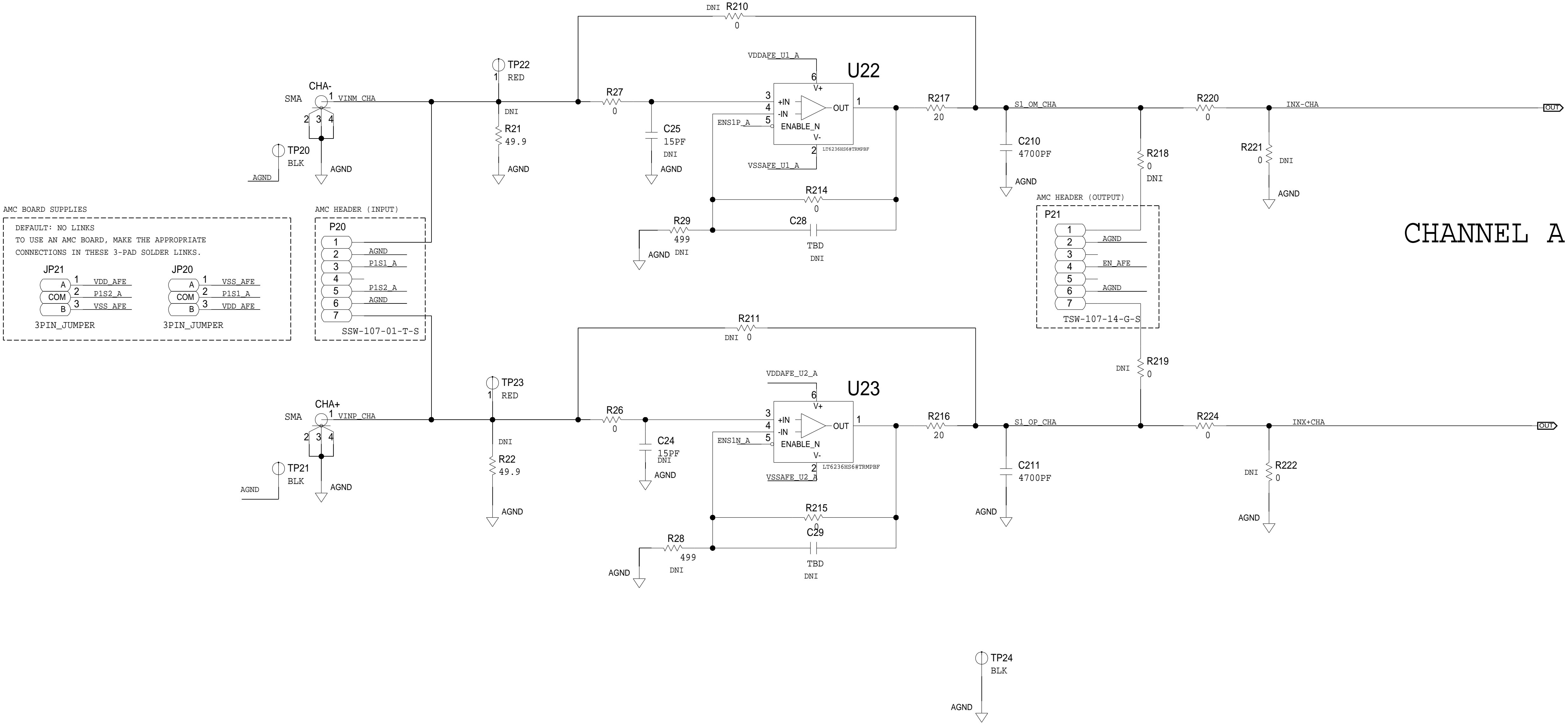
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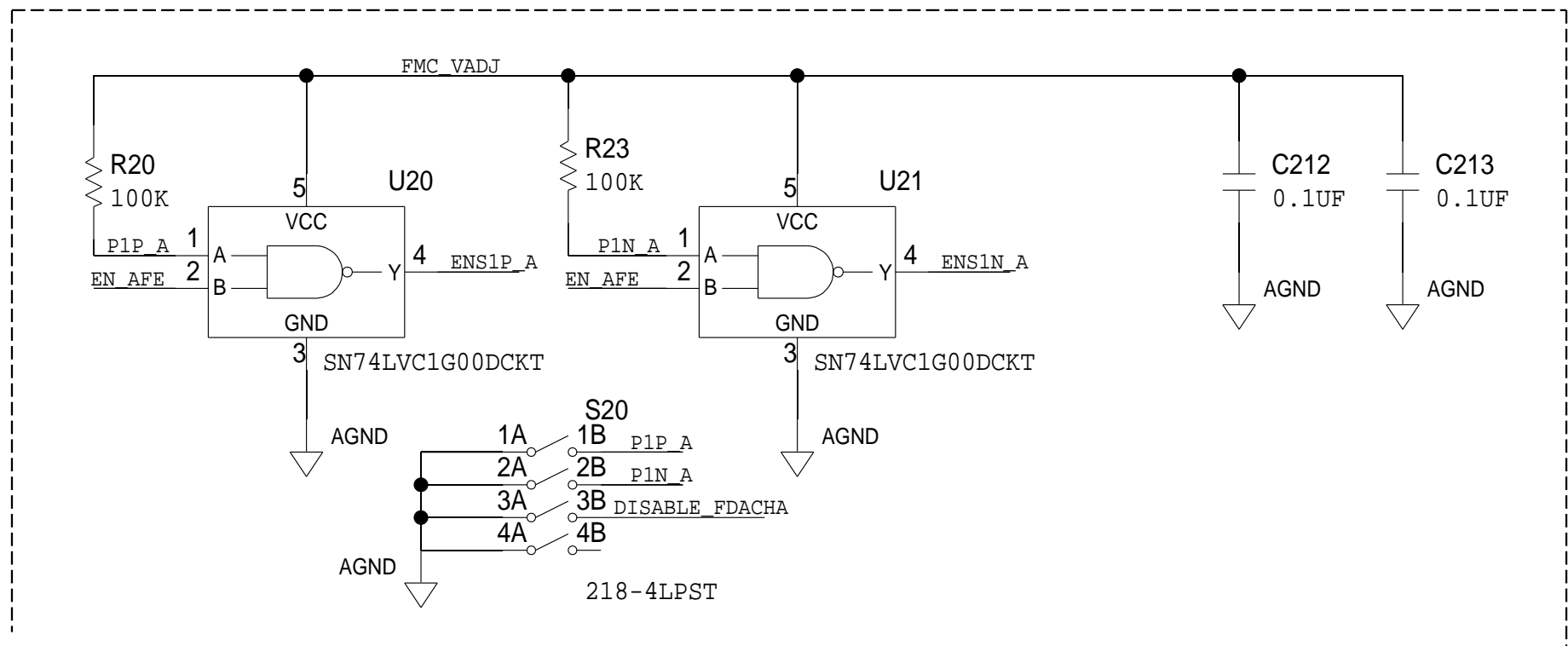
PRECISION SIGNAL CONDITIONING CIRCUITS  
CHANNEL A

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

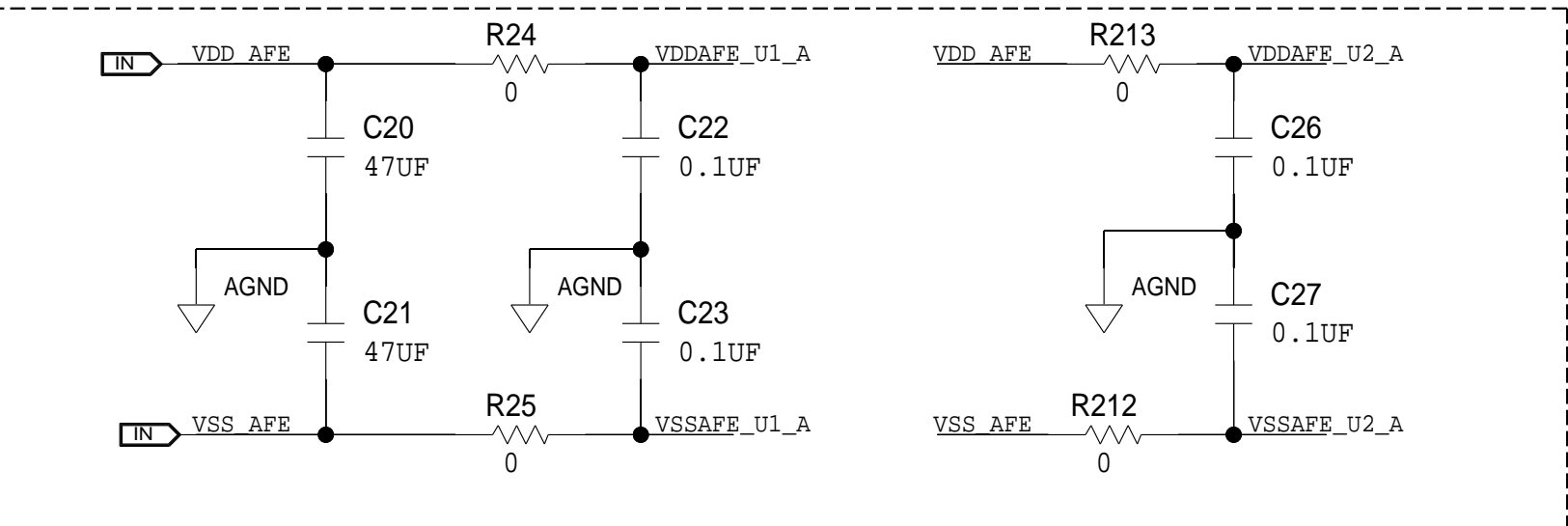


CHANNEL A ANALOG INPUTS

AMPLIFIER DISABLE LOGIC



STAGE 1 SUPPLY DECOUPLING



SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : AD4884 : AD4883, AD4884, AD4885, AD4886			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_083437-02	REV C	
PTD ENGINEER D Sloan	SIZE D	SCALE 1:1	SHEET 2 OF 12

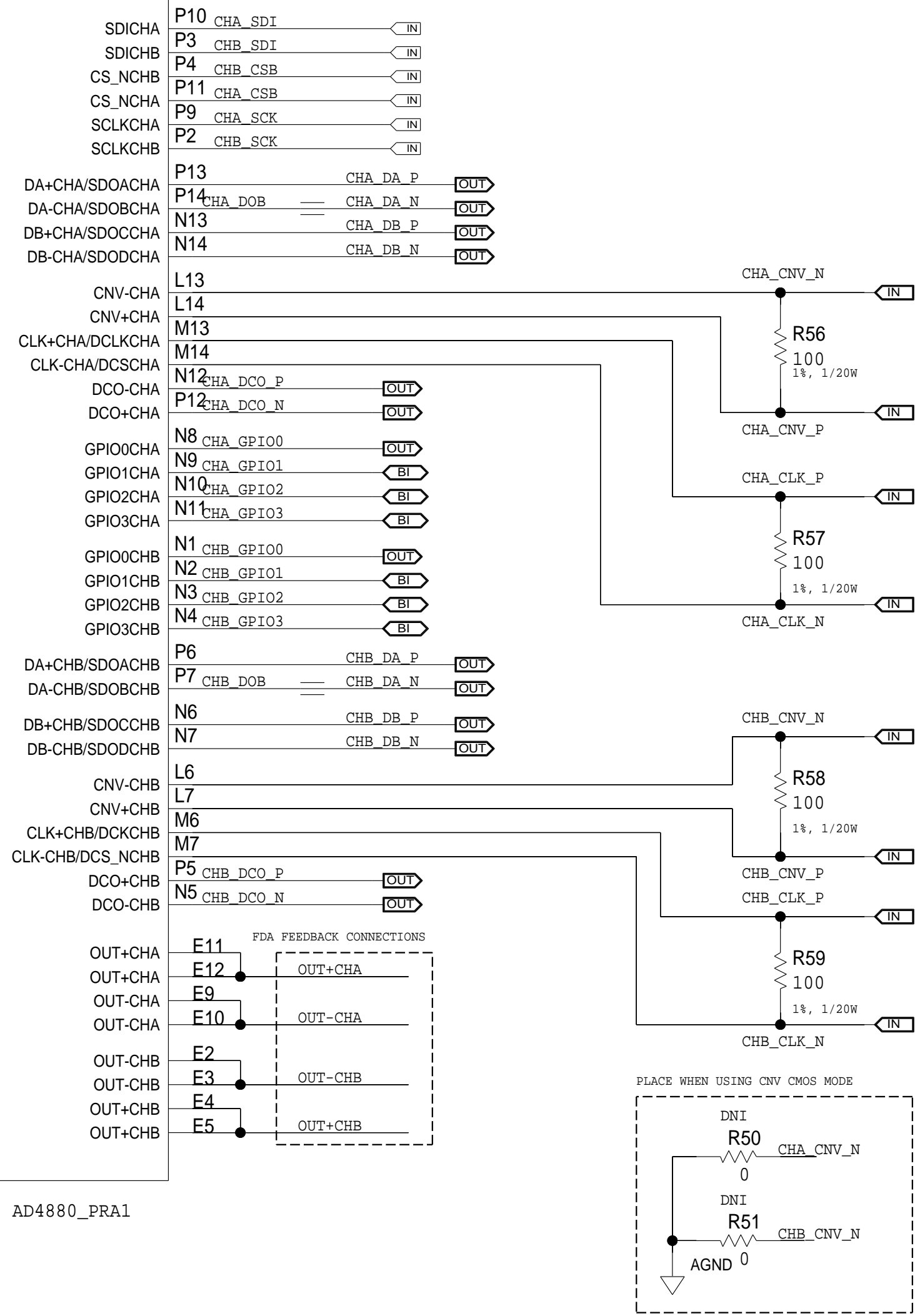
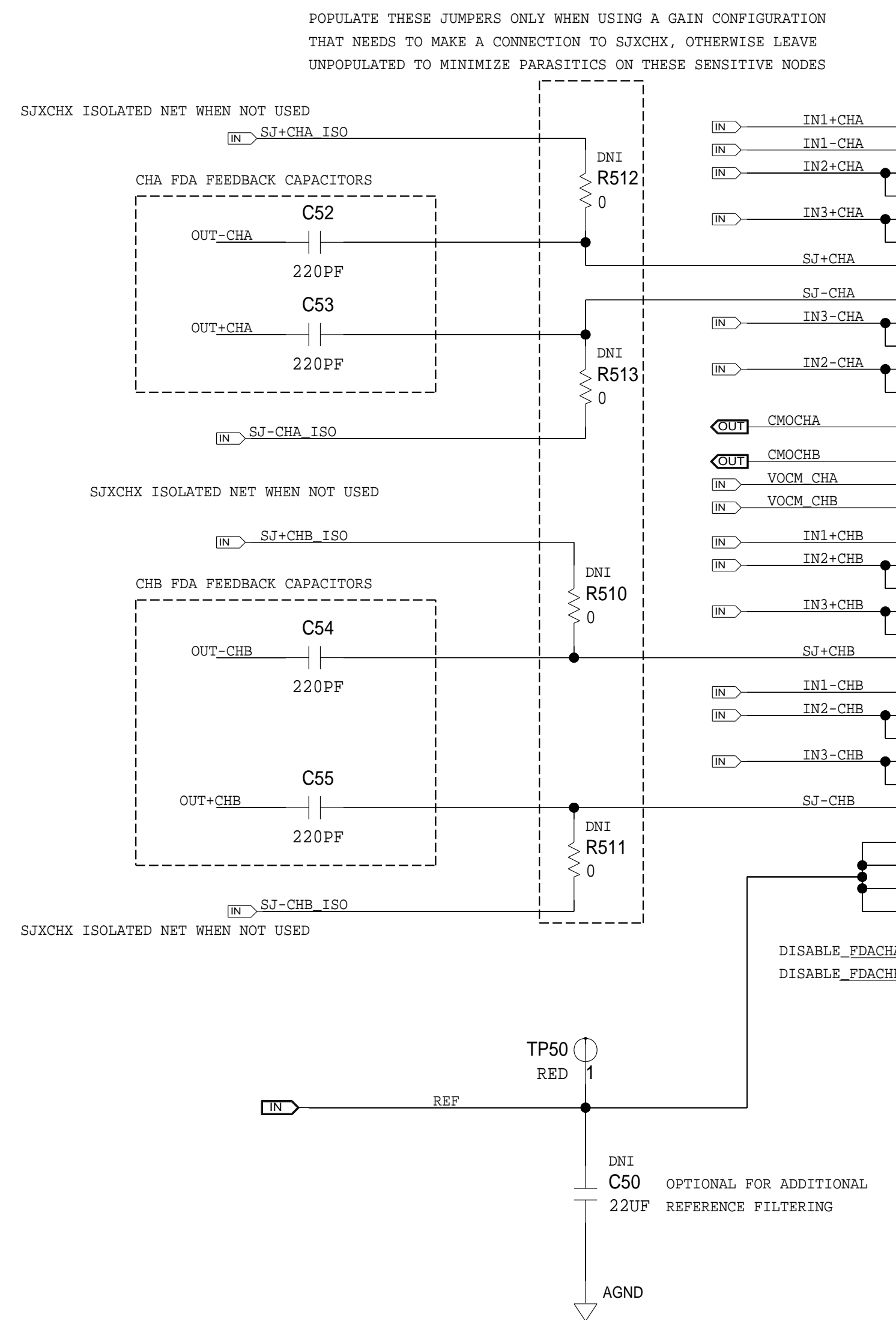
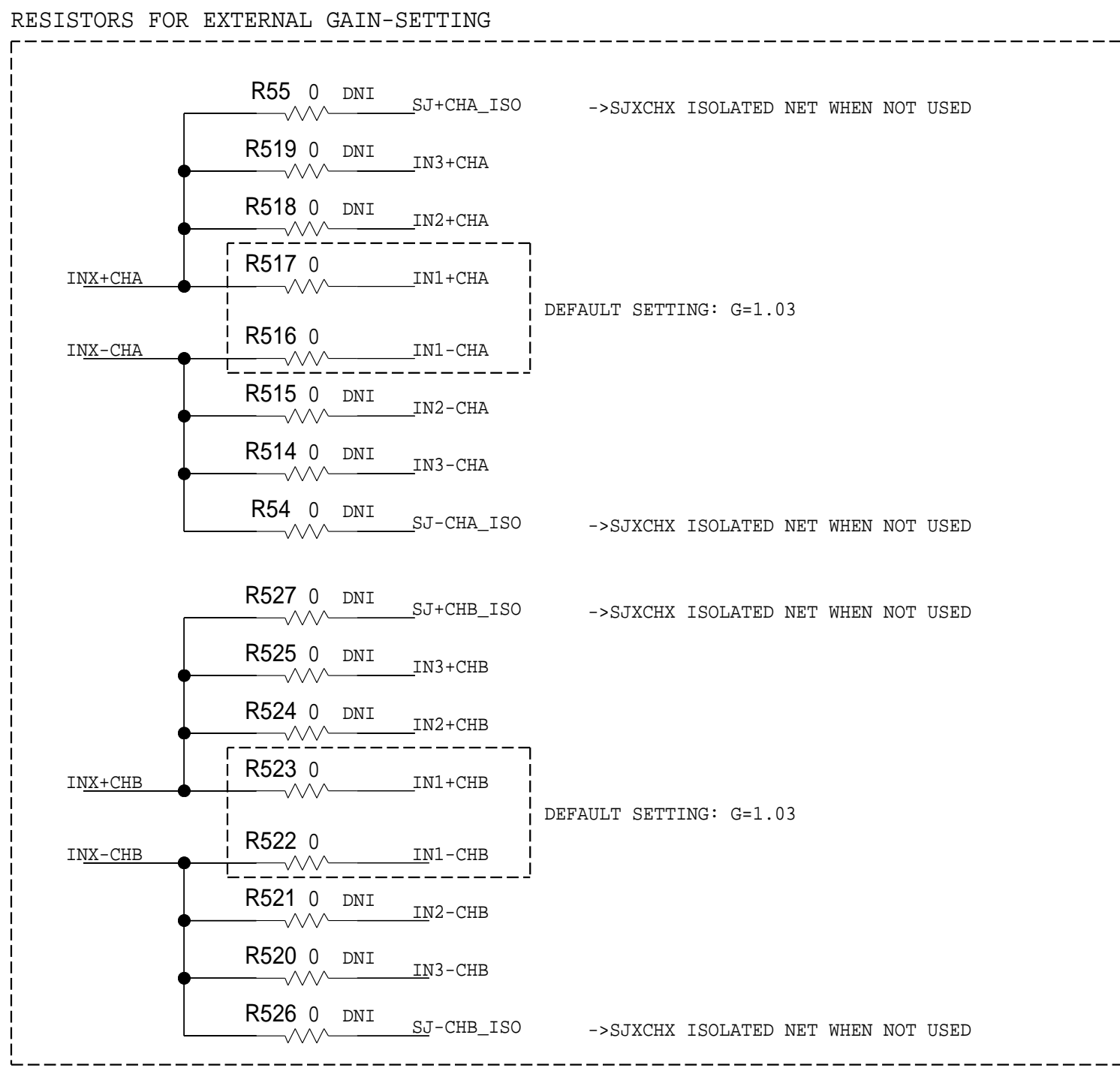
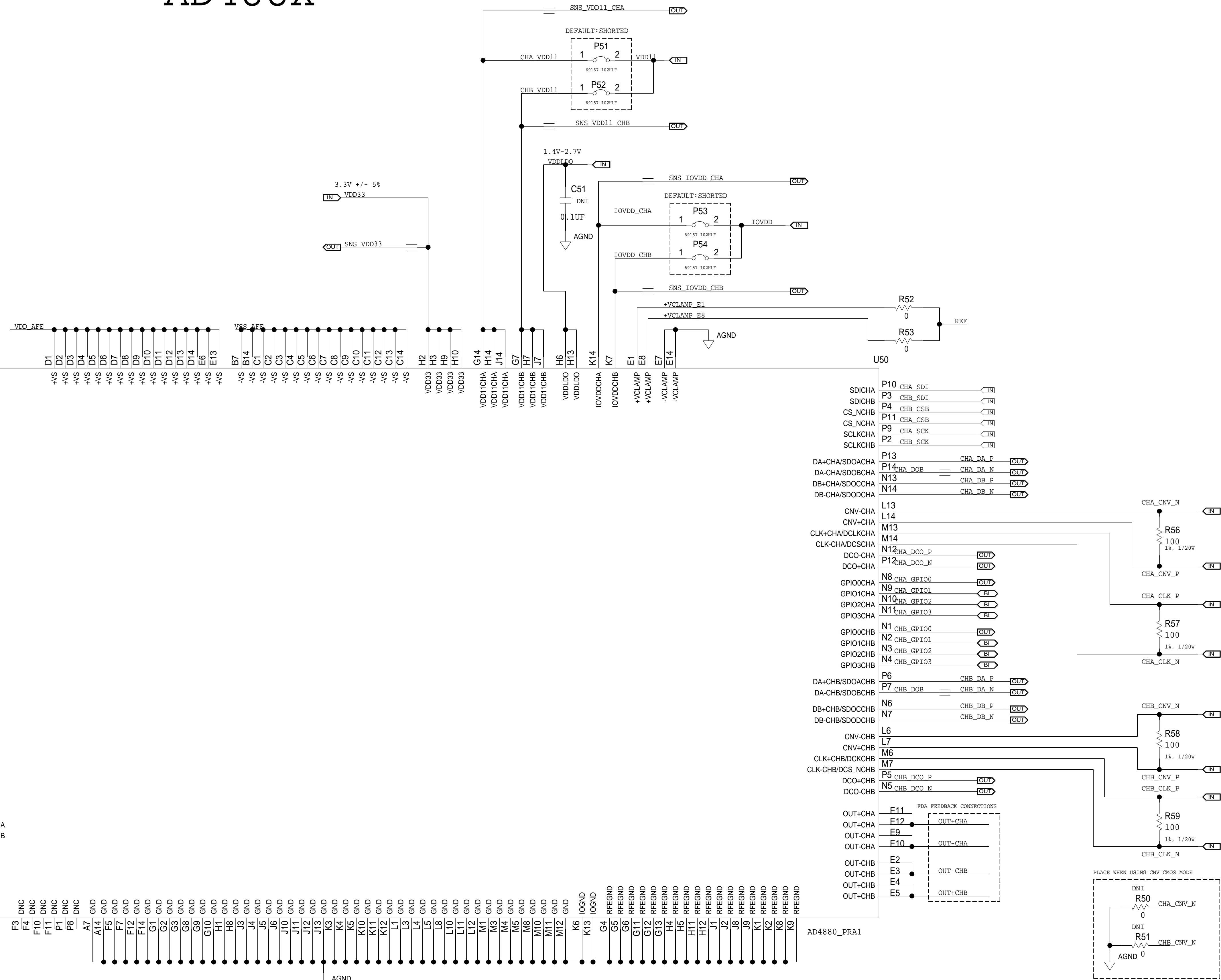






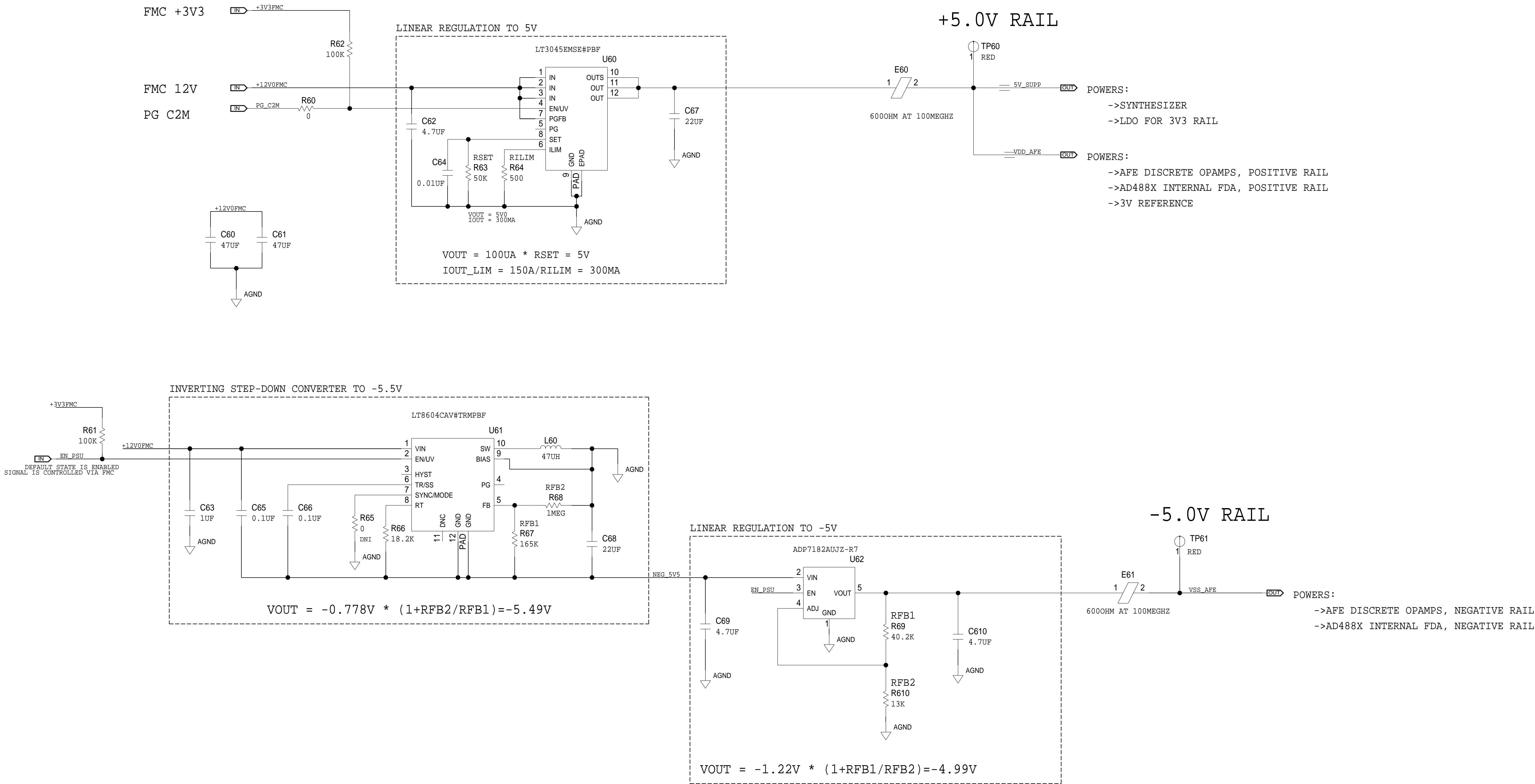


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



# REFERENCE & AMPLIFIER SUPPLY GENERATION

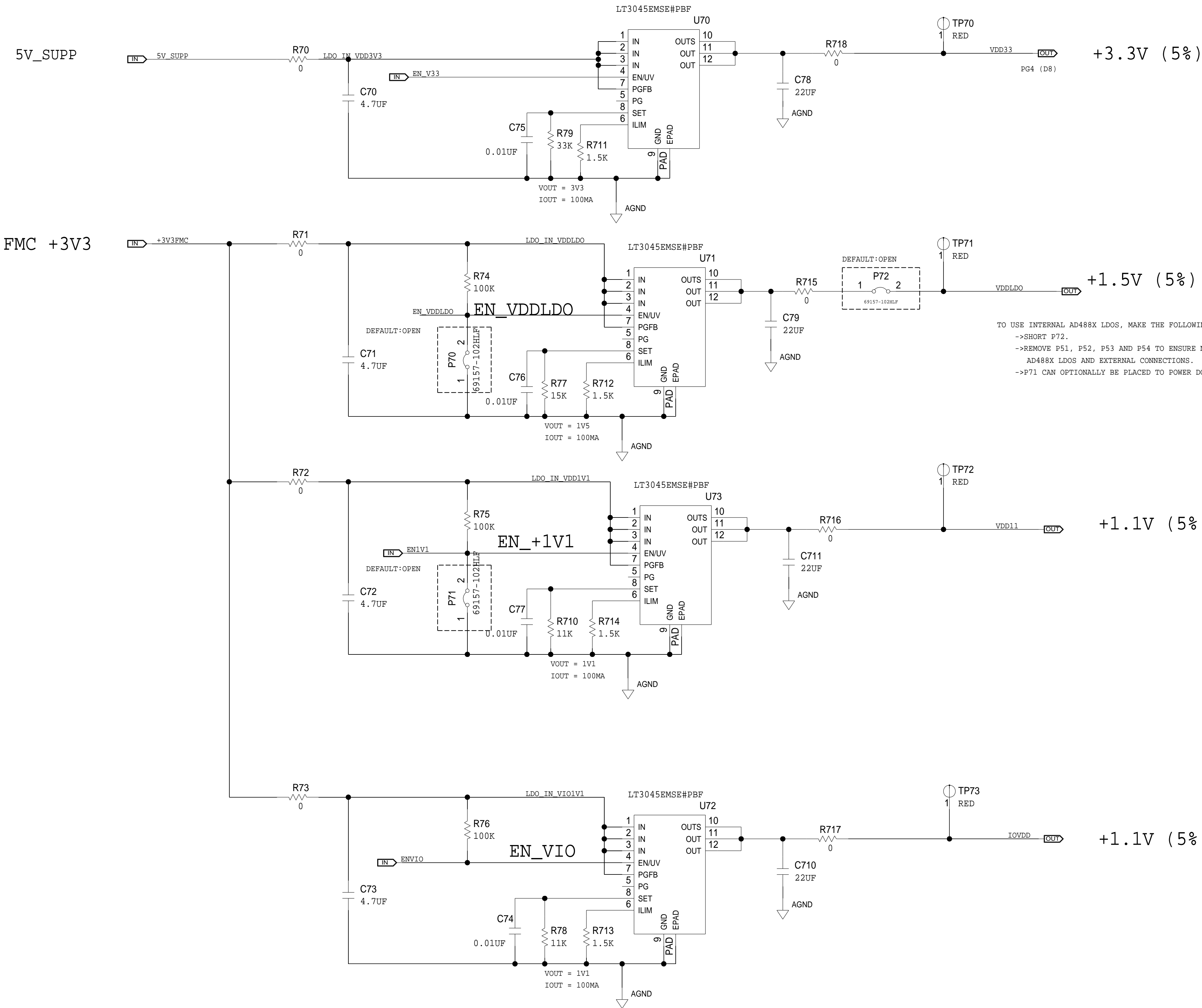
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
HW TYPE : Customer Evaluation			
Product(s): AD4884 : AD4883,AD4884,AD4885,AD4886			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_083437-02	REV C	
PTD ENGINEER D Sloan	SIZE D	SCALE 1:1	SHEET 6 OF 12

AD488X DEVICE POWER SUPPLY

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



TO USE INTERNAL AD488X LDOS, MAKE THE FOLLOWING JUMPER ADJUSTMENTS PRIOR TO POWERING UP BOARD:  
->SHORT P72.  
->REMOVE P51, P52, P53 AND P54 TO ENSURE NO CONTENTION WITH INTERNAL AD488X LDOS AND EXTERNAL CONNECTIONS.  
->P71 CAN OPTIONALLY BE PLACED TO POWER DOWN U71 THE EXTERNAL 1V1 LDO.



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DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_083437-02	REV C	
PTD ENGINEER D Sloan	SIZE D	SCALE 1:1	SHEET 7 OF 12



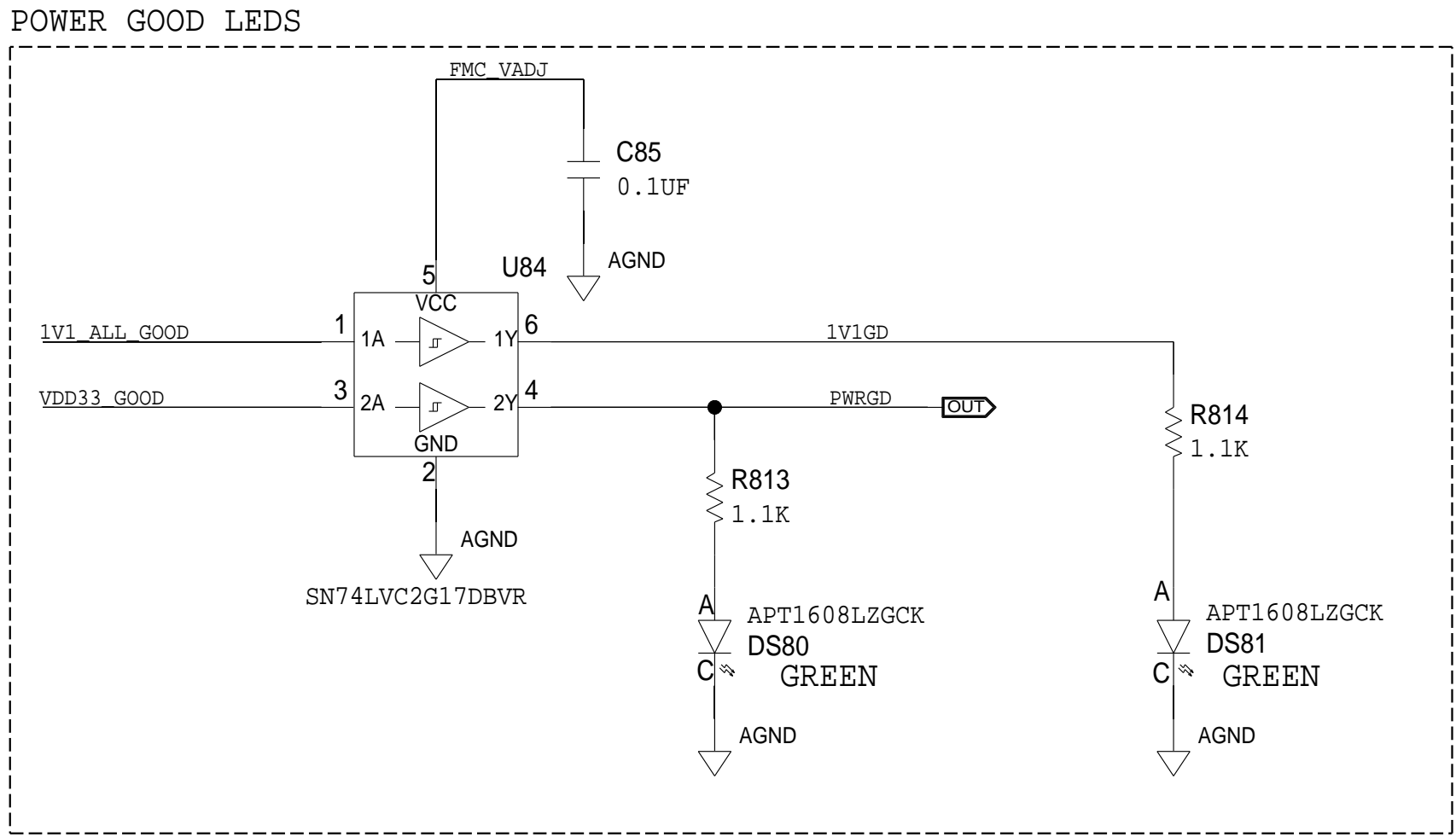
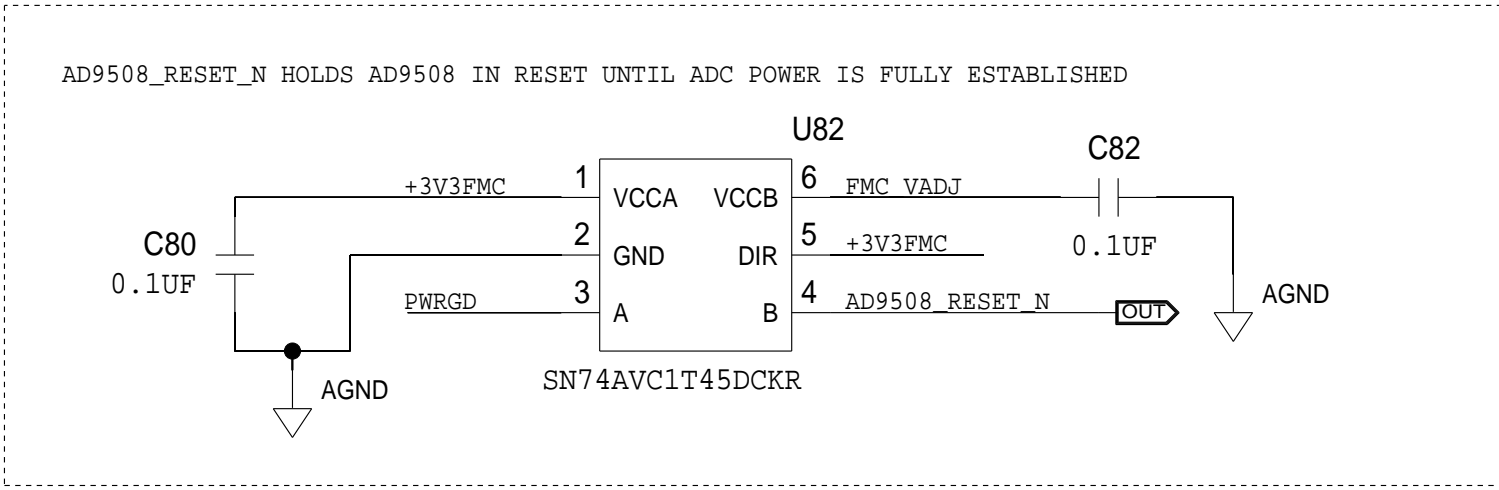
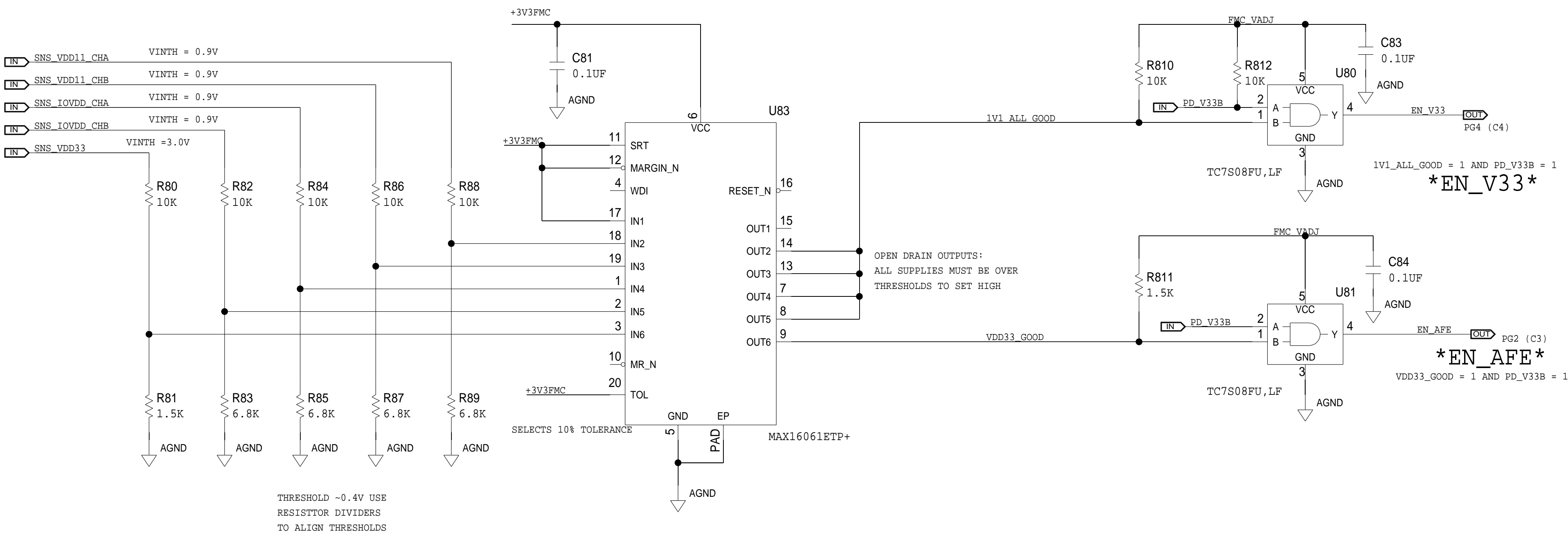
SUPPLY SEQUENCE CIRCUITS

12V FMC WILL POWER +5V0 AND -5V0 RAILS, SWITCHER STARTUP DELAYS -5V0 WRT +5V0  
PG\_C2M WILL ENABLE 5V0 LDO IC. EN\_PSU ENABLES -5V0 LDO.BOTH SIGNALS HAVE PULL UPS TO DEFAULT ON

3V3 FMC WILL PROVIDE POWER FOR OPTIONAL AD488X 1V5 LDO SUPPLY  
5V0 WILL PROVIDE SUPPLY FOR AD488X 3V3 LDO  
3V3 FMC SUPPLY WILL PROVIDE SUPPLY FOR ALL 1V1 LDO ICS  
LDO ICS CONTROL SIGNALS ALL HAVE PULL UPS:

EN\_VDDLDO HAS PU AND JUMPER OPTION TO DISABLE  
EN\_1V1 HAS PU (NO OTHER INPUT CONNECTION)  
EN\_VIO HAS PU (NO OTHER INPUT CONNECTION)

AD488X IOVDD, VDD11 WILL POWER UP  
AD488X VDD11 VOLTAGE WILL BE SENSED, VIO WILL BE SENSED  
IF PG\_2CM IS NOT PULLED LOW AT FMC AND BOTH THESE VOLTAGES PRESENT  
THE AD488X'S 3V3 SUPPLY WILL BE ENABLED WITH THE EN\_V33 SIGNAL  
PD\_V33B ALLOWS THIS EN\_V33 TO BE OVERRIDDEN VIA THE FMC (PU ENSURES DEFAULT TO NOT OVERRIDE)  
ONCE THE AD488X'S 3V3 HAS BEEN ESTABLISHED, EN\_AFE WILL ENABLE THE REFERENCE AND THE  
ANALOG FRONT-END OPAMPS (THESE CAN BE OVERRIDDEN VIA PIANO SWITCHES S20, S30)



ANALOG DEVICES	SCHEMATIC			
	HW TYPE : Customer Evaluation Product(s) : AD4884 : AD4883,AD4884,AD4885,AD4886			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_083437-02	REV C	
PTD ENGINEER D Sloan	SIZE D	SCALE 1:1	SHEET 8	OF 12

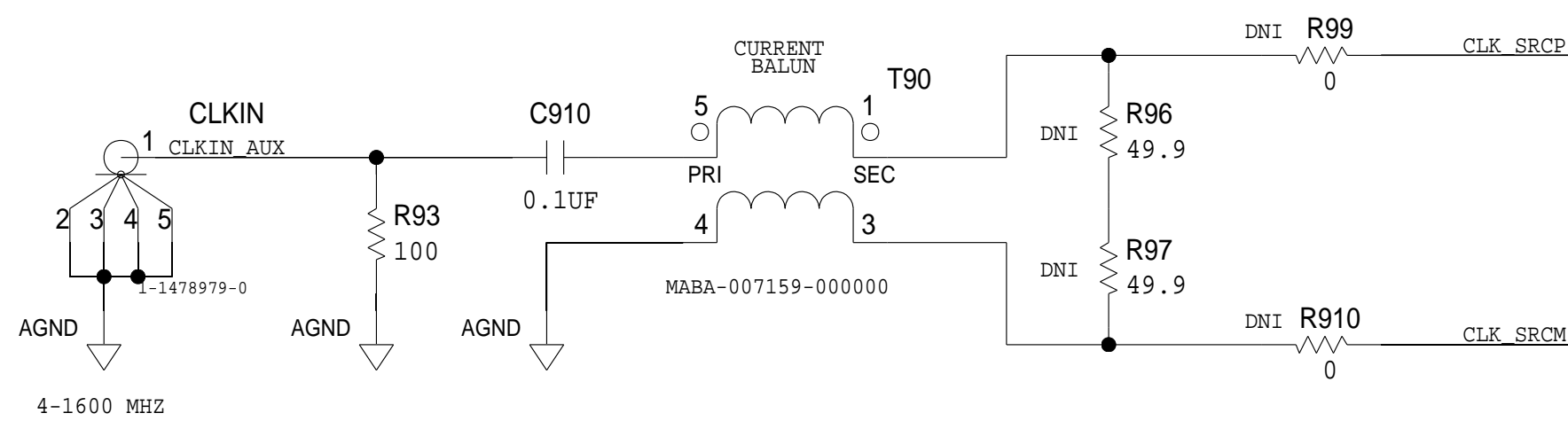


PRECISION CLOCK GENERATION/DISTRIBUTION

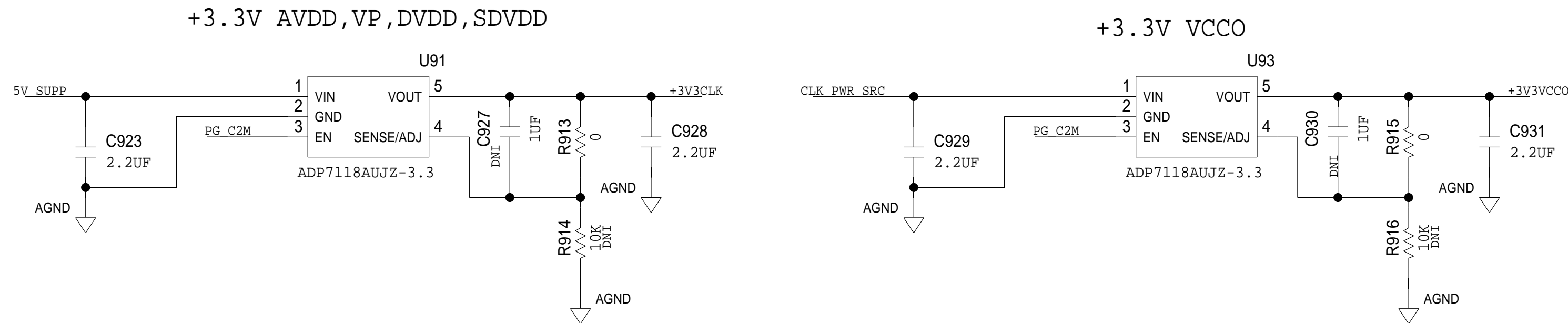
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

EXTERNAL CLOCK SOURCE

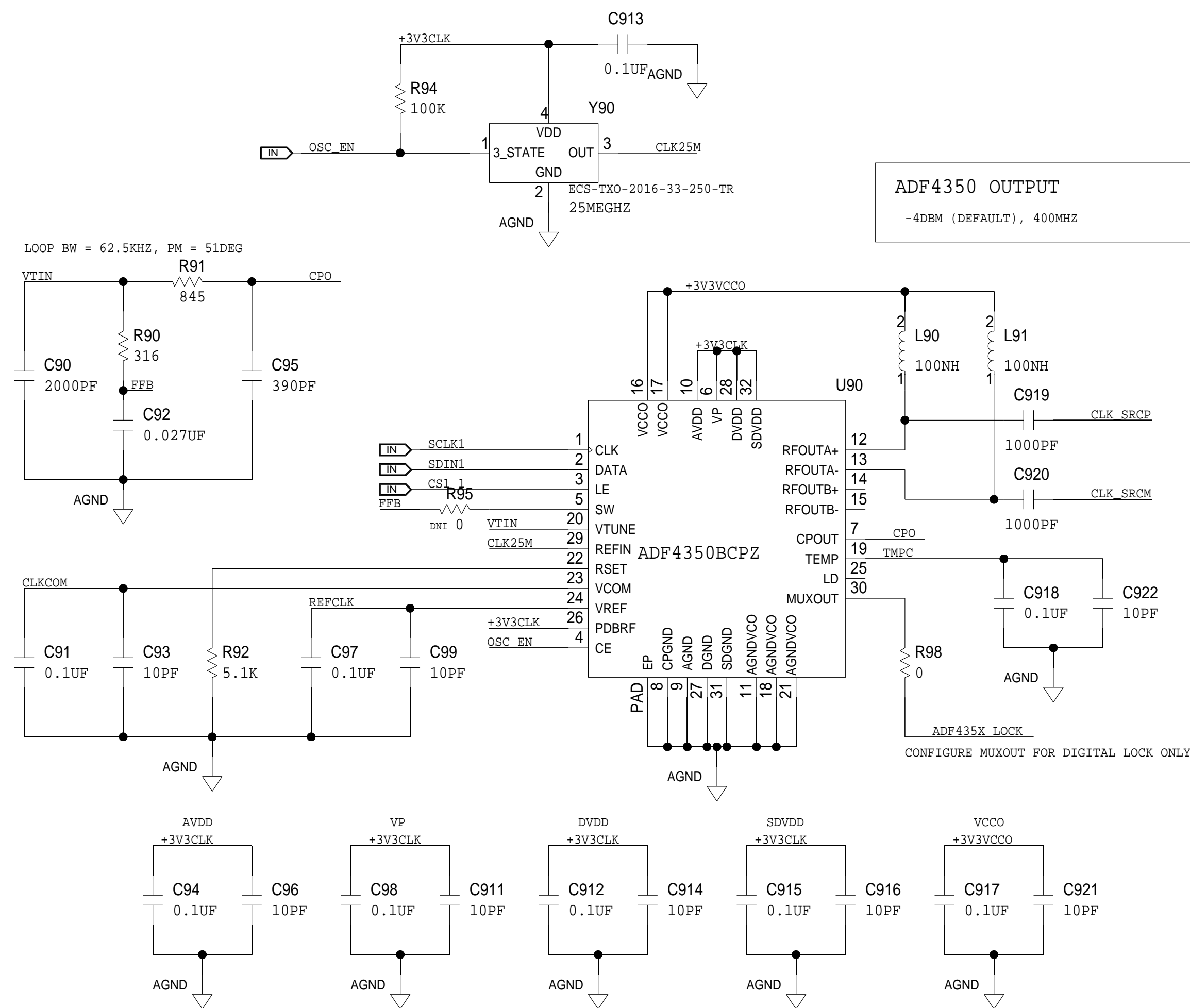
NOT ENABLED BY DEFAULT, R99 AND R910 MUST BE POPULATED AND SYNTHESIZER DISCONNECTED.



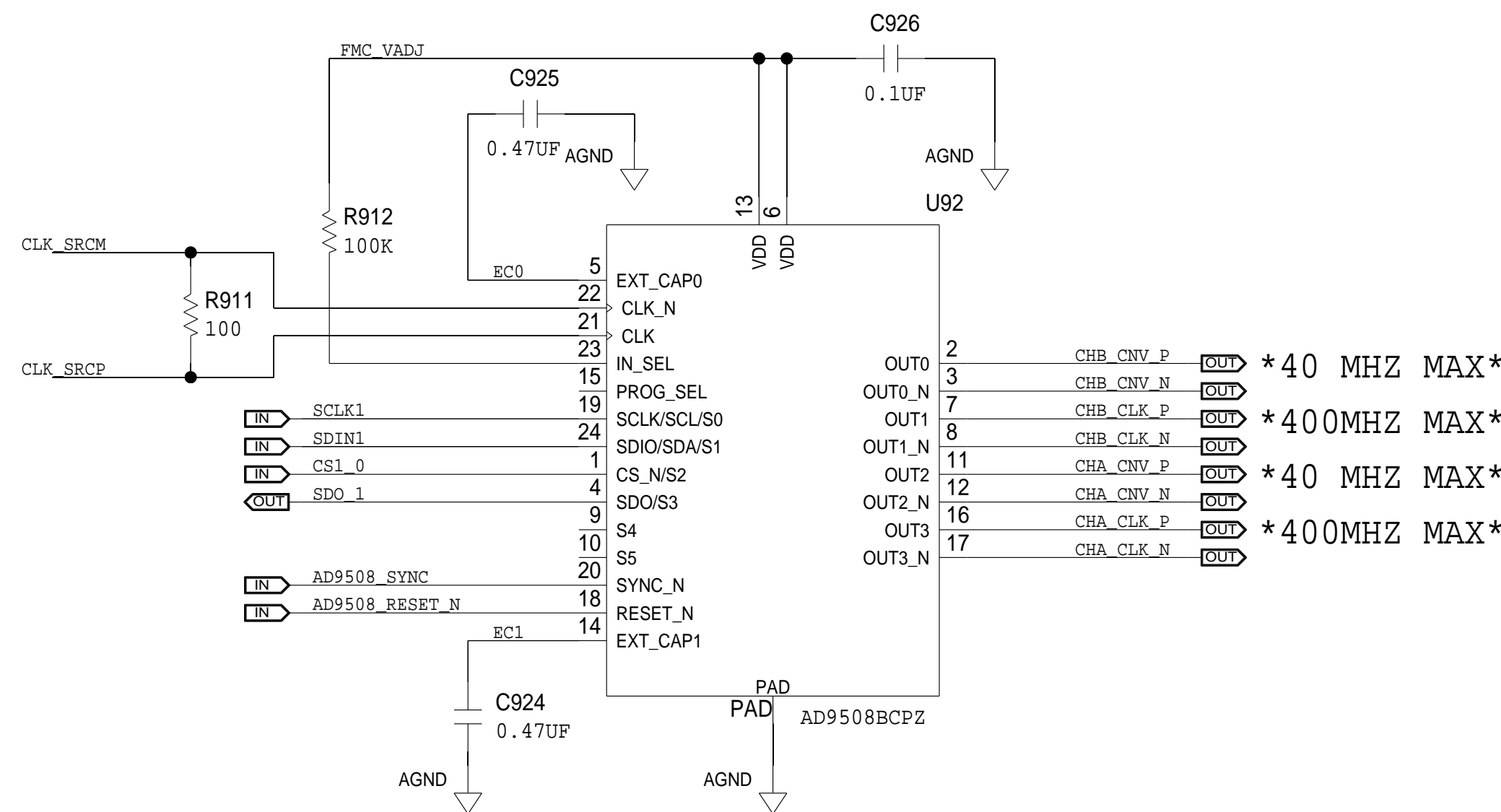
OSCILLATOR AND SYNTHESIZER SUPPLIES



REFERENCE OSCILLATOR & PLL/SYNTHESIZER



CLOCK DISTRIBUTION



- 1) PROG\_SEL INTENTIONAL NC. ENABLES SPI CONFIG MODE.
- 2) IN\_SEL TIED TO SUPPLY. ENABLES DIFFERENTIAL INPUT CLOCK MODE
- 3) S4,S5 PHYSICALLY LEFT FLOATING.
- 4) AD9508\_RESET\_N IS DERIVED FROM PSU SEQ OUTPUT (PORB).
- 5) LVDS TERMINATION PLACEMENT AT LOAD

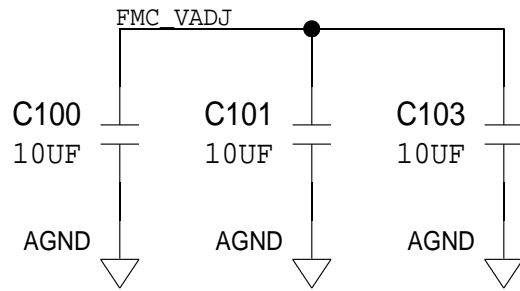
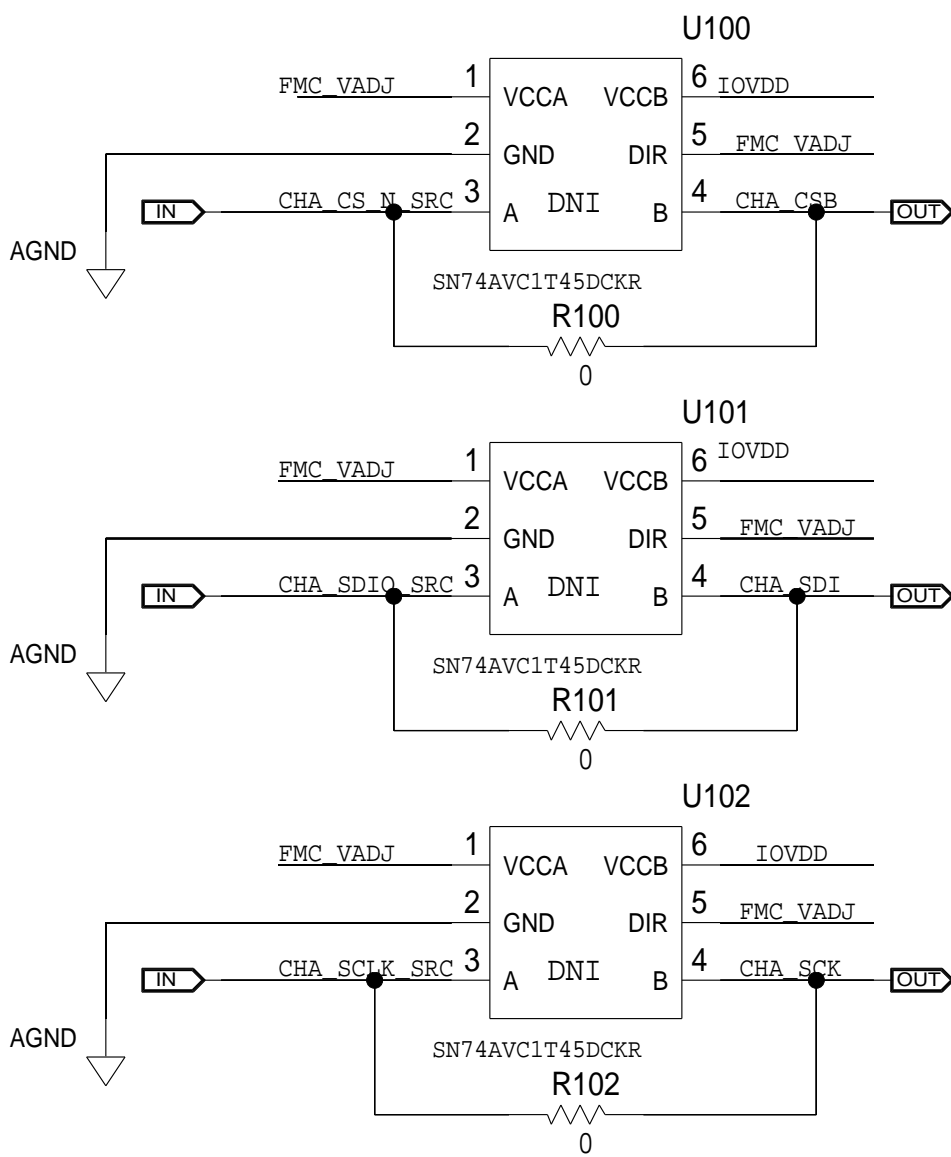


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DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_083437-02	REV C	
PTD ENGINEER D Sloan	SIZE D	SCALE 1:1	SHEET 9 OF 12

LEVEL TRANSLATION CH\_A

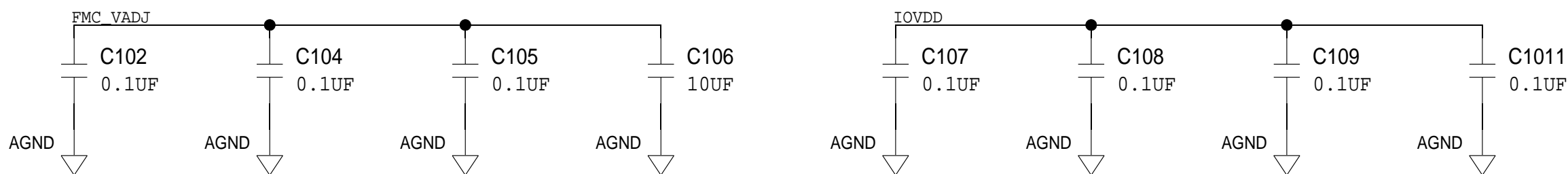
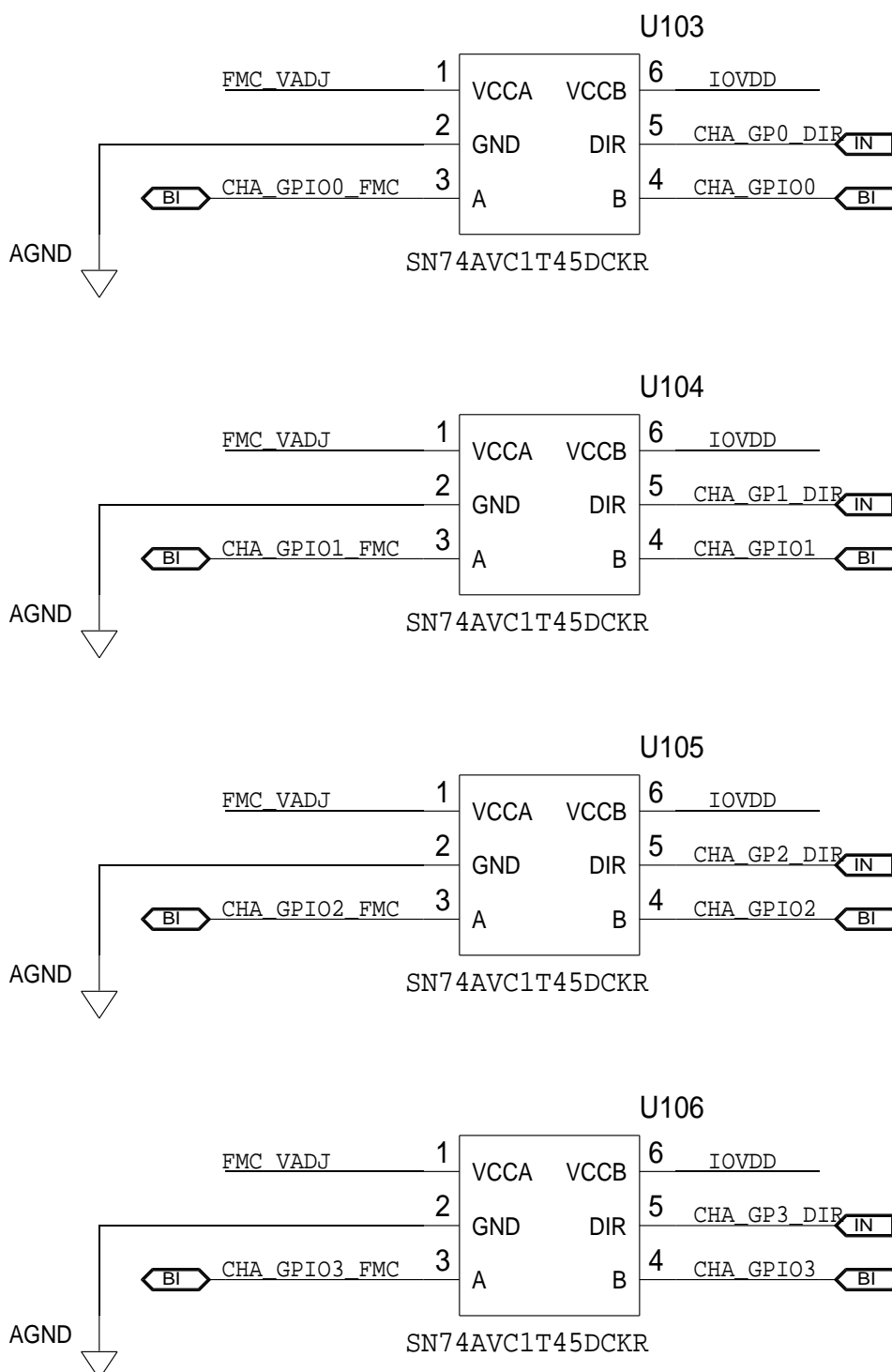
CONFIGURATION SPI LEVEL TRANSLATORS  
(NOT INSTALLED BY DEFAULT)



FMC\_HOST  
SIDE

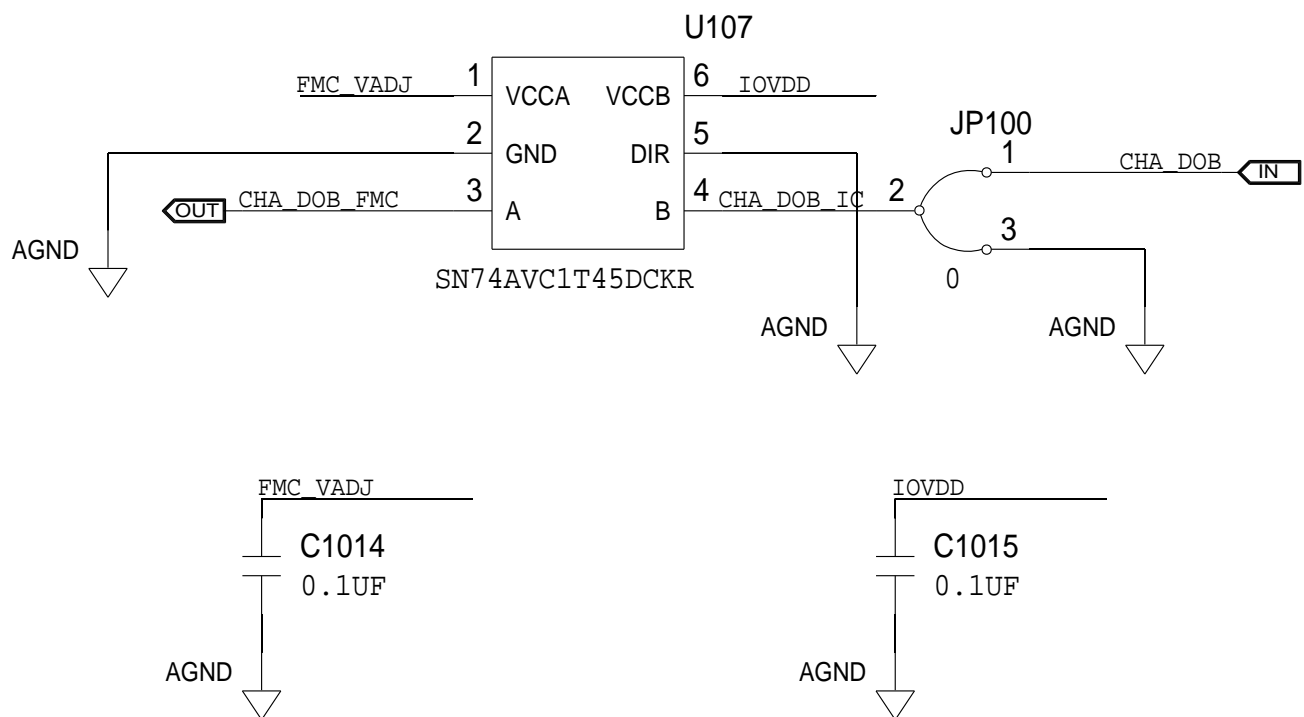
AD488X  
SIDE

GPIO LEVEL TRANSLATORS



DATA SPI LEVEL TRANSLATORS

FMC\_HOST  
SIDE



AD488X  
SIDE



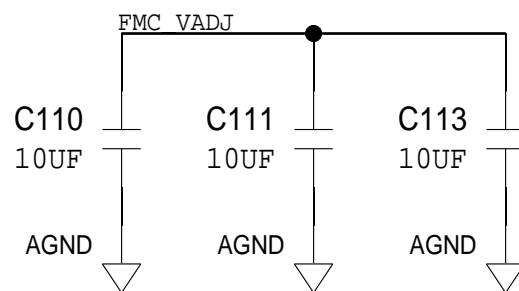
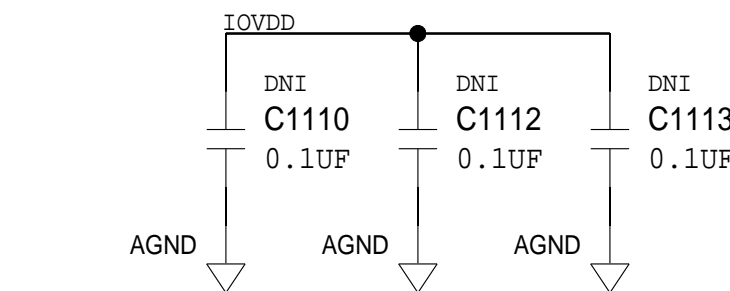
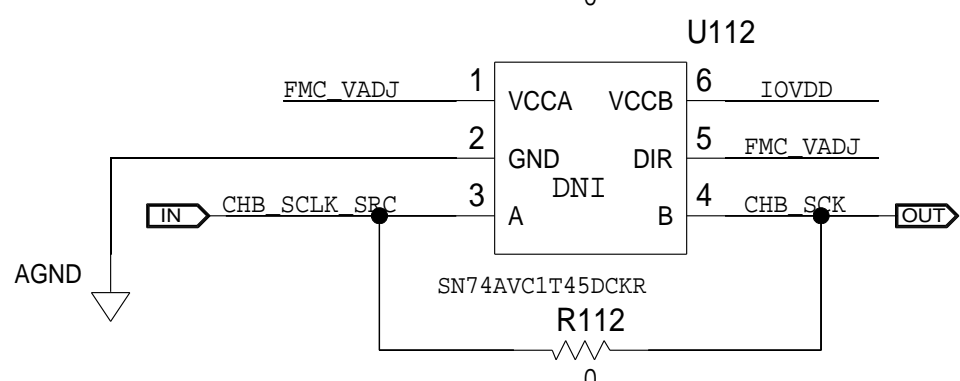
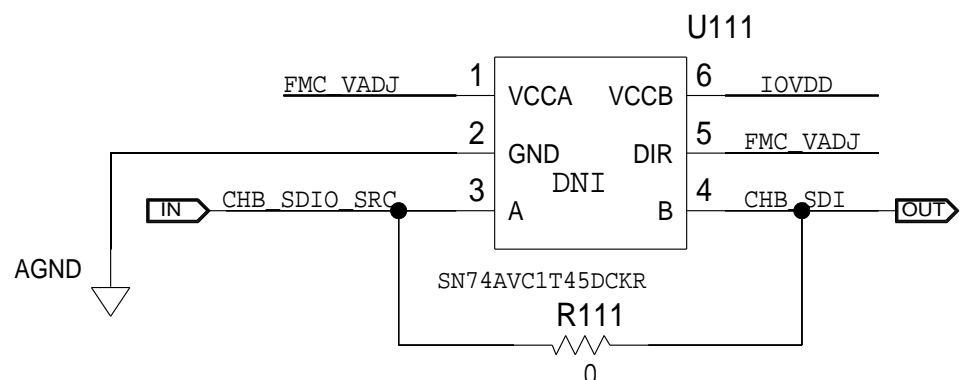
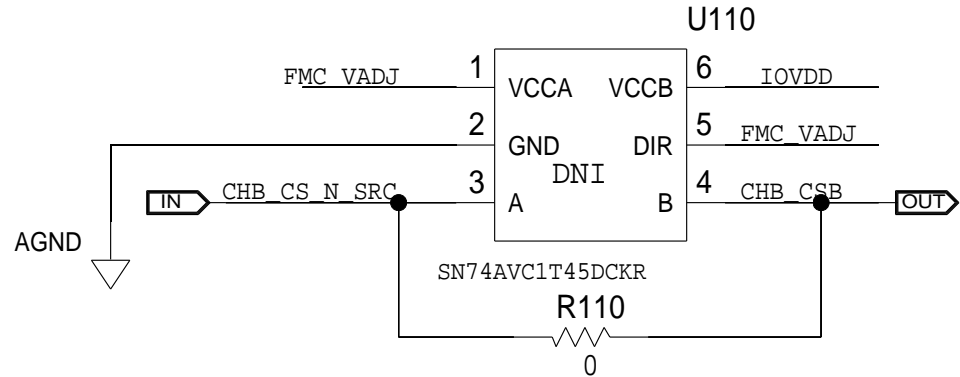
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DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_083437-02	REV C	
PTD ENGINEER D Sloan	SIZE D	SCALE 1:1	SHEET 10 OF 12

LEVEL TRANSLATION CH\_B

CONFIGURATION SPI LEVEL TRANSLATORS

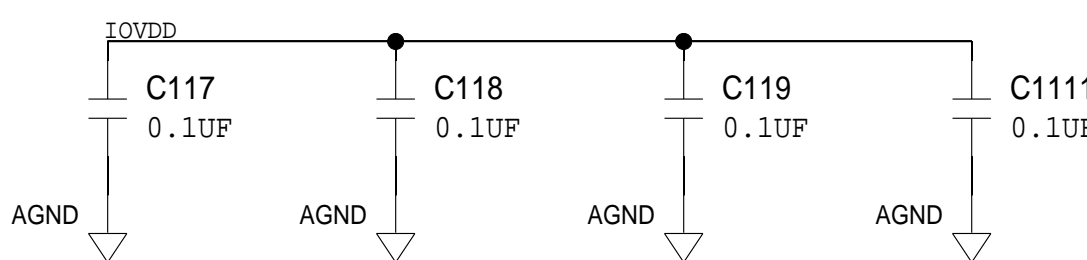
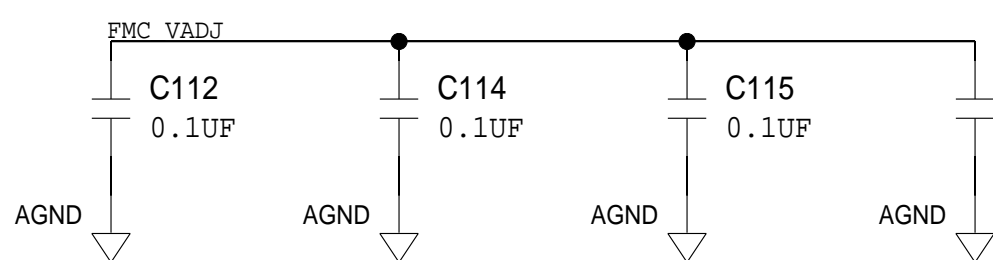
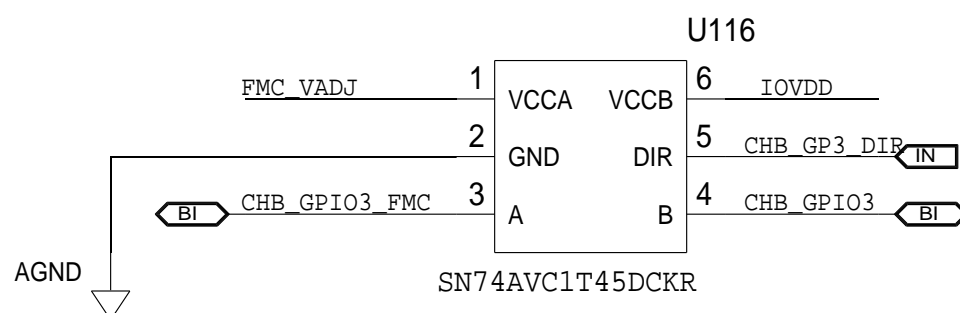
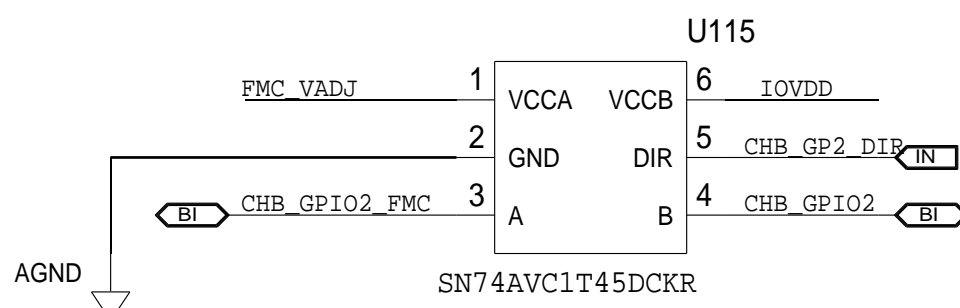
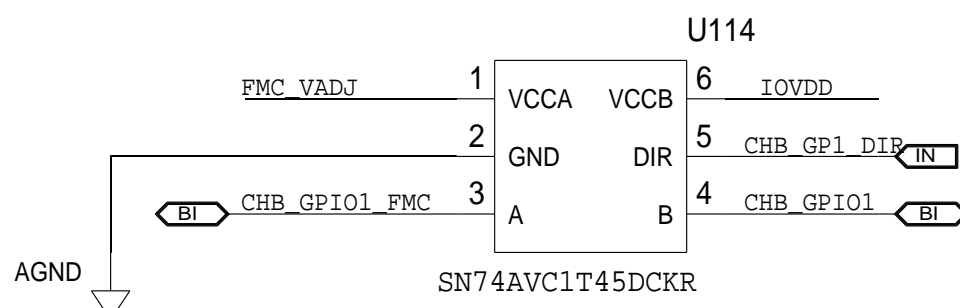
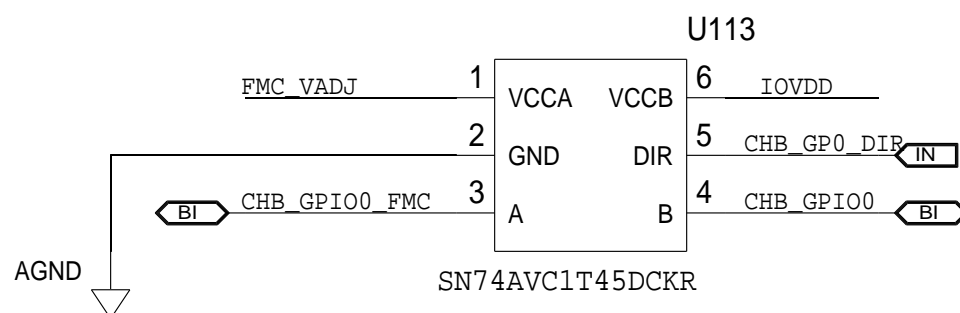
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FMC\_HOST  
SIDE

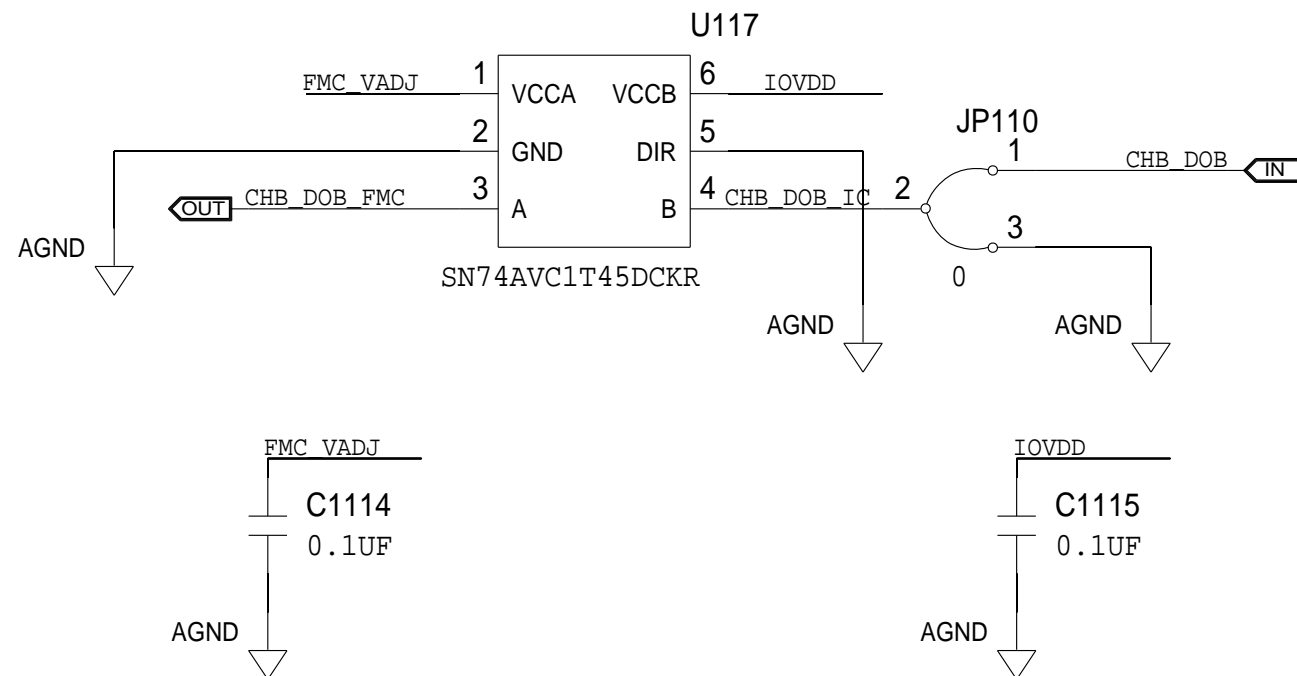
AD488X  
SIDE

GPIO LEVEL TRANSLATORS



DATA SPI LEVEL TRANSLATORS

FMC\_HOST  
SIDE



AD488X  
SIDE



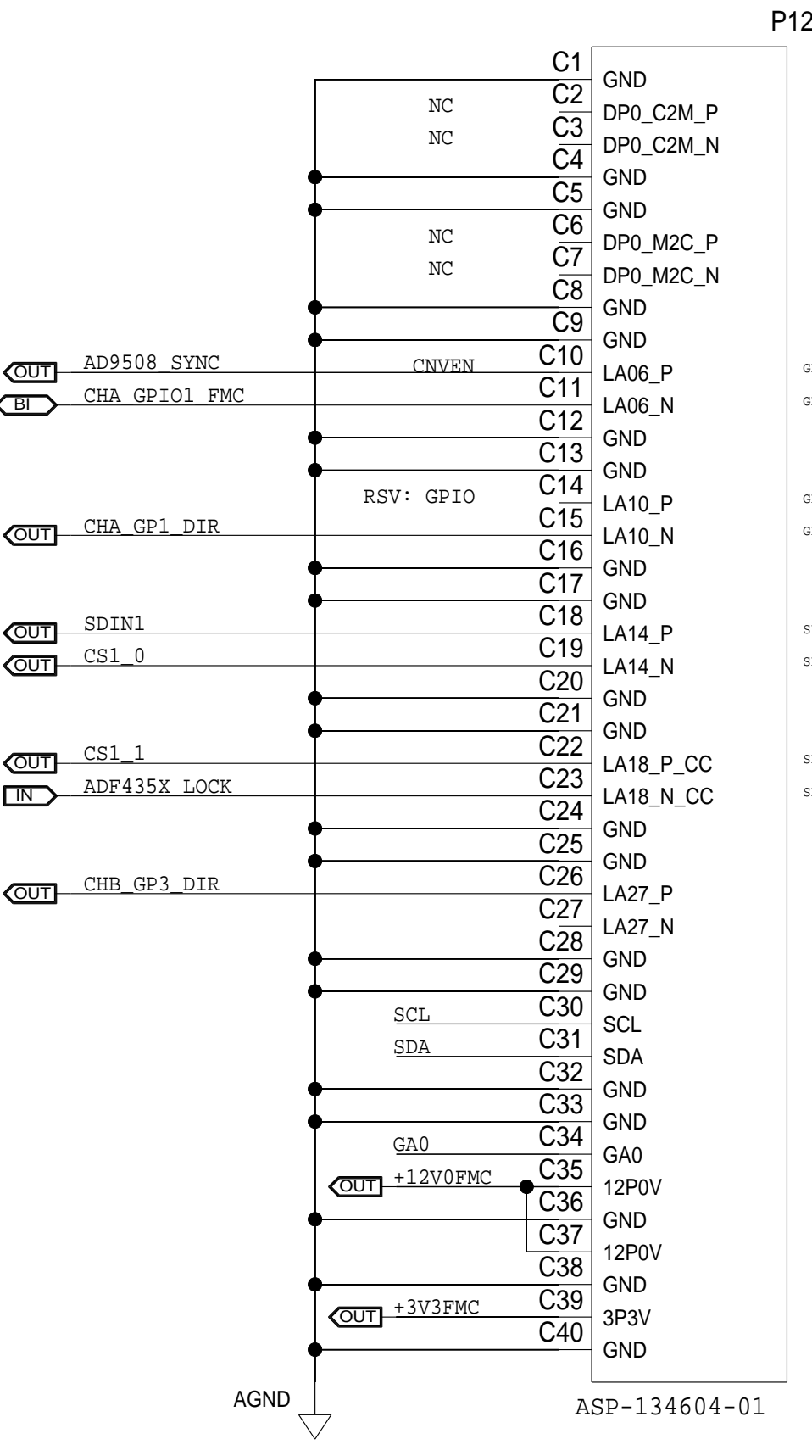
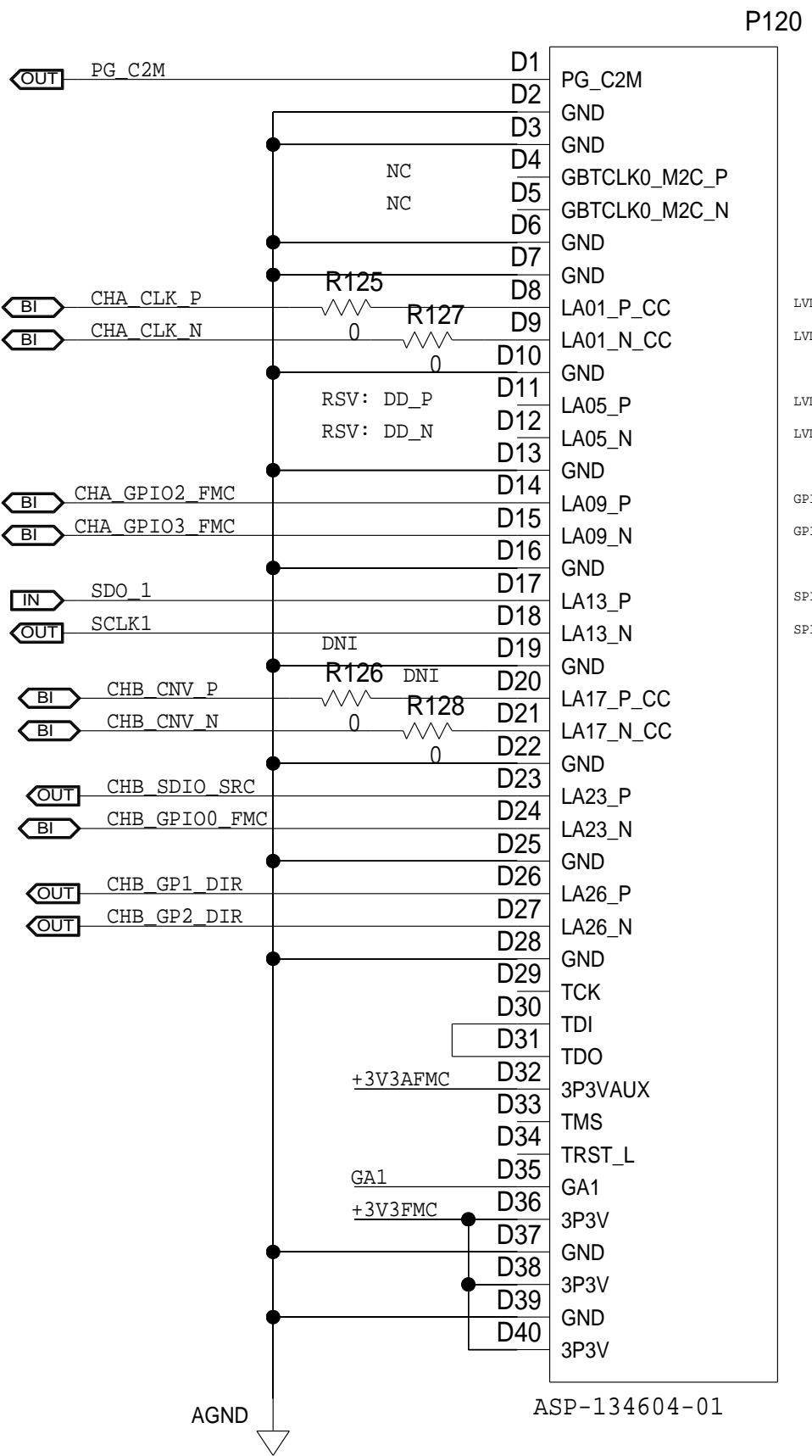
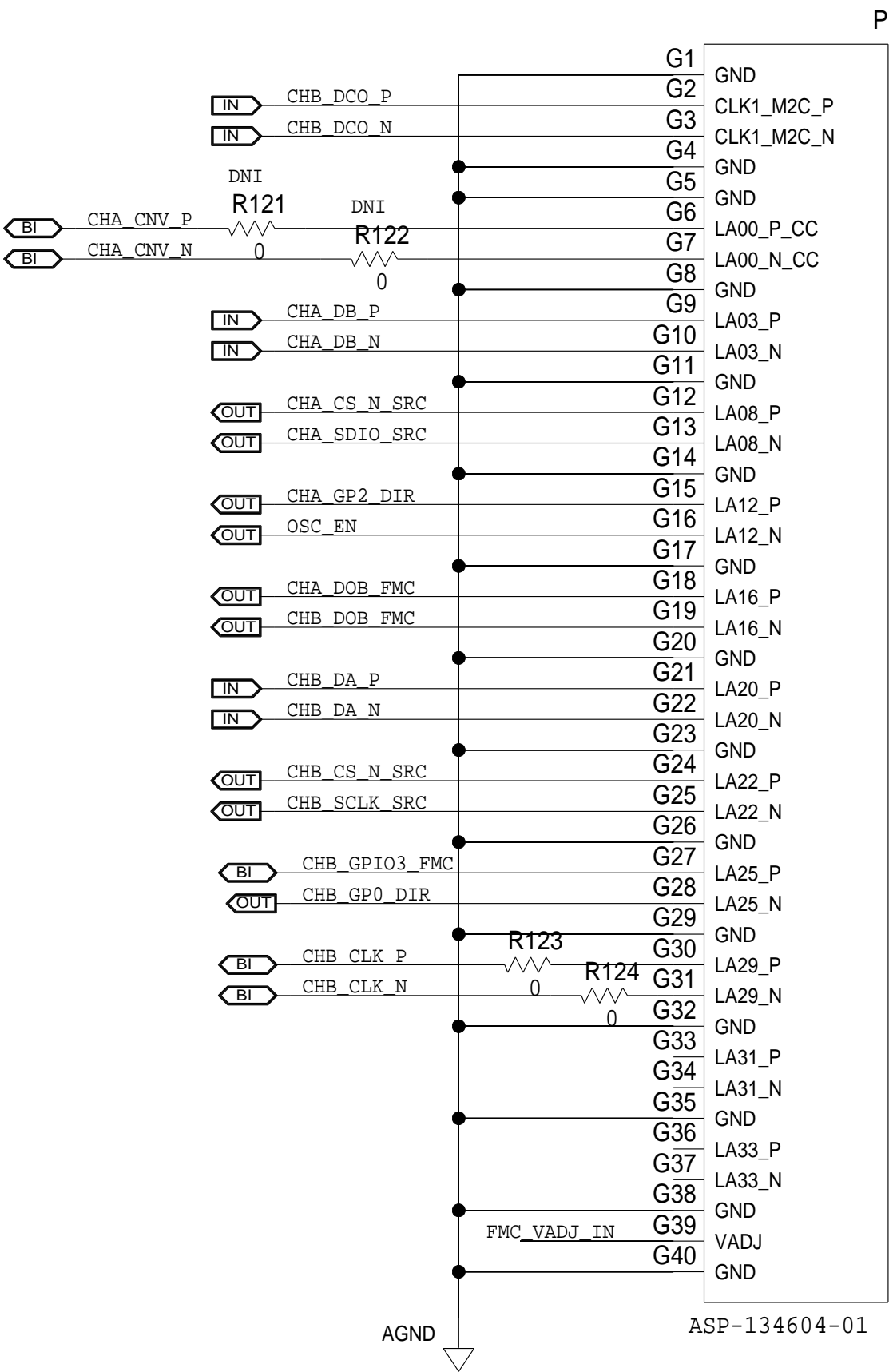
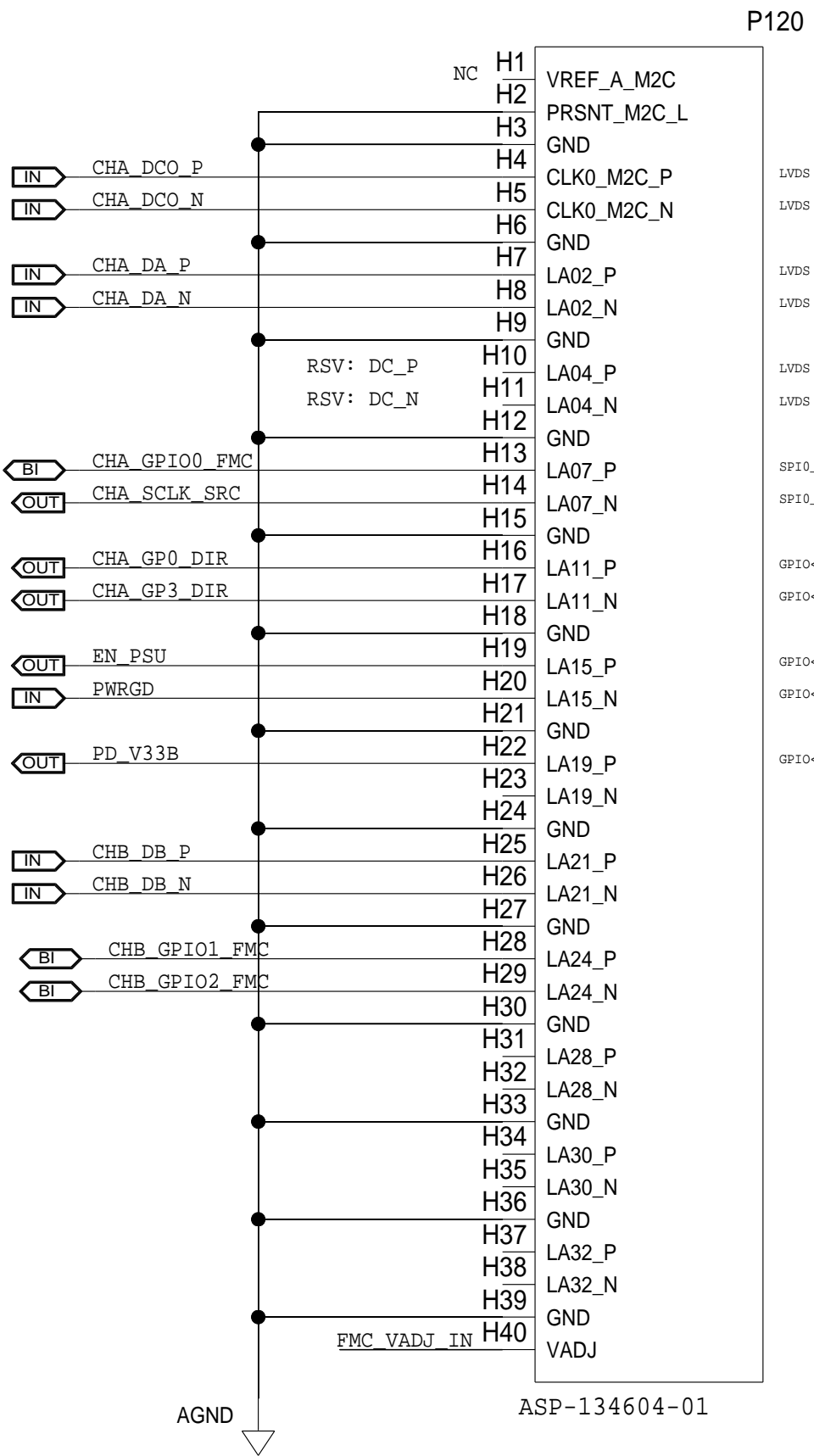
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PTD ENGINEER D Sloan	SIZE D	SCALE 1:1	SHEET 11 OF 12

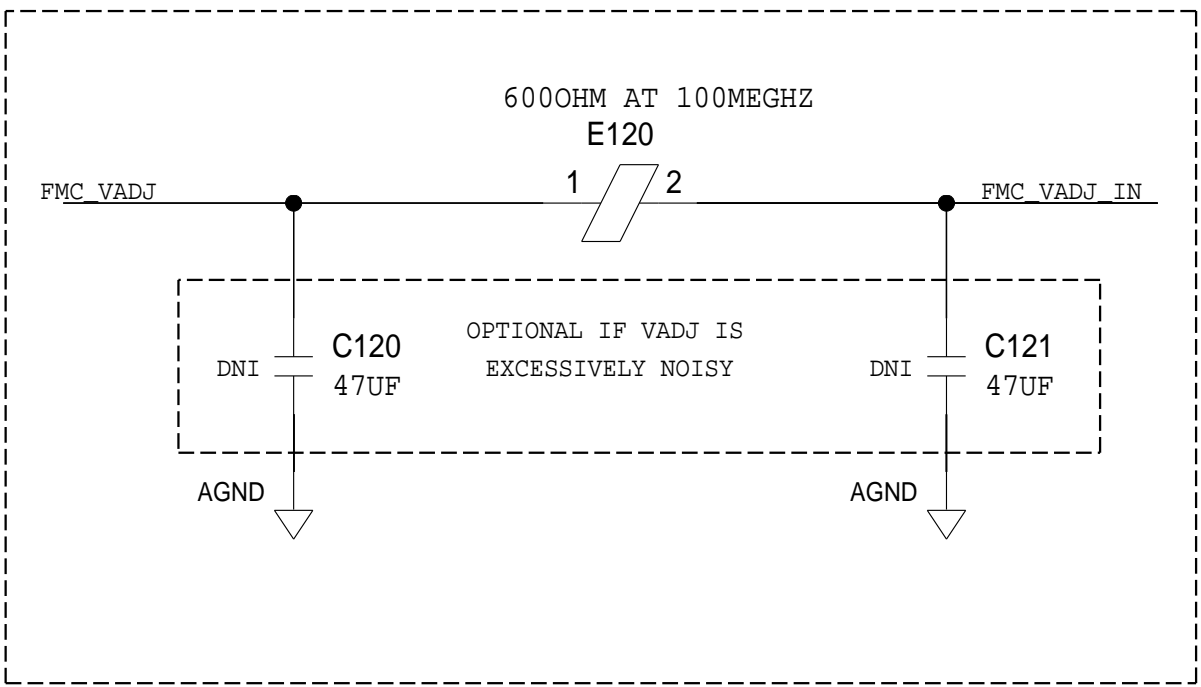


HOST (FMC) INTERFACE

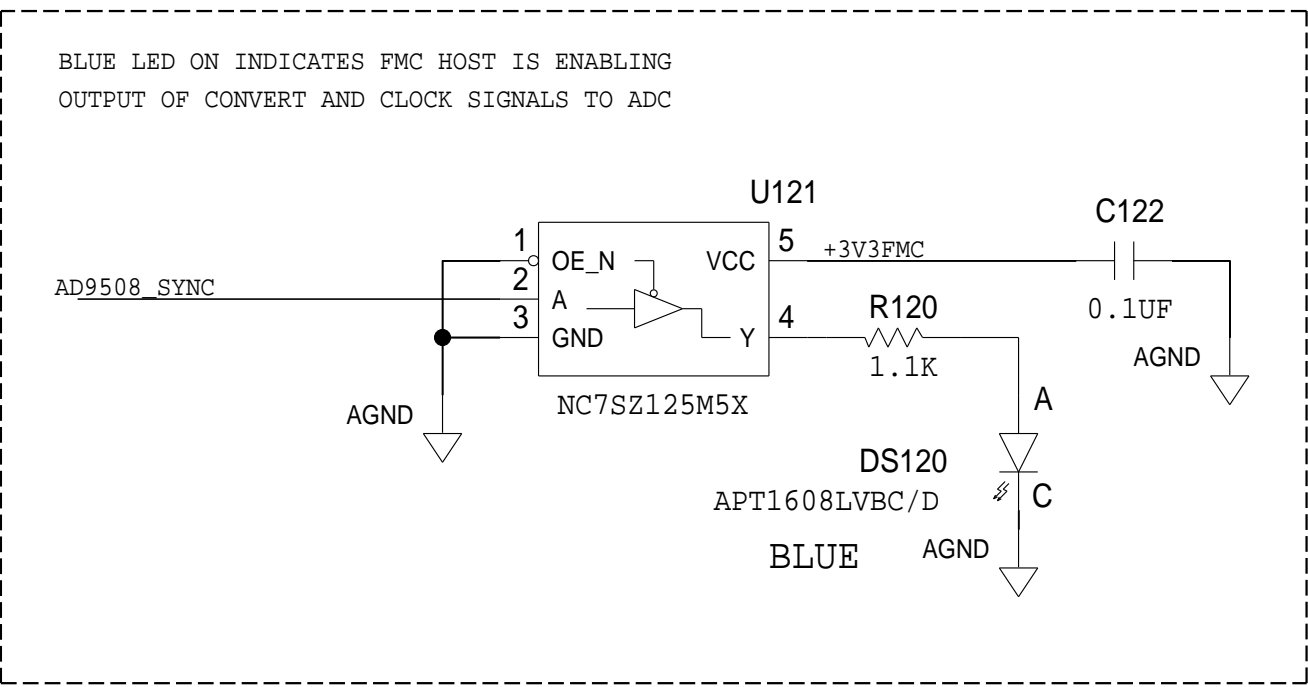
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REV	DESCRIPTION	DATE	APPROVED



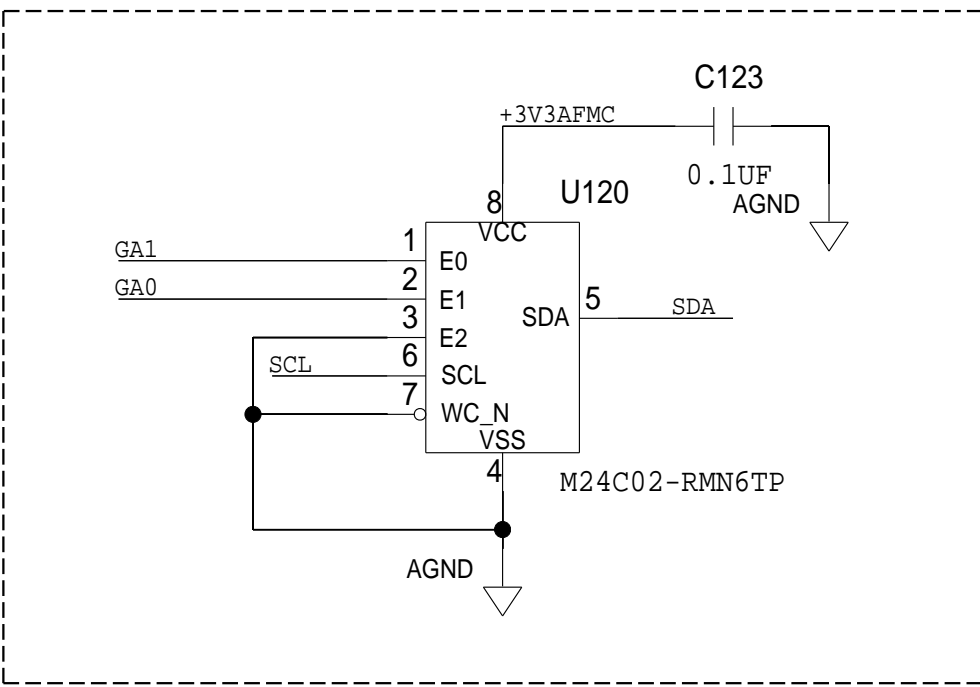
FMC\_VADJ RAIL FILTERING



CLOCKING ENABLE LED



BOARD ID EEPROM



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PTD ENGINEER D Sloan	SIZE D	SCALE 1:1	SHEET 12 OF 12