

1. DIMENSIONS ARE IN INCHES (EXCEPT WHERE NOTED).
ALL DOCUMENTS & SPECIFICATIONS REFERRED TO BELOW SHOULD BE THE LATEST REVISIONS.

2. BOARD MATERIAL:(USE CHECKED ITEMS)

- (X) ISOLA 370HR OR S1000-2 OR IT180 OR EQUIVALENT
() ISOLA-FR408HR OR EQUIVALENT
() ISOLA IS410
() MEGTRON 6
() NELCO-4000-13
() ROGERS 4350B
() ROGERS 3003
() ARLON 85N
() EM370D
() OTHER _____

3. ALL LAMINATES & BONDING MATERIALS SHOULD BE SELECTED FROM IPC-4101 OR IPC-4103.(TG-170 DEGC TO-300 DEGC)
UL FLAMMABILITY RATING 94V-0. BOARD MATERIAL & CONSTRUCTION SHALL MEET THE REQUIREMENTS OF UL796/UL796F.
4. REFER TO IPC-6010 SERIES, CLASS 2 FOR FABRICATION. WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2.
5. REFER TO LAMINATION DIAGRAM FOR OVERALL BOARD THICKNESS. TOLERANCE APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES. FINISHED THICKNESS MEASURED FROM TOP COPPER TO BOTTOM COPPER.
6. BOW & TWIST NOT TO EXCEED 0.0075 INCHES (0.75%) PER LINEAR INCH AND SHOULD BE MEASURED PER IPC-TM-650, METHOD 2.4.22.
7. ACCEPTABILITY PER ADI SPECIFICATION TS00115.

8. IMPEDANCE REQUIREMENTS: IF NO STACKUP IS DEFINED, THE VENDOR IS ALLOWED TO ADJUST THE DIELECTRIC THICKNESS & TRACE WIDTHS TO MEET THE IMPEDANCE REQUIREMENT. IF SPECIFIED, THE VENDOR MUST MEET THE REQUIREMENTS LISTED IN THE IMPEDANCE TABLE. ANY ADJUSTMENT MADE TO THE DEFINED STACKUP, TRACE WIDTH & SPACING THAT IMPACT THE REQUIREMENTS MUST HAVE WRITTEN APPROVAL FROM ADI.
9. FILLET OPTIONS TO ENHANCE RELIABILITY AT PAD JUNCTIONS WHERE SPACING PERMITS.
() FILLETS ALLOWED
(X) FILLETS NOT ALLOWED
10. THEIVING:
() VENDOR MAY ADD THEIVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS MAINTAINING A MINIMUM 0.100 INCH CLEARANCE FROM ALL COPPER FEATURES.
(X) VENDOR MAY NOT ADD THEIVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS.
11. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.003 INCHES.

12. DRILL SIZES ARE FINISHED HOLE SIZES. ALL HOLES SHALL BE LOCATED WITHIN 0.005 INCHES DTP UNLESS SPECIFIED. MINIMUM BARREL PLATING OF 0.001 INCHES. PLATED HOLES SHALL NOT BE ROUGH OR IRREGULAR SO AS TO HINDER PROPER SOLDER WICKING. BARREL RELIEF ON SOLDERMASK ALLOWED IN UNFILLED VIA IN PAD HOLES.

13. PLATING SPECIFICATION:
(X) REFER TO LAMINATION DIAGRAM FOR FINISHED COPPER WEIGHT/THICKNESS REQUIREMENTS
THE STARTING COPPER WEIGHT/THICKNESS CAN VARY AS LONG AS THE FINISHED COPPER WEIGHT/THICKNESS IS NOT LESS THAN THE SPECIFIED VALUE.

14. SURFACE FINISH:
- (X) IMMERSION GOLD (ENIG) 1.58-3.94 MICRO INCHES OVER 118-236 MICRO INCHES MIN. OF ELECTROLESS NICKEL PER IPC-4552
 - () OSP (ORGANIC SOLDERABILITY PRESERVATIVE)
 - () IMMERSION SILVER
 - () SOFT WIRE BONDABLE GOLD 30-50 MICRO INCHES OF SOFT WIRE
BONDABLE GOLD OVER 100-150 MICRO INCHES OF NICKEL
 - () EDGE CONNECTOR FINGERS ARE TO BE PLATED WITH 100 MICRO-INCHES (.0001") OF LOW STRESS
NICKEL UNDER 30 MICRO-INCHES (.00003") OF GOLD
 - () OTHER _____

15. SOLDERMASK:
- SOLDERMASK OVER BARE COPPER OR BARE GOLD (BOTH SIDES) TO MEET IPC-SM-840.
- IF PRESENT, DO NOT MODIFY SOLDERMASK DEFINED PADS (MASK OPENINGS LESS THAN COPPER PAD) WITHOUT APPROVAL.
- (X) LPI
- () OTHER_____
- COLOR
- (X) GREEN
- () OTHER_____

16. APPLY SILKSCREEN TO BOTH SIDES USING A NON-CONDUCTIVE, EPOXY BASED INK PER ARTWORK.
(X) WHITE
() OTHER


17. FINAL ELECTRICAL TEST TO BE PERFORMED USING PROVIDED IPC-D-356A NETLIST OR ODB++ FORMAT FILE.
THE PCB SHALL HAVE A VERIFICATION STAMP.

18. A TIME DOMAIN REFLECTOMETER REPORT (TDR) FOR EACH IMPEDANCE CONTROLLED LAYER & A CERTIFICATE OF COMPLIANCE SHALL BE PROVIDED BY VENDOR AT TIME OF SHIPMENT. INSTANCES WHERE TDR TESTING CAN'T BE PERFORMED BECAUSE THE TRACE LENGTH IS TOO SHORT ON THE OUTER LAYERS AT THE PIN ESCAPES IS ACCEPTABLE. ALL OTHER INSTANCES MUST BE REPORTED.

19. IF PRESENT, ALL BLIND/BURIED VIAS WITH AN ASPECT RATIO $<1:1$ TO BE PLATED SHUT WITH COPPER WHEN USED AS VIA-IN-PAD OR AS A STACKED VIA. BLIND/BURIED VIAS WITH AN ASPECT RATIO $>1:1$ TO BE FILLED WITH NON-CONDUCTIVE EPOXY.
20. FOR VIA FILL INFORMATION REFER TO DRILL CHART:
 - () NON-CONDUCTIVE EPOXY FILL ALL INCHES DRILLED VIAS
 - () COPPER FILL ALL INCHES DRILLED VIAS
21. INTENTIONAL SHORTS:
 - IF AN INTENTIONAL SHORT REPORT IS SUPPLIED AND DOES NOT MATCH THE FAB DATA THEN ADI APPROVAL IS REQUIRED.
22. PEMNUTS:
 - () PEMNUTS TO BE INSTALLED BY FABRICATOR
 - () PEMNUTS NOT TO BE INSTALLED BY FABRICATOR
 - (X) NOT APPLICABLE
23. MANUFACTURER TO ETCH/STAMP WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE UNLESS OTHERWISE SPECIFIED:
 - A. UL CODE-FLAMMABILITY RATING FOR THOSE APPROVED MATERIALS (IF APPLICABLE)
 - B. DATE CODE
 - C. LOT NUMBER
 - D. MANUFACTURER LOGO
24. PANELIZATION:
 - BOARDS TO BE SHIPPED IN ARRAY AND KEPT INTACT
 - PANEL TO BE SUBJECTED TO CUSTOMERS APPROVAL
 - PANEL SOLDER PASTE STENCIL GERBER TO BE PROVIDED TO ANALOG
25. MINIMUM DESIGN LINE WIDTH IS .008 INCH.
26. MINIMUM DESIGN LINE SPACING IS .008 INCH.

FAB NOTES REVISION: NOVEMBER 21 2022

LAMINATION DIAGRAM

LAYER NUMBER	LAYER NAME	COPPER THICKNESS (OZ., INCH)	DIELECTRIC THICKNESS (INCH)	MATERIALS
1 TOP	1 OZ., 0.0014"		FINAL CU (THICKNESS AFTER PLATING)	
			TBD	ISOLA 370HR/EQUIVALENT
2 BOTTOM	1 OZ., 0.0014"		FINAL CU (THICKNESS AFTER PLATING)	

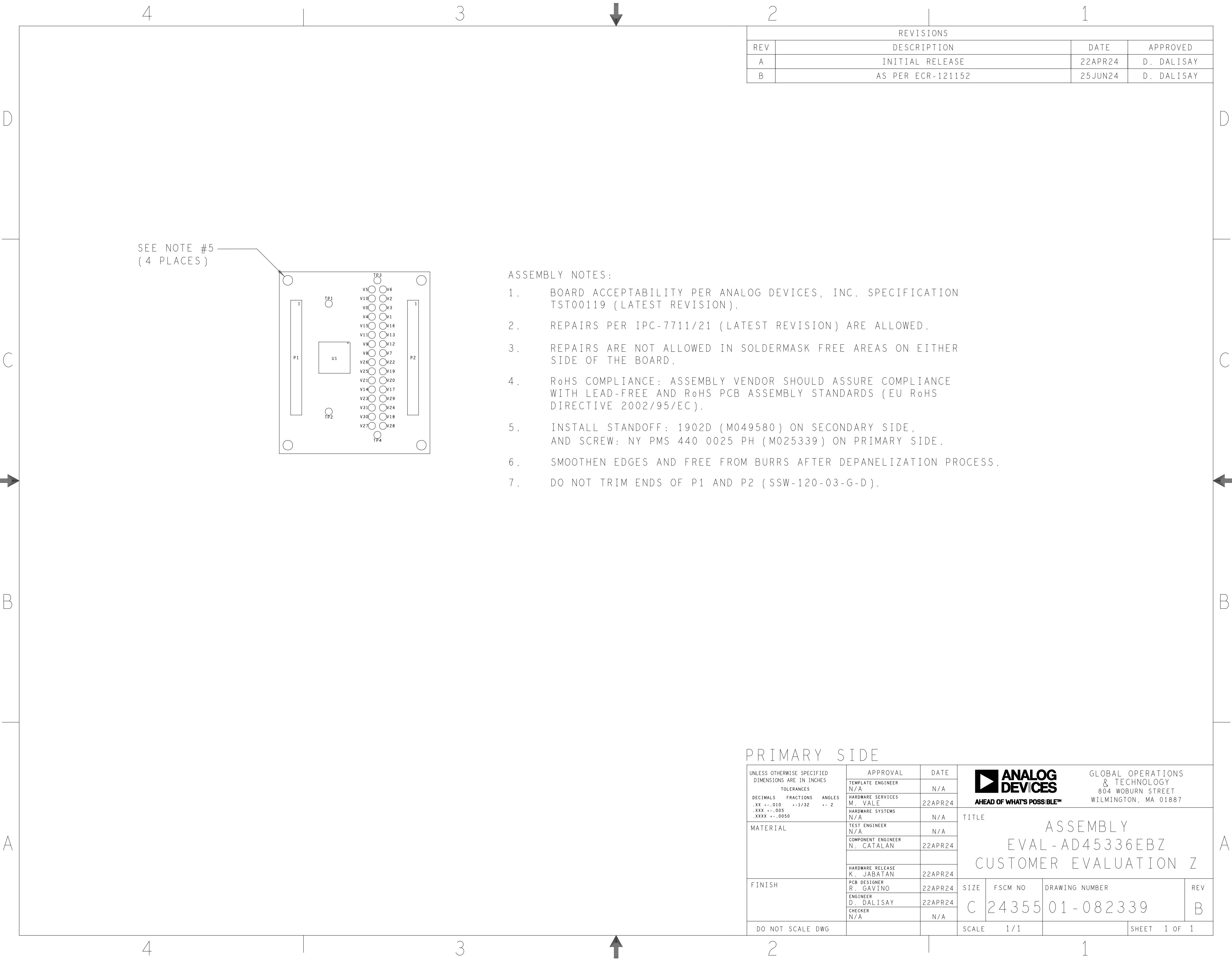
THE FINISHED PCB THICKNESS TO BE: 0.062" +/-10%



**ANALOG
DEVICES**
AHEAD OF WHAT'S POSSIBLE

GLOBAL OPERATIONS
& TECHNOLOGY
804 WOBURN STREET
WILMINGTON, MA 01887

SIZE	FSCM NO	DRAWING NUMBER	REV
C	24355	09-082339	B
SCALE	1/1		SHEET 2 OF 2




REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	22APR24	D. DALISAY
B	AS PER ECR-121152	25JUN24	D. DALISAY

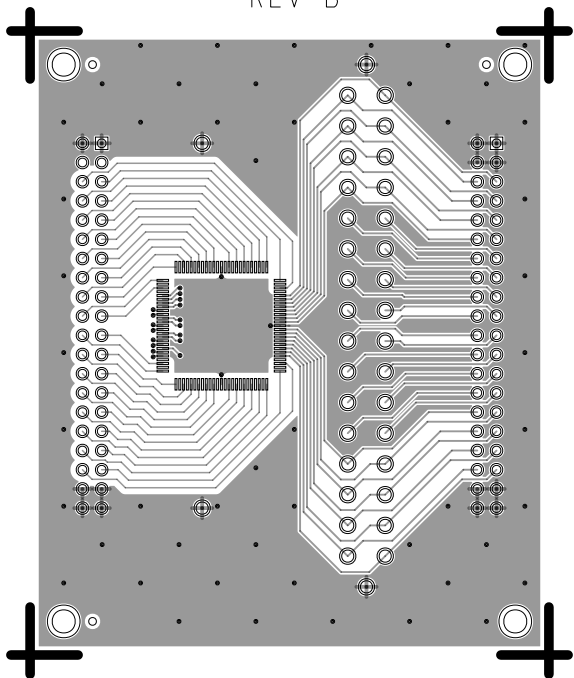
ASSEMBLY NOTES:

1. BOARD ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00119 (LATEST REVISION).
2. REPAIRS PER IPC-7711/21 (LATEST REVISION) ARE ALLOWED.
3. REPAIRS ARE NOT ALLOWED IN SOLDERMASK FREE AREAS ON EITHER SIDE OF THE BOARD.
4. RoHS COMPLIANCE: ASSEMBLY VENDOR SHOULD ASSURE COMPLIANCE WITH LEAD-FREE AND RoHS PCB ASSEMBLY STANDARDS (EU RoHS DIRECTIVE 2002/95/EC).
5. INSTALL STANDOFF: 1902D (M049580) ON SECONDARY SIDE, AND SCREW: NY PMS 440 0025 PH (M025339) ON PRIMARY SIDE.
6. SMOOTHEN EDGES AND FREE FROM BURRS AFTER DEPANELIZATION PROCESS.
7. DO NOT TRIM ENDS OF P1 AND P2 (SSW-120-03-G-D).

PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX -.010 --1/32 -- 2 .XXX -.005 .XXXX -.0050			APPROVAL		DATE		<div><div><div></div><div>AHEAD OF WHAT'S POSSIBLE™</div></div><div>GLOBAL OPERATIONS & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887</div></div>			
			TEMPLATE ENGINEER N/A		N/A					
			HARDWARE SERVICES M. VALE		22APR24					
			HARDWARE SYSTEMS N/A		N/A					
MATERIAL			TEST ENGINEER N/A		N/A					
			COMPONENT ENGINEER N. CATALAN		22APR24					
			HARDWARE RELEASE K. JABATAN		22APR24		SIZE FSCM NO DRAWING NUMBER REV C 24355 01 - 082339 B			
FINISH			PCB DESIGNER R. GAVINO		22APR24					
			ENGINEER D. DALISAY		22APR24					
			CHECKER N/A		N/A					
DO NOT SCALE DWG							SCALE 1 / 1		SHEET 1 OF 1	

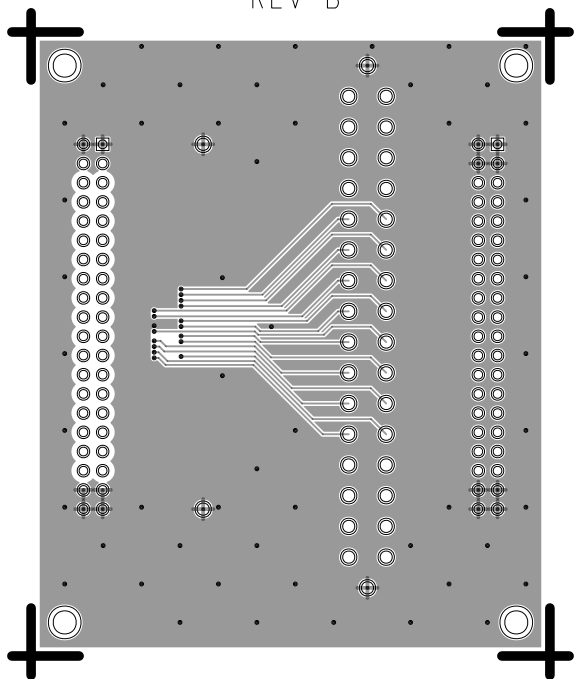
L1 PRIMARY
08-082339-01
REV B



L2 SECONDARY

08-082339-02

REV B



SILKSCREEN PRIMARY

08-082339-03

REV B



**ANALOG
DEVICES**

AHEAD OF WHAT'S POSSIBLE™

P1
2 1

TP1
GND

EVAL-AD45336EBZ
08-082339 REV B
PRIMARY SIDE

U1



40 39

TP2 GND



CAUTION
HIGH VOLTAGE



TP3 GND

V5	V6
V10	V2
V0	V3
V4	V1
V15	V16
V11	V13
V9	V12
V8	V7
V26	V22
V25	V19
V21	V20
V14	V17
V23	V29
V31	V24
V30	V18
V27	V28

P2
2 1

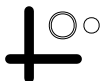
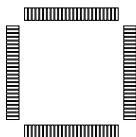
40 39

TP4
GND

SOLDERMASK PRIMARY

08-082339-04

REV B



SILKSCREEN SECONDARY

08-082339-05

REV B



SECONDARY SIDE
08-082339 REV B
EVAL-AD42330EB5



SOLDERMASK SECONDARY

08-082339-06

REV B



PASTEMASK PRIMARY

08-082339-07

REV B

