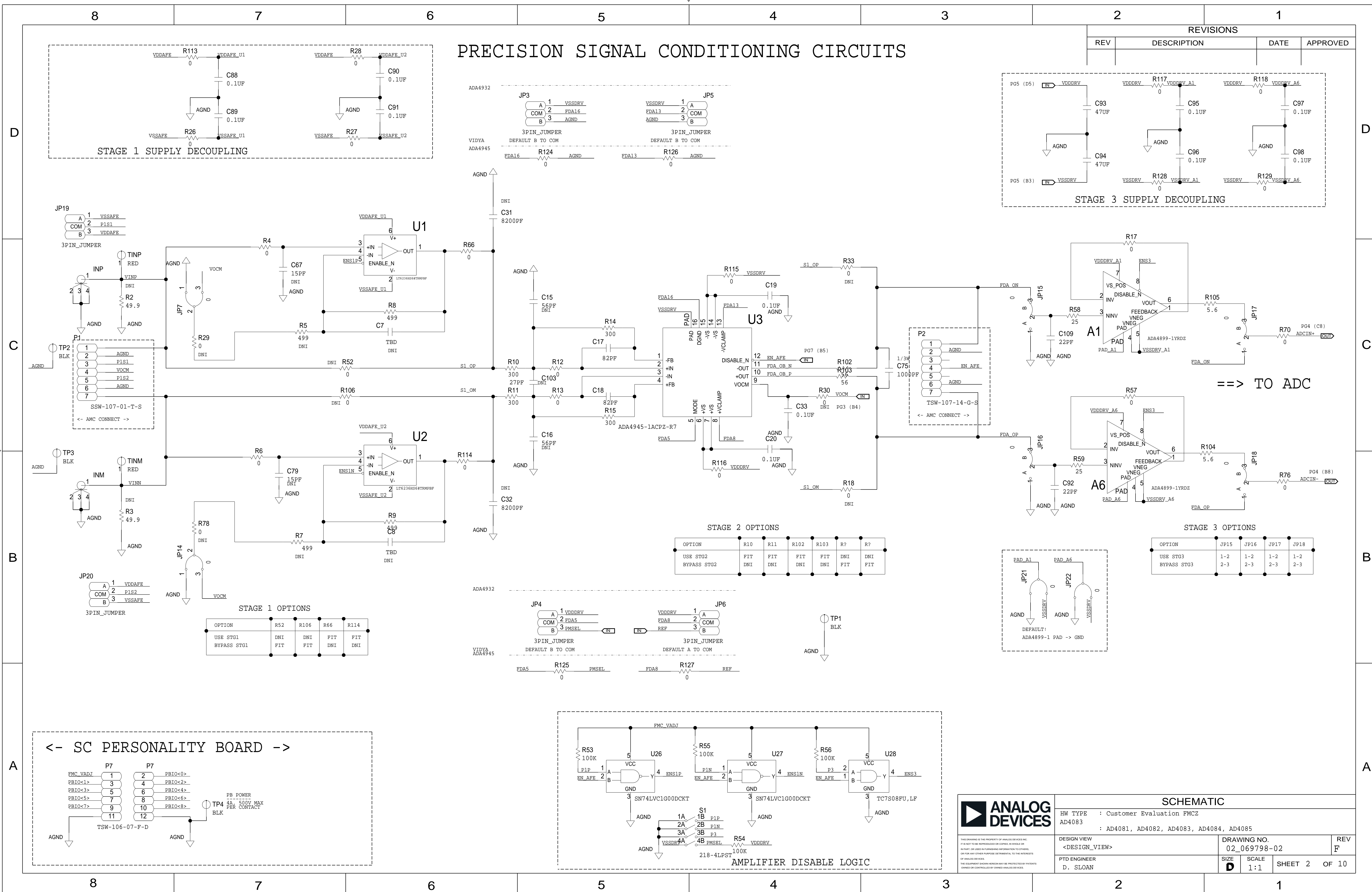


[illegible]







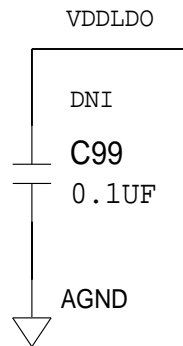


AD408X CKTS

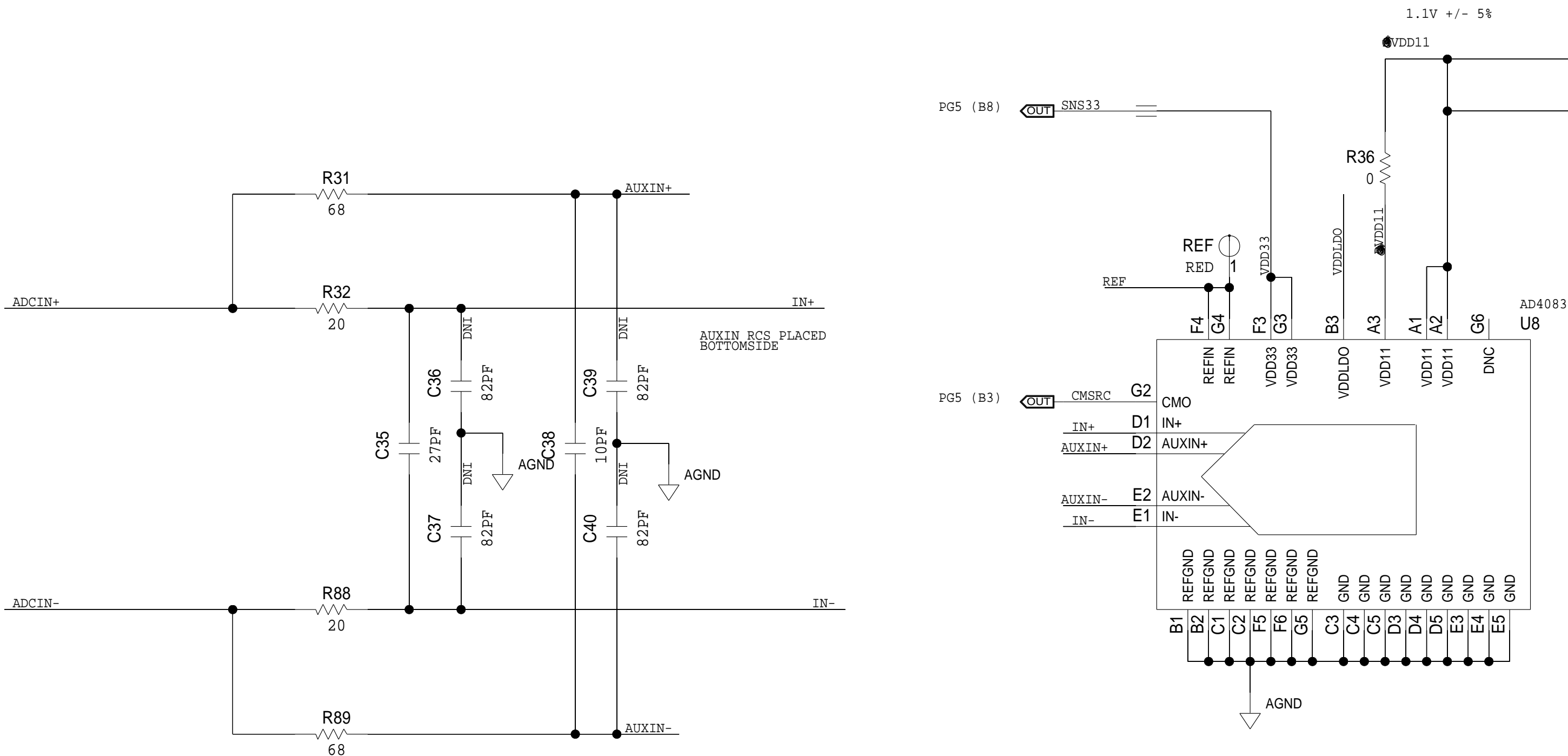
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

3.3V +/- 5%  
PG6 (D2)  VDD33 REVIEW: SHOULD TBD DECOUPLING BE ADDED CLOSE TO DUT FOR VDD33?

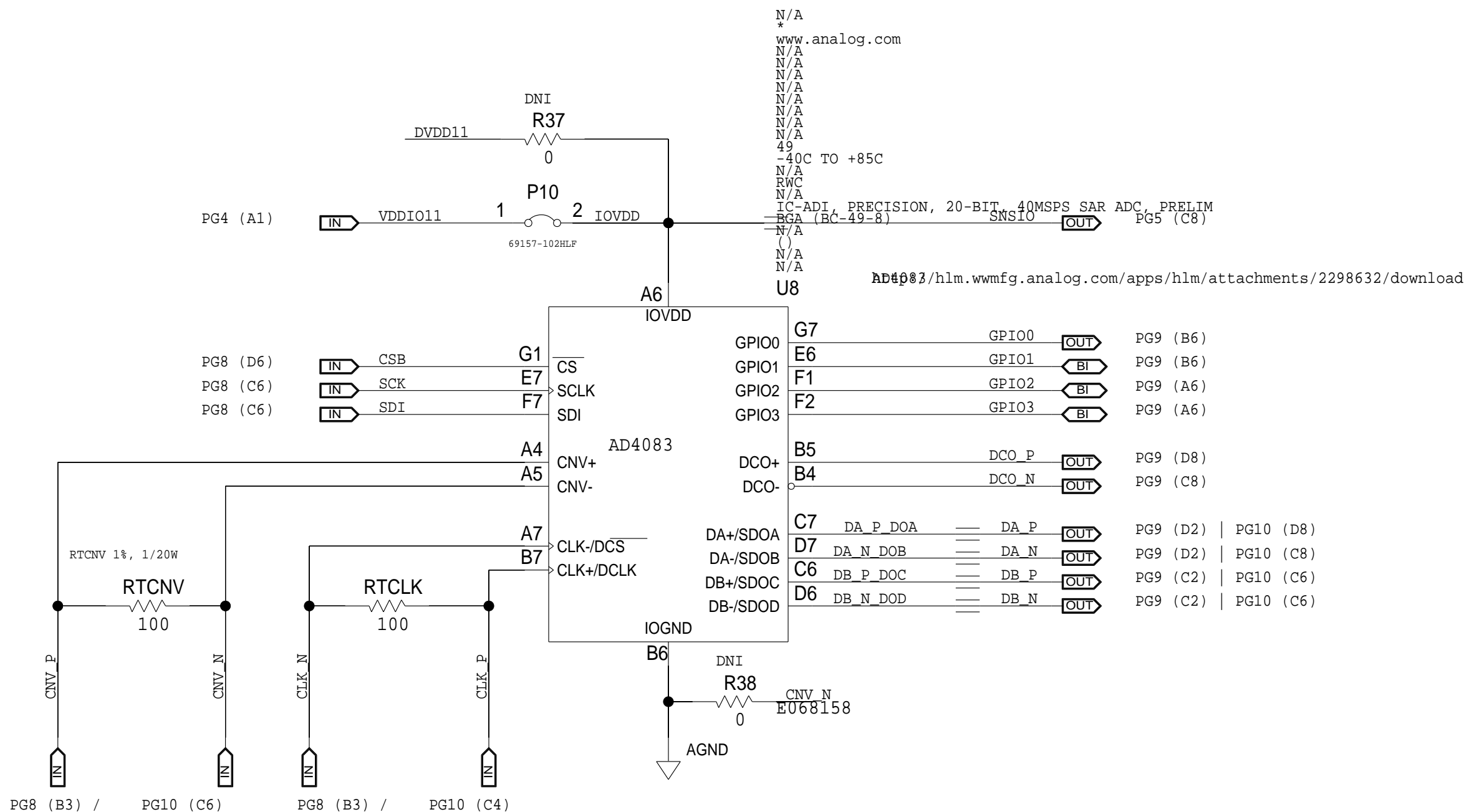
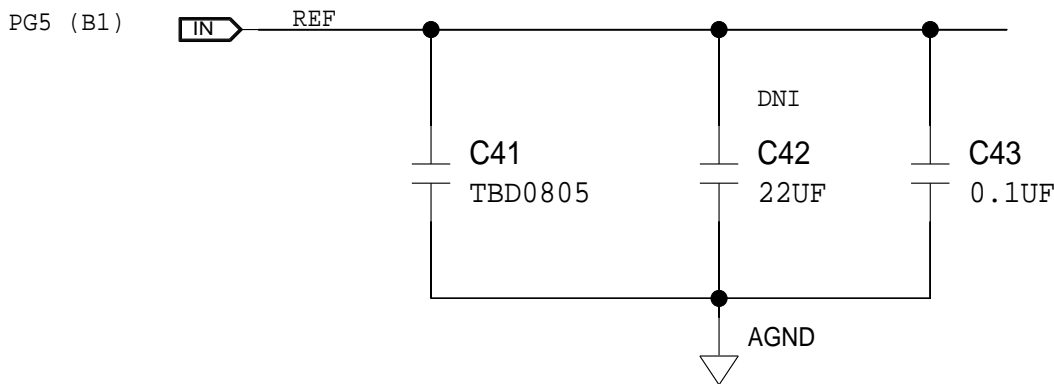
1.5V-2.75V  
PG6 (C2)  VDDLDO



INPUT NETWORK



REFERENCE FILTER

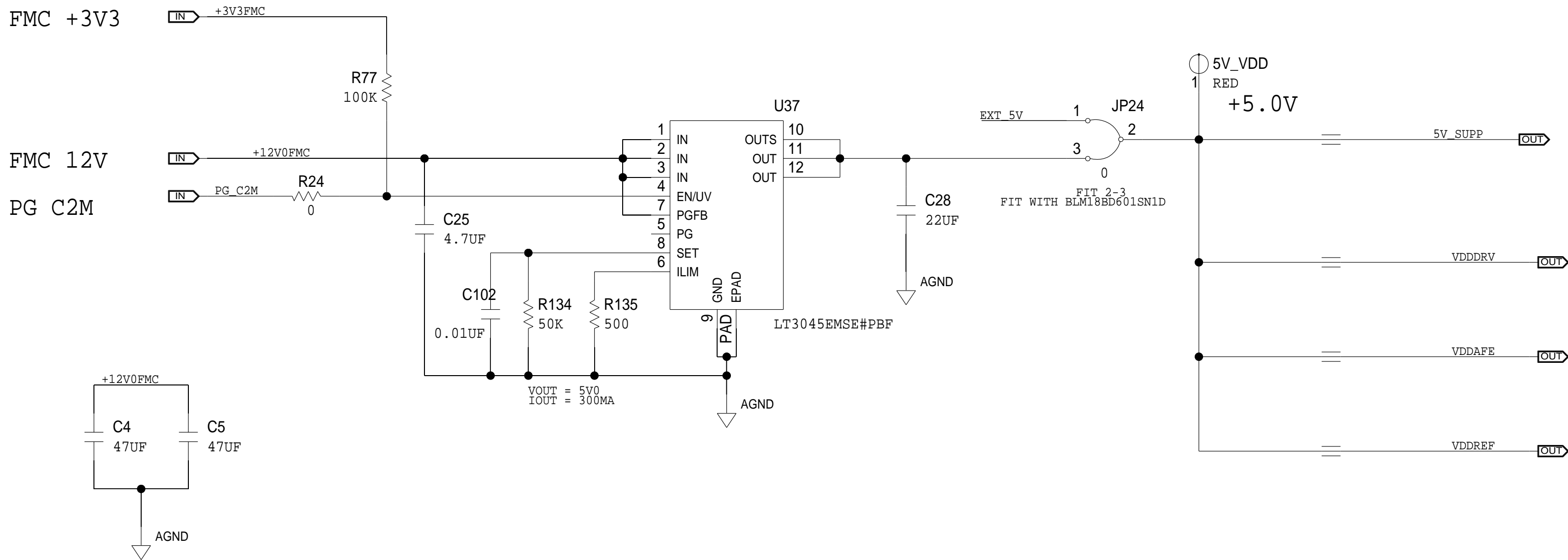


ANALOG DEVICES	SCHEMATIC			
	HW TYPE : Customer Evaluation FMCZ AD4083	DRAWING NO. 02_069798-02		REV F
DESIGN VIEW <DESIGN_VIEW>		SIZE D	SCALE 1:1	SHEET 4 OF 10
PTD ENGINEER D. SLOAN				

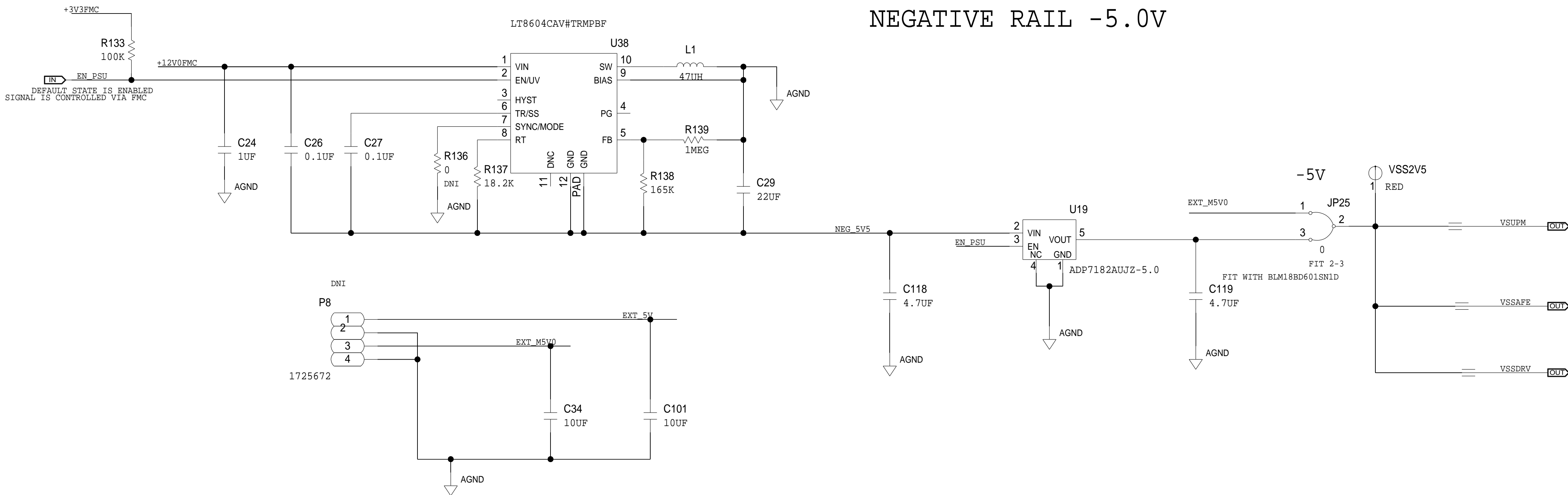
# REFERENCE & AMPLIFIER SUPPLY GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

## POSITIVE RAIL +5.0V



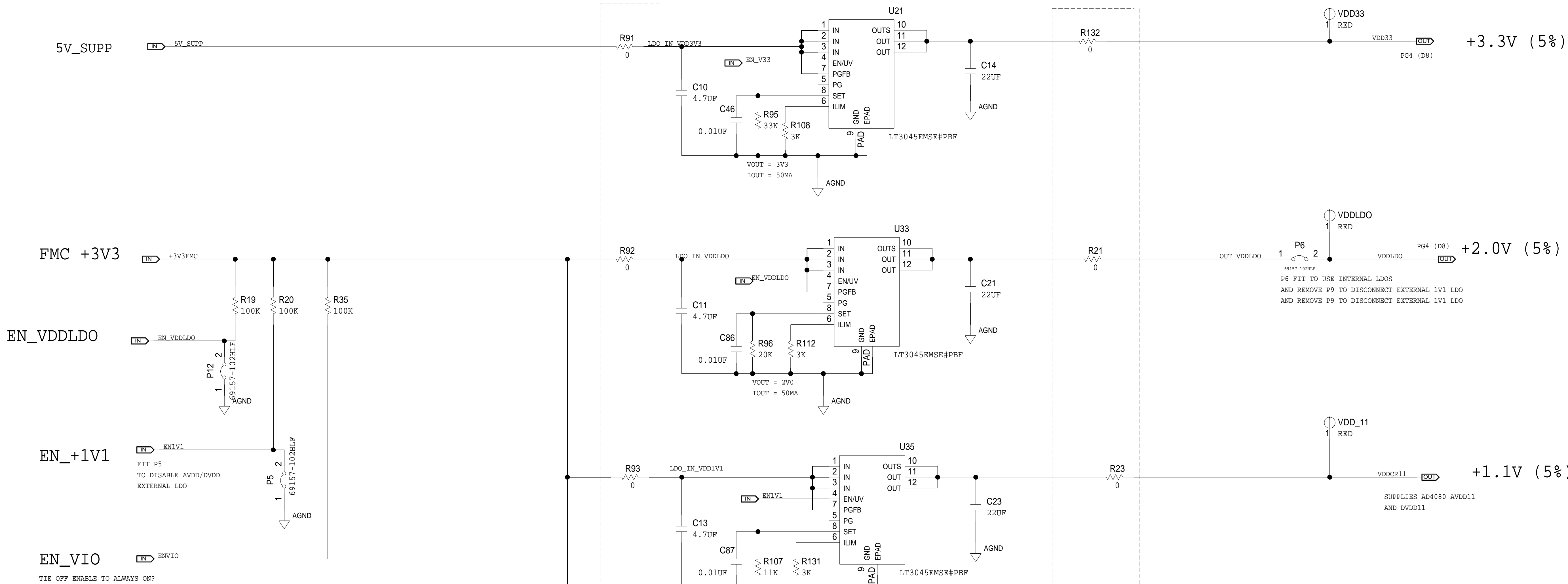
## NEGATIVE RAIL -5.0V



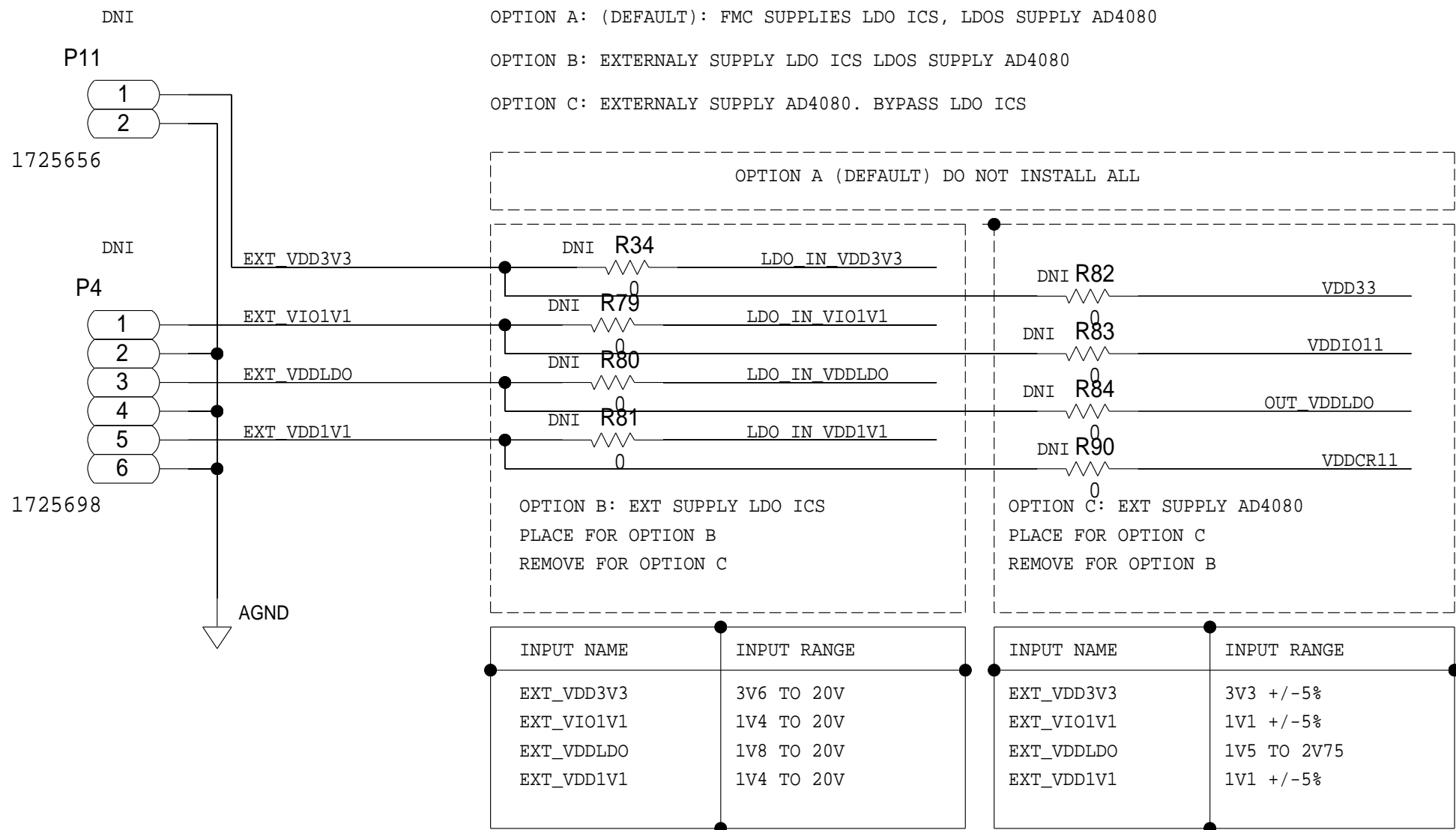
SCHEMATIC			
HW TYPE : Customer Evaluation FMCZ AD4083			
: AD4081, AD4082, AD4083, AD4084, AD4085			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_069798-02	REV F	
PTD ENGINEER D. SLOAN	SIZE D	SCALE 1:1	SHEET 5 OF 10

AD4080 DEVICE POWER SUPPLY

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



EXTERNAL SUPPLY OPTIONS



**SCHEMATIC**

HW TYPE : Customer Evaluation FMCZ  
AD4083

DESIGN VIEW : AD4081, AD4082, AD4083, AD4084, AD4085

PTD ENGINEER : D. SLOAN

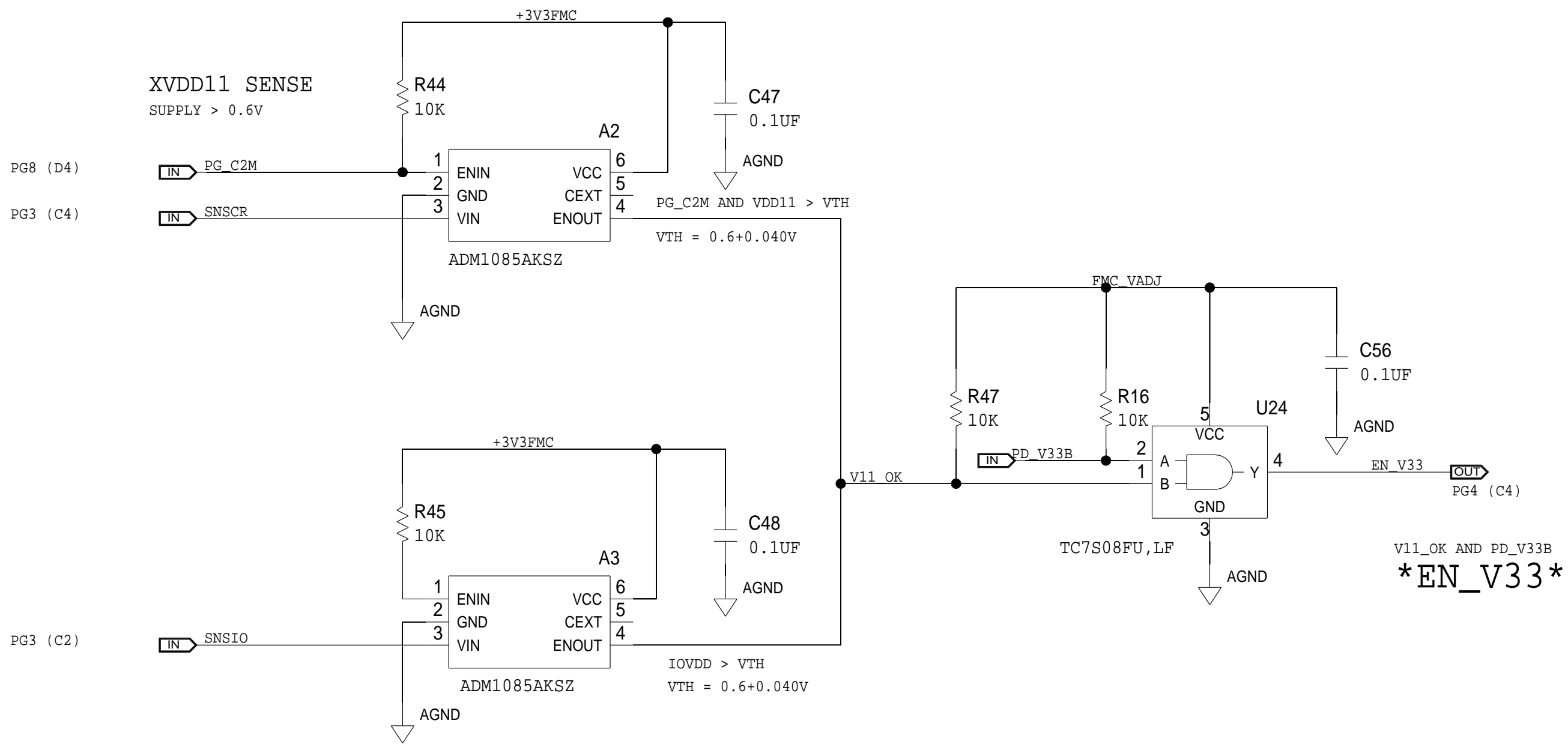
DRAWING NO. 02\_069798-02

REV F

SIZE D	SCALE 1:1	SHEET 6 OF 10
--------	-----------	---------------



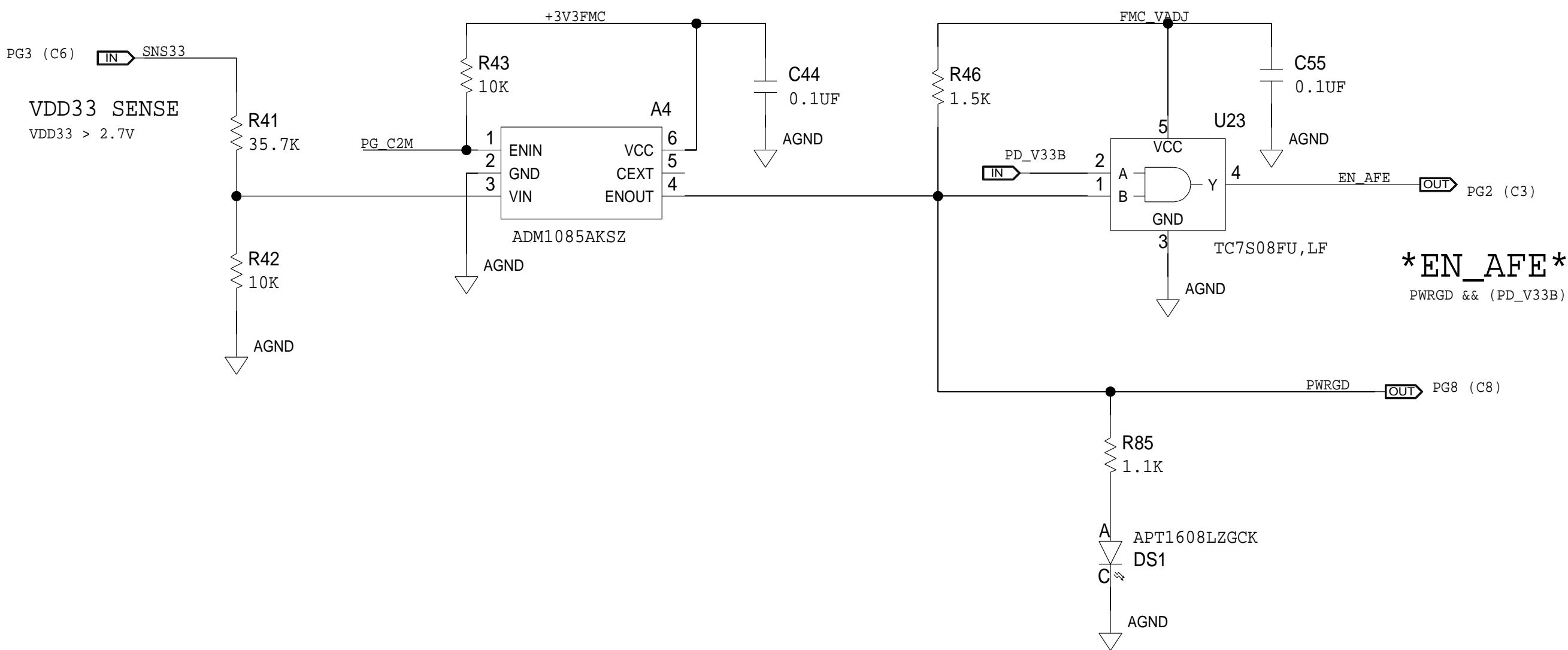
SUPPLY SEQUENCE CIRCUITS



ADM1085 SELECTED FOR OPEN DRAIN OUTPUT

\*PWRGD\*

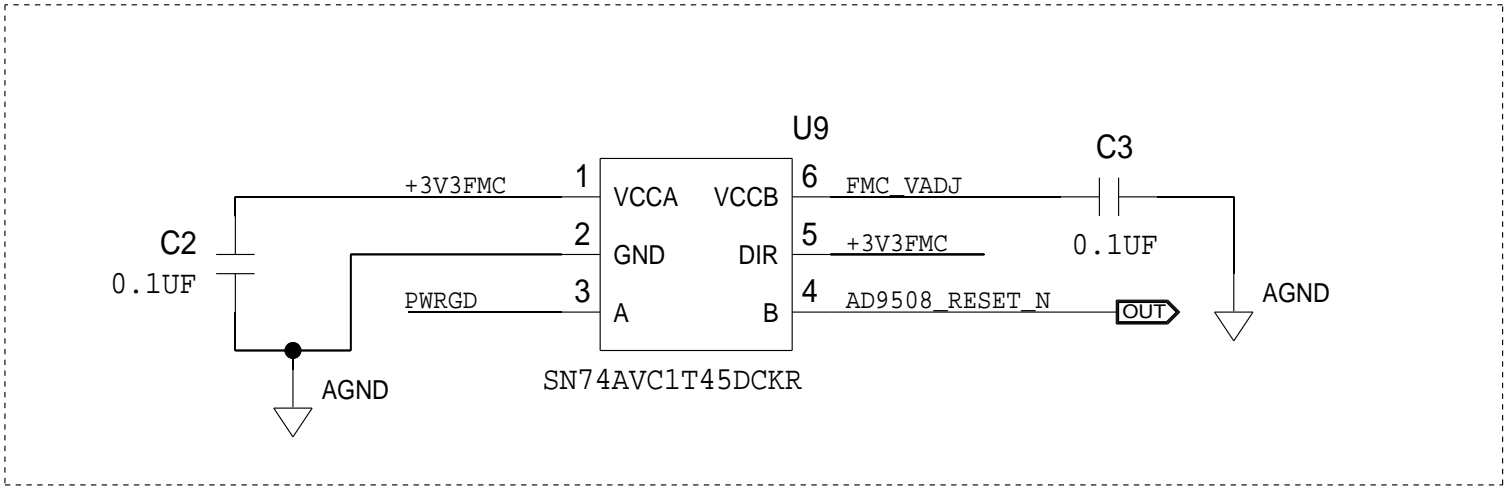
PG\_C2M && (VDD33 > VTH1/ATT) ~2.74V  
VTH = 0.6+0.040V, ATT = 0.2188



12V FMC WILL POWER +5V0 AND -2V5 RAILS, SWITCHER STARTUP DELAYS -2V5  
PGM\_CM WILL ENABLE 5V0 LDO IC PSU\_EN WILL ENABLE -2V5 LDO IC  
3V3 FMC WILL PROVIDE POWER FOR OPTIONAL AD4080 2V0 LDO SUPPLY  
5V0 WILL PROVIDE SUPPLY FOR AD4080 3V3 LDO (DISABLED)  
3V3 FMC SUPPLY WILL PROVIDE SUPPLY FOR ALL 1V1 LDO ICS  
LDO ICS CONTROL SIGNALS ALL HAVE PULL UPS:

EN\_VDDLDO HAS PU AND JUMPER OPTION TO DISABLE  
EN\_1V1 HAS PU (NO OTHER INPUT CONNECTION)  
EN\_VIO HAS PU (NO OTHER INPUT CONNECTION)

AD4080 VIO, AVDD11, DVDD1V1 WILL POWER UP  
AD4080 AVDD11, DVDD1V1 VOLTAGES WILL BE SENSED, VIO WILL BE SENSED  
IF PG\_2CM IS NOT PULLED LO AT FMC AND BOTH THESE VOLTAGES PRESENT  
THE AD4080'S 3V3 SUPPLY WILL BE ENABLED WITH THE EN\_V33 SIGNAL  
PD\_V33B ALLOWS THIS EN\_V33 TO BE OVERRIDDEN VIA THE FMC (PU ENSURES DEFAULT TO NOT OVERRIDE)  
ONCE THE AD4080'S 3V3 HAS BEEN ESTABLISHED, AFE\_EN WILL ENABLE THE REF IC, OPTION REF BUF,  
AND ALL 3 STAGES OF THE ANALOG INPUT AMPS (THESE CAN BE OVERRIDDEN VIA PIANO SW)

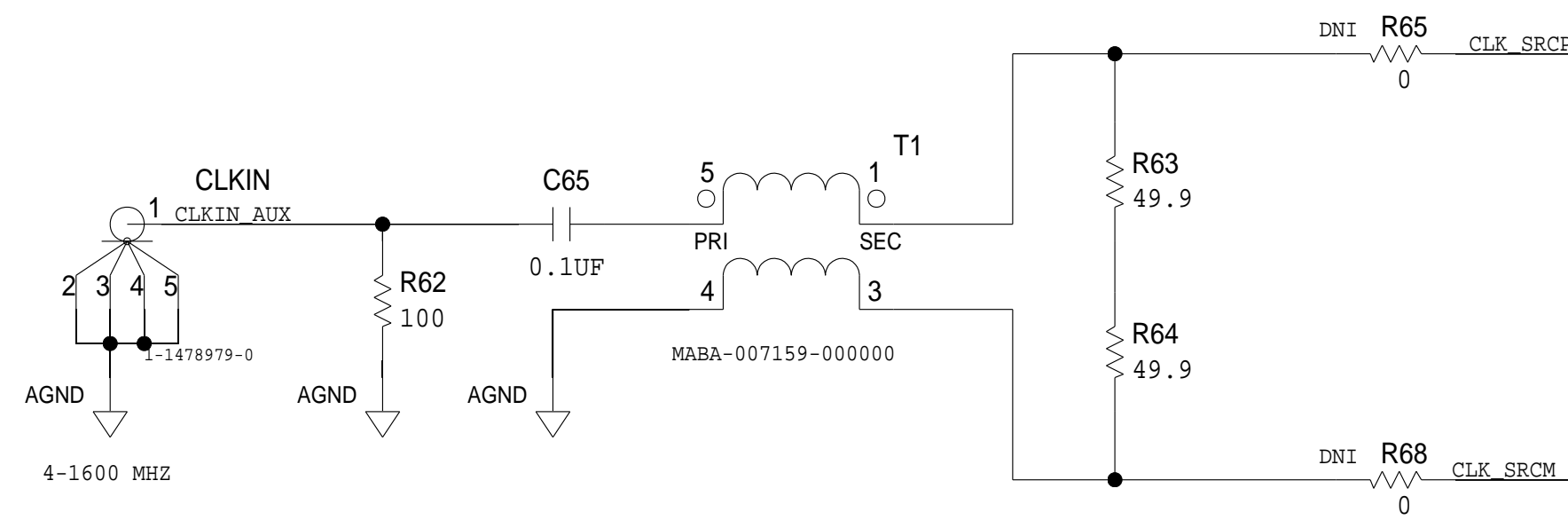


ANALOG DEVICES	SCHEMATIC			
	REV	DESCRIPTION	DATE	APPROVED
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.	HW TYPE : Customer Evaluation FMCZ AD4083			
	DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_069798-02	
	PTD ENGINEER D. SLOAN		SIZE D	SCALE 1:1
			SHEET 7	OF 10

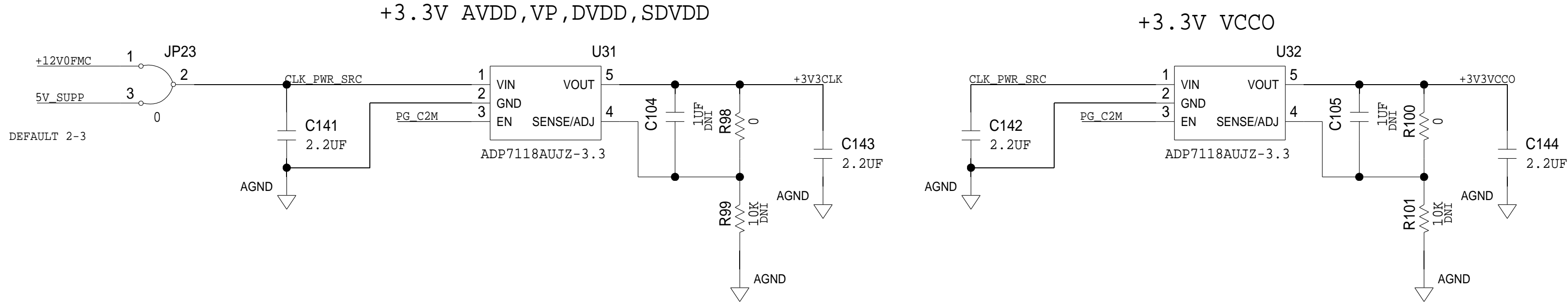
PRECISION CLOCK GENERATION/DISTRIBUTION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

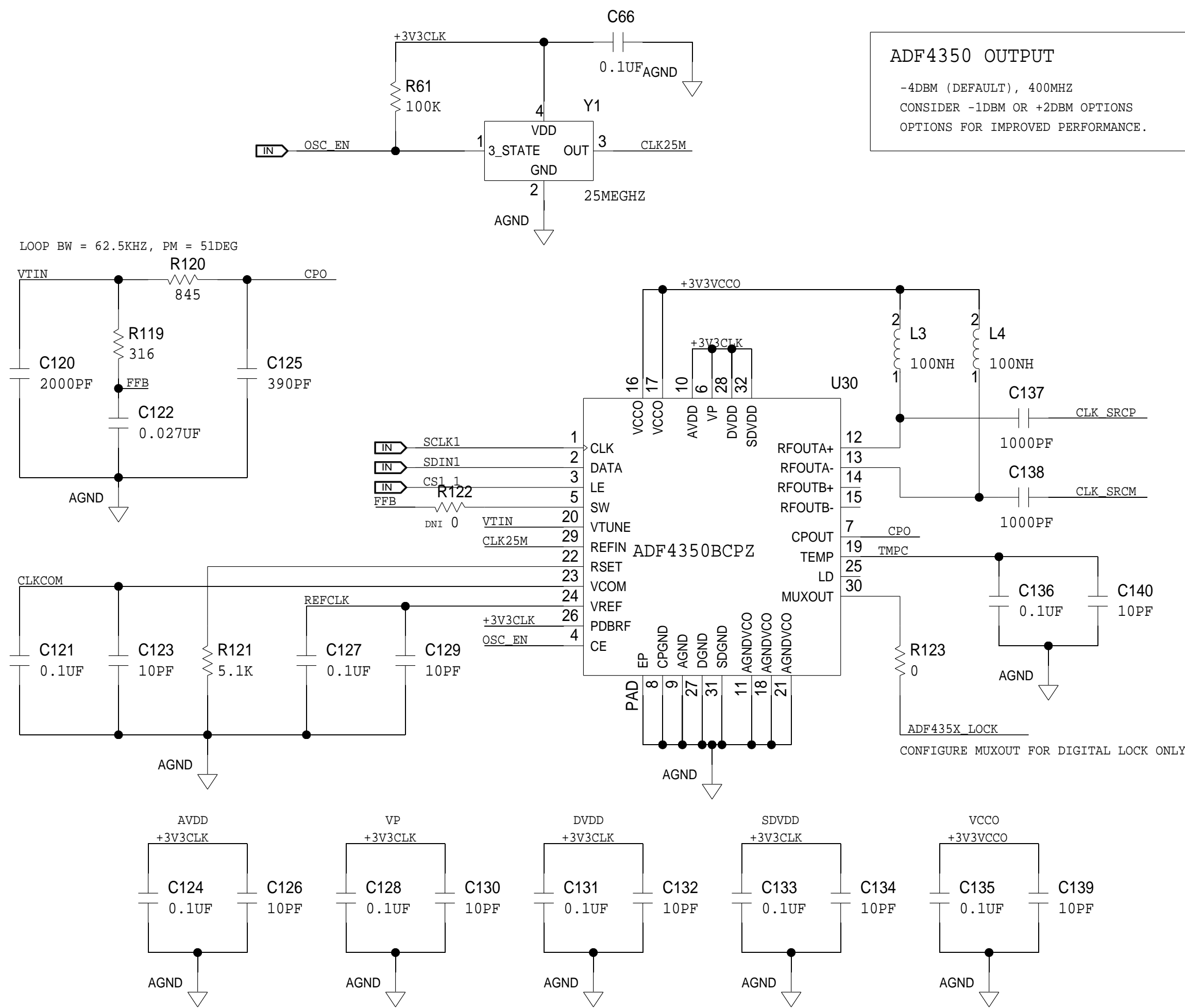
EXTERNAL CLOCK SOURCE



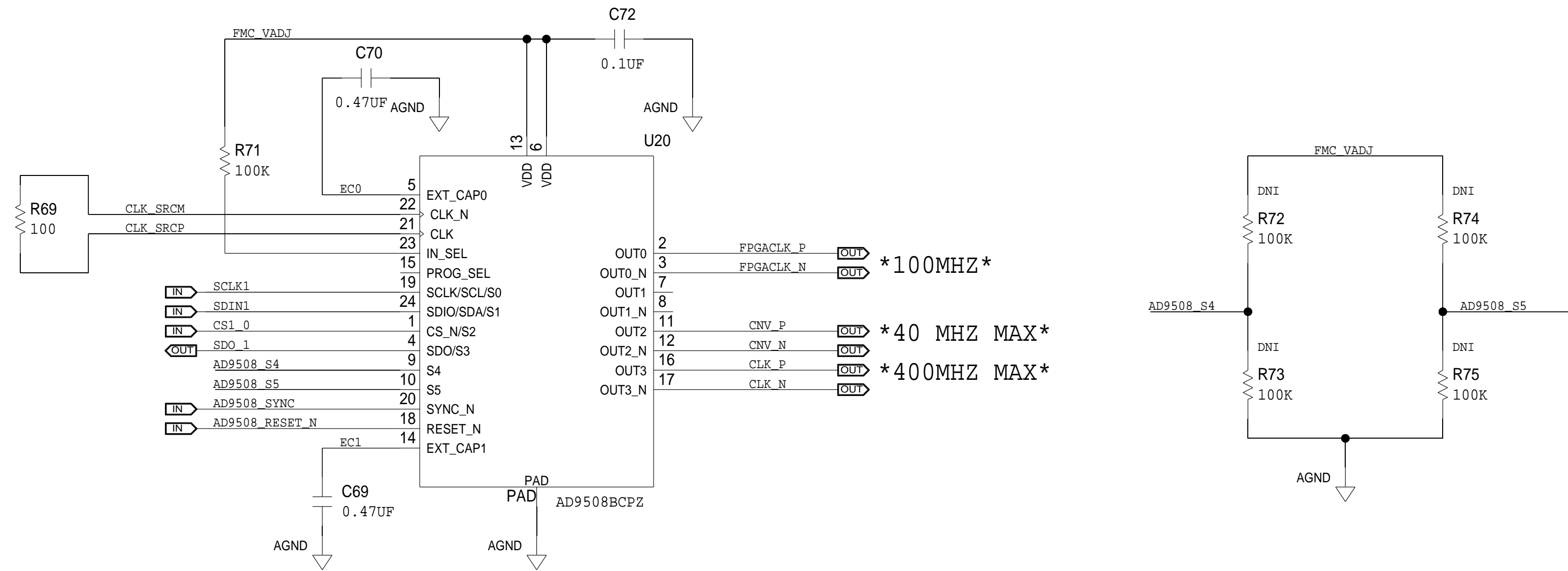
SYNTHESIZER SUPPLY



REFERENCE OSCILLATOR & PLL/SYNTHESIZER



CLOCK DISTRIBUTION



- 1) PROG\_SEL INTENTIONAL NC. ENABLES SPI CONFIG MODE.
- 2) IN\_SEL TIED TO SUPPLY. ENABLES DIFFERENTIAL INPUT CLOCK MODE
- 3) S4,S5 PHYSICALLY LEFT FLOATING. DISCUSS PROPER LOGIC STATE.
- 4) AD9508\_RESET\_N IS DERIVED FROM PSU SEQ OUTPUT (PORB).
- 5) LVDS TERMINATION PLACEMENT AT LOAD



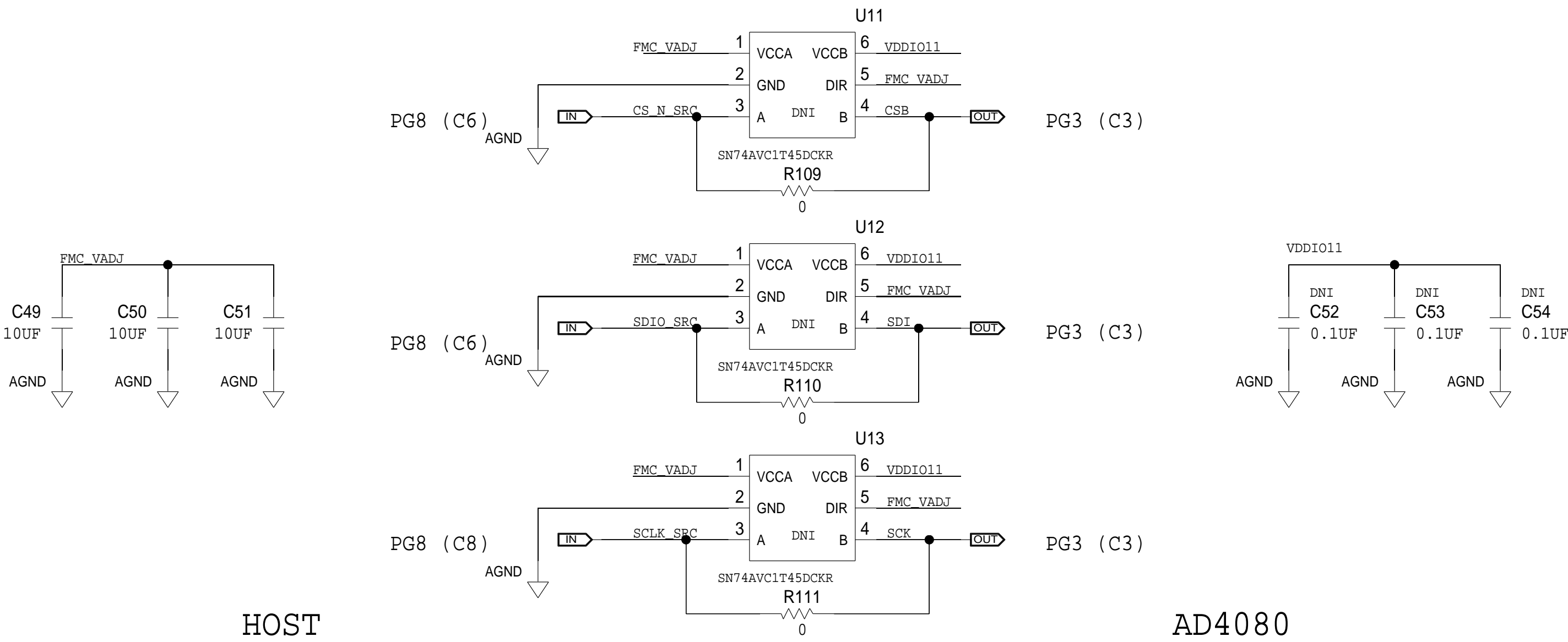
SCHEMATIC

HW TYPE : Customer Evaluation FMCZ AD4083		DRAWING NO. 02_069798-02		REV F
DESIGN VIEW <DESIGN_VIEW>		SIZE D	SCALE 1:1	SHEET 8 OF 10

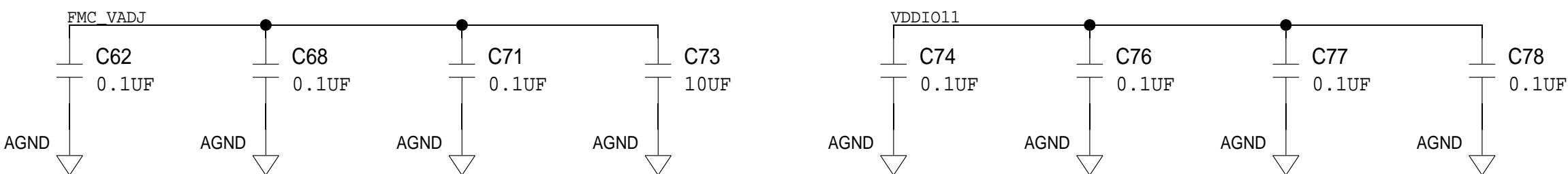
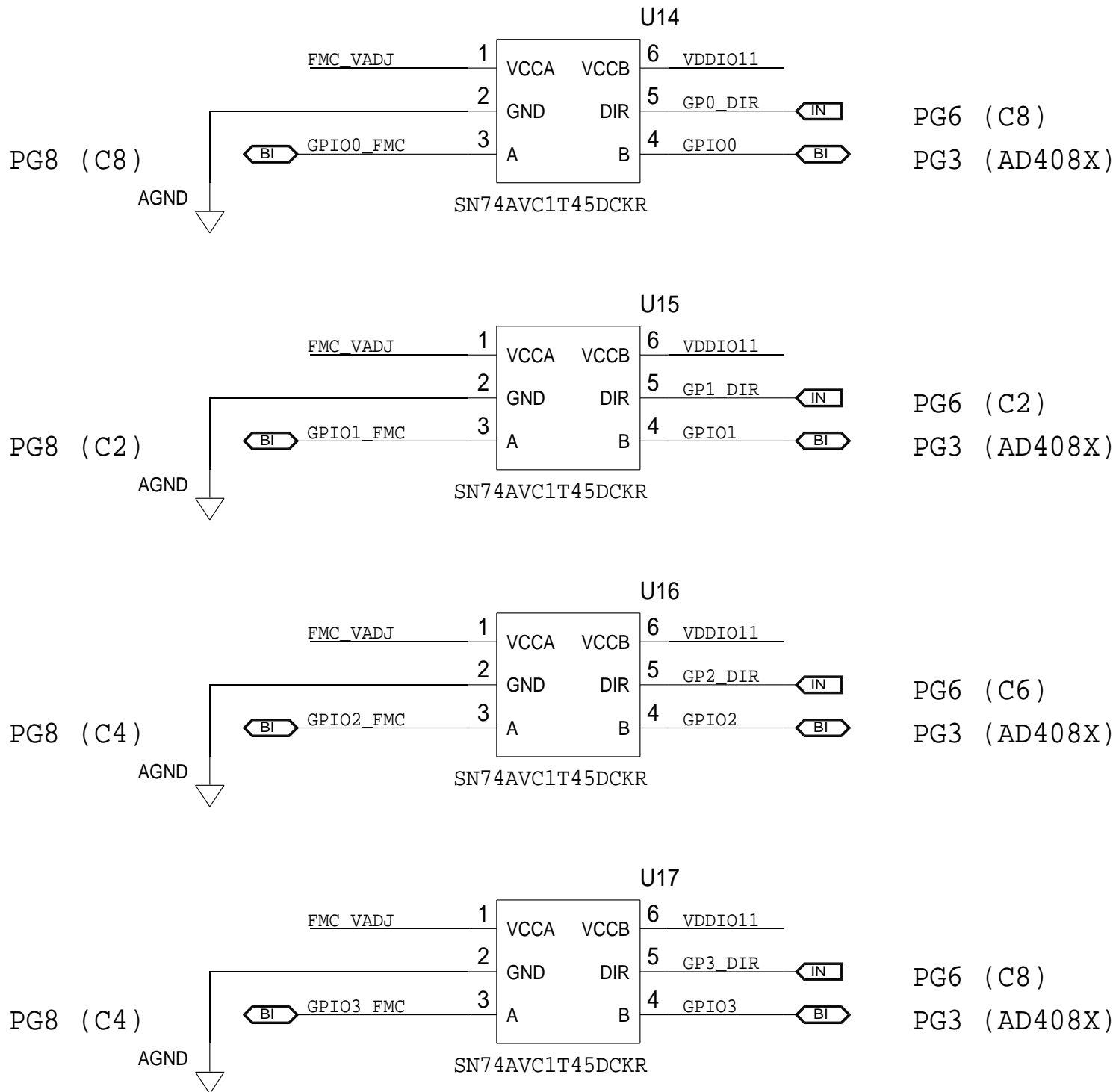


LEVEL TRANSLATION

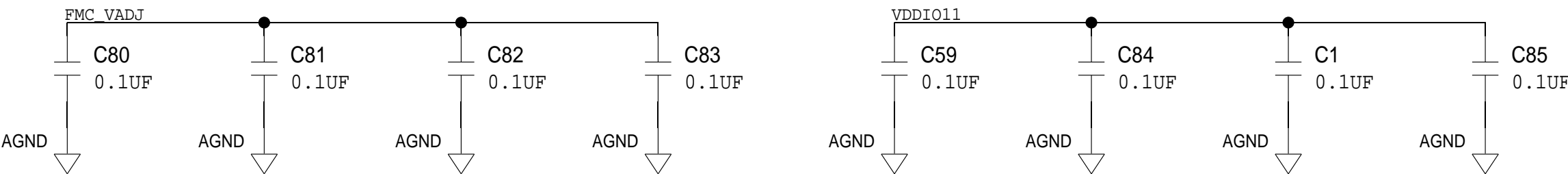
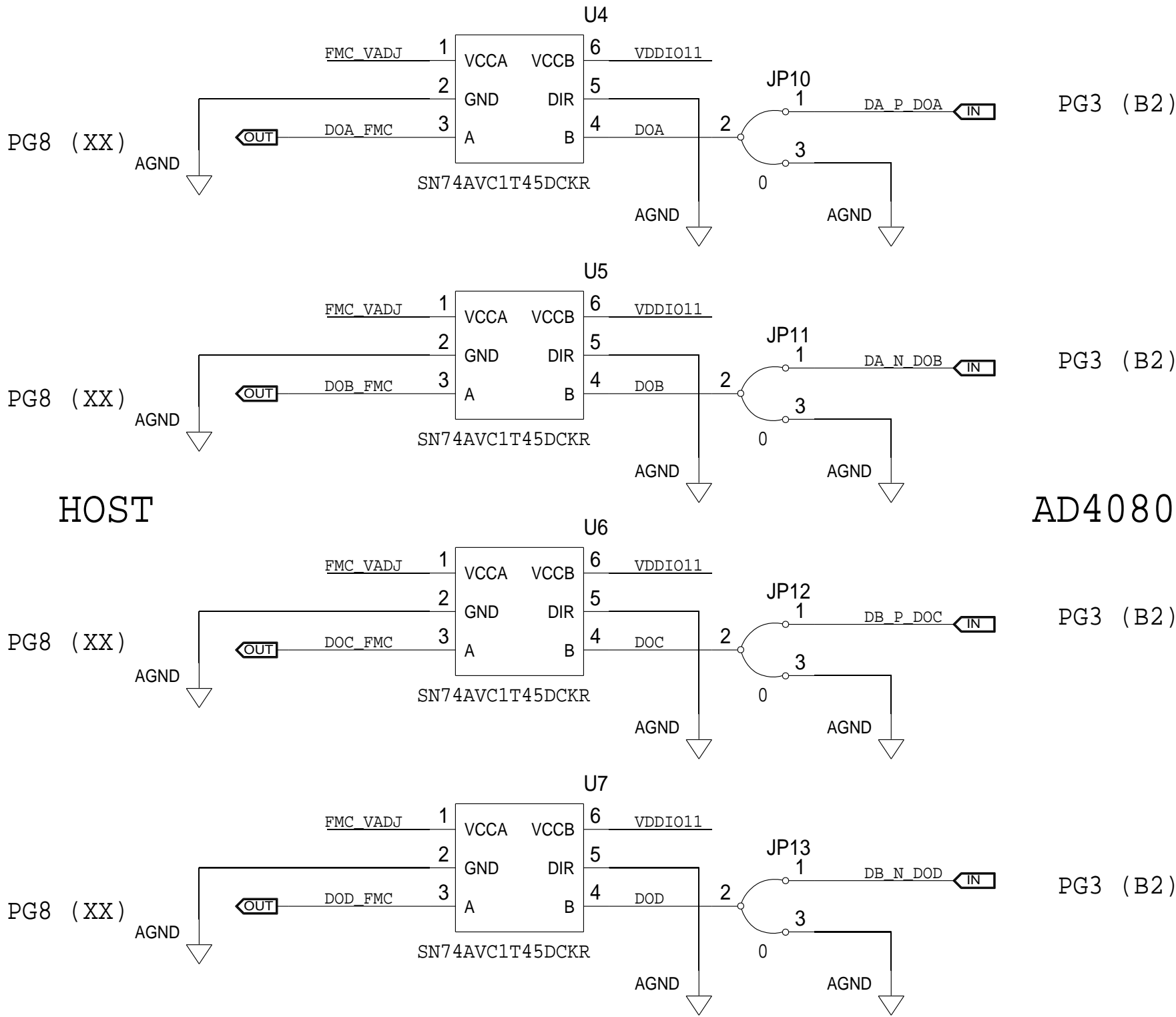
CONFIGURATION SPI LEVEL TRANSLATORS  
(CONSIDER FOR DELETION, NOT INSTALLED BY DEFAULT)



GPIO LEVEL TRANSLATORS



DATA SPI LEVEL TRANSLATORS

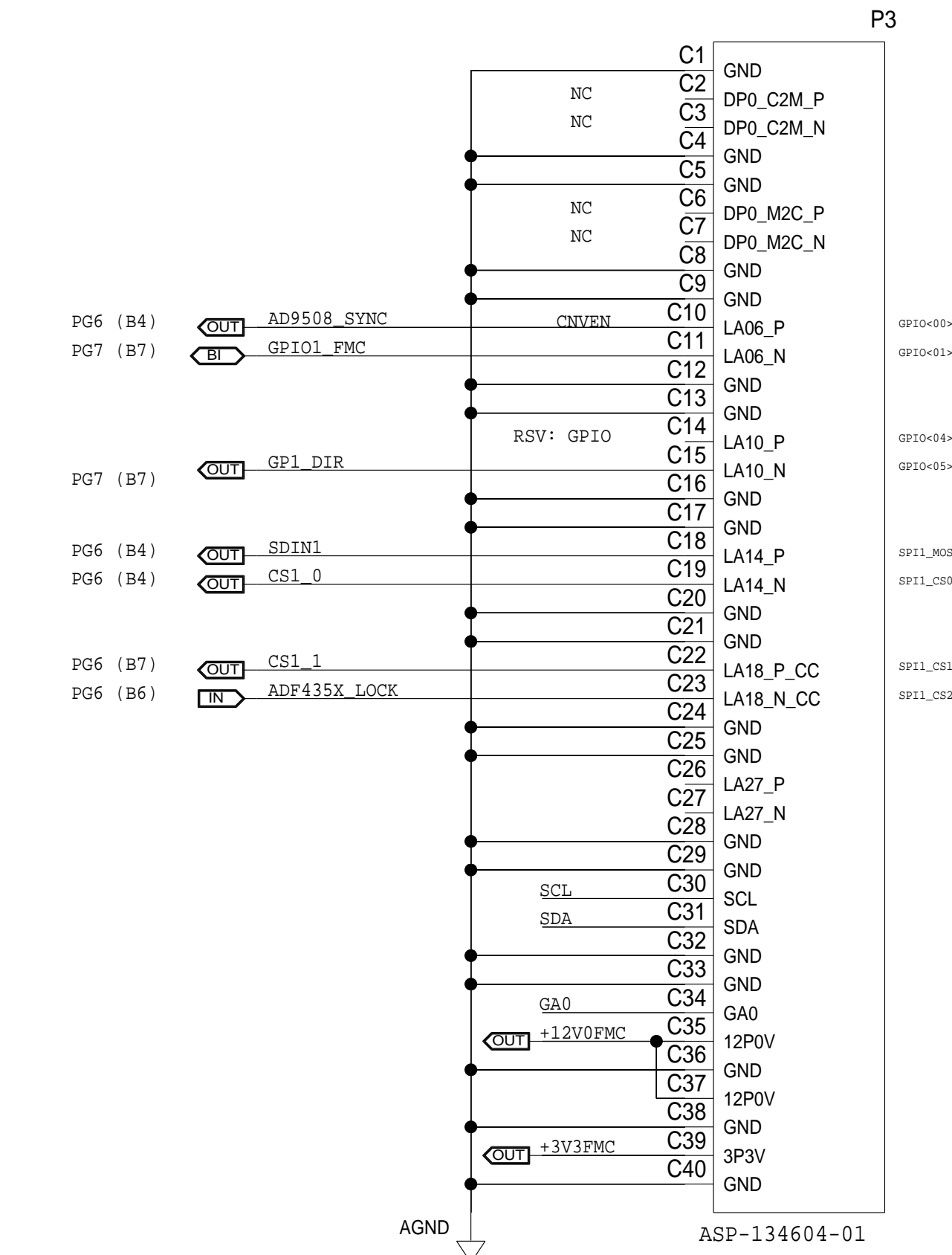
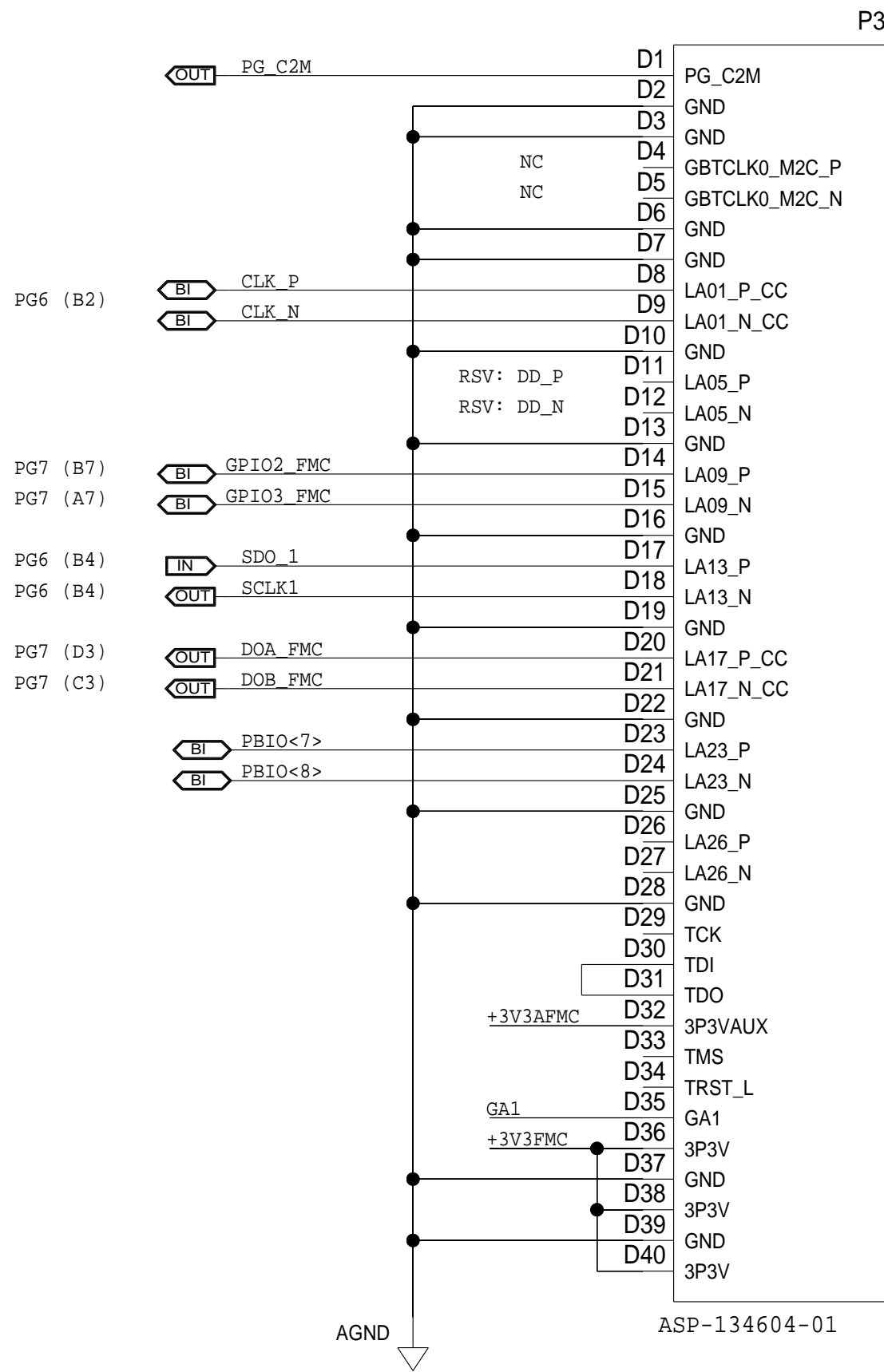
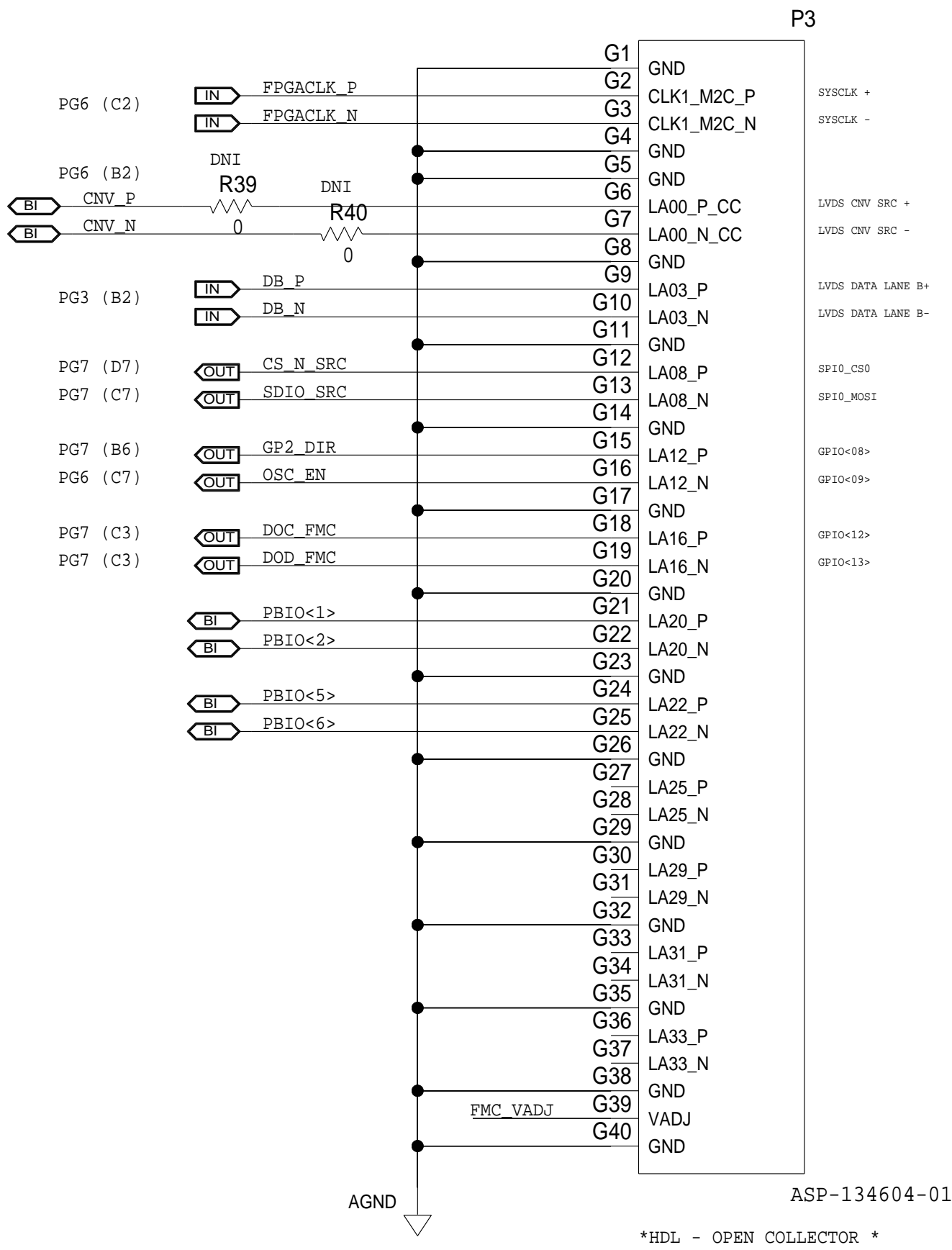
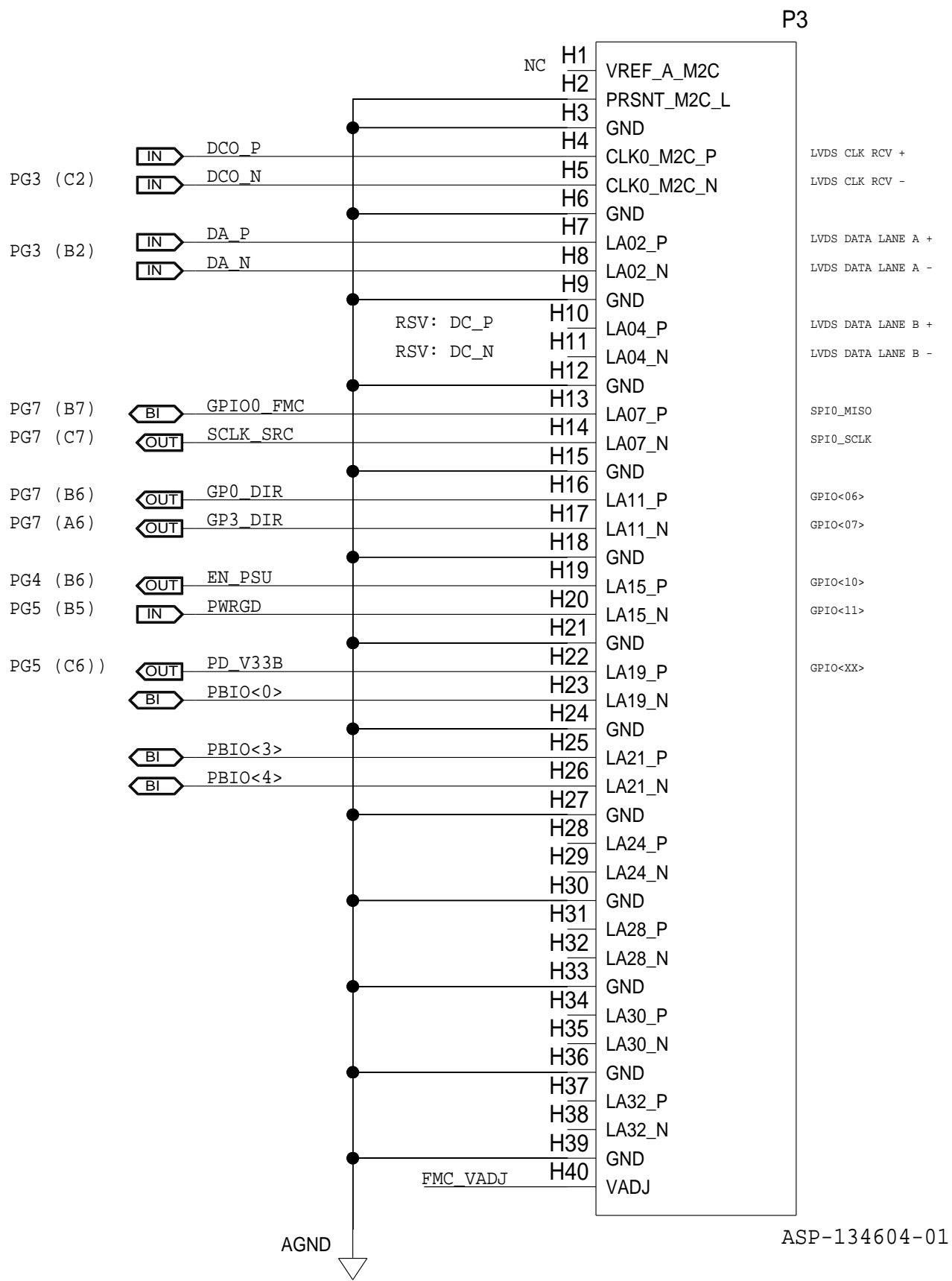


THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.  
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR  
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,  
OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS  
OF ANALOG DEVICES.  
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS  
OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.

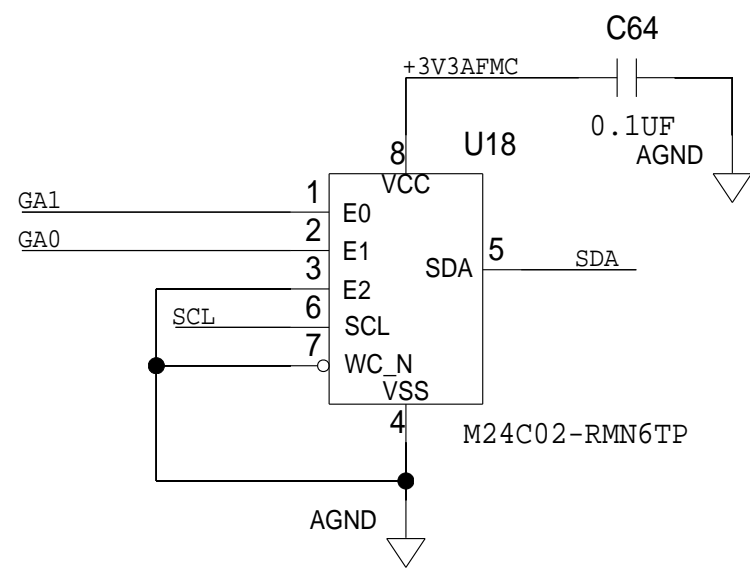
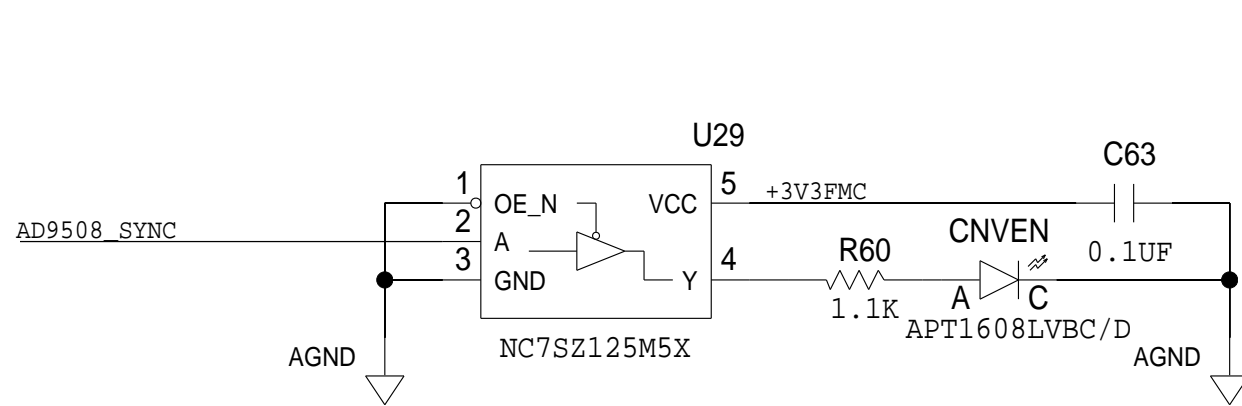
SCHEMATIC				
HW TYPE : Customer Evaluation FMCZ AD4083				
: AD4081, AD4082, AD4083, AD4084, AD4085				
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_069798-02		REV F	
PTD ENGINEER D. SLOAN	SIZE D	SCALE 1:1	SHEET 9 OF 10	

HOST (FMC) INTERFACE

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



BOARD ID EEPROM



SCHEMATIC			
HW TYPE : Customer Evaluation FMCZ AD4083			
: AD4081, AD4082, AD4083, AD4084, AD4085			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_069798-02	REV F	
PTD ENGINEER D. SLOAN	SIZE D	SCALE 1:1	SHEET 10 OF 10