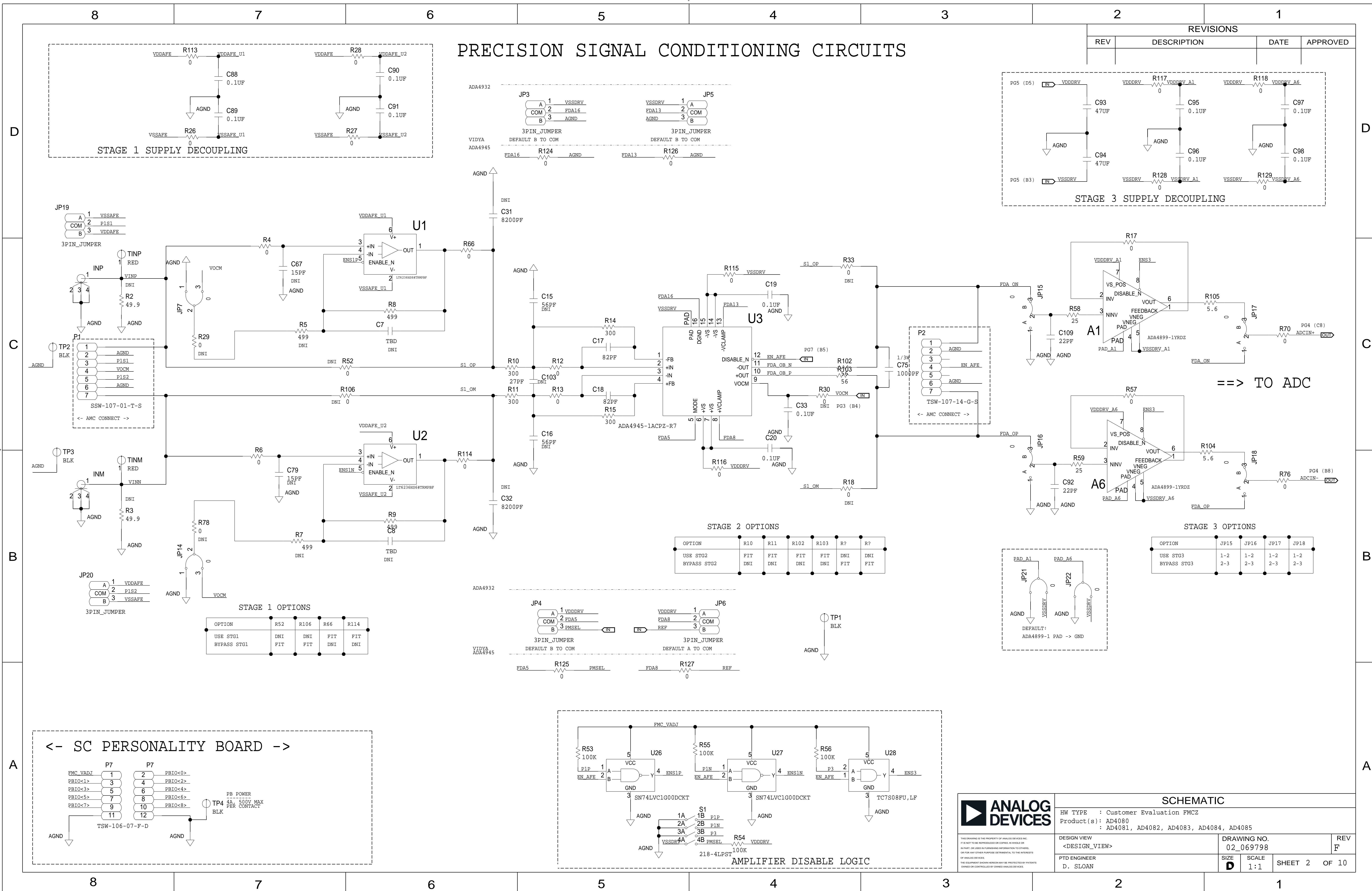
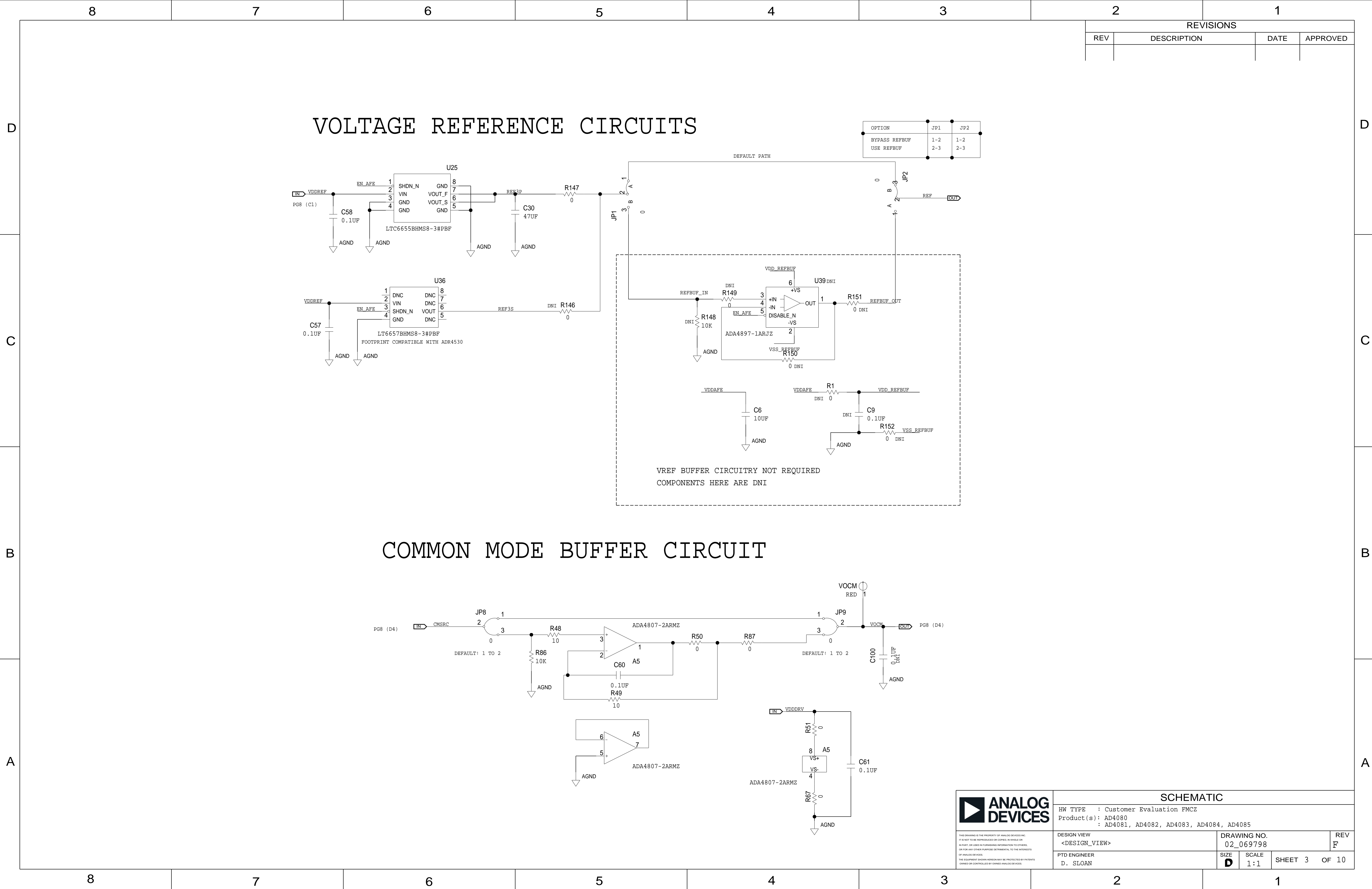


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D	THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.					JUMPER TABLE			REVISIONS																																																																																																																																																										
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P.O SPEC.		BK/BD SPEC.		SOCKET OEM		OEM PART#		HANDLER																																																																																																																																																											
8		7		6		5		4		3		2		1																																																																																																																																																					





COMMON MODE BUFFER CIRCUIT

JP8

1

2

3

0

PG8 (D4)

CMSRC

R48

10

R86

10K

AGND

ADA4807-2ARMZ

A5

1

2

3

4

5

6

7

VS+

VS-

AGND

R50

0

R87

0

JP9

1

2

3

0

VOCM

RED

1

2

3

0

C100

0.1UF

DNI

AGND

PG8 (D4)

ADA4807-2ARMZ

A5

1

2

3

4

5

6

7

VS+

VS-

AGND

VDDDRV

R51

0

8

4

VS+

VS-

AGND

R57

0

C61

0.1UF

ANALOG

DEVICES

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SCHEMATIC

HW TYPE : Customer Evaluation FMCZ

Product(s): AD4080 : AD4081, AD4082, AD4083, AD4084, AD4085

DESIGN VIEW <DESIGN_VIEW>

DRAWING NO. 02_069798

REV F

PTD ENGINEER D. SLOAN


SIZE D



SCALE 1:1

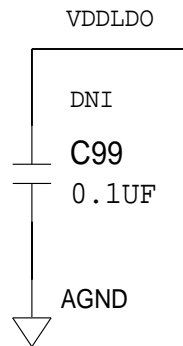
SHEET 3 OF 10

AD408X CKTS

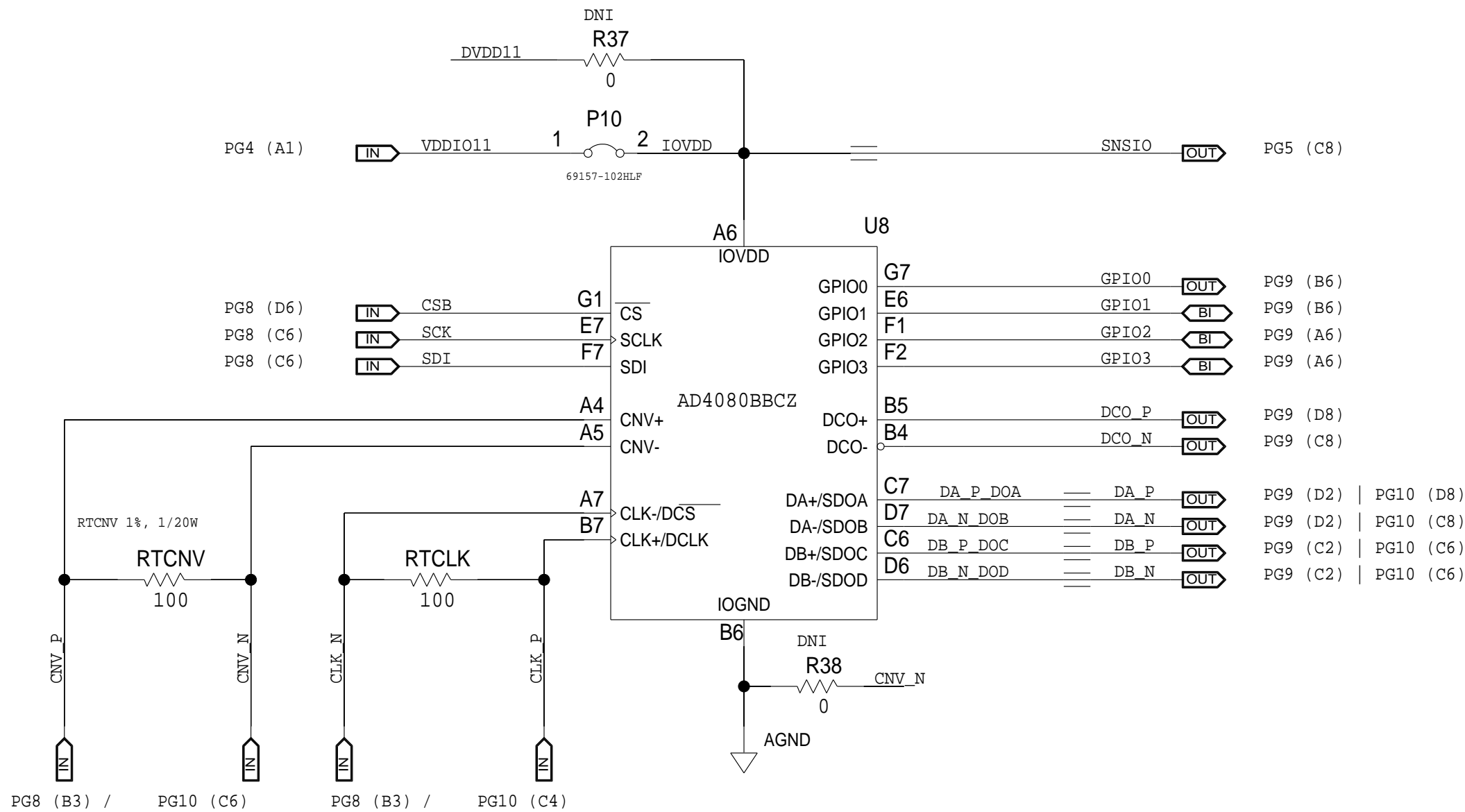
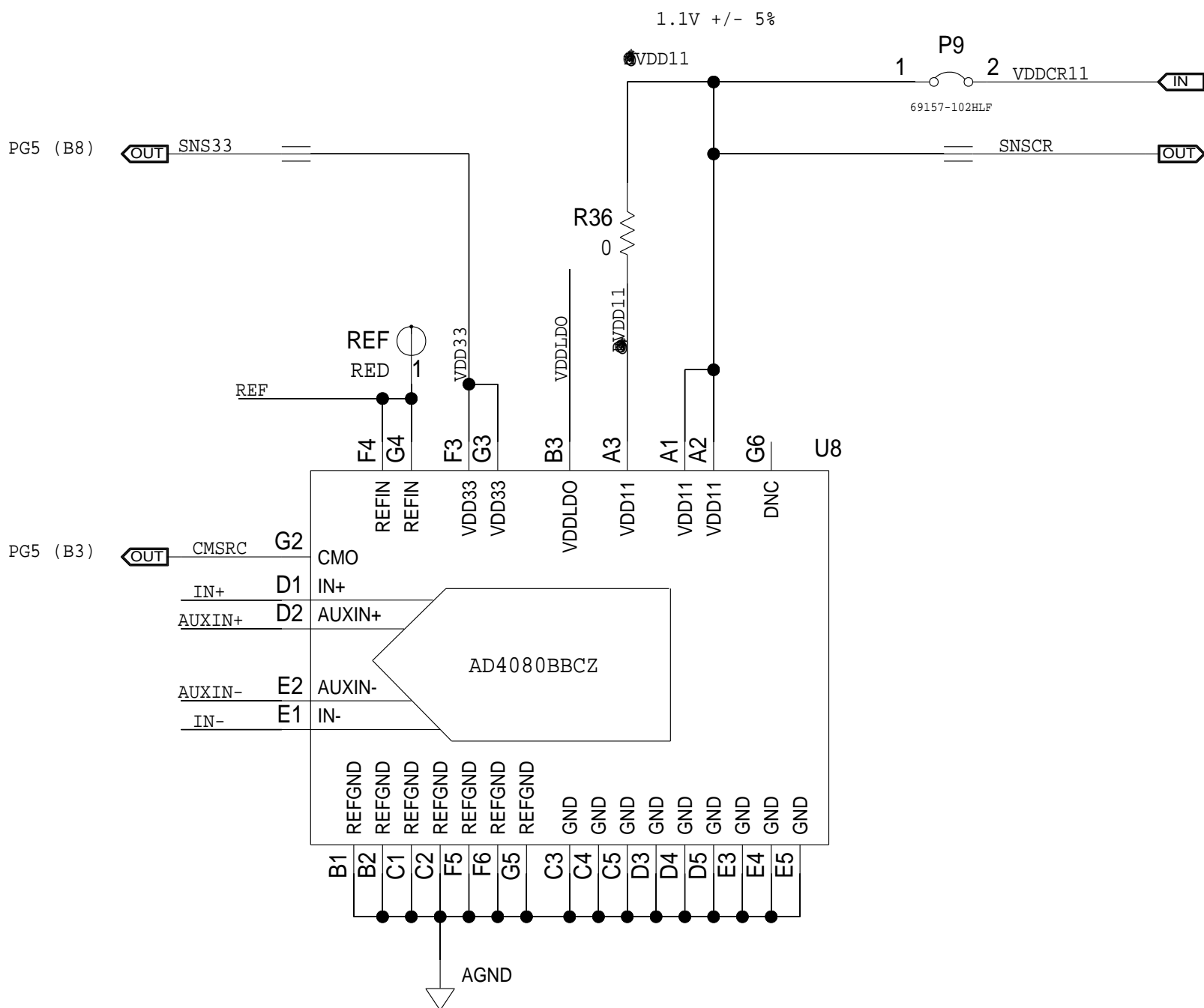
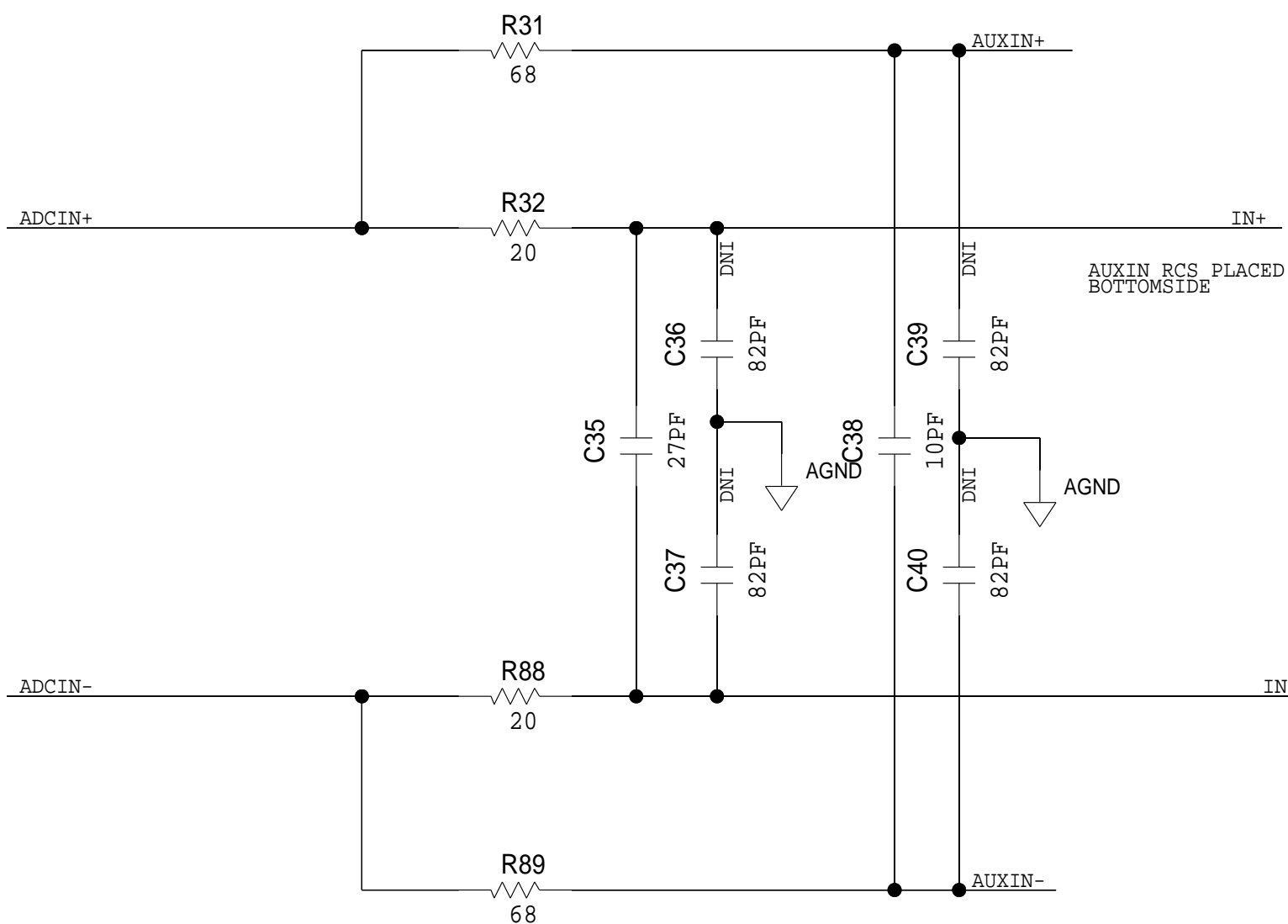
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

3.3V +/- 5%
PG6 (D2)  REVIEW: SHOULD TBD DECOUPLING BE ADDED CLOSE TO DUT FOR VDD33?

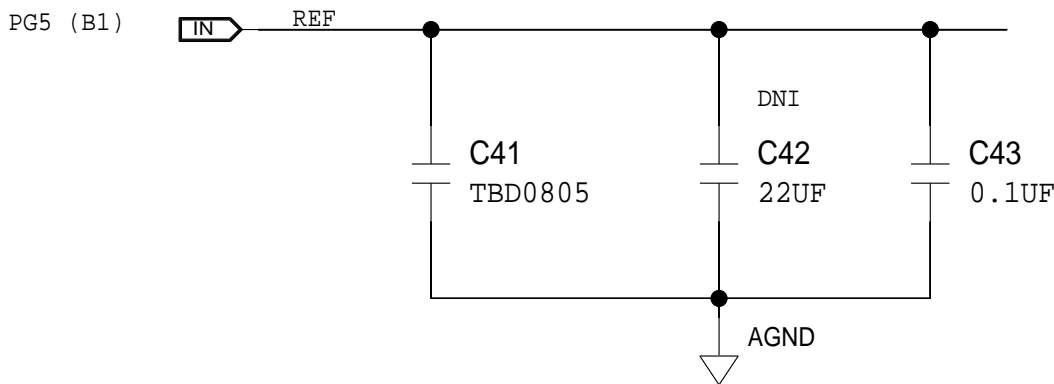
1.5V-2.75V
PG6 (C2)  



INPUT NETWORK



REFERENCE FILTER



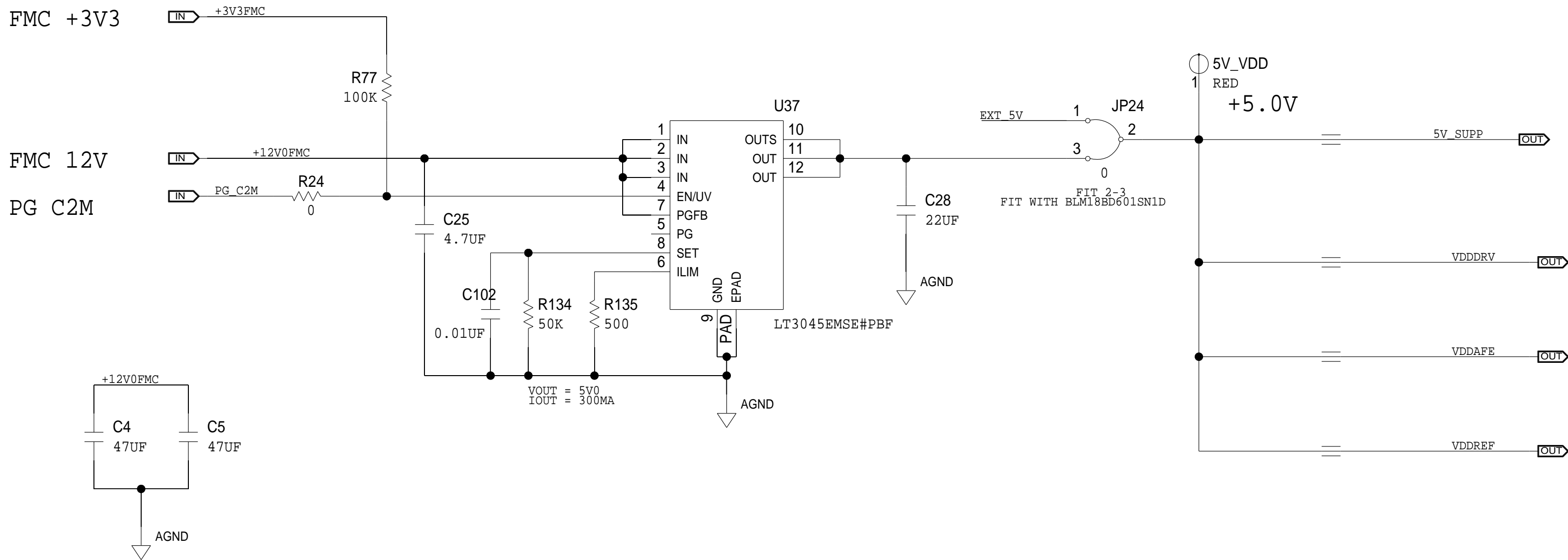
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SCHEMATIC			
HW TYPE : Customer Evaluation FMCZ Product(s): AD4080 : AD4081, AD4082, AD4083, AD4084, AD4085			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_069798	REV F	
PTD ENGINEER D. SLOAN	SIZE D	SCALE 1:1	SHEET 4 OF 10

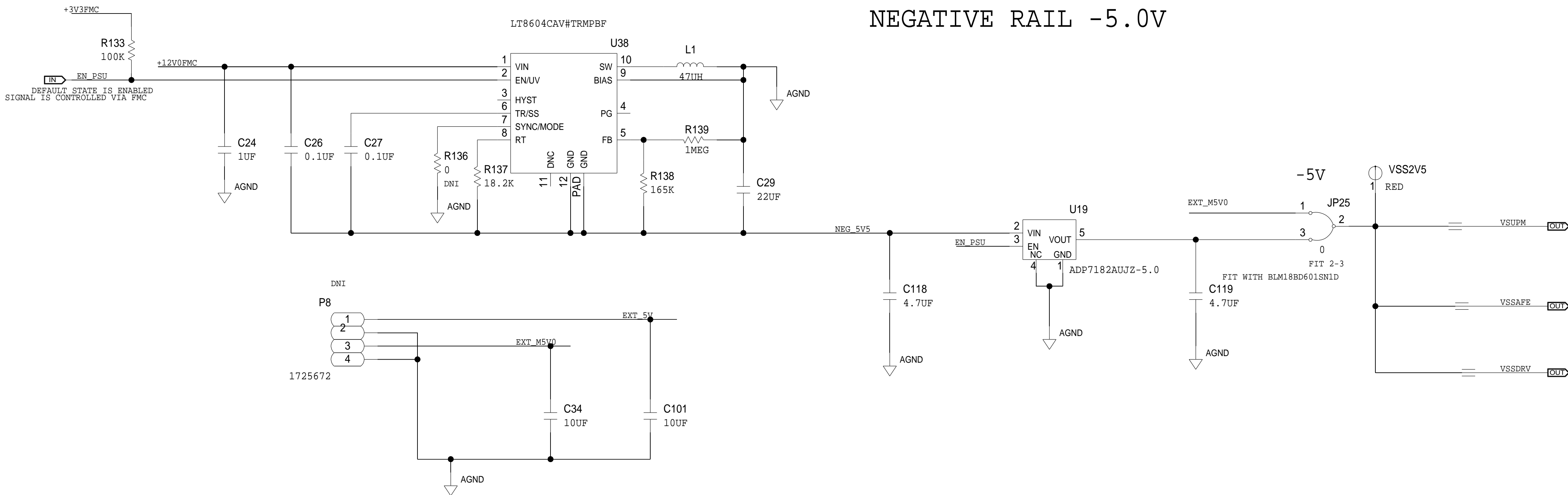
REFERENCE & AMPLIFIER SUPPLY GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POSITIVE RAIL +5.0V



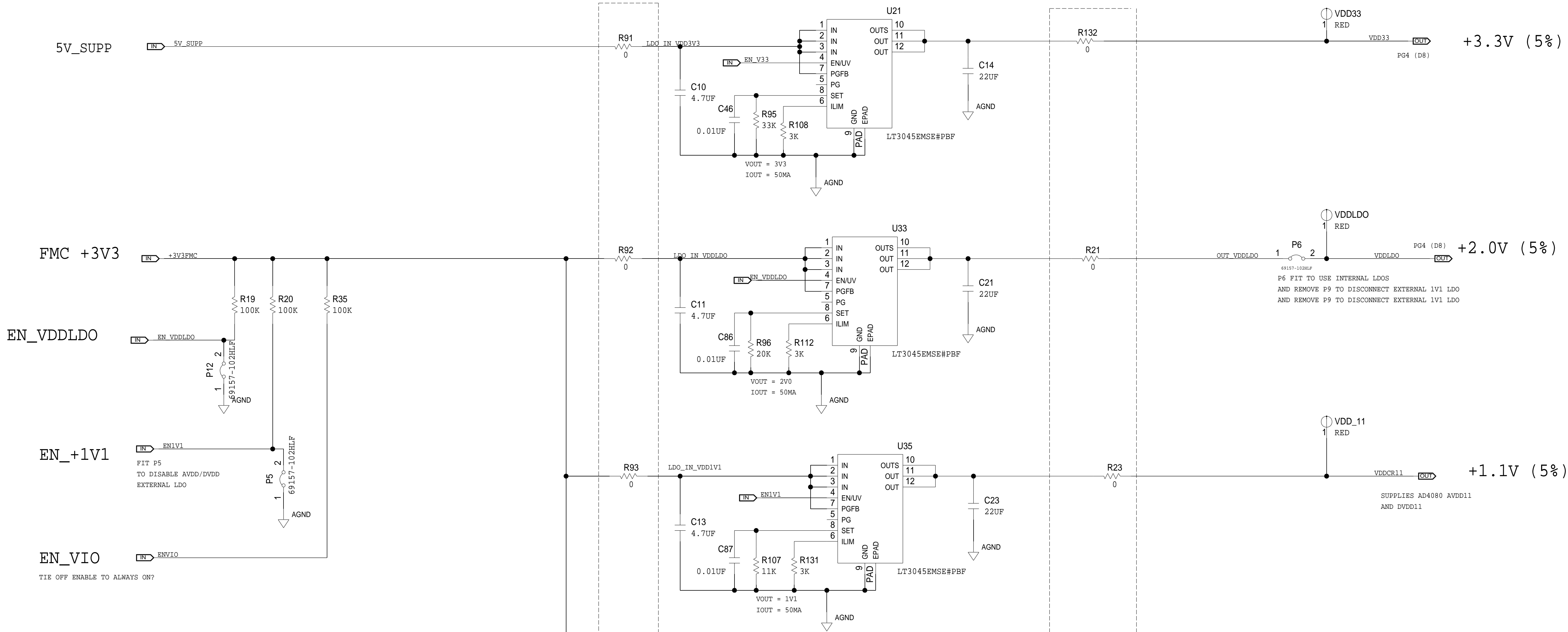
NEGATIVE RAIL -5.0V



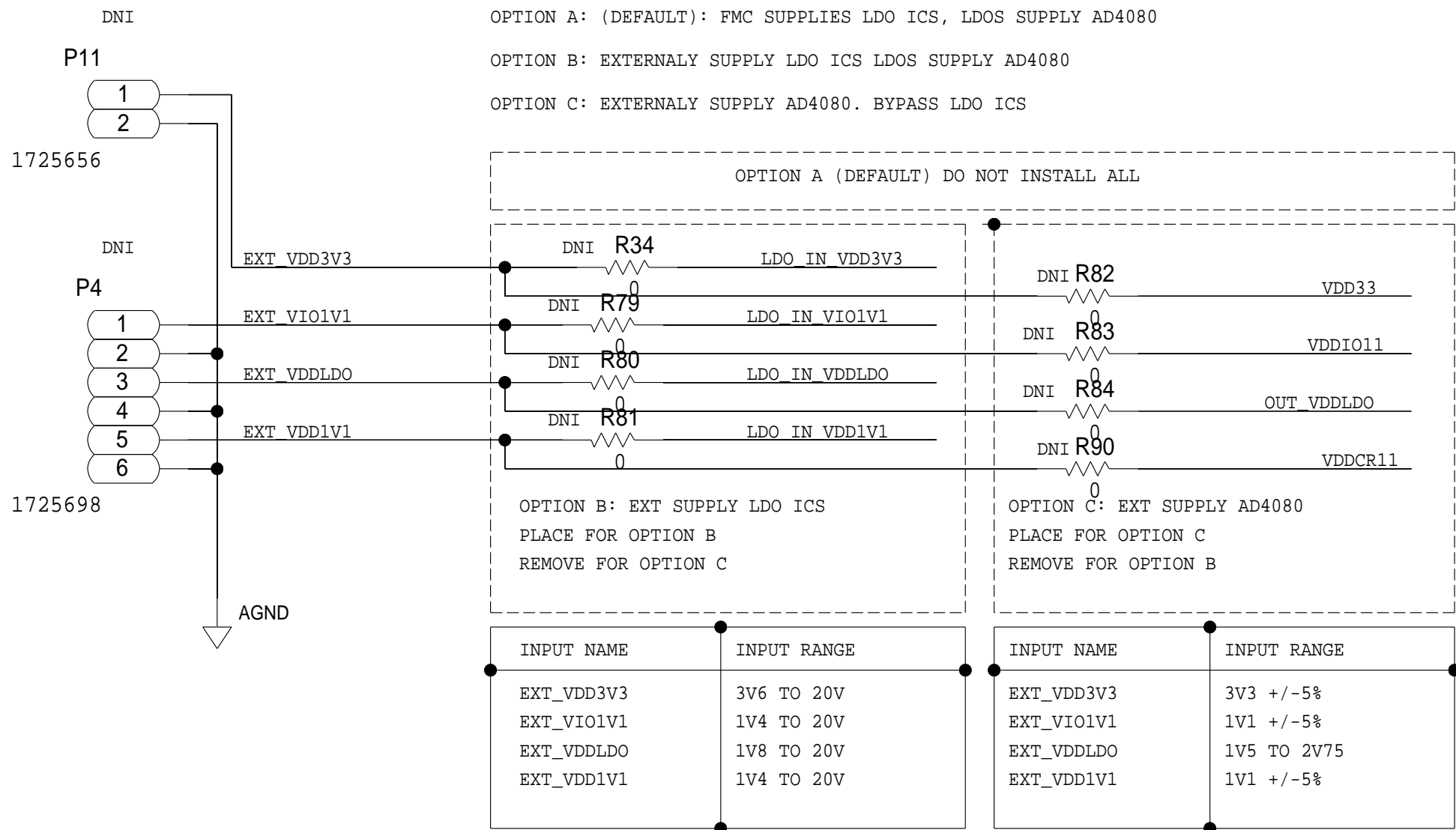
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HW TYPE : Customer Evaluation FMCZ			
Product(s): AD4080			
: AD4081, AD4082, AD4083, AD4084, AD4085			
DESIGN VIEW	DRAWING NO.		REV
<DESIGN_VIEW>	02_069798		F
PTD ENGINEER	SIZE	SCALE	SHEET 5 OF 10
D. SLOAN	D	1:1	

AD4080 DEVICE POWER SUPPLY

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



EXTERNAL SUPPLY OPTIONS

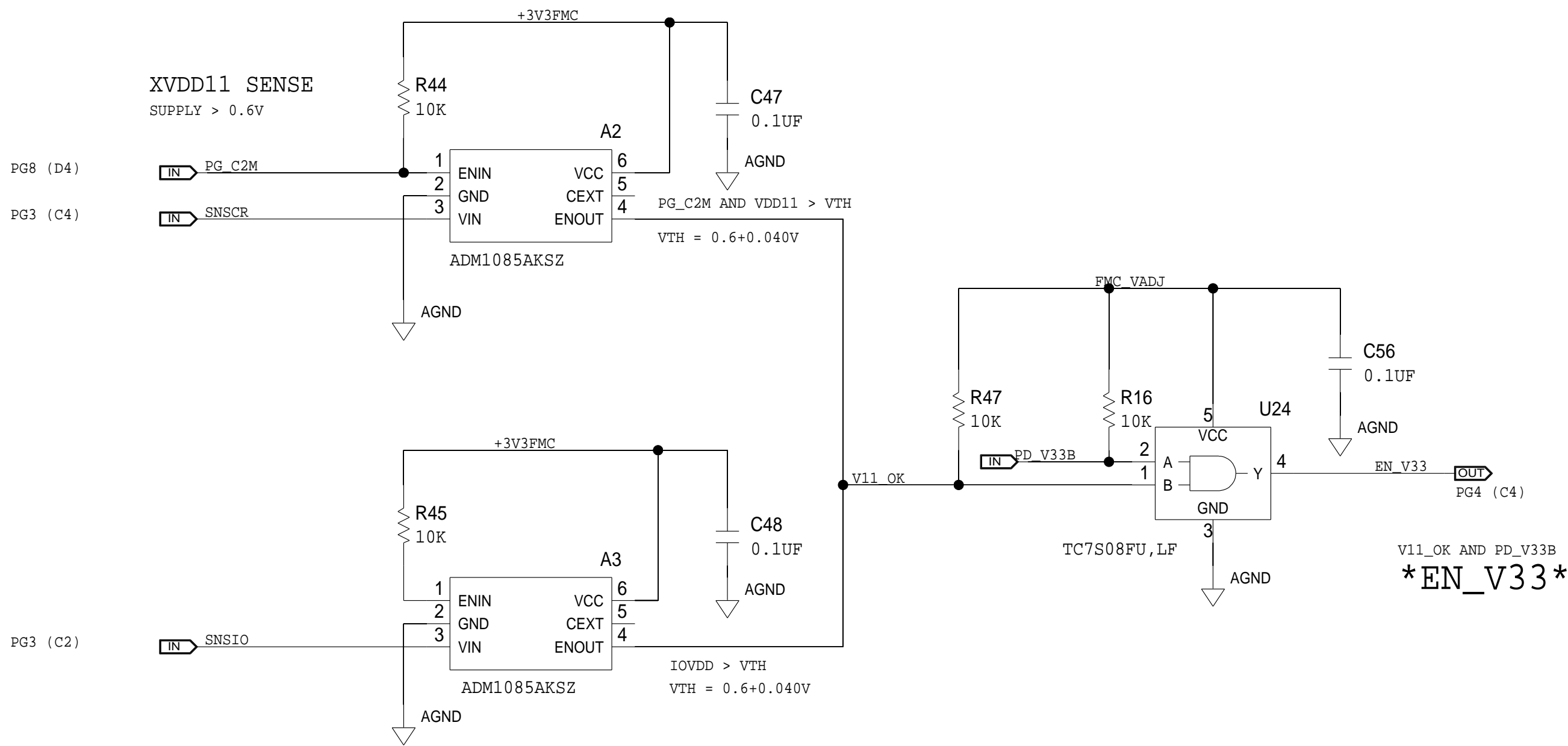


SCHEMATIC

HW TYPE : Customer Evaluation FMCZ
Product(s): AD4080
: AD4081, AD4082, AD4083, AD4084, AD4085

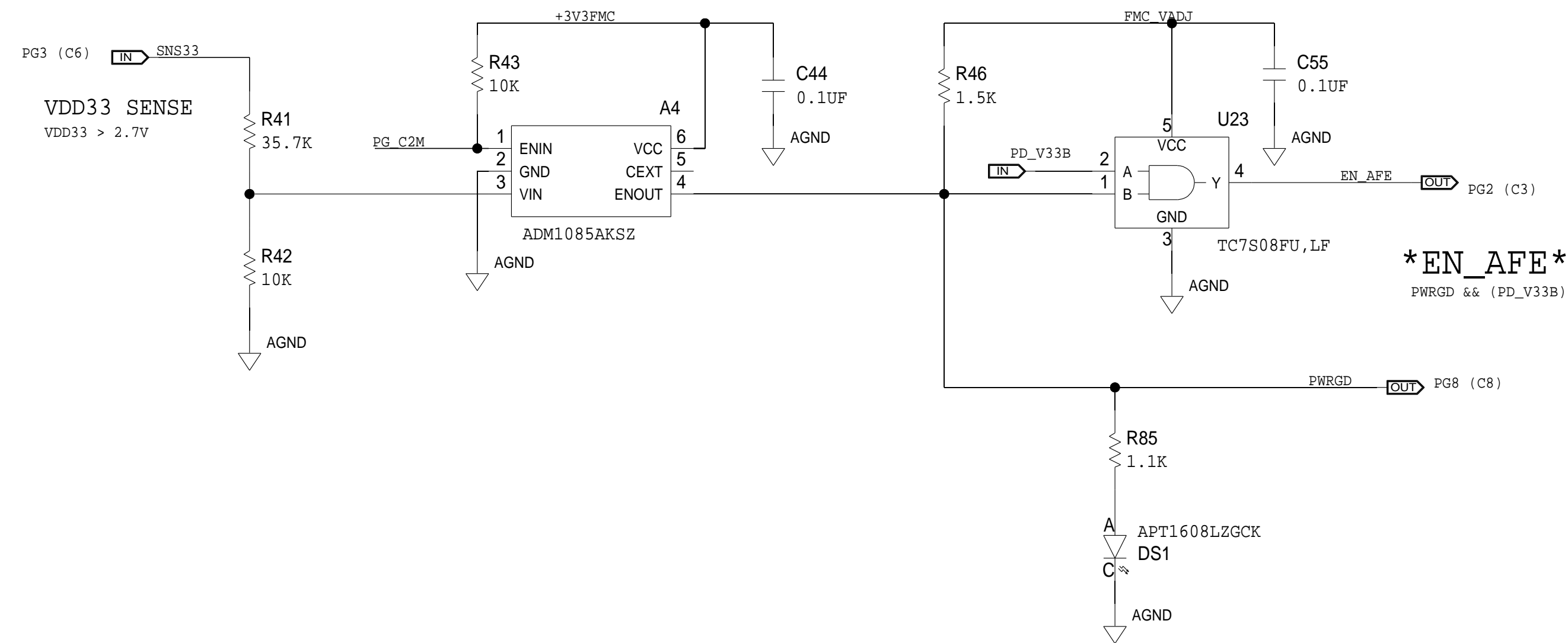
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PTD ENGINEER D. SLOAN	SIZE D	SCALE 1:1
SHEET 6		OF 10

SUPPLY SEQUENCE CIRCUITS



ADM1085 SELECTED FOR OPEN DRAIN OUTPUT

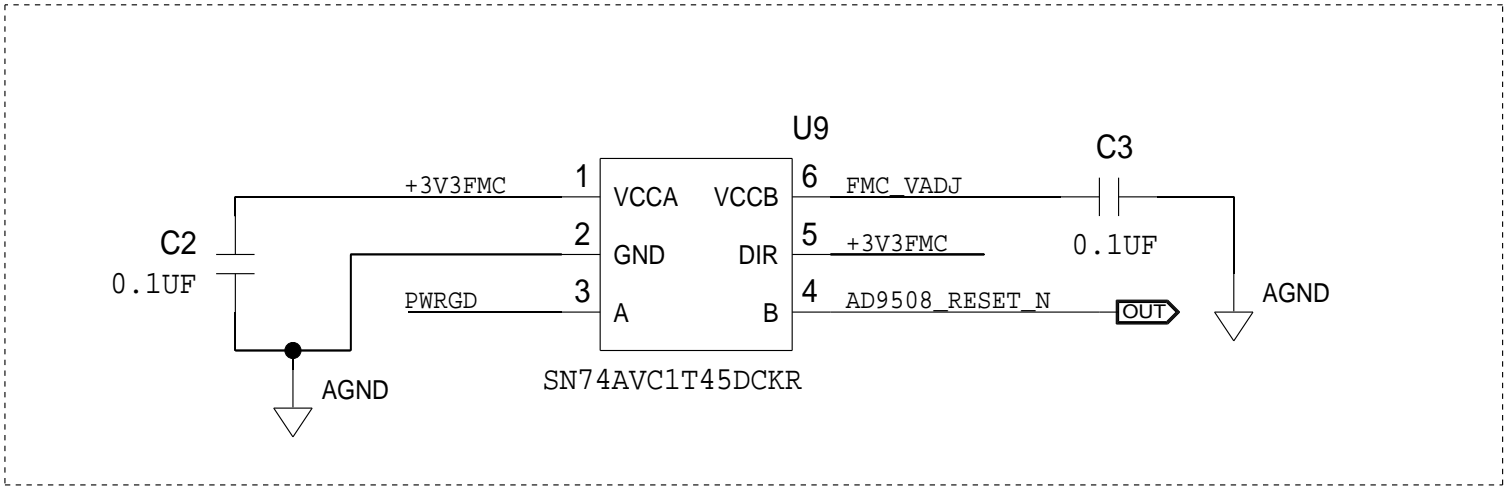
PWRGD
PG_C2M && (VDD33 > VTH1/ATT) ~2.74V
VTH = 0.6+0.040V, ATT = 0.2188



12V FMC WILL POWER +5V0 AND -2V5 RAILS, SWITCHER STARTUP DELAYS -2V5
PGM_CM WILL ENABLE 5V0 LDO IC PSU_EN WILL ENABLE -2V5 LDO IC
3V3 FMC WILL PROVIDE POWER FOR OPTIONAL AD4080 2V0 LDO SUPPLY
5V0 WILL PROVIDE SUPPLY FOR AD4080 3V3 LDO (DISABLED)
3V3 FMC SUPPLY WILL PROVIDE SUPPLY FOR ALL 1V1 LDO ICS
LDO ICS CONTROL SIGNALS ALL HAVE PULL UPS:

EN_VDDLDO HAS PU AND JUMPER OPTION TO DISABLE
EN_1V1 HAS PU (NO OTHER INPUT CONNECTION)
EN_VIO HAS PU (NO OTHER INPUT CONNECTION)

AD4080 VIO, AVDD11, DVDD1V1 WILL POWER UP
AD4080 AVDD11, DVDD1V1 VOLTAGES WILL BE SENSED, VIO WILL BE SENSED
IF PG_2CM IS NOT PULLED LO AT FMC AND BOTH THESE VOLTAGES PRESENT
THE AD4080'S 3V3 SUPPLY WILL BE ENABLED WITH THE EN_V33 SIGNAL
PD_V33B ALLOWS THIS EN_V33 TO BE OVERRIDDEN VIA THE FMC (PU ENSURES DEFAULT TO NOT OVERRIDE)
ONCE THE AD4080'S 3V3 HAS BEEN ESTABLISHED, AFE_EN WILL ENABLE THE REF IC, OPTION REF BUF,
AND ALL 3 STAGES OF THE ANALOG INPUT AMPS (THESE CAN BE OVERRIDDEN VIA PIANO SW)

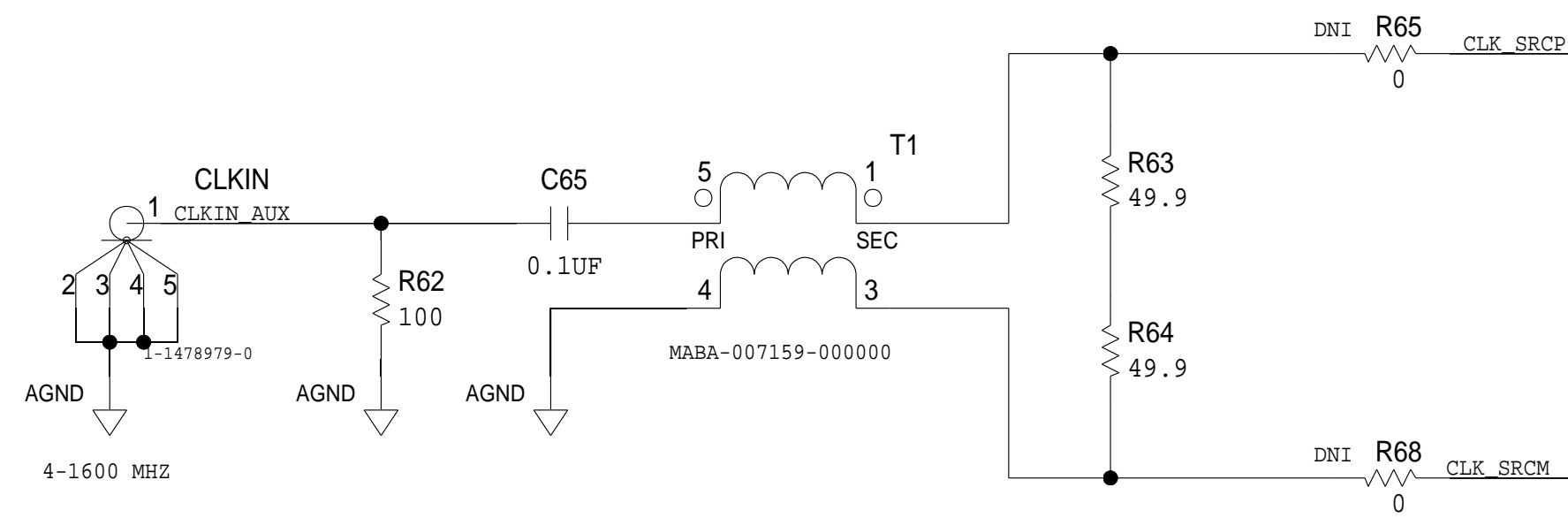


ANALOG DEVICES	SCHEMATIC			
	HW TYPE : Customer Evaluation FMCZ Product(s): AD4080 : AD4081, AD4082, AD4083, AD4084, AD4085	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_069798	REV F
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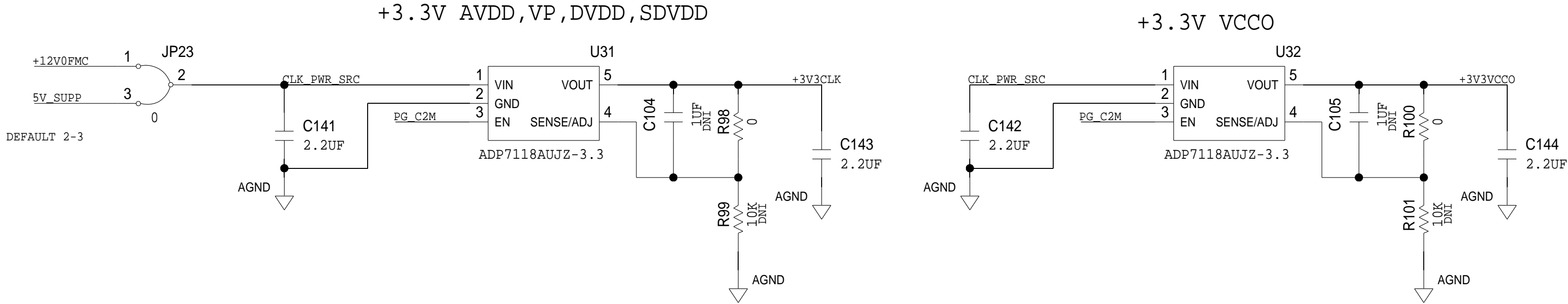
PRECISION CLOCK GENERATION/DISTRIBUTION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

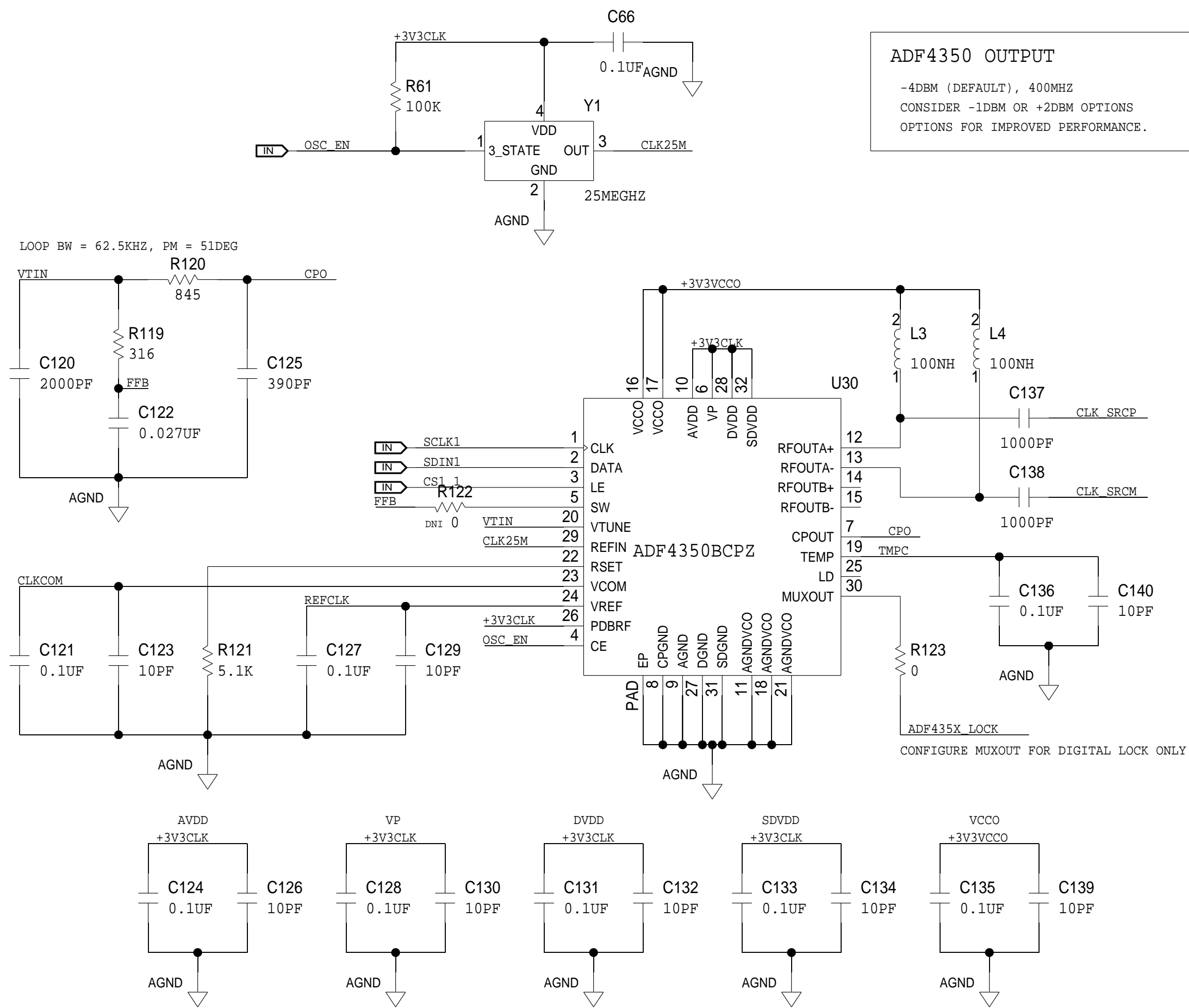
EXTERNAL CLOCK SOURCE



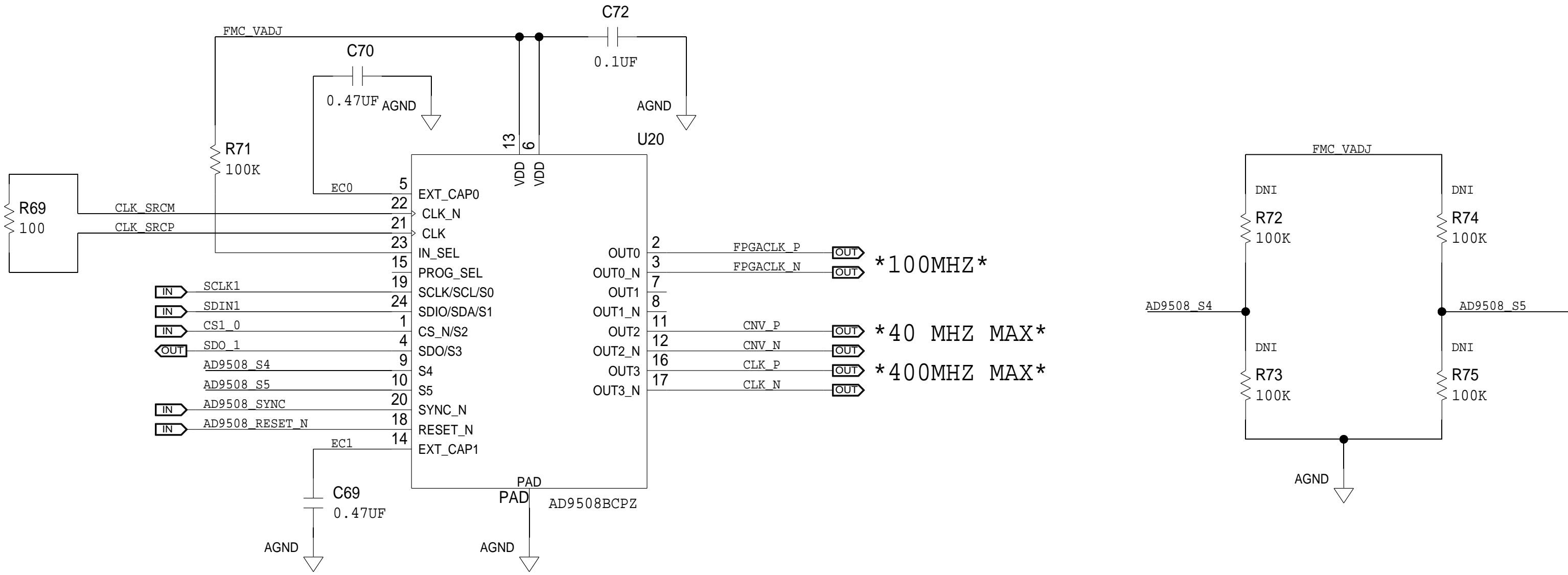
SYNTHESIZER SUPPLY



REFERENCE OSCILLATOR & PLL/SYNTHESIZER



CLOCK DISTRIBUTION



- 1) PROG_SEL INTENTIONAL NC. ENABLES SPI CONFIG MODE.
- 2) IN_SEL TIED TO SUPPLY. ENABLES DIFFERENTIAL INPUT CLOCK MODE
- 3) S4,S5 PHYSICALLY LEFT FLOATING. DISCUSS PROPER LOGIC STATE.
- 4) AD9508_RESET_N IS DERIVED FROM PSU SEQ OUTPUT (PORB).
- 5) LVDS TERMINATION PLACEMENT AT LOAD

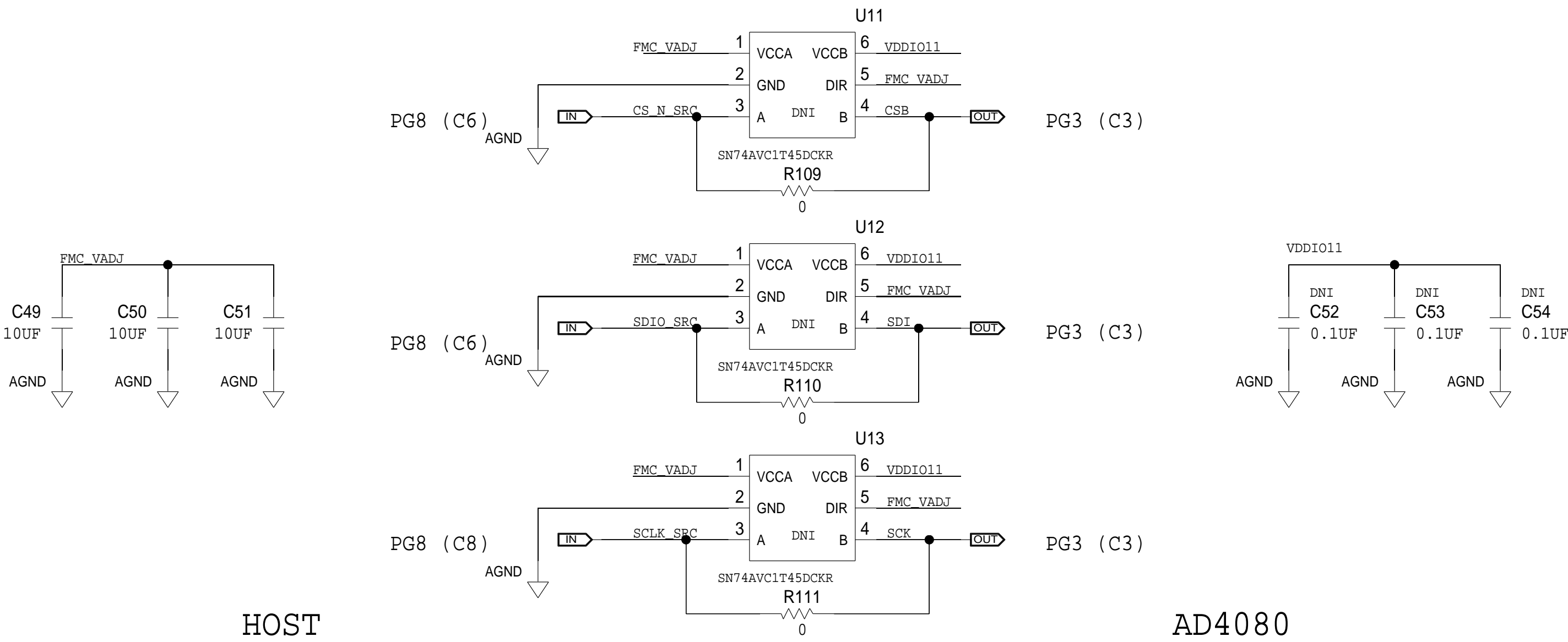


SCHEMATIC

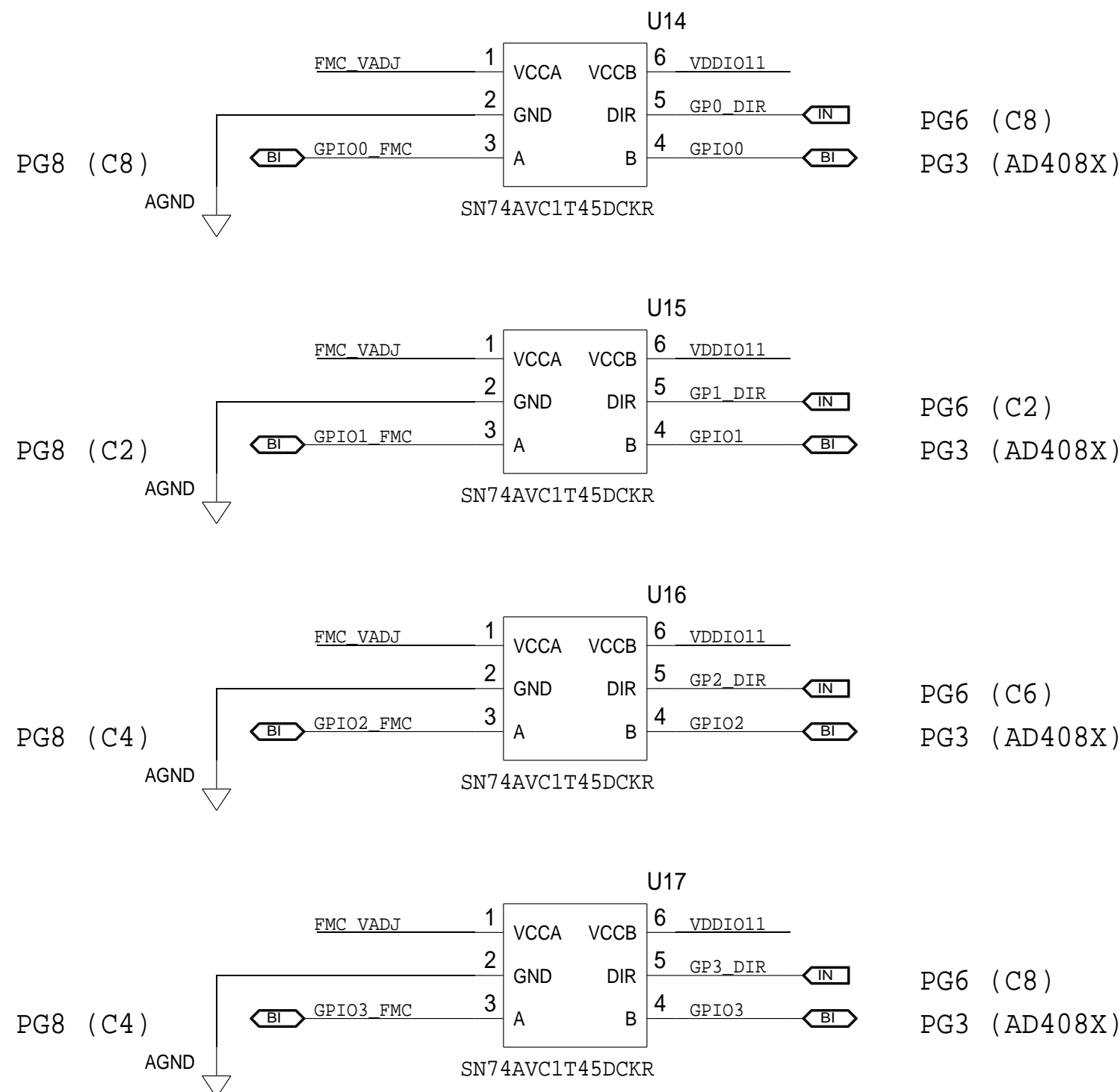
HW TYPE : Customer Evaluation FMCZ Product(s): AD4080 : AD4081, AD4082, AD4083, AD4084, AD4085			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_069798	REV F	
PTD ENGINEER D. SLOAN	SIZE D	SCALE 1:1	SHEET 8 OF 10

LEVEL TRANSLATION

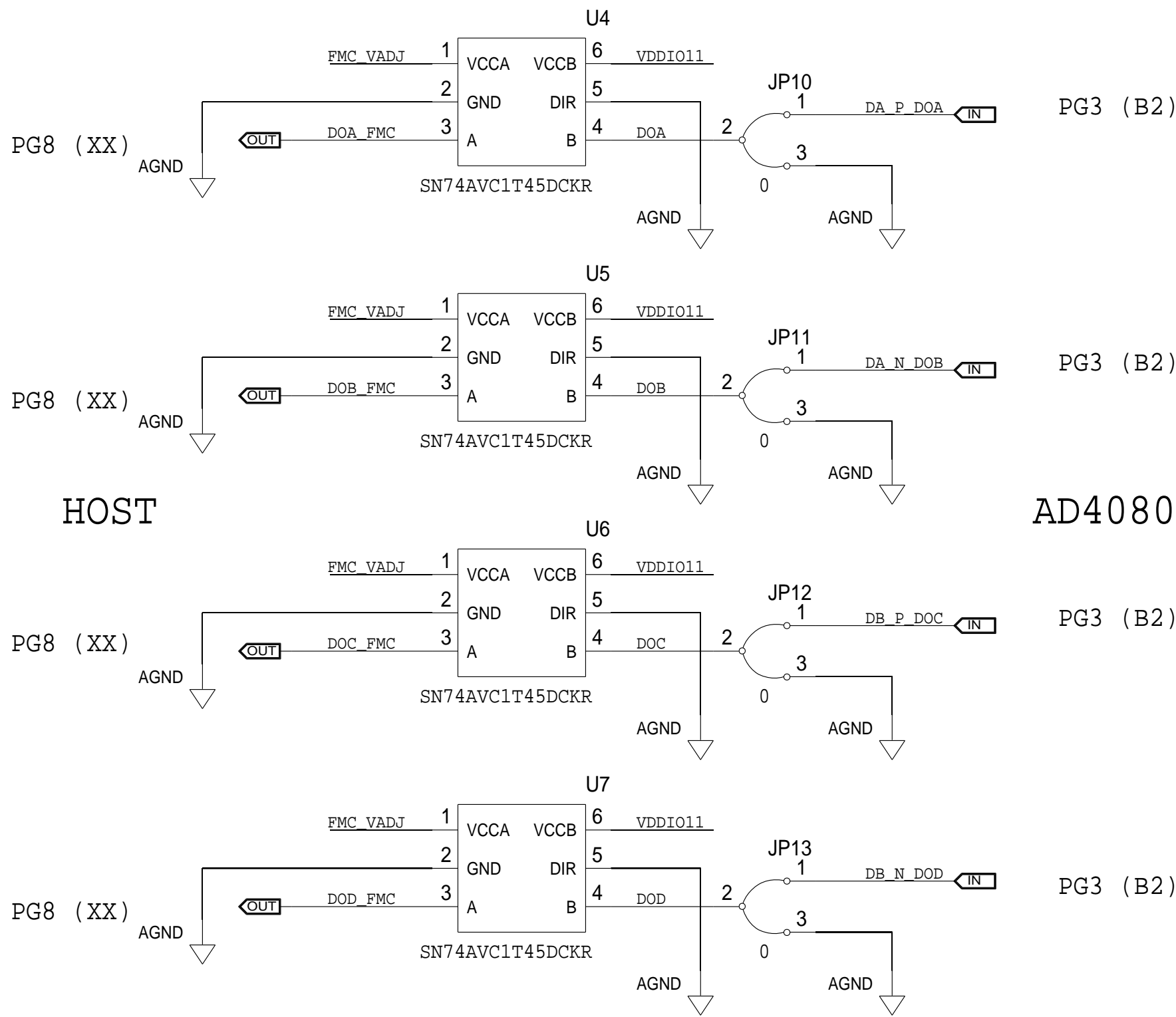
CONFIGURATION SPI LEVEL TRANSLATORS (CONSIDER FOR DELETION, NOT INSTALLED BY DEFAULT)



GPIO LEVEL TRANSLATORS

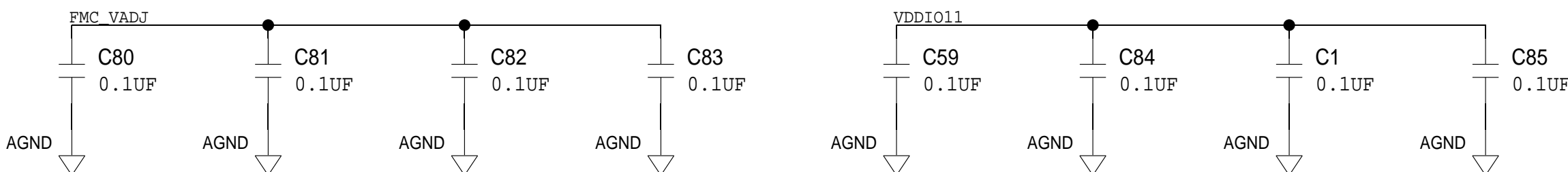


DATA SPI LEVEL TRANSLATORS



HOST

AD4080

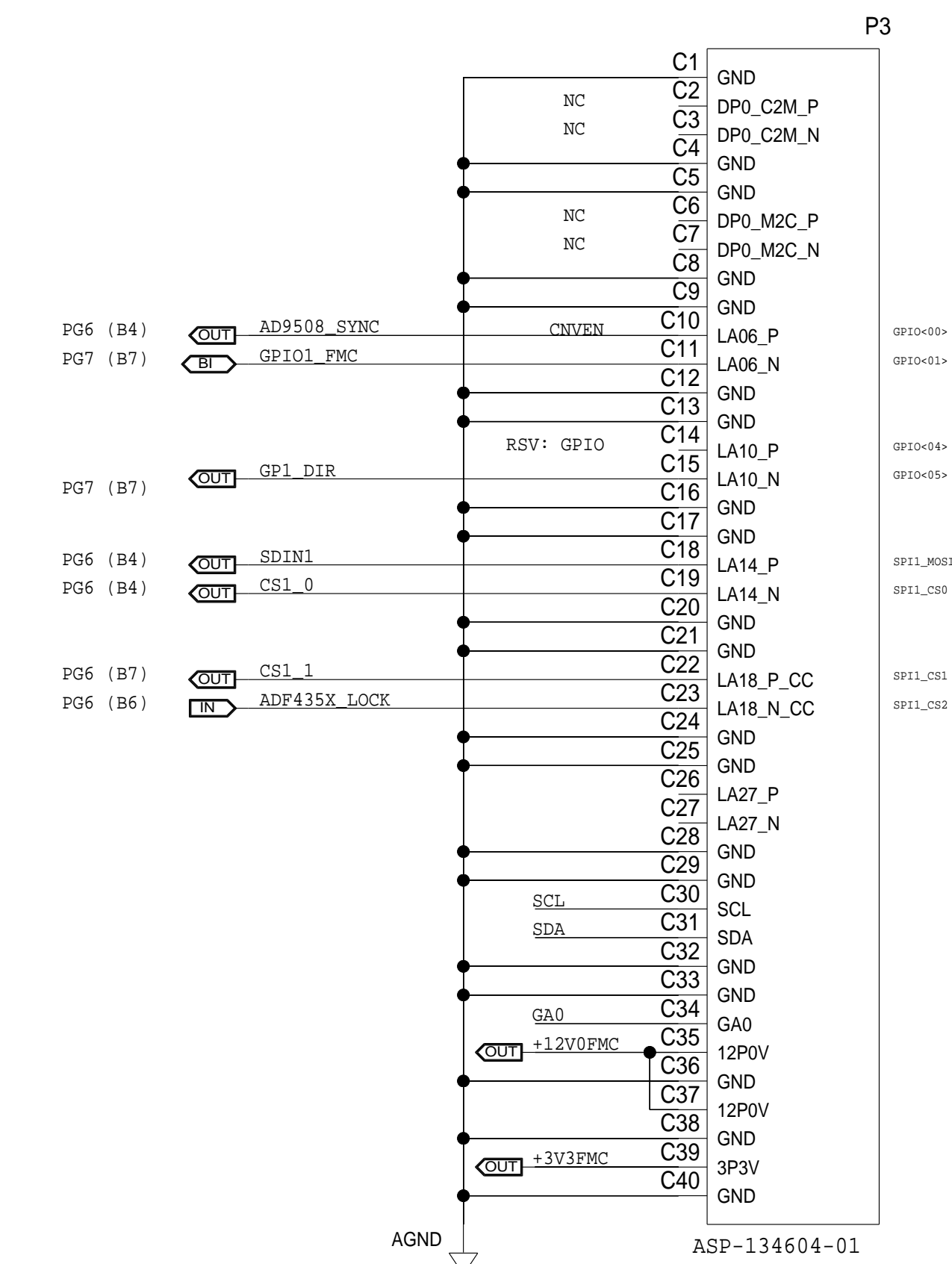
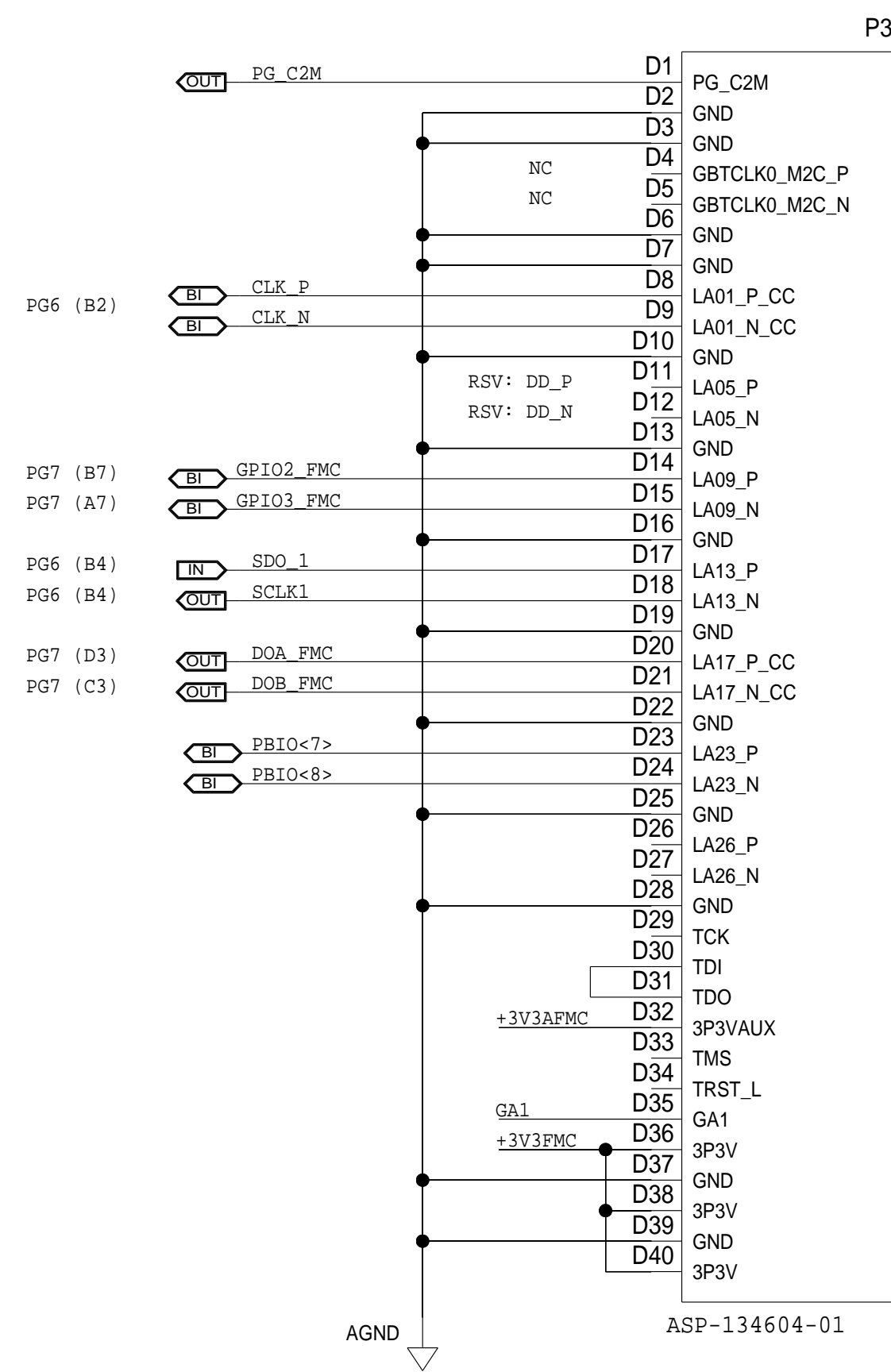
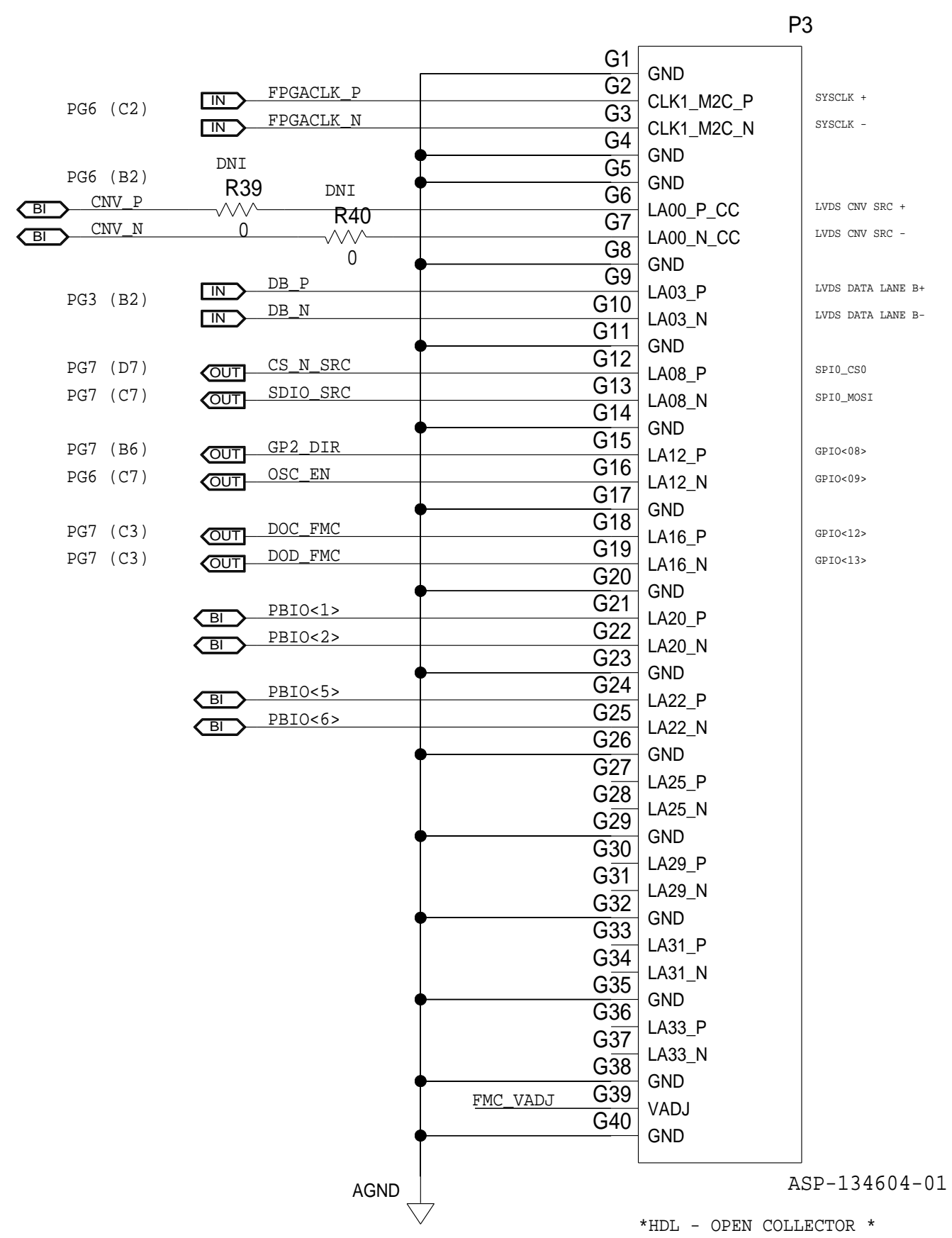
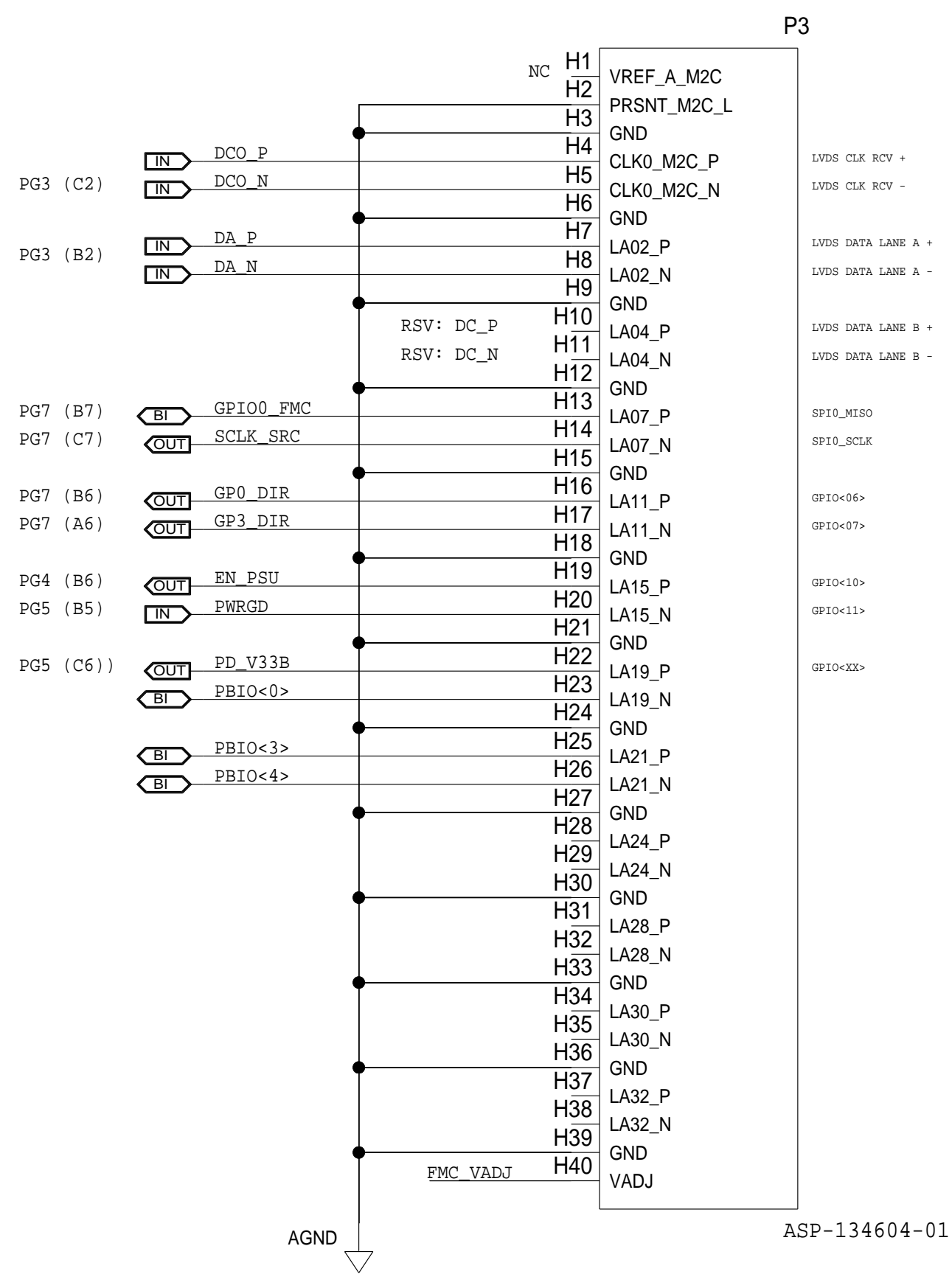


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG DEVICES		SCHEMATIC	
HW TYPE : Customer Evaluation FMCZ		Product(s): AD4080	
DESIGN VIEW		DRAWING NO. 02_069798	
<DESIGN_VIEW>		REV F	
PTD ENGINEER		SIZE D	
D. SLOAN		SCALE 1:1	
		SHEET 9 OF 10	

HOST (FMC) INTERFACE

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



BOARD ID EEPROM

