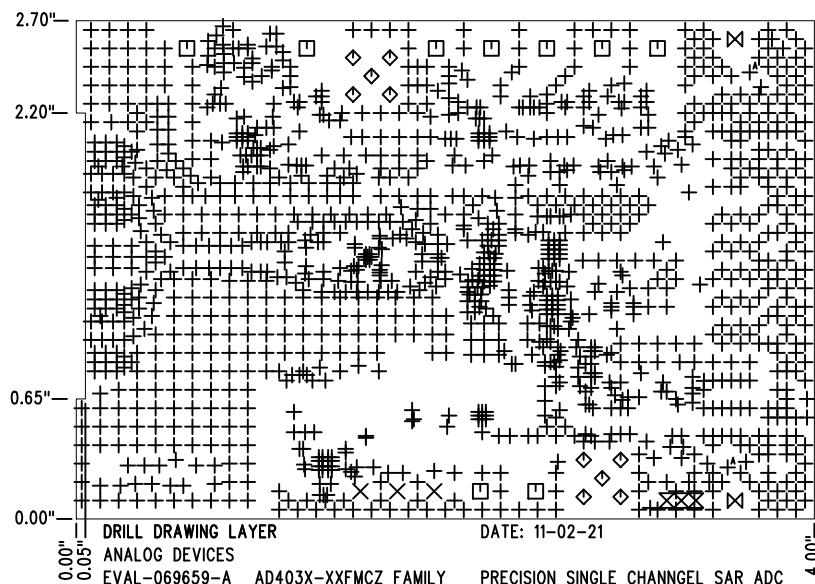
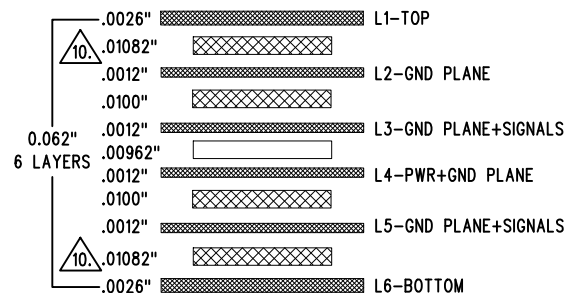


SHOWN FROM TOP SIDE



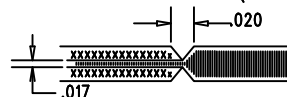
SIZE	QTY	SYM	PLATED	TOL
0.008	1406	+	YES	+/-0.003"
0.064	3	×	YES	+/-0.003"
0.094	9	□	YES	+/-0.003"
0.07	10	◇	YES	+/-0.003"
0.035	3	⊗	YES	+/-0.003"
0.12	2	⊗	NO	+/-0.003"
0.05	2	+ <sup>A</sup>	NO	+/-0.003"

## LAYER STRUCTURE




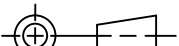
## NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, NELCO 4000-13EP.  
-FINISHED THICKNESS TO BE 0.062" +/- .005"  
-TOTAL OF 6 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.  
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.  
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.  
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.  
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.  
-GOLD IMMERSION BOTH SIDES.  
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.  
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



9. SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.

10. CONTROLLED 50 OHM +/-10% IMPEDANCE FOR LAYERS 1-2, USING 0.019" TRACE AT 26GHz FREQ.

UNLESS OTHERWISE SPECIFIED		APPROVALS		<div>ANALOG DEVICES</div> <div>2555 AUGUSTINE DRIVE SANTA CLARA, CA 95054 www.analog.com</div> <div>AHEAD OF WHAT'S POSSIBLE™</div>	
DIMENSIONS ARE IN INCHES		PCB DES.	KIM T.	TITLE: FABRICATION DRAWING	
TOLERANCES:		APP ENG.	CLARENCE M.		
0.XX" = ±0.01"					
0.XXX" = ±0.005"				PRECISION SINGLE CHANNGEL SAR ADC	
INTERPRET DIM AND TOL				SIZE	IC NO.
PER ASME Y14.5M-1994				N/A	AD403X-XXFMCZ FAMILY
THIRD ANGLE PROJECTION				REV A	
		SCALE = NONE		FILENAME: EVAL-069659-A.PCB	
				SHT 1 OF 1	