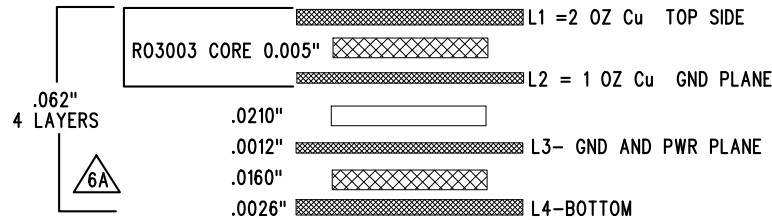
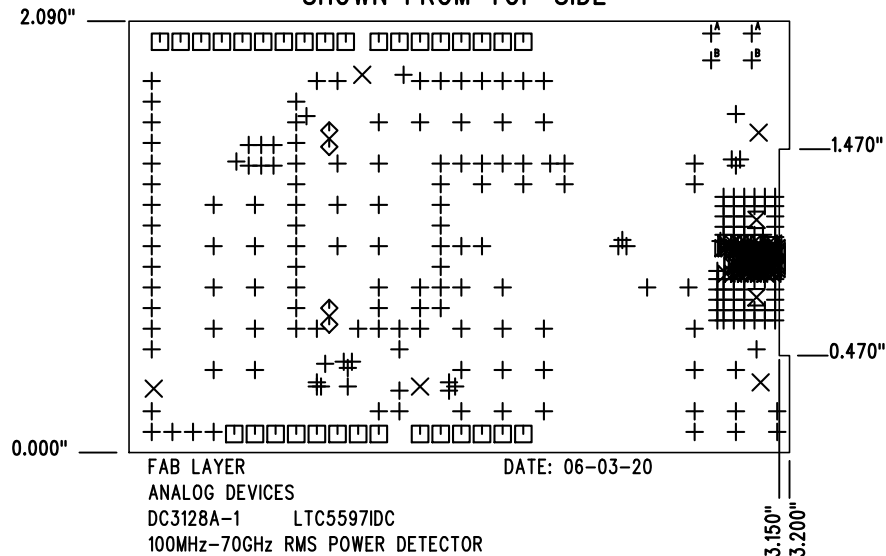


## LAYER STRUCTURE



## SHOWN FROM TOP SIDE



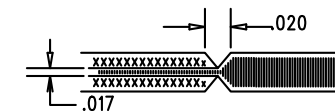
SIZE	QTY	SYM	PLATED	TOL
0.006	204	+	YES	+/-0.003"
0.065	5	X	YES	+/-0.003"
0.04	32	□	YES	+/-0.003"
0.035	4	◇	YES	+/-0.003"
0.082	2	⊗	YES	+/-0.003"
0.004	91	⊗	YES	+/-0.003"
0.05512	2	+ <sup>A</sup>	YES	+/-0.003"
0.04724	2	+ <sup>B</sup>	YES	+/-0.003"

## REVISION HISTORY

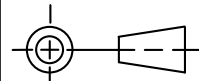
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	1	PRODUCTION	ANDY M.	06-03-20

## NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR  
BETWEEN LAYER 1 AND 2 R03003 SERIES ROGERS PREPREG 5mils  
-FINISHED THICKNESS TO BE 0.062" +/- .005"  
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.  
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.  
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.  
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.  
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.  
-GOLD IMMERSION BOTH SIDES.  
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- CONTROLLED 50 OHM +/-5% IMPEDANCE FOR LAYER 1-2  
TRACE WIDTH 10 MILS IN A COPLANAR WAVEGUIDE STRUCTURE.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.  
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING



UNLESS OTHERWISE SPECIFIED  
DIMENSIONS ARE IN INCHES  
TOLERANCES:  
0.XX" = ±0.01"  
0.XXX" = ±0.005"  
INTERPRET DIM AND TOL  
PER ASME Y14.5M-1994  
THIRD ANGLE PROJECTION



## APPROVALS

PCB DES.	KIM T.
APP ENG.	ANDY M.

SCALE = NONE



2555 AUGUSTINE DRIVE  
SANTA CLARA, CA 95054  
www.analog.com

TITLE: FABRICATION DRAWING

100MHz-70GHz RMS POWER DETECTOR

SIZE	IC NO.	REV
N/A	LTC5597IDC DEMO CIRCUIT 3128A	1

FILENAME: DC3128A-1.PCB

SHT 1 OF 1