

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	05JUN23	P. SHARMA

ASSEMBLY NOTES:

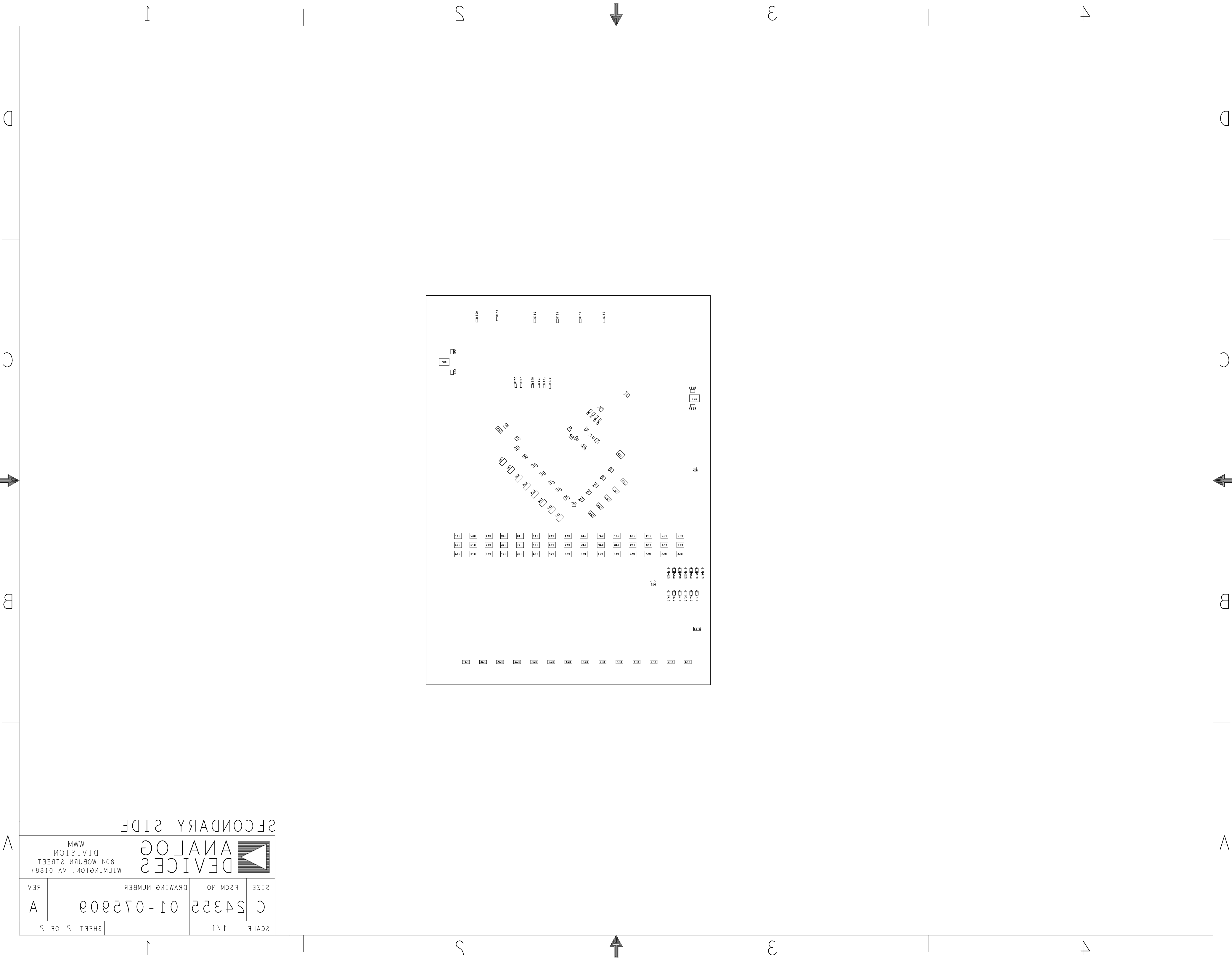
1. BOARD ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00119 (LATEST REVISION).
2. REPAIRS PER IPC-7711/21(LATEST REVISION) ARE ALLOWED.
3. REPAIRS ARE NOT ALLOWED IN SOLDERMASK FREE AREAS ON EITHER SIDE OF THE BOARD.
4. SMOOTHEN EDGES AND FREE FROM BURRS AFTER DEPANELIZATION PROCESS.
5. INSTALL SCREW (M025339) ON PRIMARY SIDE AND STANDOFFS (M025474) ON SECONDARY SIDE.
6. DEFAULT SETTINGS TO BE IN (ON) POSITION.
7. INSTALL JUMPER SHUNT (M031256) ON LOCATIONS BELOW:
A. BOP-
B. P+B14
8. RoHS COMPLIANCE: ASSEMBLY VENDOR SHOULD ASSURE COMPLIANCE WITH LEAD-FREE AND RoHS PCB ASSEMBLY STANDARDS (EU RoHS DIRECTIVE 2002/95/EC).

9. ATTACH STICKER LABEL PER U1 COMPONENT BOM VARIANT DECLARATION:

- * ADES1754EVKIT# FOR 05-075909-01
- * ADES1755EVKIT# FOR 05-075909-02
- * ADES1756EVKIT# FOR 05-075909-03
- * ADES1752EVKIT# FOR 05-075909-04

PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX -.010 --1/32 -- 2 .XXX -.005 .XXXX -.0050	APPROVAL		DATE		<div><div><div></div></div><div>ANALOG DEVICES</div></div> <div>GLOBAL OPERATION & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887</div>							
	TEMPLATE ENGINEER											
	HARDWARE SERVICES M. VALE		05JUN23		TITLE ASSEMBLY ADES175X_EVKIT_A CUSTOMER EVAL_Z							
	HARDWARE SYSTEMS											
MATERIAL	TEST ENGINEER				SIZE C							
	COMPONENT ENGINEER N. CATALAN		05JUN23						FSCM NO 24355			
	TEST PROCESS											
	HARDWARE RELEASE K. JABATAN		05JUN23						REV A			
FINISH	DESIGNER P. SHARMA		05JUN23		SCALE 1 / 1							
	PTD ENGINEER P. SHARMA		05JUN23						SHEET 1 OF 2			
	CHECKER											
DO NOT SCALE DWG												



SECONDARY SIDE

WILMINGTON, MA 01887

804 WOBURN STREET

DIVISION

MWM

ANALOG

DEVICES

SCALE 1:1

24352

01-075009

REV A

24352

01-075009

REV A

SCALE 1:1

24352

01-075009

REV A

24352

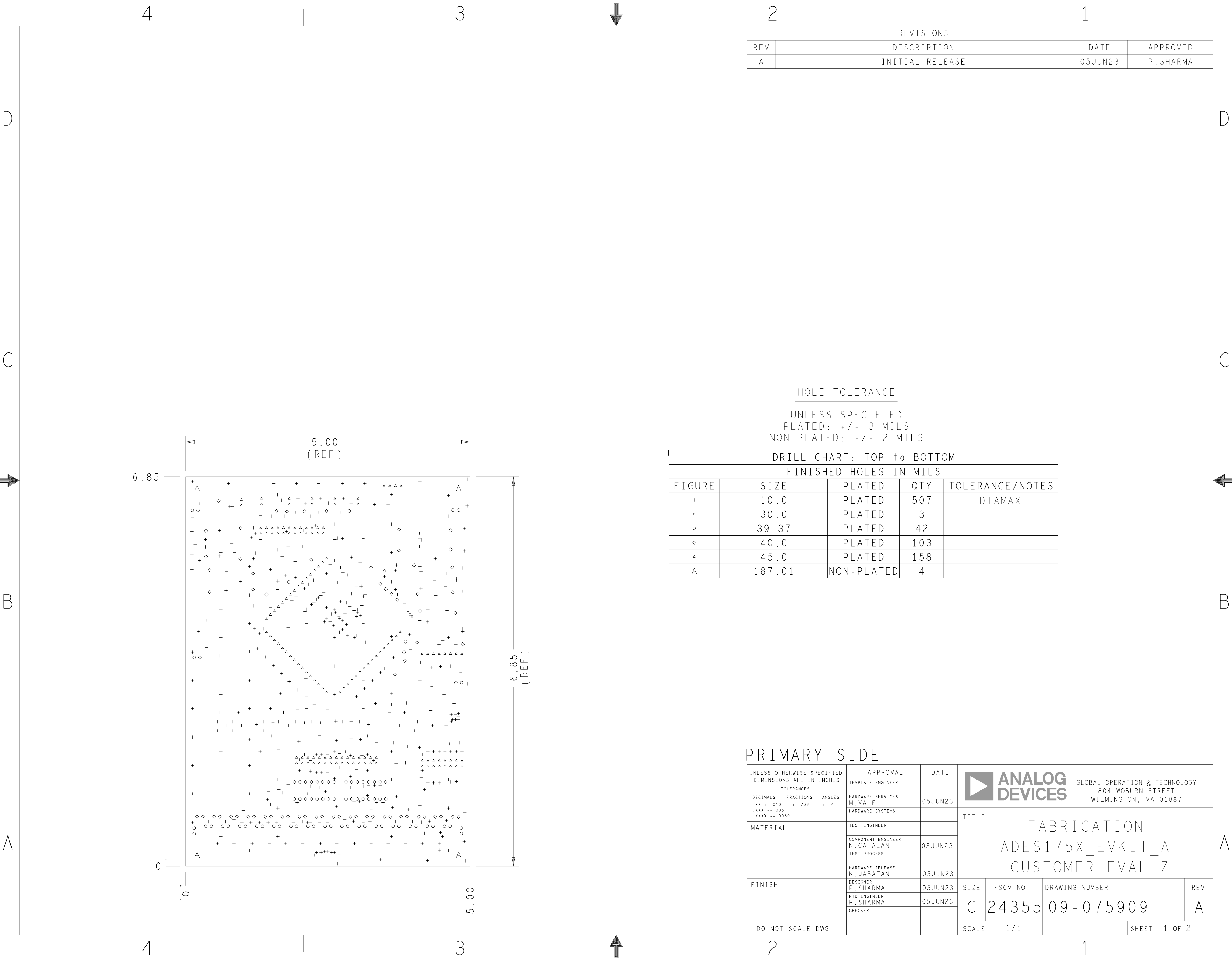
01-075009

REV A

24352

01-075009

REV A



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	05JUN23	P. SHARMA

HOLE TOLERANCE
UNLESS SPECIFIED
PLATED: +/- 3 MILS
NON PLATED: +/- 2 MILS

DRILL CHART: TOP to BOTTOM				
FINISHED HOLES IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
+	10.0	PLATED	507	DIAMAX
◻	30.0	PLATED	3	
○	39.37	PLATED	42	
◊	40.0	PLATED	103	
△	45.0	PLATED	158	
A	187.01	NON-PLATED	4	

PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX -.010 --1/32 -- 2 .XXX -.005 .XXXX -.0050			APPROVAL		DATE		<div><div></div><div>ANALOG DEVICES</div></div> <div>GLOBAL OPERATION & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887</div>	
			TEMPLATE ENGINEER					
MATERIAL			HARDWARE SERVICES M. VALE		05JUN23		TITLE FABRICATION ADES175X_EVKIT_A CUSTOMER EVAL_Z	
			HARDWARE SYSTEMS					
			TEST ENGINEER					
			COMPONENT ENGINEER N. CATALAN		05JUN23			
FINISH			TEST PROCESS				SIZE FSCM NO DRAWING NUMBER REV C 24355 09-075909 A	
			HARDWARE RELEASE K. JABATAN		05JUN23			
			DESIGNER P. SHARMA		05JUN23			
			PTD ENGINEER P. SHARMA		05JUN23			
			CHECKER					
DO NOT SCALE DWG							SCALE 1 / 1 SHEET 1 OF 2	

NOTES : UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES (EXCEPT WHERE NOTED).
ALL DOCUMENTS & SPECIFICATIONS REFERRED TO BELOW SHOULD BE THE LATEST REVISIONS.

MATERIAL : HOMOGENOUS MATERIALS IN THIS BOARD SHALL BE COMPLAINT WITH THE EU DIRECTIVE 2002/95/EC

2. BOARD MATERIAL:(USE CHECKED ITEMS)
 (X) ISOLA 370HR OR S1000-2 OR IT180 OR EQUIVALENT
 () ISOLA-FR408HR OR EQUIVALENT
 () ISOLA IS410
 () MEGTRON 6
 () NELCO-4000-13
 () ROGERS 4350B
 () ROGERS 3003
 () ARLON 85N
 () EM370D
 () OTHER _____
3. ALL LAMINATES & BONDING MATERIALS SHOULD BE SELECTED FROM IPC-4101 OR IPC-4103,(TG>170 DEGC TD>300 DEGC)
 UL FLAMMABILITY RATING 94V-0. BOARD MATERIAL & CONSTRUCTION SHALL MEET THE REQUIREMENTS OF UL796/UL796F.
4. REFER TO IPC-6010 SERIES, CLASS 2 FOR FABRICATION.WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2.
5. REFER TO LAMINATION DIAGRAM FOR OVERALL BOARD THICKNESS. TOLERANCE APPLIES AFTER ALL LAMINATION AND PLATING
 PROCESSES. FINISHED THICKNESS MEASURED FROM TOP COPPER TO BOTTOM COPPER.
6. BOW & TWIST NOT TO EXCEED 0.0075 INCHES (0.75%) PER LINEAR INCH AND SHOULD BE MEASURED PER IPC-TM-650, METHOD 2.4.22.
7. ACCEPTABILITY PER ADI SPECIFICATION TST00115.

TOOLING:

8. IMPEDANCE REQUIREMENTS: IF NO STACKUP IS DEFINED, THE VENDOR IS ALLOWED TO ADJUST THE DIELECTRIC THICKNESS & TRACE WIDTHS TO MEET THE IMPEDANCE REQUIREMENT. IF SPECIFIED, THE VENDOR MUST MEET THE REQUIREMENTS LISTED IN THE IMPEDANCE TABLE. ANY ADJUSTMENT MADE TO THE DEFINED STACKUP TRACE WIDTH & SPACING THAT IMPACT THE REQUIREMENTS MUST HAVE WRITTEN APPROVAL FROM ADI.
9. FILLET OPTIONS TO ENHANCE RELIABILITY AT PAD JUNCTIONS WHERE SPACING PERMITS.
() FILLETS ALLOWED
(X) FILLETS NOT ALLOWED
10. THIEVING:
() VENDOR MAY ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS MAINTAINING A MINIMUM 0.100 INCH CLEARANCE FROM ALL COPPER FEATURES,
(X) VENDOR MAY NOT ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS.
11. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.003 INCHES.

FINISH:

12. DRILL SIZES ARE FINISHED HOLE SIZES. ALL HOLES SHALL BE LOCATED WITHIN 0.005 INCHES DTP, UNLESS SPECIFIED. MINIMUM BARREL PLATING OF 0.001 INCHES. PLATED HOLES SHALL NOT BE ROUGH OR IRREGULAR SO AS TO HINDER PROPER SOLDER WICKING. BARREL RELIEF ON SOLDERMASK ALLOWED IN UNFILLED VIA IN PAD HOLES.

13. PLATING SPECIFICATION:
 (X) REFER TO LAMINATION DIAGRAM FOR FINISHED COPPER WEIGHT/THICKNESS REQUIRMENTS
 THE STARTING COPPER WEIGHT/THICKNESS CAN VARY AS LONG AS THE FINISHED COPPER WEIGHT/THICKNESS IS NOT LESS THAN THE SPECIFIED VALUE.

14. SURFACE FINISH:
 (X) IMMERSION GOLD (ENIG) 1.58-3.94 MICRO INCHES OVER 118-236 MICRO INCHES MIN. OF ELECTROLESS NICKEL PER IPC-4552
 () OSP (ORGANIC SOLDERABILITY PRESERVATIVE)
 () IMMERSION SILVER
 () SOFT WIRE BONDABLE GOLD 30-50 MICRO INCHES OF SOFT WIRE
 BONDABLE GOLD OVER 100-150 MICRO INCHES OF NICKEL
 () EDGE CONNECTOR FINGERS ARE TO BE PLATED WITH 100 MICRO-INCHES(.0001") OF LOW STRESS
 NICKEL UNDER 30 MICRO-INCHES (.0003') OF GOLD
 () OTHER_____

15. SOLDERMASK:
 SOLDERMASK OVER BARE COPPER OR BARE GOLD (BOTH SIDES) TO MEET IPC-SM-840.
 IF PRESENT, DO NOT MODIFY SOLDERMASK DEFINED PADS (MASK OPENINGS LESS THAN COPPER PAD) WITHOUT APPROVAL.
 (X) LPI
 () OTHER_____

COLOR
 (X) GREEN
 () OTHER_____

16. APPLY SILKSCREEN TO BOTH SIDES USING A NON-CONDUCTIVE, EPOXY BASED INK PER ARTWORK.
 (X) WHITE
 () OTHER_____

TESTING:

17. FINAL ELECTRICAL TEST TO BE PERFORMED USING PROVIDED IPC-D-356A NETLIST OR ODB++ FORMAT FILE. THE PCB SHALL HAVE A VERIFICATION STAMP.
18. A TIME DOMAIN REFLECTOMETER REPORT (TDR) FOR EACH IMPEDANCE CONTROLLED LAYER & A CERTIFICATE OF COMPLIANCE SHALL BE PROVIDED BY VENDOR AT TIME OF SHIPMENT. INSTANCES WHERE TDR TESTING CAN'T BE PERFORMED BECAUSE THE TRACE LENGTH IS TOO SHORT ON THE OUTER LAYERS AT THE PIN ESCAPES IS ACCEPTABLE, ALL OTHER INSTANCES MUST BE REPORTED.

MISCELLANEOUS :

19. IF PRESENT, ALL BLIND/BURIED VIAS WITH AN ASPECT RATIO <1:1 TO BE PLATED SHUT WITH COPPER WHEN USED AS VIA-IN-PAD OR AS A STACKED VIA. BLIND/BURIED VIAS WITH AN ASPECT RATIO >1:1 TO BE FILLED WITH NON-CONDUCTIVE EPOXY.
20. FOR VIA FILL INFORMATION REFER TO DRILL CHART:
() NON-CONDUCTIVE EPOXY FILL ALL 0.XXXX INCHES DRILLED VIAS
() COPPER FILL ALL 0.XXXX INCHES DRILLED VIAS
21. INTENTIONAL SHORTS:
IF AN INTENTIONAL SHORT REPORT IS SUPPLIED AND DOES NOT MATCH THE FAB DATA THEN ADI APPROVAL IS REQUIRED.
22. PEMNUTS:
() PEMNUTS TO BE INSTALLED BY FABRICATOR
() PEMNUTS NOT TO BE INSTALLED BY FABRICATOR
(X) NOT APPLICABLE
23. MANUFACTURER TO ETCH/STAMP WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE UNLESS OTHERWISE SPECIFIED:
A. UL CODE-FLAMMABILITY RATING FOR THOSE APPROVED MATERIALS(IF APPLICABLE)
B. DATE CODE
C. LOT NUMBER
D. MANUFACTURER LOGO
25. PANELIZATION:
BOARDS TO BE SHIPPED IN ARRAY AND KEPT INTACT
PANEL TO BE SUBJECTED TO CUSTOMERS APPROVAL
PANEL SOLDER PASTE STENCIL GERBER TO BE PROVIDED TO ANALOG

27. MINIMUM DESIGN LINE WIDTH IS .005 INCH.
28. MINIMUM DESIGN LINE SPACING IS .008 INCH.

FAB NOTES REVISION: 2ND NOVEMBER 2022

4 LAYER STACKUP

LAMINATION DIAGRAM				
LAYER NUMBER	LAYER NAME	COPPER THICKNESS (OZ, INCH)	DIELECTRIC THICKNESS (INCH)	MATERIALS
1	TOP	1 OZ, 0.0014"		FINAL CU (THICKNESS AFTER PLATING)
			0.006	ISOLA 370HR/EQUIVALENT
2	L2_GND	1 OZ, 0.0014"		CU CLAD
			0.045	ISOLA 370HR/EQUIVALENT
3	L3_GND	1 OZ, 0.0014"		CU CLAD
			0.006	ISOLA 370HR/EQUIVALENT
4	BOTTOM	1 OZ, 0.0014"		FINAL CU (THICKNESS AFTER PLATING)


THE FINISHED PCB THICKNESS TO BE: 0.062" +/-10%

IMPEDANCE TABLE

IMPEDANCE TOLERANCE: +/-10%				
LAYER	50 OHM TRACE WIDTH	65 OHM TRACE WIDTH	100 OHM TRACE WIDTH/SPACE	75 OHM TRACE WIDTH/SPACE
TOP	0.01000	-	0.00800/0.00800	-
GND3	0.00700	-	-	-
BOTTOM	0.01000	-	0.00800/0.00800	-

NOTE: DO NOT EDIT THIS TABLE MANUALLY:USE IMPEDANCE TABLE GENERATOR FROM MAXIMTOOLS

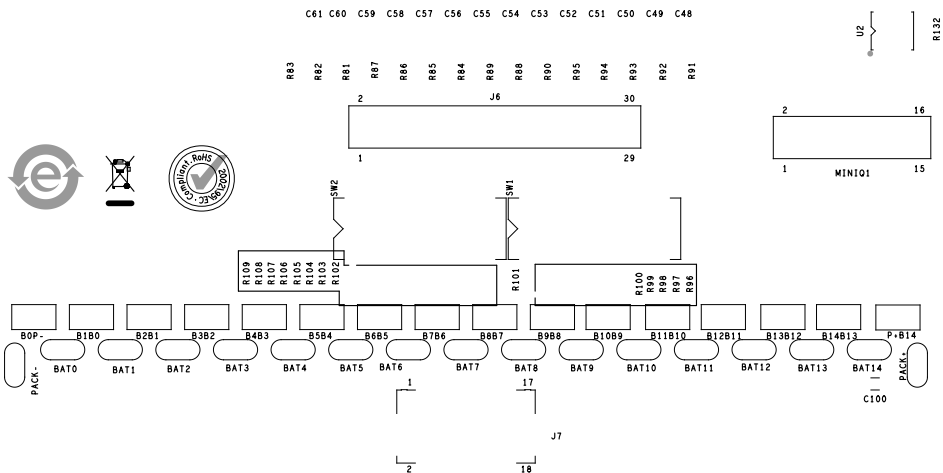
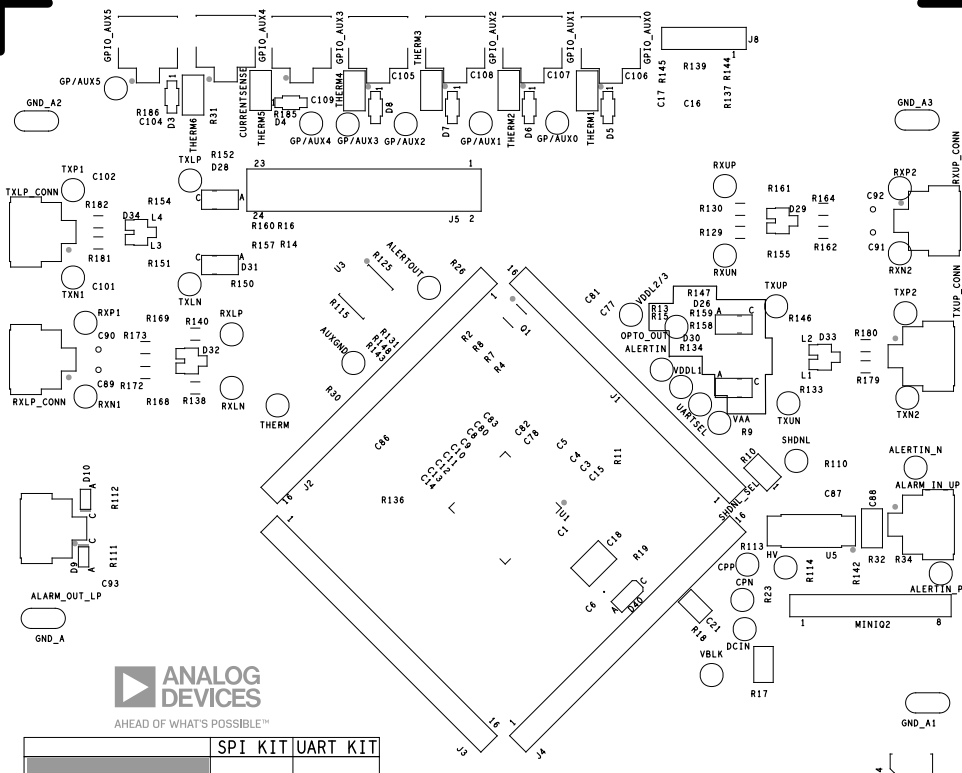
PRIMARY SIDE

	<h1>ANALOG DEVICES</h1>		WWM DIVISION	
			804 WOBURN STREET WILMINGTON, MA 01887	
SIZE	FSCM NO	DRAWING NUMBER		REV
C	24355	09-075909		A
SCALE	1/1			SHEET 2 OF 2

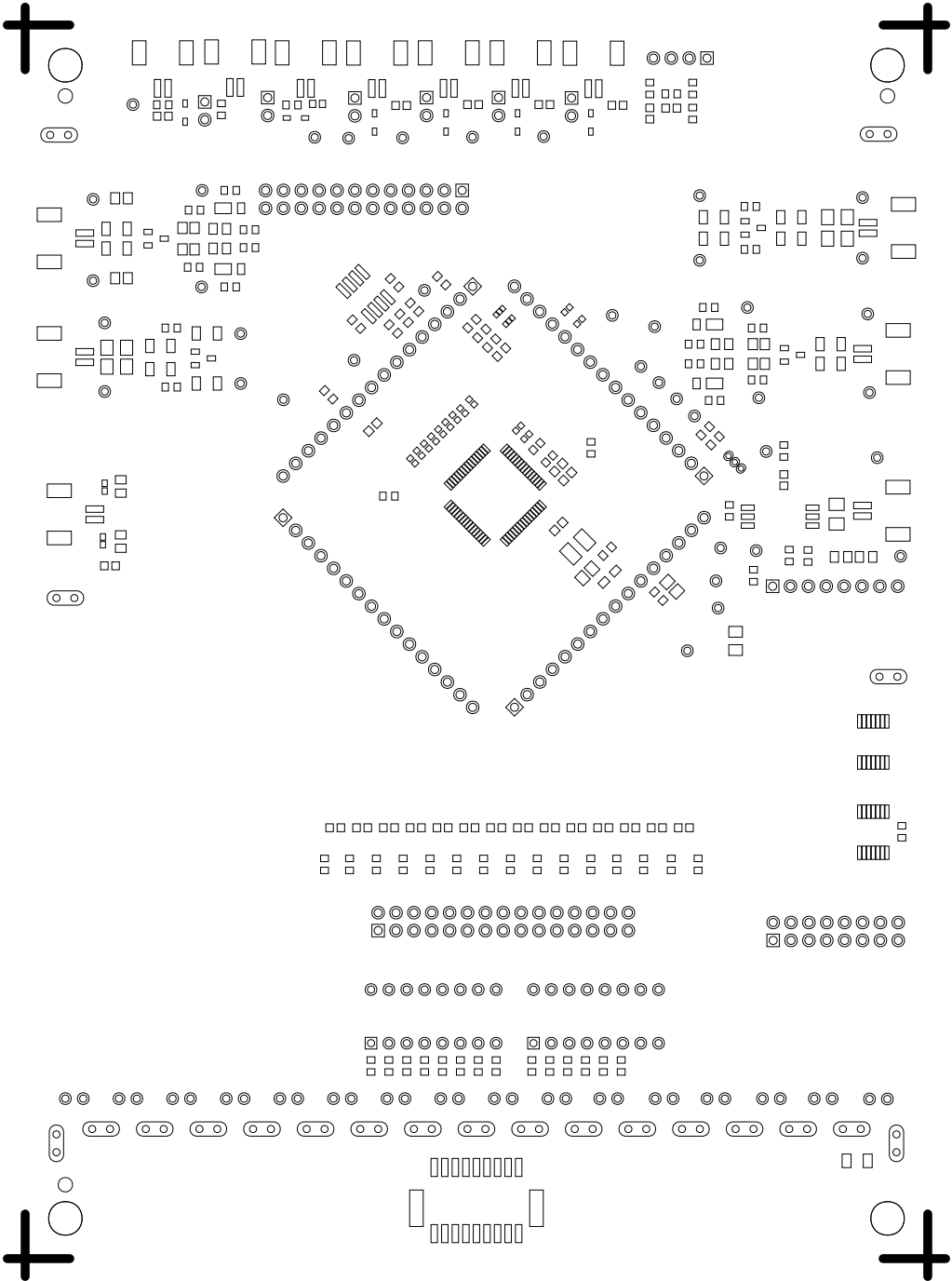
SILKSCREEN PRIMARY

08-075909-03

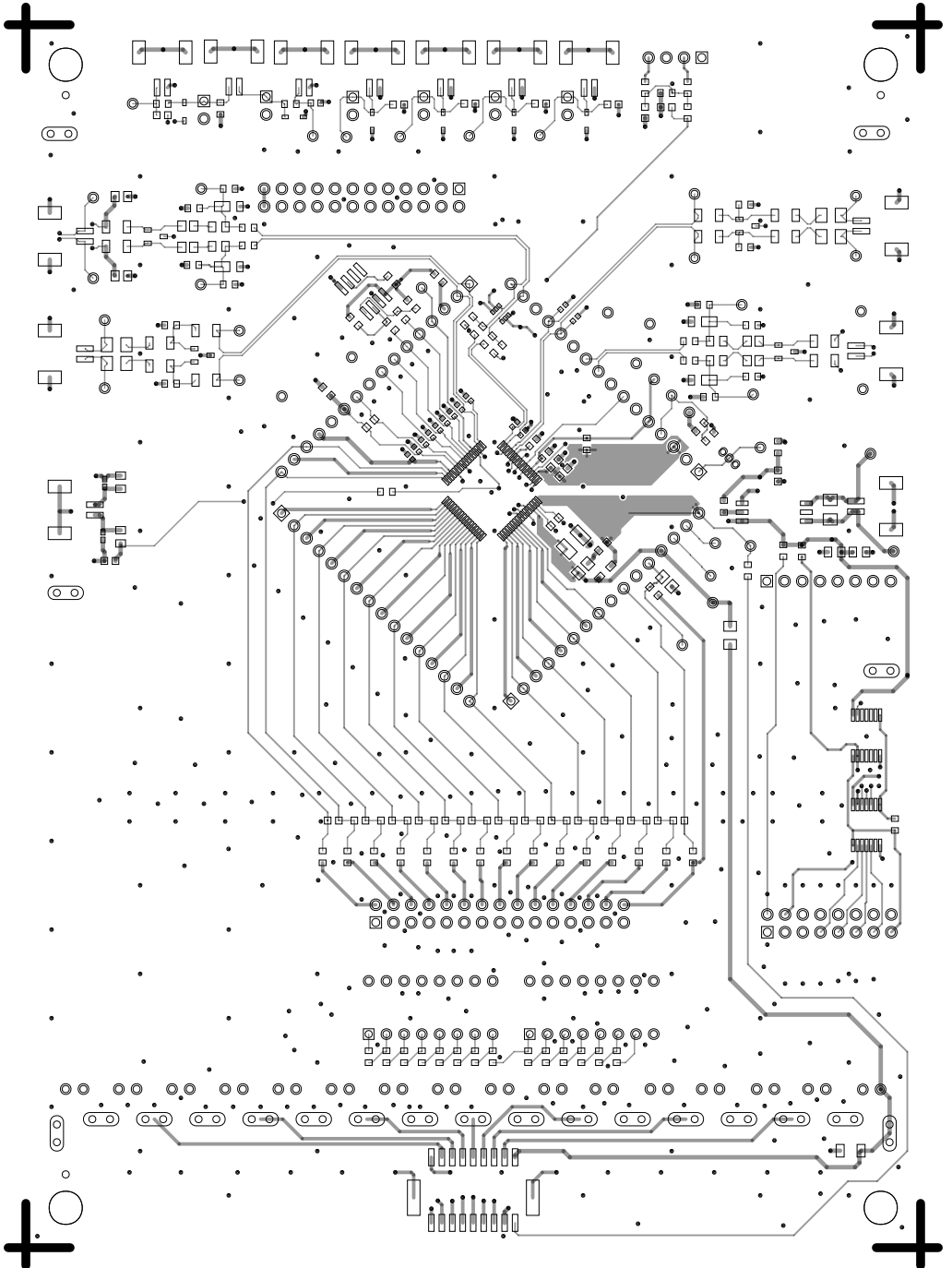
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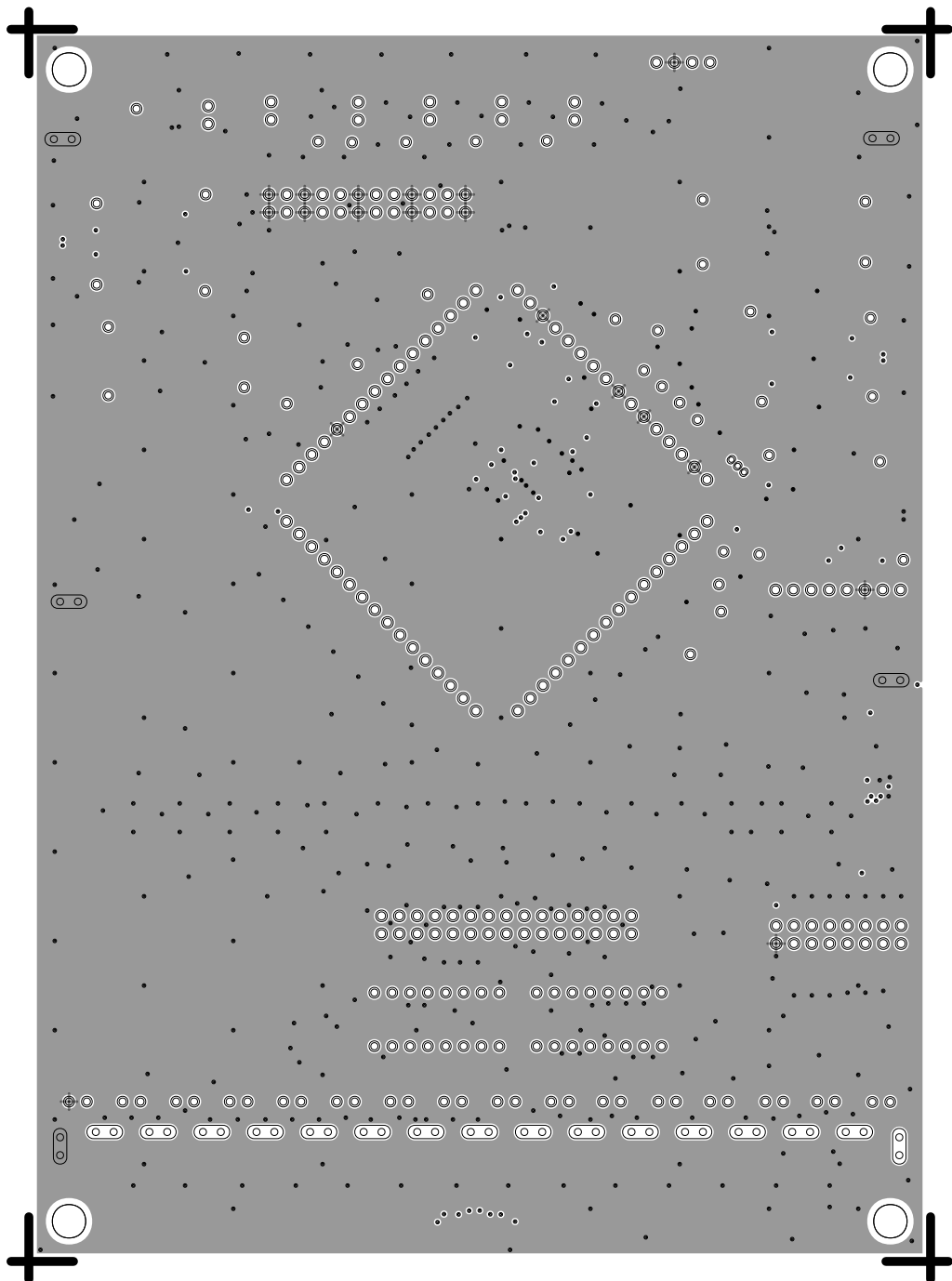
SOLDERMASK PRIMARY
08-075909-04
REV A



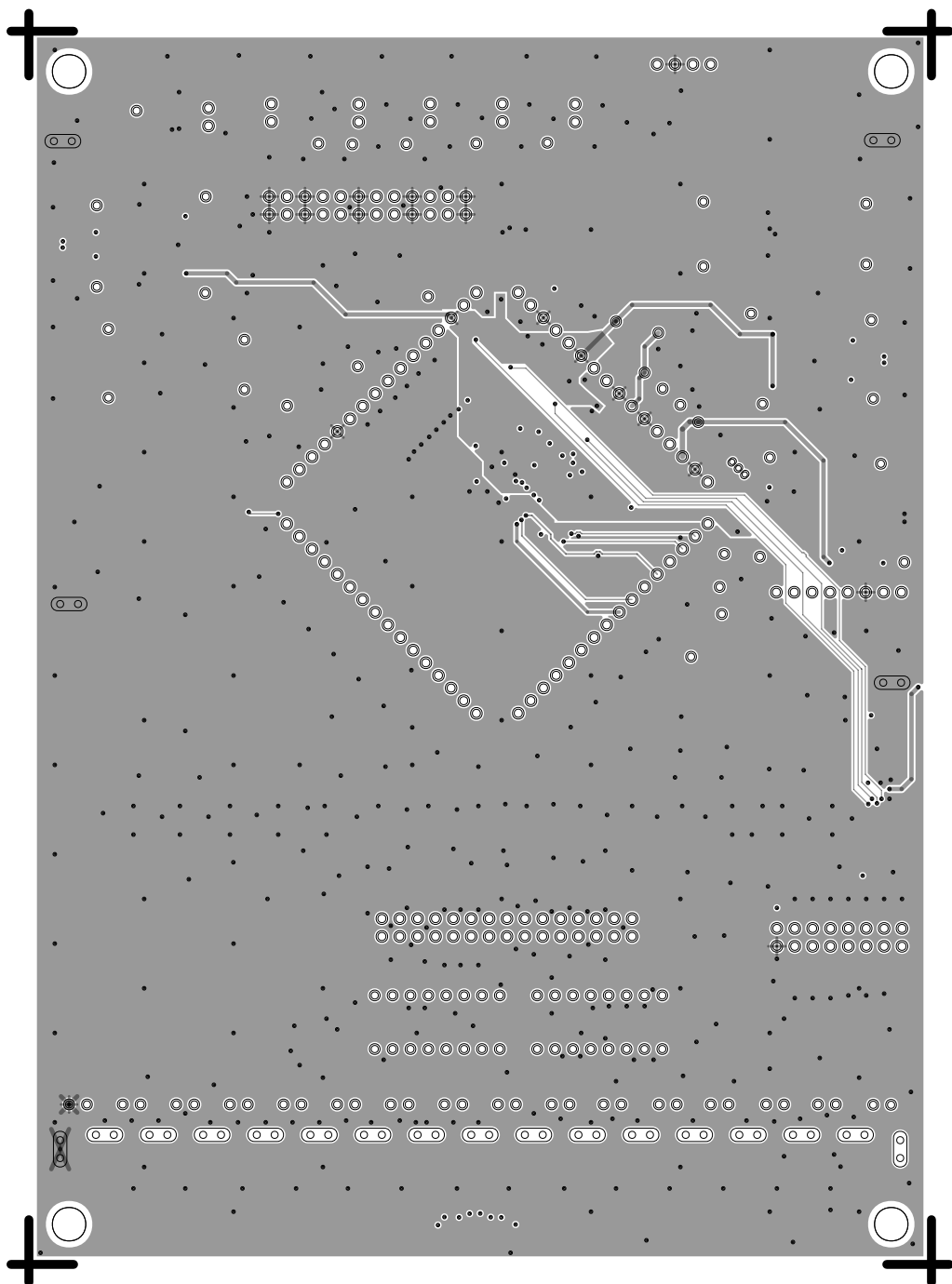
L1 PRIMARY
08-075909-01
REV A



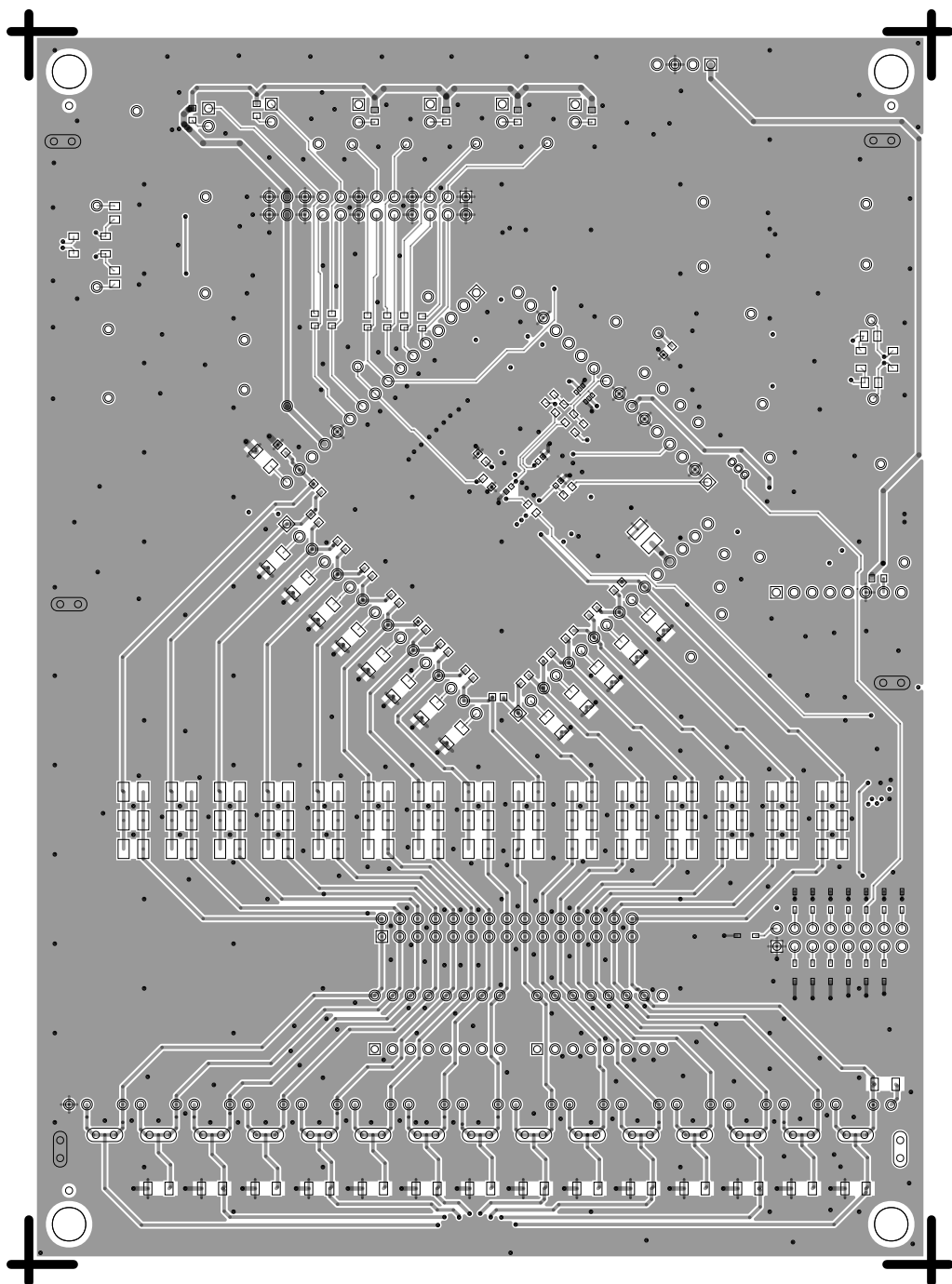
L2_GND
08-075909-07
REV A



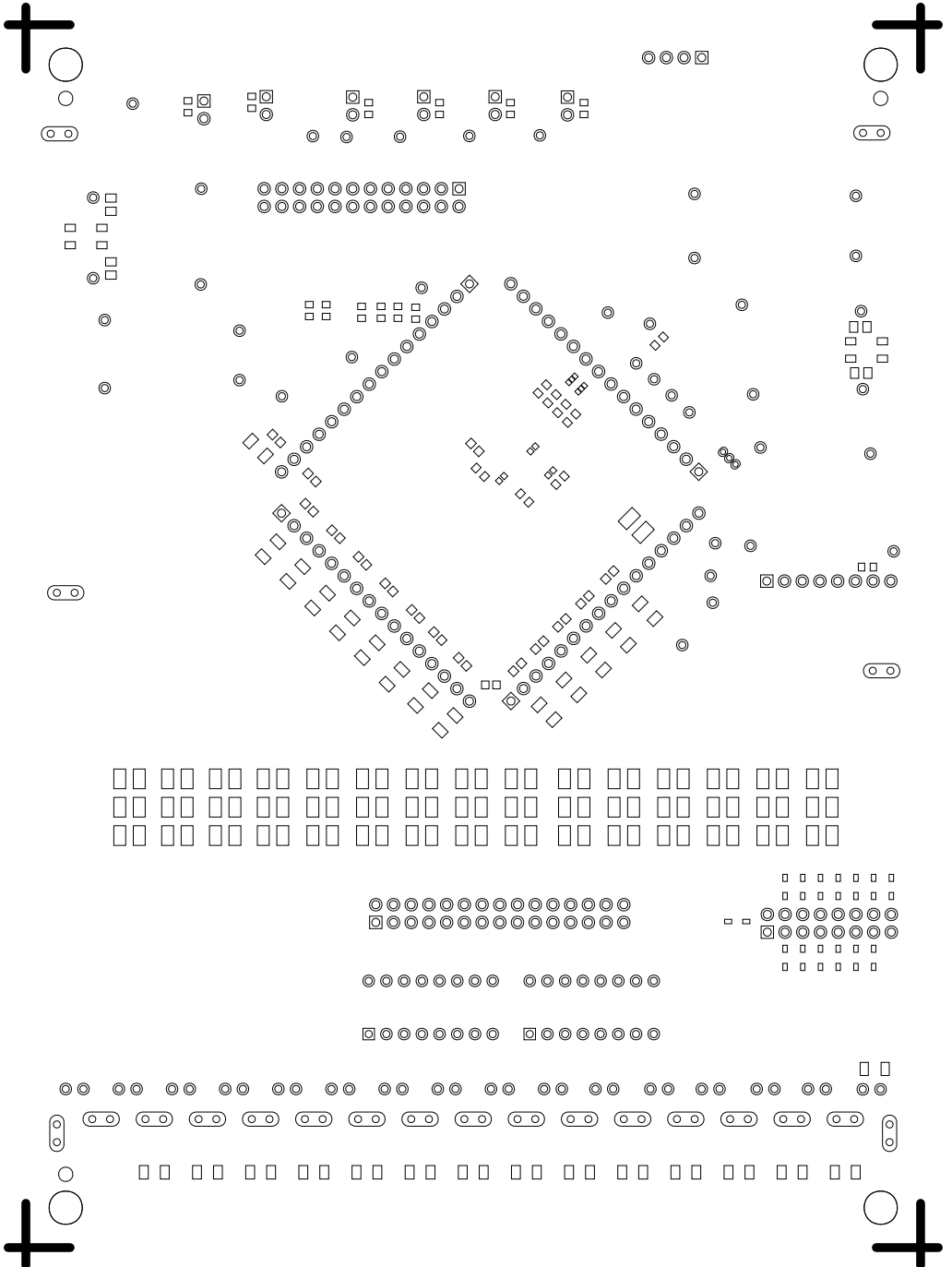
L3_GND
08-075909-08
REV A



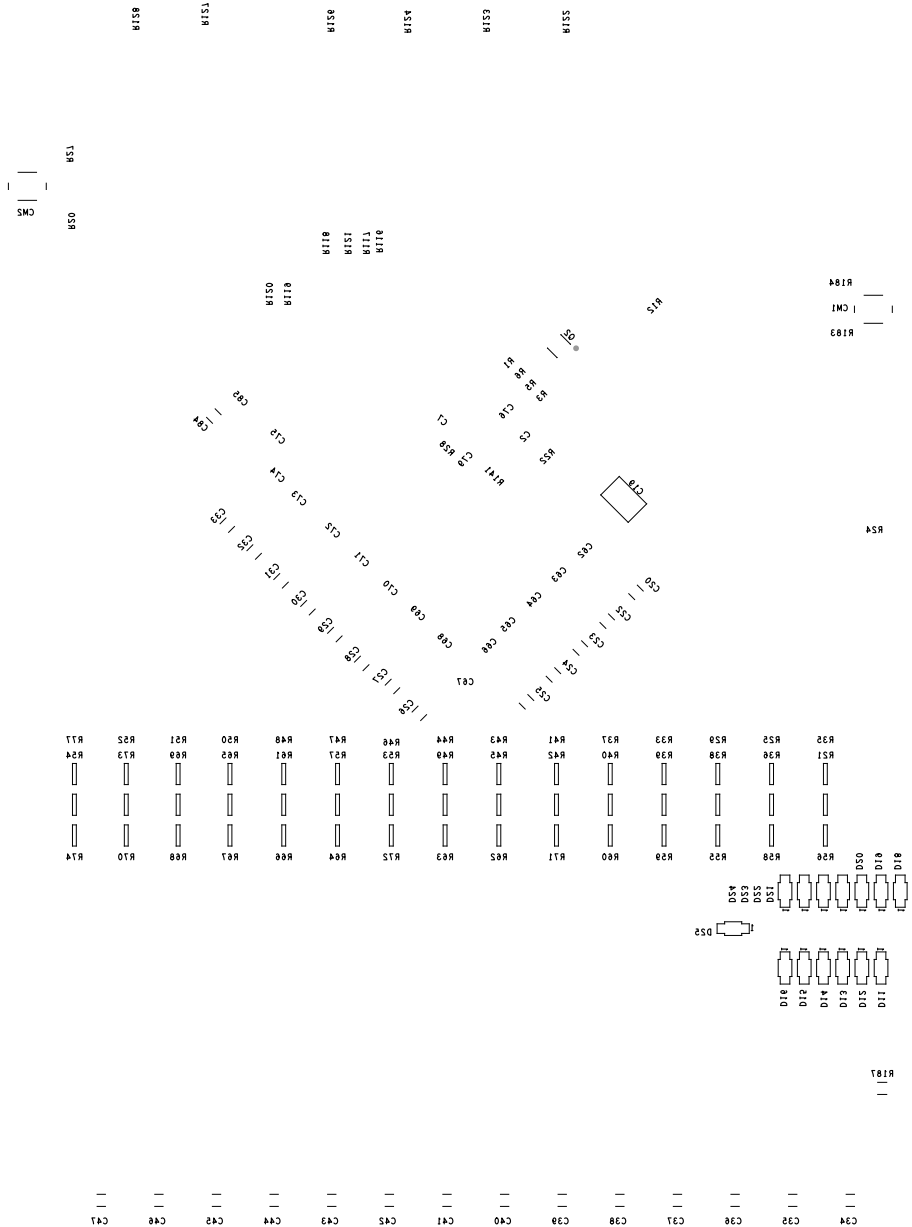
L4 SECONDARY
08-075909-02
REV A



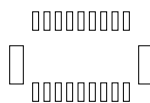
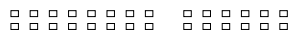
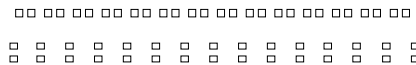
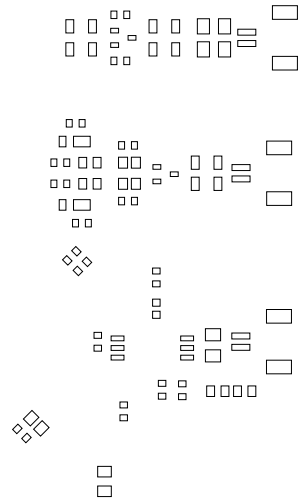
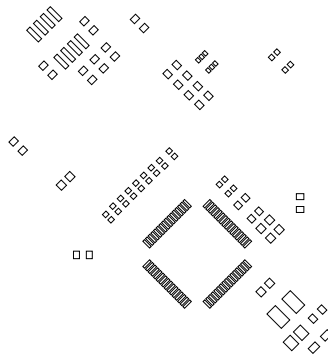
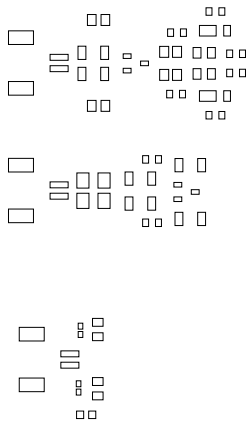
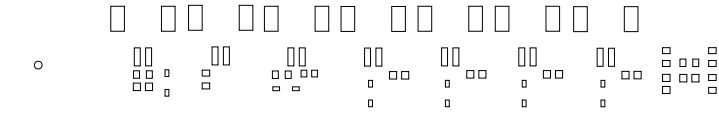
SOLDERMASK SECONDARY
08-075909-06
REV A



SILKSCREEN SECONDARY
08-075909-05
REV A



PASTEMASK PRIMARY
08-075909-09
REV A



PASTEMASK SECONDARY
08-075909-10
REV A

