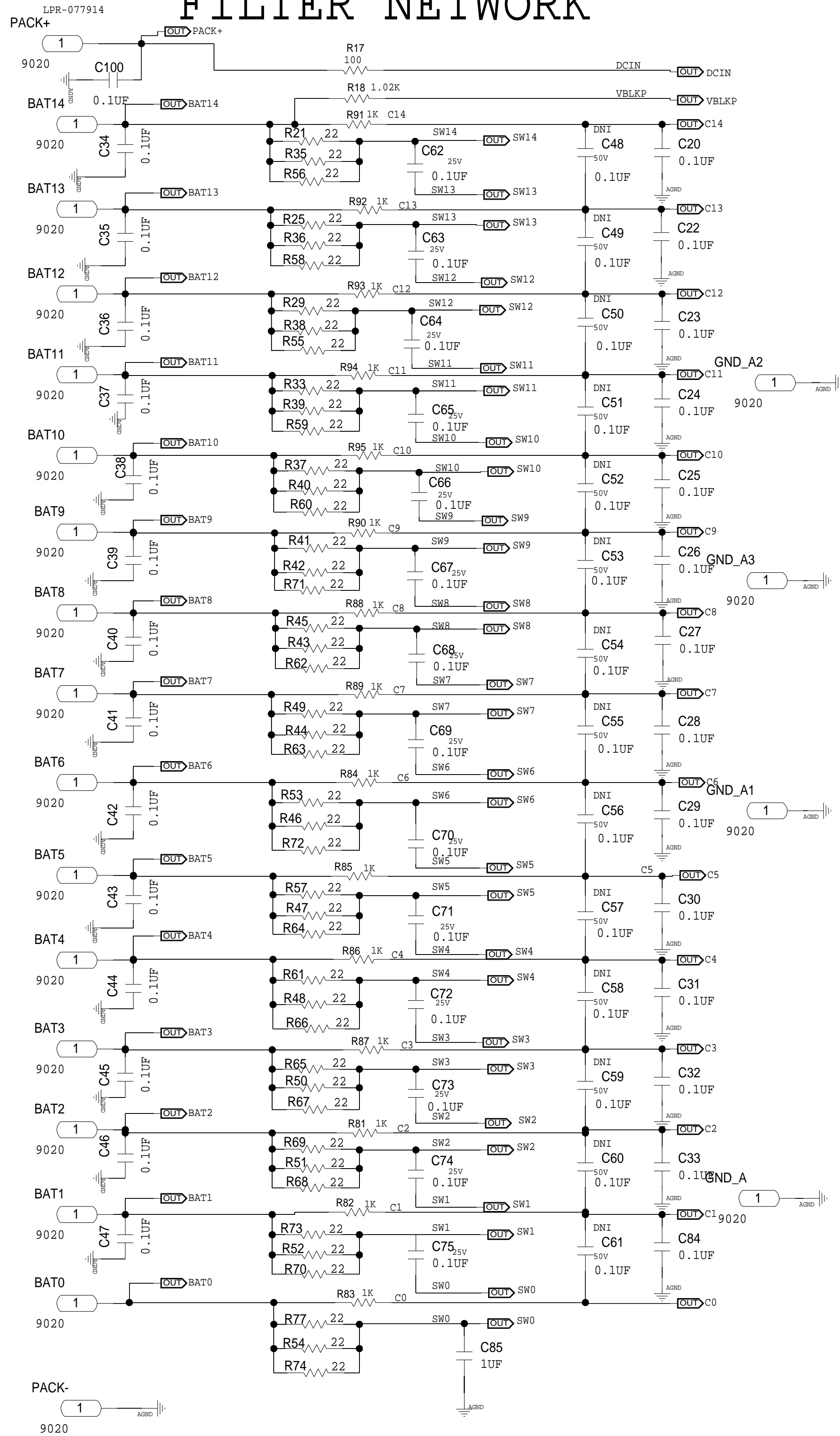


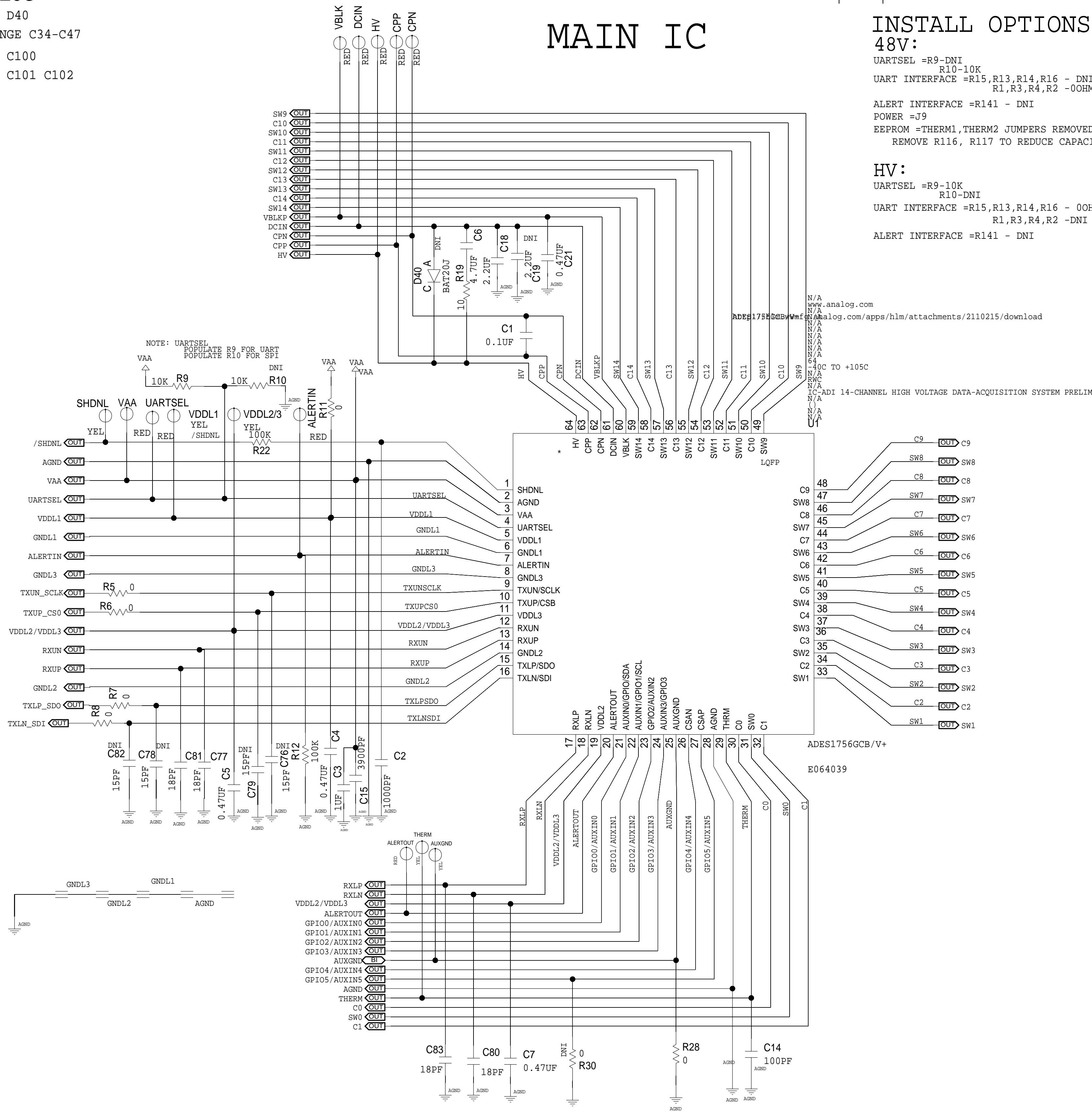
CELL AND SW INPUT
FILTER NETWORK



CHANGE LOG

PAGE 2: ADD D40
PAGE 2: CHANGE C34-C47
PAGE 2: ADD C100
PAGE 4: ADD C101 C102

MAIN IC



INSTALL OPTIONS:
48V:

UARTSEL =R9-DNI
R10-10K
UART INTERFACE =R15,R13,R14,R16 - DNI
R1,R3,R4,R2 -0OHM
ALERT INTERFACE =R141 - DNI
POWER =J9
EEPROM =THERM1,THERM2 JUMPERS REMOVED
REMOVE R116, R117 TO REDUCE CAPACITIVE LOAD

HV:

UARTSEL =R9-10K
R10-DNI
UART INTERFACE =R15,R13,R14,R16 - 0OHM
R1,R3,R4,R2 -DNI
ALERT INTERFACE =R141 - DNI

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

SCHEMATIC			
HW TYPE : Customer Evaluation Z Product(s): ADES175X_EVKIT_A : NA			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_075909-03	REV A	
PTD ENGINEER P. SHARMA	SIZE D	SCALE 1:1	SHEET 2 OF 5

UART UPPER PORT

REQUESTED FOR 4 PINS LOGICAL SYMBOL

UART LOWER PORT

SPI BUS LEVEL SHIFTER

MINIQ USB HEADERS

HIGH Z MODE UART TX COMPONENTS

UPPER PORT

LOWER PORT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.

SCHEMATIC			
HW TYPE : Customer Evaluation Z Product(s): ADES175X_EVKIT_A : NA			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_075909-03	REV A	
PTD ENGINEER P. SHARMA	SIZE D	SCALE 1:1	SHEET 4 OF 5

