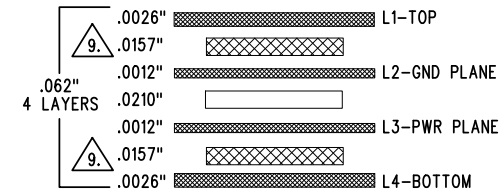


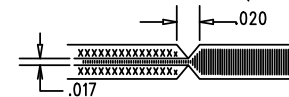
REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	3	PRODUCTION	MARK T.	05-03-18

LAYER STRUCTURE



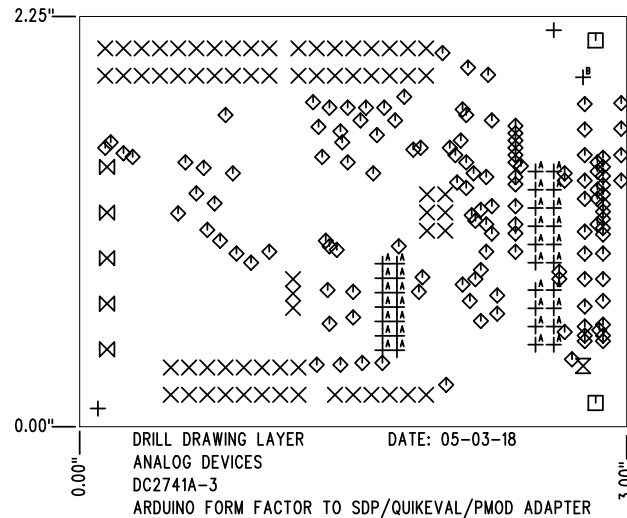
NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.
-FINISHED THICKNESS TO BE 0.062" +/- .005"
-TOTAL OF 4 LAYERS WITH 4 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
-GOLD IMMERSION BOTH SIDES.
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):


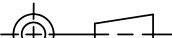


9. SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.

SHOWN FROM TOP SIDE



SIZE	QTY	SYM	PLATED	TOL
0.07	2	+	NO	+/-0.003"
0.035	67	X	YES	+/-0.003"
0.125	2	□	NO	+/-0.003"
0.012	133	◇	YES	+/-0.003"
0.045	1	⊗	NO	+/-0.003"
0.063	5	⊗	YES	+/-0.003"
0.04	34	+ ^A	YES	+/-0.003"
0.03	1	+ ^B	NO	+/-0.003"

UNLESS OTHERWISE SPECIFIED		APPROVALS		<div>ANALOG DEVICES</div> <div>AHEAD OF WHAT'S POSSIBLE™</div>	1630 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-1900 www.analog.com ADI CONFIDENTIAL- FOR CUSTOMER USE ONLY	
DIMENSIONS ARE IN INCHES		PCB DES.	KIM T.		TITLE: FABRICATION DRAWING ARDUINO FORM FACTOR TO SDP/QUIKEVAL/PMOD ADAPTER	
TOLERANCES:		APP ENG.	MARK T.			
0.XX" = ±0.01"						
0.XXX" = ±0.005"						
INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION				SIZE	IC NO.	REV
				N/A	DEMO CIRCUIT 2741A	3
		SCALE = NONE		FILENAME: DC2741A-3.PCB		SHT 1 OF 1