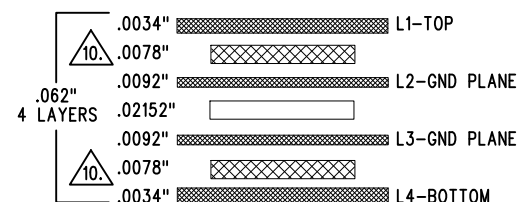


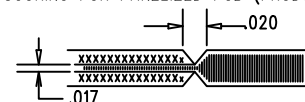
REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	1	1ST PROTOTYPE	CLARENCE M.	03-18-14

LAYER STRUCTURE



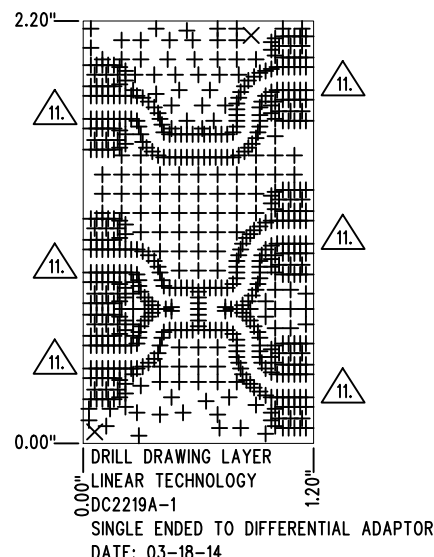
NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, FR-408HR OR EQUIVALENT.
-FINISHED THICKNESS TO BE 0.062" +/- .005"
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
-GOLD IMMERSION BOTH SIDES.
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



- CONTROLLED 50 OHM +/-10% IMPEDANCE FOR LAYERS 1-2 USING 0.03" TRACE.
- SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.
- INNER AND OUTER LAYER COPPER SHALL BE EXPOSED ALONG BOARD EDGES. DO NOT MODIFY INNER LAYER COPPER BACKOFF OUTLINE (SMA CONNECTOR).

SHOWN FROM TOP SIDE



SIZE	QTY	SYM	PLATED	TOL
0.01	608	+	YES	+/-0.003"
0.07	2	X	NO	+/-0.003"

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: 0.XX" = ±0.01" 0.XXX" = ±0.005" INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION	APPROVALS				1630 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-1900 www.linear.com LTC CONFIDENTIAL - FOR CUSTOMER USE ONLY	
	PCB DES.	KIM T.				
	APP ENG.	CLARENCE M.			TITLE: FABRICATION DRAWING	
					SINGLE ENDED TO DIFFERENTIAL ADAPTOR	
					SIZE N/A	IC NO. DEMO CIRCUIT 2219A
		SCALE = NONE	FILENAME: DC2219A-1.PCB		SHT 1 OF 1	REV 1