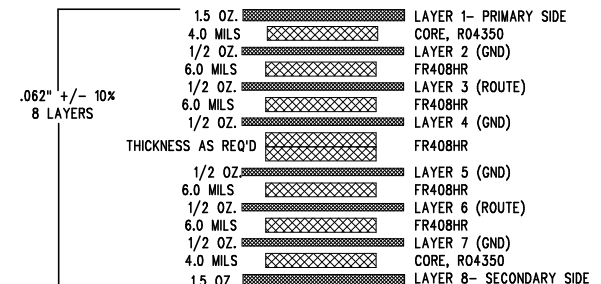




NOTES: UNLESS OTHERWISE SPECIFIED

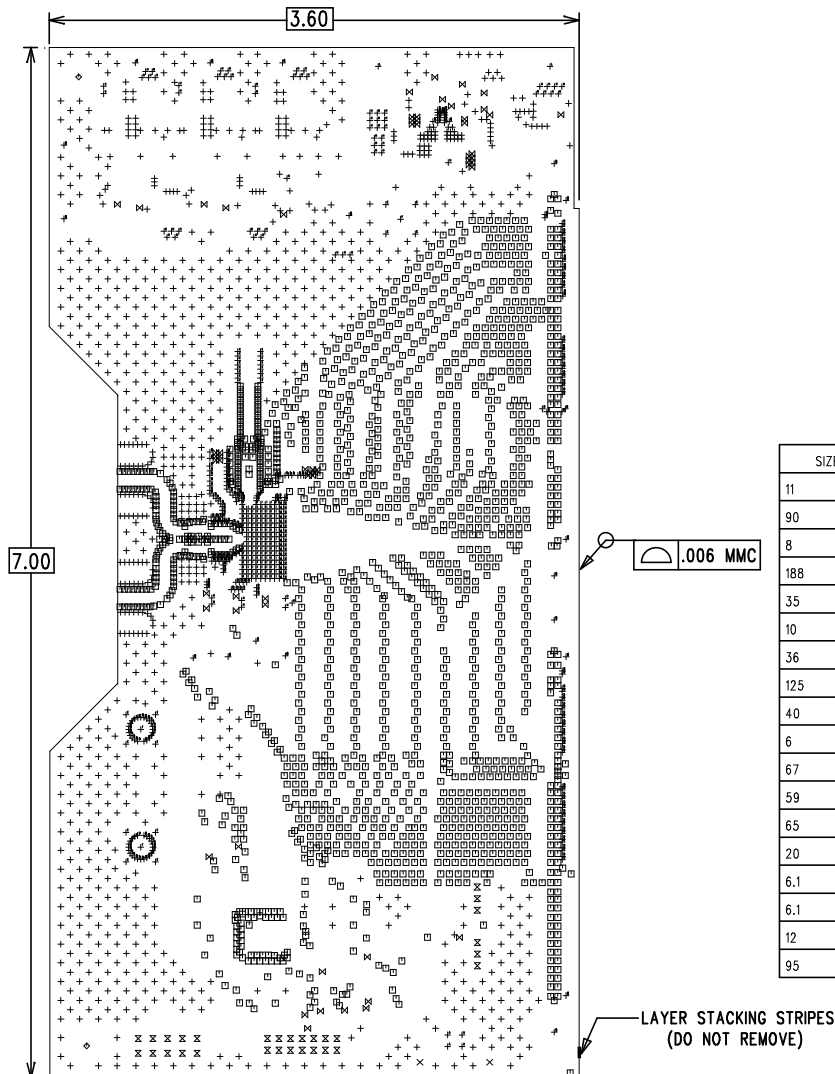
REVISION HISTORY				
ECO	REV	DESCRIPTION	APPR	DATE
—	3	PRODUCTION	CMA/OTT	01-30-14

- FAB PER IPC-A-600.
- MATERIAL: —LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR408HR OR EQUIVALENT.
—FINISHED THICKNESS TO BE 0.062" +/- .005"
—TOTAL OF 8 LAYERS, FINISHED COPPER THICKNESS AS PER FIG.1, "STACKUP DETAILS".
—FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
- DRILLING: —DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
—ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
—HOLE LOCATION TOLERANCES AS FOLLOWS:
3 MILS DIAMETER TRUE POSITION TOLERANCE FOR ALL HOLES
40 MILS DIAMETER OR LESS.
6 MILS DIAMETER TRUE POSITION TOLERANCE FOR ALL OTHER HOLES.
- FINISH: —SMOBC USING LPI BOTH SIDES, COLOR BLACK.
—GOLD IMMERSION BOTH SIDES.
—SILKSCREEN LEGENDS SHALL BE WHITE NON-CONDUCTIVE EPOXY INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
NOTE: MAXIMUM SOLDERMASK CLEARANCE ANNULAR RING FOR U1 BGA PADS SHALL NOT EXCEED 2.5 MILS.
- PCBS ARE TO BE RoHS COMPLIANT.
- BOARDS SHALL BE PANELIZED USING ROUTE AND RETAIN METHOD.
THERE SHALL BE A MINIMUM OF TWO RETAINING TABS ON ALL BOARD EDGES GREATER THAN 2.5 INCHES LONG. ENSURE NO RETAINING TABS ARE PLACED INSIDE PCB EDGES WHERE CONNECTORS J5 AND J6 ARE LOCATED.
- BOARD USES TWO DIFFERENT FIXED IMPEDANCE DESIGN GEOMETRIES AS FOLLOWS:
9.1 ALL 33 MIL WIDE TRACES ON TOP SIDE ARE DESIGNED AS SURFACE MICROSTRIP, AND SHALL HAVE AN IMPEDANCE OF 50 OHMS +/- 10%, MEASURED FROM LAYER 1 TO THE LAYER 4 GROUND PLANE LAYER, AT A FREQUENCY OF 2 GHz.
9.2 DIFFERENTIAL PAIRS ARE ON LAYERS 3 AND 6. TRACES ARE SYMMETRICAL STRIPLINE, AND SHALL HAVE A DIFFERENTIAL IMPEDANCE OF 100 OHMS +/- 10% AT 2GHz.
9.3 HYBRID CONSTRUCTION STACKUP AS PER FIG.1, "STACKUP DETAILS".
- VIA-IN-PAD FOR U1, QTY 166. ALL 6.1 MIL DIA. VIAS SHALL BE IPC4761 TYPE VII, NON-CONDUCTIVE FILLED AND CAPPED VIAS. NOTE THIS INCLUDES 6.1 MIL DIA. BLIND VIAS L1-L3.
- VIAS IN PAD FOR J4, 12 MIL DIA., QTY 12, SHALL BE IPC4761 TYPE VII, NON-CONDUCTIVE FILLED AND CAPPED VIAS.
- ELECTRICAL TEST STAMPS SHALL BE ON SECONDARY SIDE ONLY.

FIG.1 STACKUP DETAILS



UNLESS OTHERWISE SPECIFIED		APPROVALS		 LINEAR TECHNOLOGY 1630 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-1900 www.linear.com LTC CONFIDENTIAL - FOR CUSTOMER USE ONLY	
DIMENSIONS ARE IN INCHES		PCB DES.	M.HAWKINS		
TOLERANCES:		APP ENG.	CLARENCE M.	TITLE: FABRICATION DRAWING	
0.XX" = ±0.01"				LTC2000 HIGH SPEED DAC	
0.XXX" = ±0.005"				SIZE	
INTERPRET DIM AND TOL PER ASME Y14.5M-1994				IC NO. LTC2000-X FAMILY	
THIRD ANGLE PROJECTION				DEMO CIRCUIT 2085A	
				REV	
				3	
		SCALE = NONE		FILENAME: DC2085A-3.PCB	
				SHT 1 OF 1	

LAYER STACKING STRIPES
(DO NOT REMOVE)