

## DESCRIPTION

Demonstration Circuit 609C features the LTC4259A, a quad –48V network power controller designed for use in IEEE802.3af compliant systems. Integrated in a 36-pin SSOP package are four independent channels controlling external N-channel FETs, each with foldback current limiting, inrush current control, fast short-circuit limiting, AC and DC disconnect sense and complete Powered Device (PD) detection and classification capability. DC609C inserts power onto the signal pairs of an existing system to power four IP phones or other PDs. This eliminates the need for an external power source to power the PDs. Should the user find the need to shut off a channel, a momentary shutdown switch for each port disconnects power for the respective port and a Reset switch resets the LTC4259A.

The LTC3803 is used in a boost converter topology to generate a +3.3V supply from the –48V supply for the digital portion of the LTC4259A. The I<sup>2</sup>C interface is

used to configure the LTC4259A and read back status to a host controller. Separate data in and data out I<sup>2</sup>C lines simplify the connection of opto-isolation circuitry. The DC609C is a part of the LTC QuickEval family of Linear Technology demonstration circuits providing a convenient way to interface demonstration circuits with SPI or I<sup>2</sup>C buses with a PC. Up to sixteen LTC4259As, with their own distinct I<sup>2</sup>C address, can be connected in parallel to the bus, allowing for up to 64 controlled channels. The LTC4259A includes an open drain /INT output to drive an Interrupt line for fault detection without the need for software polling. Also powered off of the 3.3V supply is a sine wave oscillator using the LT1498 dual op-amp to generate the 105Hz AC signal required for AC disconnect.

**Design files for this circuit board are available. Call the LTC factory.**

## QUICK START PROCEDURE

Demonstration Circuit 609C is setup for evaluation of the LTC4259A. Please refer to Figure 1 and follow the procedure below for proper operation.

1. Move the AUTO jumper (JP4) to VDD to set the LTC4259A to Auto mode. (To disable Auto mode, move the jumper to the GND position).
2. Select BOARDVDD (JP2) for VDD to be supplied by the VEE power supply.
3. Select BOARDAC (JP5) to drive the LTC4259A OSCIN pin with the on-board AC signal.
4. Tie SDAIN to SDAOUT (JP3) to configure the I<sup>2</sup>C bus as a bi-directional SDA line.
5. Connect the 14-pin ribbon cable to the LTC QuickEval DC590 controller board.
6. Connect the DC590 to a PC via a USB A-B cable and open the QuickEval program for quick evaluation control of the LTC4259A.\*
7. Connect the VEE and GND inputs to a –48V power supply .
8. Connect the PDs to the “Out to PD” side of the board through the RJ45 connectors.

\* The QuickEval system is used for quick interfacing with the LTC4259A. An external host controller can be connected directly to the SDA and SCL lines. The LTC4259A can also run autonomously without the need for a PC or a microcontroller.

# QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 609C

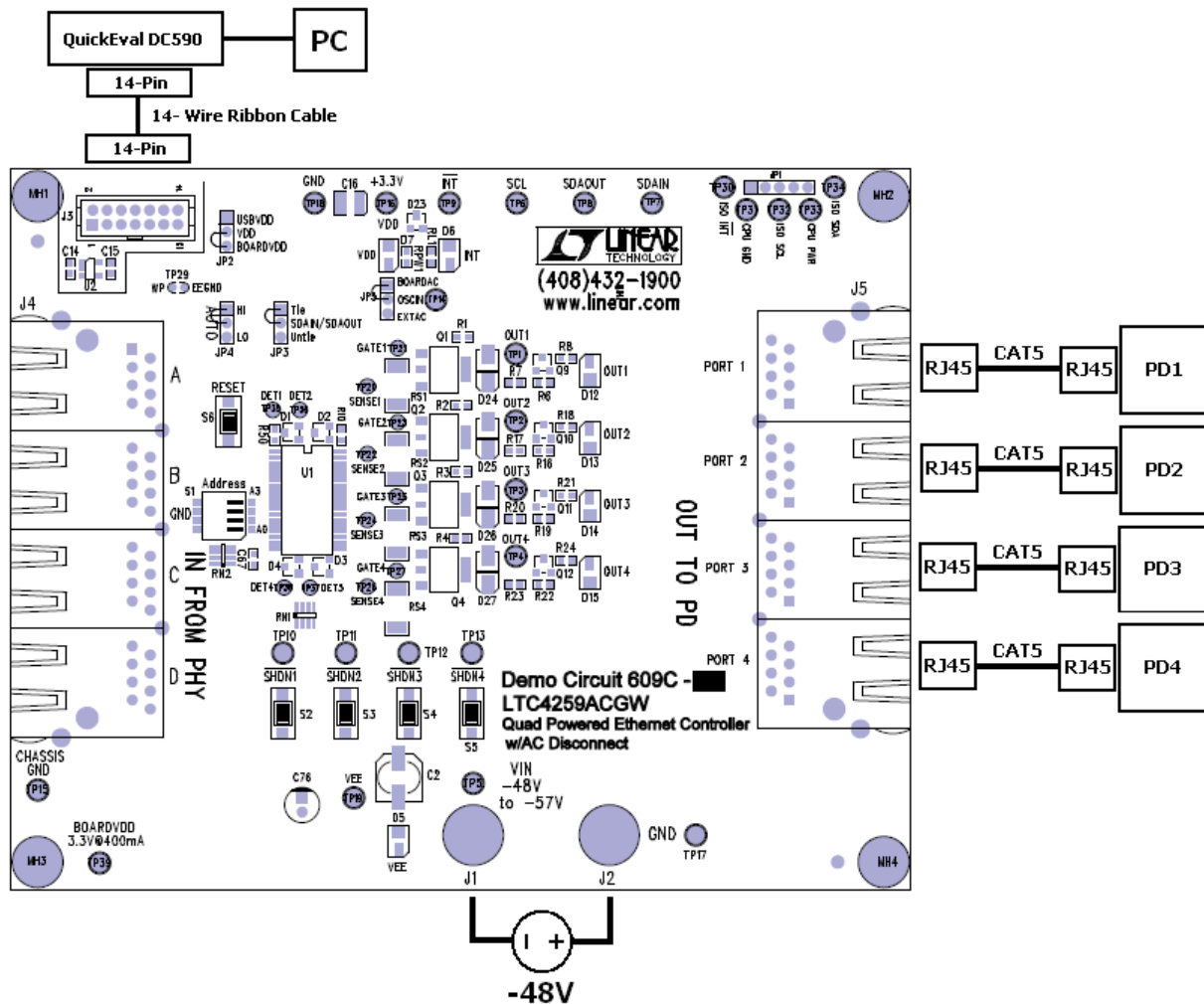


Figure 1. DC609C Quick Setup

## OPERATION

### Introduction

The DC609C demonstrates the LTC4259A IEEE802.3af Power Sourcing Equipment (PSE) controller, capable of fully compliant detection, classification, port powering, and AC and/or DC disconnect. The DC609C provides a quick and simple fully compliant IEEE 802.3af PSE solution requiring only a -48V supply and is capable of working as a stand-alone PSE without the requirement of a host controller. To do this, +3.3V VDD is supplied by the on board boost converter, the LTC4259A is set to Auto mode (Auto pin logic high), and the required AC OSCIN is provided by the on board sine wave source. The LTC4259A will carry out detection at each port and power on a valid PD. The LTC4259A will also disconnect power from the powered on port if the PD is disconnected or no longer maintains the *AC Maintain Power Signature* (MPS).

For additional control, the LTC4259A has 27 accessible internal registers written and read through the I<sup>2</sup>C port. The DC609C options of communicating with the IC are the QuickEval system, direct connection with a host controller to the I<sup>2</sup>C lines, or through opto-couplers. Additional options selected via I<sup>2</sup>C include DC disconnect and Port Classification as well as fully manual control.

Other features of the DC609C are powered on LED indicators for each port, selectable I<sup>2</sup>C address via S1, and reset switches for the LTC4259A and each port.

### Supply Voltages:

Connect -48V to the DC609C. A green LED by VEE will indicate when -39V is exceeded with proper polarity. For normal operation with the LTC4259A and for IEEE802.3af compliance, this VEE should remain within the range of -48V to -57V. Diode D18 protects the DC609C against inadvertent reverse polarity of the 48V supply and is not needed in a final design.

JP2 selects the VDD source, either the on board boost regulator, the QuickEval USB controller or an external 3.3V supply. If BOARDVDD is selected, the VDD pin on the LTC4259A is connected to the output of the LTC3803 -48V to +3.3V DC/DC boost converter on the board. If a QuickEval USB controller is connected from a computer, it can supply the +3.3V to VDD by selecting USBVDD. Leave JP2 open when supplying an external VDD. The green VDD LED indicates VDD is supplied with power.

### Operation Mode:

Each port is configured through the Operation Mode register to one of the four operation modes: Shutdown, Manual, Semiauto, or Auto.

**Shutdown:** Power OFF, Detection and Class OFF

**Manual:** Will not advance between states, manually detect and class

**Semiauto:** Detect and Class but wait for instruction to turn on Power

**Auto:** Detect, Class, Power On Automatically

Port detection and classification are enabled in the internal Detect/Class Enable register. When a port is in Semiauto or Auto mode with both detect and class enabled, detection will detect if a valid PD is present. If one is detected, classification will then determine what power class the device belongs to. A Port will be automatically turned on after a Detect Good if previously set to Auto mode. In Manual mode, a single detect or classification may be stepped through on a port-by-port basis.

### Auto Mode:

The Auto Mode is controlled by JP4 and sets the state of the LTC4259A internal registers after a reset or power on event. The bits are shown in the last two columns of the data sheet register map. The Auto Pin High state is used for automatic detection and power on of a PD without

having to set any configuration. When the Auto pin is tied to ground, the LTC4259A powers up in manual mode and must be setup through its I<sup>2</sup>C interface.

## Endpoint vs. Midspan PSE:

An Endpoint PSE is coincident with a DTE/Router/Switch and provides power across the signal pairs (pairs 1/2 and 3/6) and/or spare pairs (pairs 4/5 and 7/8). The DC609C connects 48V to the center taps of transformers L1 and L2, which distributes the power across the differential lines for each port. The board can be inserted into existing systems by connecting the cable from the DTE/Router/Switch to the “IN FROM PHY” RJ45 connectors on the left side of the board and the PD to the “OUT TO PD” on the right side of the board. Note that the DC609C is configured to provide Endpoint PSE handshaking with a PD.

A Midspan PSE is defined in the IEEE standards as a device that is between the MDIs and can only be configured to supply power on the spare pairs. Power to the spare pairs can be directly connected and does not need to go through transformers. Timing differences between and Endpoint and Midspan PSE are explained in the IEEE standards to avoid conflict between the two should a PD ever be connected at the same time to the two. Contact Applications for information on Midspan back-off timing through hardware or software implementation.

## Powered Devices (PDs):

An IEEE802.3af compatible PD must present a 25K $\Omega$  Signature Resistance and be capable of accepting power on both the spare pairs and the signal pairs. PDs are connected through the RJ45 connectors on the output side (“OUT TO PD”) of the board DC609C. The DC609C ports supply power to lines 1-2 and 3-6. LEDs for each port indicate if the port is on or off.

A valid PD also has the option of signaling its power class. The LTC4259A reads this class and reports to a microcontroller for power management.

## AC Disconnect:

The LTC4259A uses AC disconnect as its default disconnect detection when the Auto pin is high. A PSE that implements the AC disconnect method must maintain power to a port if a maximum of 27k $\Omega$  impedance is seen at the port output. The PSE must remove power if this impedance is greater than 1.98M $\Omega$ . A PD must present an AC MPS of less than 26.25k $\Omega$  to insure it remains on with AC disconnect. Components C1, C61-C63, R5, R13-R15 are connected in parallel with the Detect diodes providing a signal path for AC MPS detection and the S1B diodes are in series with the port output to isolate the AC MPS detection signal when the PD is disconnected. AC disconnect is a sensitive detection and requires strict adherence to the specifications of the Cdetect. Cdetect must be either a 0.47 $\mu$ F - 100V - X7R ceramic capacitor or a 0.22 $\mu$ F - 100V film capacitor. An AC sine wave, nominally 100Hz, 2.2Vpp with a 1.2V offset, must be connected to the OSCIN to drive the AC Disconnect. The circuit with the LT1498, a dual op-amp, is configured to meet these requirements. Select BOARDAC to connect the output of this circuit to OSCIN, or EXTAC to disconnect and allow for an external AC signal to be connected.

## Push Button Switches:

The Reset push button (S6), when pushed, pulls the Reset pin to ground to halt I<sup>2</sup>C communication with the LTC4259A and turn off all ports. Releasing the switch returns the Reset pin high and the internal registers are set to the Reset state values as a function of the Auto Pin state. I<sup>2</sup>C Communication can then be established again with the LTC4259A.

Each output port has its own Shutdown switch (S2-S5) to shutdown power to the port, regardless of its state. Detect and Class are disabled for the port after a PB Shutdown.

## Addressing:

The LTC4259A I<sup>2</sup>C address is programmable over the range of 0100000Y to 0101111Y ('Y' is the read/write bit) by setting address pins A3-A0 high or low through S1. The LTC4259A responds to the I<sup>2</sup>C address 0110000Y regardless of the settings of address pins A3-A0. The SMBus Alert Response Address is 0001100Y.

## I<sup>2</sup>C Bus Lines:

There are three possible ways to connect to the I<sup>2</sup>C bus lines on the DC609C.

### 1) QuickEval

Use the QuickEval system by tying SDAIN and SDAOUT together via JP3, select USBVDD with JP2, and connect the 14-pin ribbon cable from the DC590 board to the DC609C. Open the QuickEval, which will identify the DC609C and bring up the LTC4259A interface on the PC. The QuickEval components are for demonstration purposes only and not needed in the final design.

### 2) Opto-Isolation

DC609C has an opto-isolation circuit to isolate the board's power supply from an I<sup>2</sup>C host. Isolation requirements are defined in the IEEE802.3af standards. Connect to CPU GND, CPU PWR, ISO SCL, and ISO SDA. Set VDD (JP2) to BOARDVDD and untie SDAIN and SDAOUT with JP3.

### 3) Direct I<sup>2</sup>C Connection

SDAIN, SDAOUT, and SCL are accessed through the respective test point turrets. SDAIN and SCL both have 2kOhm pullup resistors to VDD. Tie SDAOUT to SDAIN through JP3 and select BOARDVDD with JP2.

## Interrupt:

The Interrupt pin is accessed by the test turret or opto-isolated through ISO /INT. The Interrupt pin must be enabled, Interrupt mask must be set, and an interrupt must occur for the /INT pin to assert low. A red LED indicates if the /INT has been pulled low. If the /INT pin is cleared, the Interrupt must occur again for the /INT to be triggered again.

## Multiple Boards:

Up to 16 DC609C boards (or LTC4259A's) with distinct I<sup>2</sup>C addresses selected through S1 (A3-A0) can be connected in parallel to evaluate N x 4 ports, where N is the number of boards. Connect from board to board VDD, VEE, GND, SDAOUT, SDAIN, SCL, and /Int. A single LTC3803 DC to DC circuit, LT1498 circuit, and opto-isolation circuit is capable of driving VDD, OSCIN, and the I<sup>2</sup>C lines respectively to sixteen LTC4259As.

## QUICKEVAL INTERFACE

(Refer to Figure 2)

### 1) Write Address:

The address of the LTC4259A first needs to be selected before any commands are sent or received. Address pins 6 through 10 ( $A_3$  to  $A_0$ ) are tied either high or low to assign the address of  $(010A_3A_2A_1A_0)_b$ . All LTC4259As respond to the address of  $(0110000)_b$  regardless of the state of  $A_3$ - $A_0$ . A drop down menu on the interface lists in hexadecimal the LTC4259A acceptable addresses with a write bit in the I<sup>2</sup>C address byte. For example, an address byte with the "All LTC4259As" address and a write bit is  $(01100000)_b$  and translates to  $(60)_h$ . An address byte with a Read bit does not need to be selected; the program will set the read bit when reading from the LTC4259A.

### 2) Register List & Start Poll/Refresh Buttons:

Click on START POLL to initiate a continuous register read out every 500 milliseconds, or REFRESH/SINGLE for a single poll sweep. The poll sequence updates the readout displays throughout the interface. When the poll is running, the START POLL button becomes STOP POLL. Click on the STOP POLL button to stop the poll and make the START POLL button visible again.

During the polling sequence the Read Only and Read/Write registers are read. The read protocol is used for each of the registers to be read ( $\{Start, Address/Write, Ack, Register, Ack, Repeat Start, Address/Read, Ack, Read Data, NACK, Stop\}$ ). In the Register List box the Read registers and their current values are listed.

### 3) Register Send/Clear:

The drop down menu lists all the register names and addresses. The label to the right of the selected register indicates that the register is a Read Only (RO), Read/Write (R/W), Clear on Read (CoR), or Write Only (WO).

If a R/W or WO register is selected, a text box, Send button, and Continuous Send check will appear. Enter the data byte in hexadecimal and click Send to send the data byte to the selected Write register ( $\{Start, Address/Write, Ack, Register, Ack, Data, Ack, Stop\}$ ). The Continuous Send check is enabled when the polling sequence is on and disabled when polling is off. Enter the data in the text box and check the Continuous Send to send that data to the selected write register every poll cycle. Uncheck Continuous Send to stop this event.

For CoR registers, a clear button will be present. Click on this button to clear out the selected register.

### 4) Port Display:

Each port is displayed with its operating mode, detect status, and class status. This display is updated every poll cycle.

The operating mode for the port is displayed first. The mode is set by writing to the Operating Mode register  $(12)_h$  or selecting the mode in the drop down menu.

The Turn ON (Turn OFF) button sets the respective port bit in the Power Enable PB  $(19)_h$  register and powers on or off the port. An indicator on the interface turns green to indicate the power is good at the port and turns red when the port is off.

Reset sets the corresponding Reset Port bit in the Global PB  $(1A)_h$  register and resets the port. The port is turned off if it was on and detect and class are disabled. This is a Pushbutton (PB) bit and will return to zero.

The Detect button and Class button will step a single detection or classification cycle in manual mode or enable in Semioauto or Auto mode. The bits are set in the Detect/Class Restart PB  $(18)_h$  register but returns to zeros.

### 5) Reset/Shutdown All Buttons:

Click on Reset to send data byte  $10_h$  to register  $1A_h$ . This is the same as pushing the external Reset switch on the board.

Click SHDN to turn off and reset all ports by sending data F0h and 0Fh to register 19h and 1Ah respectively.

## 6) Hide/Advanced:

When the form is opened, a basic interface is shown. For more advanced options, click on the “Advanced>>” button. To hide these advanced features, click on “Hide<<”.

## 7) Configurations:

Quick and direct LTC4259A configurations are done here. The Auto High and Auto Low send commands to configure the part as if it was reset with Auto Pin high or low. Register (16h) Timing Configurations are set by selecting the time from each drop down menu for the appropriate timer. DC disconnect, AC disconnect, Classification, and Detect are enabled for each port by checking the boxes. This sets registers (13)h and (14)h, Disconnect Enable and Detect /Class Enable.

## 8) Events:

The RO Events registers are read during each poll cycle and the statuses are displayed. The port numbers next to the first seven events indicate that particular event for that port has occurred. For the supply events, a True or False denotes if an Over Temperature, OSC Fail, VDDUVLO, or VEEUVLO condition has occurred. To clear a particular Events register, click on the adjacent clear button to send a read command to the appropriate CoR register. Even if the register is cleared out, the bits remain set if the event is still present.

## 9) Interrupts:

The interrupt pin is enabled by setting the eighth bit in the Miscellaneous Configuration (17)h register. The bits in the Interrupt Mask (01)h register are set by checking the interrupts. An indicator on the interface is displayed for each of the selected interrupts. If the interrupt is present, the corresponding bit in the Interrupt (00)h register will be set and that indicator will turn on. To assert the Interrupt Pin of the LTC4259A low, the Interrupt Pin must be enabled, an Interrupt Mask bit must be set, and the interrupt condition of the masked bit must occur.

The ARA button sends an SMBus Alert Response Address command. This will read the address of any device that is asserting the Interrupt line low and display the address in hexadecimal. The first 7 MSBs are the address and the LSB bit is a Don't Care. When an address is read, that device is reset and releases the Interrupt line high. If multiple devices are holding the Interrupt line low, the first address found is decided through arbitration. An NF will appear if no devices are found to be holding the Interrupt line low.

The Clear Pin and Clear Ints. buttons set bit 6 and 7 of the Global PB (1A)h register respectively. Clearing the interrupt pin releases the Interrupt pin. Clearing the interrupts releases the Interrupt pin, clears all the Event registers, and the Supply Fault bit in the Supply Status register.

## \* Controller Board (LTC QuickEval Check):

This displays communication information with the USB host controller board and the demo board. A timer is monitoring connection. If the correct DC609C board is not connected or an error in the USB communications has occurred, the program will return to the main QuickEvalWindow.

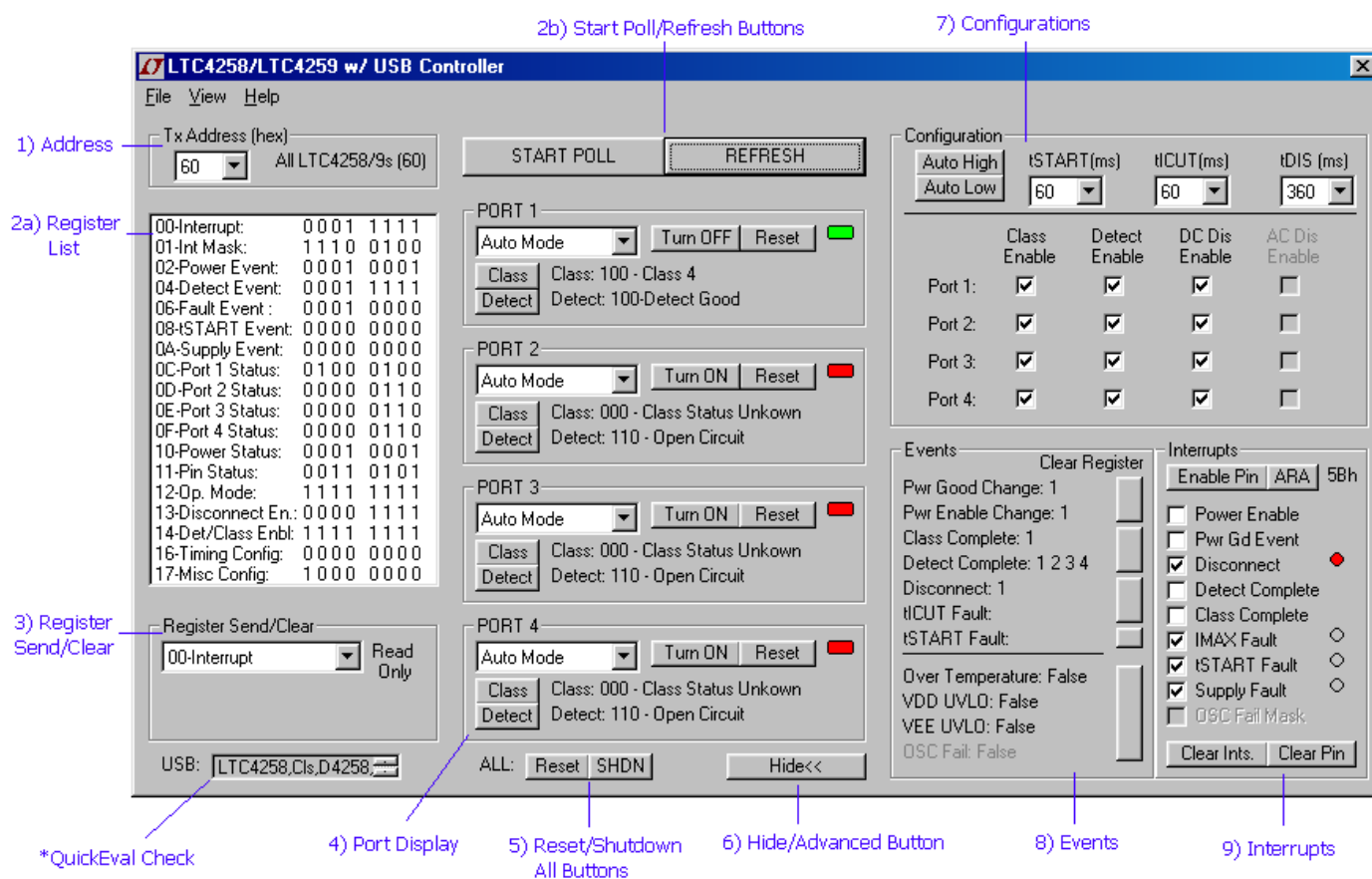
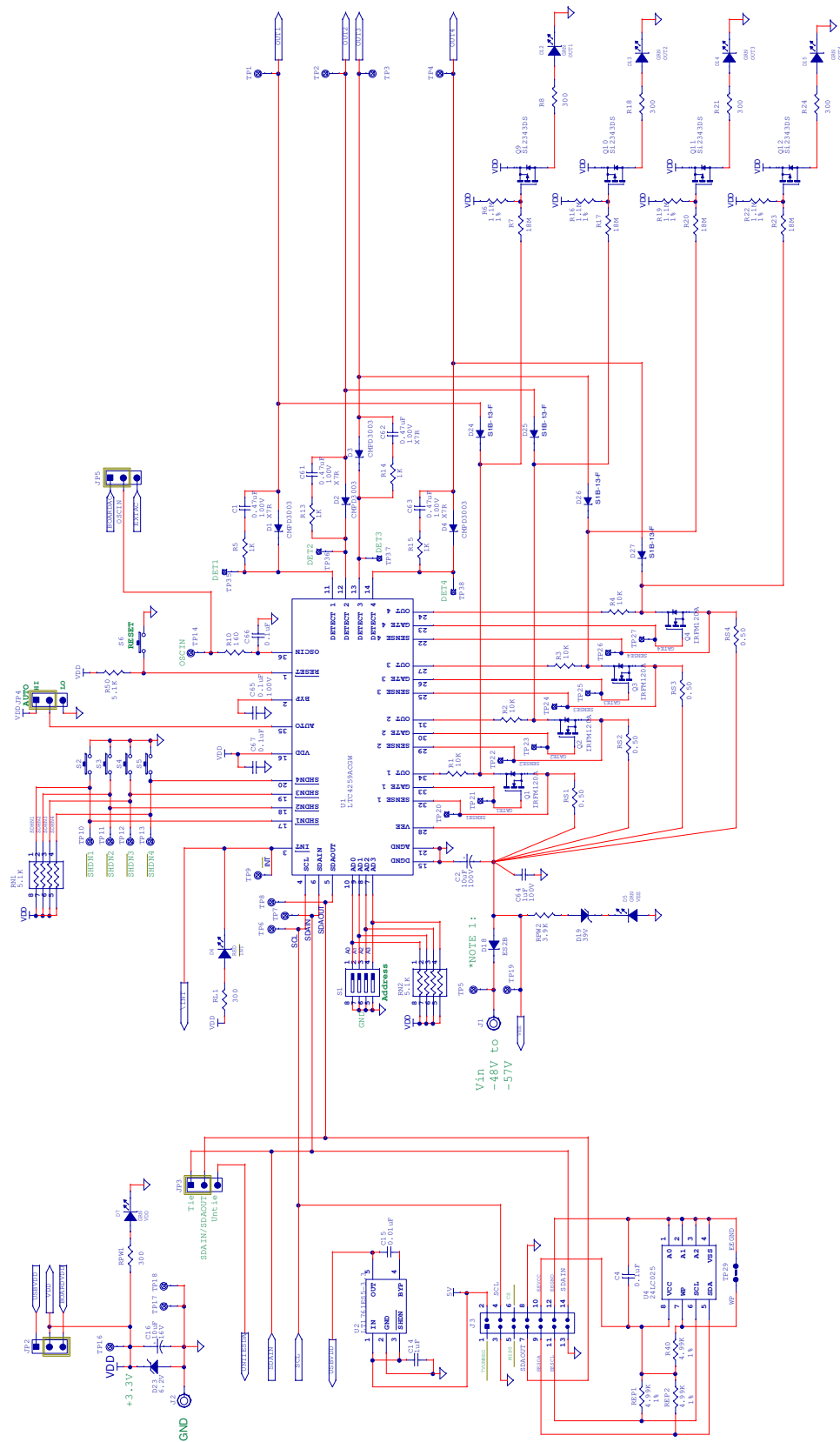


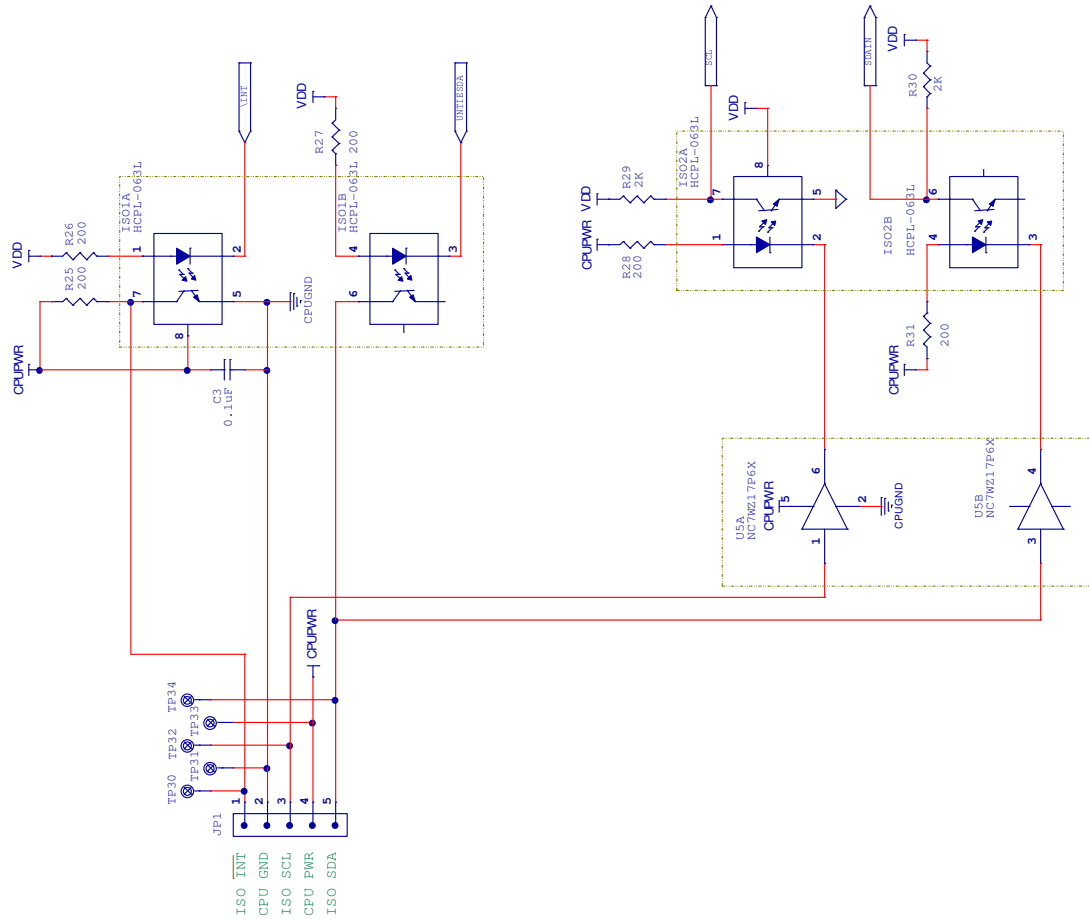
Figure 2. LTC4259A QuickEval Interface

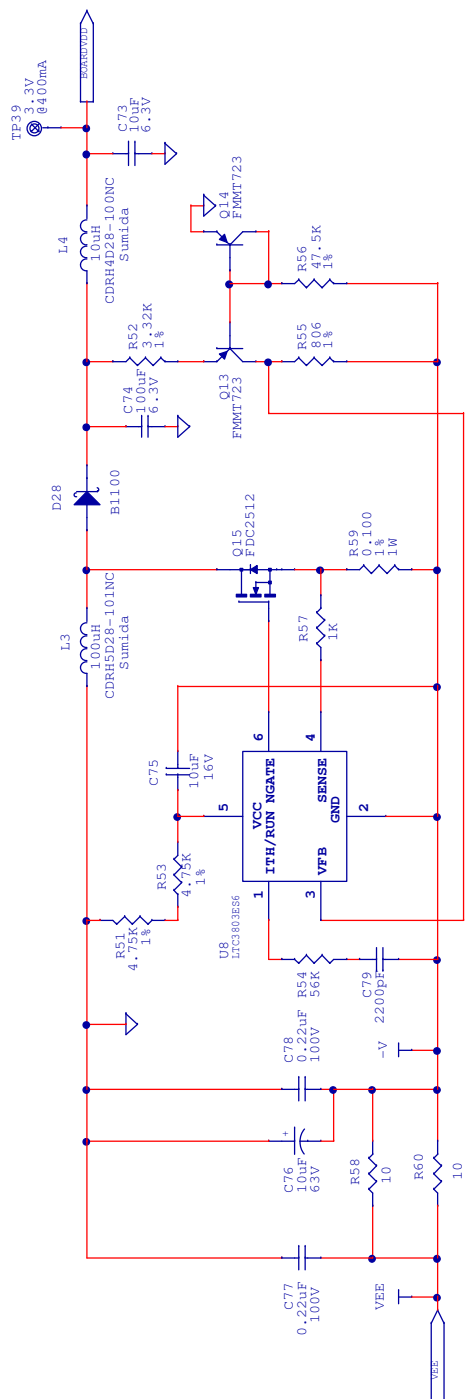


# QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 609C



## OPTIONAL CIRCUIT





# QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 609C

IN  
FROM  
PHY

