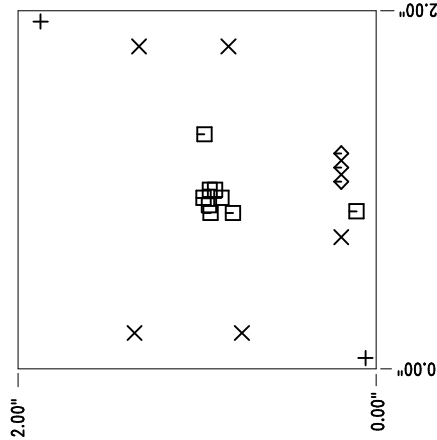
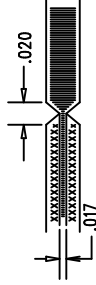



A cross-sectional diagram of a multi-layered structure. The diagram shows four distinct layers. The topmost layer is labeled 'TOP SIDE'. Below it is 'INNER LAYER 2', followed by 'INNER LAYER 3', and the bottommost layer is labeled 'BOTTOM SIDE'. The layers are shown in a perspective view, with the bottom layer being the thickest and the top layer being the thinnest. The layers are separated by thin gaps, and the overall structure is shown in a perspective view.

NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC-A-600.
2. MATERIAL: -EPOXY FIBERGLASS, NEMA GRADE FR-4
-FINISHED THICKNESS TO BE $0.062" \pm .005"$
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS.
AND 1 OZ. CU ON THE INNER LAYERS.
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
4. DRILLING: -DRILL HOLES PER SCHEDULE, PLATE THROUGH
HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE $\pm 0.003"$
IN RELATION TO CENTER
5. FINISH: -SN0BC USING LPI BOTH SIDES, COLOR GREEN.
-GOLD IMMERSION BOTH SIDES.
-LEAD FREE SOLDER CAN BE USED FOR PROTOTYPE)
-FOR SILKSCREEN: USE WHITE NON-CONDUCTIVE INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
7. PCBs ARE TO BE RoHS COMPLIANT.
8. SCORING FOR PANELIZED PCB:



SIZE	QTY	SYM	PLATED	TOL
70	2	+	NO	+/-3
95	5	×	YES	+/-3
10	9	□	YES	+/-3
35	3	◇	YES	+/-3

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: 0.XX" = ± 0.01 " 0.XXX" = ± 0.005 " INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION	APPROVALS			1630 MCRASTY BLVD MILPITAS, CA 95035 PH: (408) 332-1600 WWW.LINEAR.COM LITC CONFIDENTIAL - FOR CUSTOMER USE ONLY
	PCB DES.	JW		
	APP ENG.	MOLLY Z.		
TITLE: FABRICATION DRAWING			40V, 500mA, 2.2MHz BUCK REGULATOR IN 2x2 DFN	
	SIZE	IC NO.	LT3502AEDC	REV
	N/A		DEMO CIRCUIT 1099B	1
SCALE = NONE			FILENAME: 1099B-1PCB	SHT 1 OF 1
