ADRV9029 SOFTWARE RELEASE NOTES SW5.1.0.27

BUILD TYPE: **RELEASE**

RELEASE DATE: **JANUARY 22, 2020**

INCLUDED DELIVERABLES:

ARM Firmware Revision: **5.1.0.9**
Gain Tables Revision: **5.1.0.2**
API Revision: **5.1.0.21**
GUI Revision: **5.1.0.30**
(NOTE: Stream files must be generated from the GUI for the selected profile as they are use case dependent.)

PREVIOUS BUILD: **5.0.1.17**
(NOTE: This is the reference baseline for all changes outlined in this document.)

SUPPORTED USE CASES: **UC13-NLS, UC14-LS, UC14-NLS, UC14C-LS, UC26C-LS, UC26C-NLS, UC49-NLS, UC50-NLS, UC51-LS, UC51-NLS, UC51C-LS, UC51C-NLS, UC54-NLS, UC55-NLS, UC59-LS, UC61-LS, UC83C-LS, UC90-NLS, UC93C-LS, UC93C-NLS, UC95C-LS, UC95C-NLS, UC98-LS, UC98-NLS**

INIT CALIBRATION:

The following calibrations were enabled during software verification for this release.

Init Calibration	Enabled	Init Calibration	Enabled	Init Calibration	Enabled	Init Calibration	Enabled
RESERVED		HD2 Init		Rx LO Delay		Loopback Rx DC Offset	X
RESERVED		RESERVED		Loopback Rx QEC Init		ORx DC Offset	X
CFR Init	X	Closed Loop Gain Control Init	X	Loopback Rx LO Delay	X	Rx DC Offset	X
RESERVED		DPD Init	X	Tx QEC Init	X	Loopback Rx TIA Filter	X
Rx Gain Phase	X	Tx DAC Init	X	Tx LO Leakage External Init	X	ORx TIA Filter	X
Rx Gain Delay	X	ORx QEC Init	X	Tx LO Leakage Init	X	Rx TIA Filter	X
Tx Atten Table Linearization	X	ORx LO Delay		Path Delay	X	ADC Tuner	X
Tx Atten Delay	X	Rx QEC Init	X	ADC Flash	X	Tx Baseband Filter	X

OVERVIEW

The SW5.1.0.27 release build provides updates in the ARM firmware, stream files, API, and GUI software to support ADRV9029. Changes outlined in this document are relative to the previous release build listed above. The updates included in this build are:

- Initial broad market release for ADRV9029 device.

The following sections describe the changes and enhancements provided in this build.

API CHANGES

1. Update for adi_adrv9025_CpuCmdStatusOpcodeGet to check the correct bits for Stream opcode.
2. Added use cases: UC51C-NLS for NP 12 and 16, UC51C-LS for NP 12 and 16. The following 2T2R profiles are also added (profile naming indicates specific Tx/Rx channels utilized):
   - UC90-NLS TX1TX2, RX1RX2
   - UC51-NLS TX1TX2, RX1RX2
   - UC51-NLS TX1TX2, RX3RX4
   - UC13-NLS TX1TX2, RX1RX2
   - UC59-NLS TX1TX2, RX3RX4
3. Resolved memory issue of adcProfileLut definitions occupying large amounts of stack memory.
4. Added new API to enable sysref timing debug –
   - API uses both clock and 9025 device and is contained in adi_device_share.c
   - adi_device_share_setupHoldMonitorTimingBlock returns two arrays of hold and setup words which can be used to tell if sysref is meeting timing requirements with respect to devclk for a given coarse or fine clock adjustment.

ARM FIRMWARE CHANGES

Channel Setup

1. Updated ARM calculations to avoid any precision loss when calculating Rx NCO frequency tuning word from desired frequency offset.

Calibrations

No changes

GUI CHANGES

1. Resolved GUI issues with certain JESD204C profiles not programming successfully.
2. Removed additional commas at end of arrays and enums in generated initData files.
3. Fix to ensure initData files are generated correctly for all product numbers.

STREAM CHANGES

1. The ORx high stream was changed slightly alter the TIA power up sequence - this improves TIA robustness over temperature.

KNOWN ISSUES/LIMITATIONS

1. AUX LO operation is not supported for 2T4R profiles.
2. Slightly degraded Tx QEC calibration performance was seen for Tx3 channel. This is currently being investigated.
3. When a large tone appears near the RX/ORX band edge, ADI has occasionally observed reduced RX/ORX QEC performance.
4. RX/ORX QEC tracking convergence time may be impacted when a large tone is present near DC.
5. TX LOL can degrade with signals close to DC when using a 100 µs subframe duration.
6. TX LOL can degrade slightly when testing with CW signals at specific frequencies – no issue observed with modulated signals.
7. This software version has not been fully verified for operation with LO frequencies from 75MHz – 600MHz. This operation will be fully verified in an upcoming release version.

ADDITIONAL INFORMATION

1. The API command ***adi_adrv9025_DpdModelConfigSet()*** supports programming a DPD model with a maximum of 190 coefficients for 200MHz DPD applications.
2. A user defined macro **ADI_ADRV9025_MAX_DPD_FEATURES** has been included in adi_adrv9025_user.h, which specifies the maximum no. of DPD coefficients supported. By default, **ADI_ADRV9025_MAX_DPD_FEATURES** is set to 190. This macro needs to be modified by the user.

3. The user should integrate ARM-D (ADRV9025_DPDCORE_FW.bin) along with the default ARM-C (ADRV9025_FW.bin) to ensure successful boot up. This is required even if not using ADI internal DPD.
4. The user is advised to optimize the LEMC/LMFC offset for the deframer to get the correct data and deterministic latency. The user can refer to SELECTING THE OPTIMAL LMFC/LEMC OFFSET FOR A ADRV902X DEFRAMER section in the user guide for detailed information on sweeping the LEMC/LMFC offset for ADRV902X.
5. ADI recommends setting ORx Attenuation to 10dB at higher LO frequencies, to take advantage of the LO leakage algorithm's rejection of coupling.
6. Tracking cals should be disabled prior to changing LO frequency.
7. Customers should add adi_adrv9025_PllLoopFilterSet in their startup sequence immediately before adi_adrv9025_PostMcsInit to set the loop filter bandwidth to 600 kHz.
8. It is recommended that customers run the external TX LOL init calibration. When running init calibrations, be sure to disable all tracking calibrations.

SUPPORTED USE CASES

The following use cases are included in this software package. For a list of verified use cases, see the Supported Use Cases list on page 1 of this document.

Use Case	Np Value		Tx Channels			ORx Channels			Rx Channels			JESD Lane Rate (Gpbs)
	Tx	Rx/ Orx	BW (MHz)	Data Rate (MSPS)	Channels	BW (MHz)	Data Rate (MSPS)	Channels	BW (MHz)	Data Rate (MSPS)	Channels	
13-NLS	16	16	100/225	245.76	4	225	245.76	2	100	122.88	4	9.8304
14-LS	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	14.7
14-NLS	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	14.7
14C-LS	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	24.3302
26C-LS	16	16	200/450	491.52	4	450	491.52	2	200	245.76	4	16.2202
26C-NLS	16	16	200/450	491.52	4	450	491.52	2	200	245.76	4	16.2202
49-NLS[1,2]	16	16	200/450	245.76	4	450	491.52	2	100	122.88	4	9.8304
50-NLS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	100	122.88	4	9.8304
51-LS[1,3,4]	16	16	200/450	245.76	4	450	245.76	2	200	245.76	4	9.8304
51C-LS[1,3,4]	16	16	200/450	245.76	4	450	245.76	2	200	245.76	4	16.2202
51C-LS-Np12[1,3,4]	12	12	200/450	245.76	4	450	245.76	2	200	245.76	4	12.165
51-NLS[1,3,4]	16	16	200/450	245.76	4	450	245.76	2	200	245.76	4	9.8304
51C-NLS[1,3,4]	16	16	200/450	245.76	4	450	245.76	2	200	245.76	4	16.2202
51C-NLS-Np12[1,3,4]	12	12	200/450	245.76	4	450	245.76	2	200	245.76	4	12.165
54-NLS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	200	122.88	4	9.8304
55-NLS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	160	122.88	4	9.8304
59-NLS[1,2]	16	16	200/450	250	4	450	250	2	200	250	4	10
59-LS[1,2]	16	16	200/450	250	4	450	250	2	200	250	4	10
61-LS	12	12	200/300	368.64	4	300	368.64	2	200	368.64	4	11.0592
83C-LS	16	16	200/337	368.64	4	337	368.64	2	200	368.64	4	24.3302
90-NLS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	100	122.88	4	4.9152
93C-LS*	12	24	200/450	491.52	4	450	491.52	2	300	245.76	4	24.3302
93C-NLS*	12	24	200/450	491.52	4	450	491.52	2	300	245.76	4	24.3302
95C-LS*	16	16	200/450	491.52	4	450	491.52	2	300	245.76	4	16.2202
95C-NLS*	16	16	200/450	491.52	4	450	491.52	2	300	245.76	4	16.2202
98-LS*	12	12	200/450	491.52	4	450	491.52	2	300	245.76	4	14.7
98-NLS*	12	12	200/450	491.52	4	450	491.52	2	300	245.76	4	14.7

Notes: LS = Link Sharing; NLS = Non-Link Sharing

[1] DPD specific profile

[2] Internal DPD actuator rate is 491.52 MSPS (DPD HB enabled)

[3] Internal DPD actuator rate is 983.04 MSPS (DPD HB enabled)

[4] DPD x4 HB enabled

Additional Note: Other use cases not included in the above table may be present in the build package – these use cases have not been verified by ADI and there is no guarantee of operation/performance.

* These profiles exceed the datasheet maximum bandwidth specification and therefore may not meet all datasheet performance specs.