REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 19-06-11	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, 3 kV RMS, SIGNAL AND POWER ISOLATED, CAN TRANSCEIVER FOR CAN FD, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/19604**
	REV	**PAGE** 1 **OF** 20

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AMSC N/A

5962-V049-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3 kV RMS, signal and power isolated, controller area network (CAN) transceiver for CAN flexible data rate (FD) microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19604	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADM3057E-EP	3 kV RMS, signal and power isolated, CAN transceiver for CAN FD

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MS-013-AC	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V to +6 V
Input offset voltage (VIO)	-0.5 V to +6 V
Logic side input/output: TXD, RXD, AUX_{IN}, SILENT, STBY	-0.5 V to V_{IO} + 0.5 V
CANH, CANL	-40 V to +40 V
AUX_{OUT}, RS	-0.5 V to V_{ISOIN} + 0.5 V
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature range (TJ)	150°C maximum
Power dissipation (P_D)	(T_J maximum – T_A) / θ_{JA}
Electrostatic discharge (ESD) rating:	
IEC 61000-4-2, CANH/CANL	
Across isolation barrier to GND_1	±8 kV
Contact discharge to GND_2	±8 kV
Air discharge to GND_2	±15 kV
Human body model (HDM) all pins, 1.5 kΩ, 100 pF	4 kV
Moisture sensitivity level (MSL)	MSL3
Thermal resistance, junction to ambient (θ_{JA})	53°C/W

1.4 Recommended operating conditions. 3/

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Operating free-air temperature range (T_A)	-55°C to +105°C

1.5 Package characteristics.

Resistance (input to output) (R_{I-O})	10^{13} Ω typical 4/
Capacitance (input to output) (C_{I-O}) with f = 1 MHz	3.7 pF typical 4/
Input capacitance (C_I)	4.0 pF typical 5/

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Unless otherwise specified, pin voltage with respect to GND, are on the same side.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
4/ The device is considered a 2-terminal device: pin 1 through pin 10 are shorted together, and pin 11 through pin 20 are shorted together.
5/ Input capacitance is from any input data pin to ground.

2. APPLICABLE DOCUMENTS

International Electrotechnical Commission

IEC 61000-4-2 – Electromagnetic Compatibility (EMC) - Part 4-2:
Testing and measurement techniques - Electrostatic discharge immunity test

(Copies of these documents are available online at https://www.iec.ch.)

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figures 4 through 10.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current							
Logic side power current	I_{CC}						
Standby		STBY high, AUX_{IN} low, load resistance (R_L) = 60 Ω	+25°C	01	13.5 typical		mA
			-55°C to +105°C			30	
Recessive state (or) silent		TXD and/or SILENT high, R_L = 60 Ω	+25°C	01	27 typical		mA
			-55°C to +105°C			40	
Dominant state		Fault condition, R_L = 60 Ω	+25°C	01	180 typical		mA
			-55°C to +105°C			260	
70% dominant / 30% recessive		1 Mbps	+25°C	01	138 typical		mA
		5 Mbps	+25°C		151 typical		
			-55°C to +105°C			200	
		12 Mbps	+25°C		177 typical		
			-55°C to +105°C			220	
Switching frequency	f_{OSC}	Frequency hopping center	+25°C	01	180 typical		MHz
Logic side coupler current							
Normal mode		TXD high, low or switching, AUX_{IN} low	+25°C	01	3.6 typical		mA
			-55°C to +105°C			5	
Standby mode		STBY mode	+25°C	01	1.2 typical		mA
			-55°C to +105°C			2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver							
Differential outputs		See figure 4					
Recessive state, normal mode.		TXD high, R_L and common mode filter capacitor (C_F) open					
CANH, CANL voltage	V_{CANL}, V_{CANH}		-55°C to +105°C	01	2.0	3.0	V
Differential output voltage	V_{OD}		-55°C to +105°C	01	-500	+50	mV
Dominant state, normal mode.		TXD and silent low, C_F open					
CANH voltage	V_{CANH}	50 Ω ≤ R_L ≤ 65 Ω	-55°C to +105°C	01	2.75	4.5	V
CANL voltage	V_{CANL}	50 Ω ≤ R_L ≤ 65 Ω	-55°C to +105°C	01	0.5	2.0	V
Differential output voltage	V_{OD}	50 Ω ≤ R_L ≤ 65 Ω	-55°C to +105°C	01	1.5	3.0	V
		45 Ω ≤ R_L ≤ 70 Ω			1.4	3.3	
		R_L = 2240 Ω			1.5	5.0	
Standby mode.		STBY high, R_L and C_F open					
CANH, CANL voltage	V_{CANL}, V_{CANH}		-55°C to +105°C	01	-0.1	+0.1	V
Differential output voltage	V_{OD}		-55°C to +105°C	01	-200	+200	mV
Output symmetry (V_{ISOIN} – V_{CANH} – V_{CANL})	V_{SYM}	R_L = 60 Ω, C_F = 4.7 nF, RS low	-55°C to +105°C	01	-0.55	+0.55	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver - continued							
Short circuit current	$\|I_{SC}\|$	R_L open					
Absolute CANH		V_{CANH} = -3 V	-55°C to +105°C	01		115	mA
Absolute CANL		V_{CANL} = 18 V	-55°C to +105°C	01		115	mA
Steady state CANH		V_{CANH} = -24 V	-55°C to +105°C	01		115	mA
Steady state CANL		V_{CANL} = 24 V	-55°C to +105°C	01		115	mA
Logic inputs (TXD, SILENT, STBY, AUX_{IN})							
Input voltage, high	V_{IH}		-55°C to +105°C	01	0.65 x V_{IO}		V
Input voltage, low	V_{IL}		-55°C to +105°C	01		0.35 x V_{IO}	V
Complementary metal oxide semiconductor (CMOS) logic input currents	$\|I_{IH}\|$, $\|I_{IL}\|$	Input high or low	-55°C to +105°C	01		10	µA
Receiver							
Differential inputs							
Differential input voltage range	V_{ID}	C_{RXD} open, see figure 5, -25 V < V_{CANL}, V_{CANH} < +25 V					
Recessive			-55°C to +105°C	01	-1.0	+0.5	V
		STBY high			-1.0	+0.4	
Dominant			-55°C to +105°C	01	0.9	5.0	V
		STBY high			1.15	5.0	
Input voltage hysteresis	V_{HYS}		+25°C	01	150 typical		mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver – continued.							
Differential inputs – continued.							
Unpowered input leakage current	$\|I_{IN(OFF)}\|$	V_{CANH}, V_{CANL} = 5 V, V_{CC} = 0 V	-55°C to +105°C	01		10	µA
Input resistance, CANH, CANL	R_{INH}, R_{INL}		-55°C to +105°C	01	6	25	kΩ
Input resistance, differential	R_{DIFF}		-55°C to +105°C	01	20	100	kΩ
Input resistance, matching	m_R	$m_R = 2 \times (R_{INH} - R_{INL}) / (R_{INH} + R_{INL})$	-55°C to +105°C	01	-0.03	+0.03	Ω/Ω
Input capacitance, CANH, CANL	C_{INH}, CR_{INL}		+25°C	01	35 typical		pF
Input capacitance, differential	C_{DIFF}		+25°C	01	12 typical		pF
Logic outputs (RXD, AUX_{OUT})							
Output voltage, low	V_{OL}	Output current (I_{OUT}) = 2 mA	+25°C	01	0.2 typical		V
			-55°C to +105°			0.4	
Output voltage, high RXD	V_{OH}	I_{OUT} = -2 mA	-55°C to +105°C	01	V_{IO} – 0.2		V
Output voltage, high AUX_{OUT}	V_{OH}	I_{OUT} = -2 mA	-55°C to +105°C	01	+2.4		V
Short circuit current RXD	I_{OS}	Output voltage (V_{OUT}) = GND_1 or V_{IO}	-55°C to +105°C	01	7	85	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Common mode transient immunity. 3/ Common mode voltage (V_{CM}) ≥ 1 kV, transient magnitude ≥ 800 V							
Input high, recessive	$\|CM_H\|$	V_{IN} = V_{IO} (AUX_{IN}, TXD) or CANH/CANL recessive	+25°C	01	100 typical		kV/μs
			-55°C to +105°		75		
Input high, dominant	$\|CM_L\|$	V_{IN} = 0 V (AUX_{IN}, TXD) or CANH/CANL dominant	+25°C	01	100 typical		kV/μs
			-55°C to +105°		75		
Slope control							
Input voltage for standby mode	V_{STB}		-55°C to +105°	01	4.0		V
Current for slope control mode	I_{SLOPE}	RS voltage (V_{RS}) = 0 V	-55°C to +105°	01		-240	μA
Slope control mode voltage	V_{SLOPE}	RS current (I_{RS}) = 10 μA	-55°C to +105°	01	2.1		V
Input voltage for high speed mode	V_{HS}		-55°C to +105°	01		1	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications							
Driver	SILENT low, bit time on the TXD pin as transmitted by the CAN controller (t_{BIT_TXD}) = 200 ns, see figure 6 and figure 7, slope resistance (R_{SLOPE}) = 0 Ω, R_L = 60 Ω, load capacitance (C_L) = 100 pF						
Maximum data rate			-55°C to +105°	01	12		Mbps
Propagation delay from TXD to bus (Recessive to Dominant)	t_{TXD_DOM}		+25°C	01	35 typical		ns
			-55°C to +105°			60	
Propagation delay from TXD to bus (Dominant to Recessive)	t_{TXD_REC}		+25°C	01	46 typical		ns
			-55°C to +105°			70	
Transmit dominant timeout	t_{DT}	TXD low, see figure 8	-55°C to +105°	01	1175	4000	μs
Receiver	SILENT low, see figure 6 and figure 7, R_L = 60 Ω, C_L = 100 pF, RXD capacitance (C_{RXD}) = 15 pF						
Falling edge loop propagation delay (TXD to RXD), full speed mode	t_{LOOP_FALL}	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns	-55°C to +105°	01		150	ns
Falling edge loop propagation delay (TXD to RXD), slope control mode	t_{LOOP_FALL}	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 μs	-55°C to +105°	01		300	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications – continued.							
Receiver – continued.	SILENT low, see figure 6 and figure 7, R_L = 60 Ω, C_L = 100 pF, RXD capacitance (C_{RXD}) = 15 pF						
Rising edge loop propagation delay (TXD to RXD), full speed mode	t_{LOOP_FALL}	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns	-55°C to +105°	01		150	ns
Rising edge loop propagation delay (TXD to RXD), slope control mode	t_{LOOP_RISE}	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 µs	-55°C to +105°	01		300	ns
Loop delay symmetry (minimum recessive bit width)		2 Mbps, t_{BIT_TXD} = 500 ns	-55°C to +105°	01	450	550	ns
		5 Mbps, t_{BIT_TXD} = 200 ns			160	220	
		8 Mbps, t_{BIT_TXD} = 125 ns			85	140	
		12 Mbps, t_{BIT_TXD} = 83.3 ns			50	91.6	
CANH, CANL slew rate	|SR|	SILENT low, see figure 7, R_L = 60 Ω, C_L = 100 pF, R_{SLOPE} = 47 kΩ	+25°C	01	7 typical		V/µs
Standby mode							
Minimum pulse width detected (receiver filter time)	t_{FILTER}	STBY high, see figure 9	-55°C to +105°	01	1	5	µs
Wake up pattern detection reset time	t_{WUPR}	STBY high, see figure 9	-55°C to +105°	01	1175	4000	µs
Normal mode to standby mode time	t_{STBY_ON}		-55°C to +105°	01		25	µs
Standby mode to normal mode time	t_{STBY_OFF}	Time until RXD valid	-55°C to +105°	01		25	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

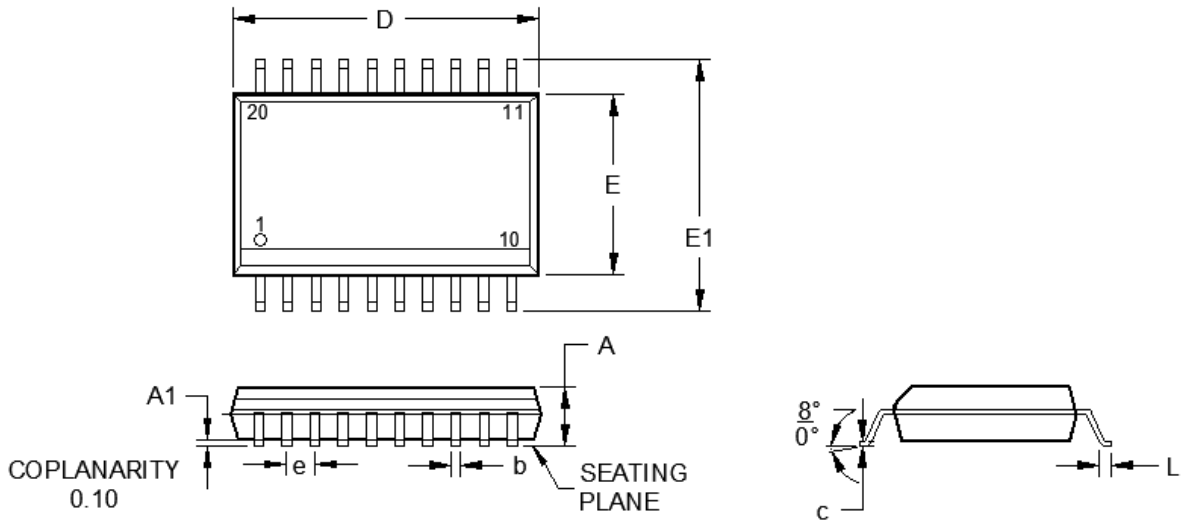
Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications – continued.							
Auxiliary signal							
Maximum switching rate	f_{AUX}		-55°C to +105°	01	20		kHz
AUX_{IN} to AUX_{OUT} propagation delay	t_{AUX}		-55°C to +105°	01		25	µs
Silent mode							
Normal mode to silent mode time	t_{SILENT_ON}	TXD low, R_{SLOPE} = 0 Ω, see figure 10	+25°C	01	40 typical		ns
			-55°C to +105°			100	
Silent mode to normal mode time	t_{SILENT_OFF}	TXD low, R_{SLOPE} = 0 Ω, see figure 10	+25°C	01	50 typical		ns
			-55°C to +105°			100	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, all voltages are relative to their respective ground. 4.5 V ≤ V_{CC} ≤ 5.5 V, 1.7 V ≤ V_{IO} ≤ 5.5 V, −55°C ≤ T_A ≤ +105°C, and STBY low. Unless otherwise specified, typical specifications are at V_{CC} = V_{IO} = 5 V and T_A = 25°C.

3/ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining AUX_{OUT} ≥ 2.4 V, CANH/CANL recessive, or RXD ≥ V_{IO} − 0.2 V. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining AUX_{OUT} ≤ 0.4 V, CANH/CANL dominant, or RXD ≤ 0.4 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Case X



Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	.0925	.1043	2.35	2.65
A1	.0039	.0118	0.10	0.30
b	.0122	.0201	0.31	0.51
c	.0079	.0301	0.20	0.33
D	.4961	.5118	12.60	13.00
e	.0500 BSC		1.27 BSC	
E	.2913	.2992	7.40	7.60
E1	.3937	.4193	10.00	10.65
L	.0157	.0500	0.40	1.27

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-013-AC.

FIGURE 1. Case outline.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	GND_1	Ground, logic side.
2	GND_1	Ground, logic side.
3	V_{CC}	Power supply, 4.5 V to 5.5 V. This pin requires 0.1 μF and 10 μF decoupling capacitors.
4	V_{IO}	Coupler power supply, 1.7 V to 5.5 V. This pin requires 0.01 μF and 0.1 μF decoupling capacitors.
5	RXD	Receiver output data
6	SILENT	Silent mode select with input high. Bring this input low or leave the pin unconnected (internal pull down) for normal mode.
7	TXD	Driver input data. This pin has a weak internal pull-up resistor to V_{IO}.
8	STBY	Standby mode select with input high. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
9	AUX_{IN}	Auxiliary channel input. This pin sets the AUX_{OUT} output.
10	GND_1	Ground, logic side.
11	GND_2	Ground, bus side.
12	RS	Slope control pin. Short this pin to ground for full speed operation or use a weak pull-down resistor (for example, 47 kΩ) for slope control mode. An input high signal places the CAN transceiver in standby mode.
13	CANL	CAN low input/output.
14	CANH	CAN high input/output.
15	GND_2	Ground, bus side.
16	V_{ISOIN}	Isolated power supply input for the CAN transceiver bus side digital isolator. This pin requires 0.01 μF and 0.1 μF decoupling capacitors.
17	AUX_{OUT}	Isolated auxiliary channel output. The state of AUX_{OUT} is latched when STBY is high. By default, AUX_{OUT} is low at startup or when V_{IO} is unpowered.
18	GND_{ISO}	Ground for the isolated DC-to-DC converter. Connect these pins together through one ferrite bead to PCB ground (bus side).
19	V_{ISOOUT}	Isolated power supply output. This pin requires 0.22 μF and 10 μF capacitors to GND_{ISO}. Connect this pin through a ferrite bead and short the PCB trace to V_{ISOIN} for operation.
20	GND_{ISO}	Ground for the isolated DC-to-DC converter. Connect these pins together through one ferrite bead to PCB ground (bus side).

FIGURE 2. Terminal connections.

Power		Inputs 1/ 2/					Mode	Output 2/		Input/Output
V_{CC}	V_{IO}	TXD	SILENT	STBY	AUX_{IN}	RS		RXD 3/	AUX_{OUT}	CANH/CANL
On	On	Low	Low	Low	Low	Low/ pull-down	Normal/ slope mode	Low	Low	Dominant 4/
On	On	Low	Low	Low	High	Low/ pull-down	Normal/ slope mode	Low	High	Dominant 4/
On	On	High	Low	Low	Low	Low/ pull-down	Normal/ slope mode	High/per bus	Low	Recessive/set by bus
On	On	High	Low	Low	High	Low/ pull-down	Normal/ slope mode	High/per bus	High	Recessive/set by bus
On	On	X	High	Low	Low	X	Listen only	High/per bus	Low	Recessive/set by bus
On	On	X	High	Low	High	X	Listen only	High/per bus	High	Recessive/set by bus
On	On	X	X	High	X	X	Standby	High/WUP/filtered	Last state	Bias to GND_2/set by bus
On	On	X	X	X	Low	Pull-up	Standby 5/	High/WUP/filtered	Low	Bias to GND_2/set by bus
On	On	X	X	X	High	Pull-up	Standby 5/	High/WUP/filtered	High	Bias to GND_2/set by bus
On	Off	Z	Z	Z	Z	Low/ pull-down	Normal/ slope mode	Z	Low	Recessive/set by bus
Off	On	X	X	X	X	X	Transceiver off	High	Z	High impedance/set by bus
Off	Off	Z	Z	Z	Z	Z	Transceiver off	Z	Z	High impedance/set by bus

1/ X means irrelevant.
2/ Z means high impedance within one diode drop of ground.
3/ WUP means remote wake-up pattern.
4/ Limited by t_{DT}.
5/ RS can only set the transceiver to standby mode. RS does not control the digital isolator.

FIGURE 3. Truth table.

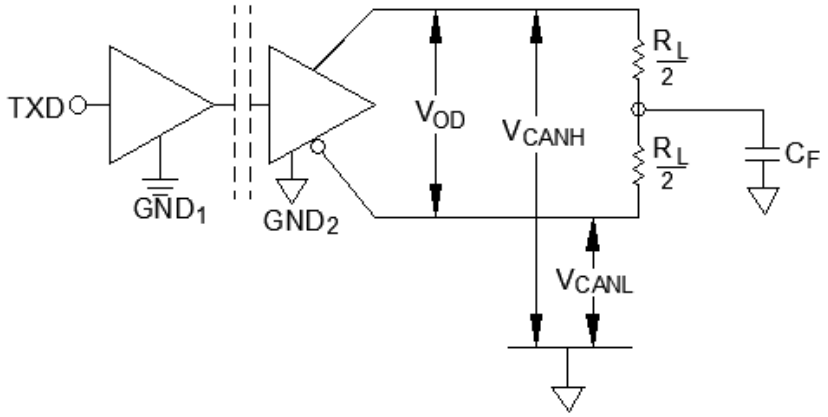


FIGURE 4. Driver voltage measurement.

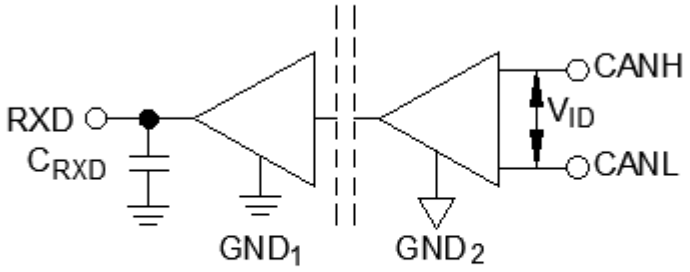


FIGURE 5. Receiver voltage measurement.

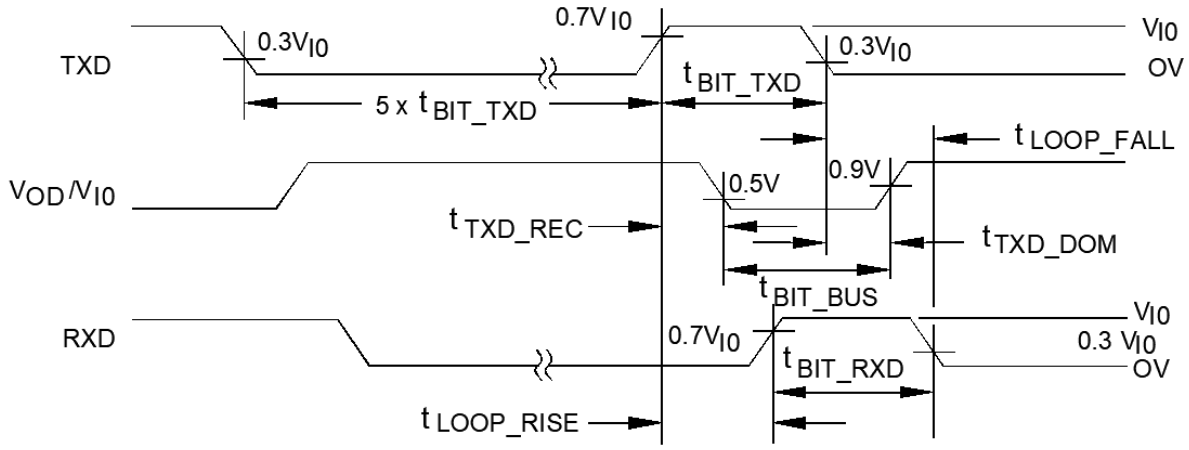
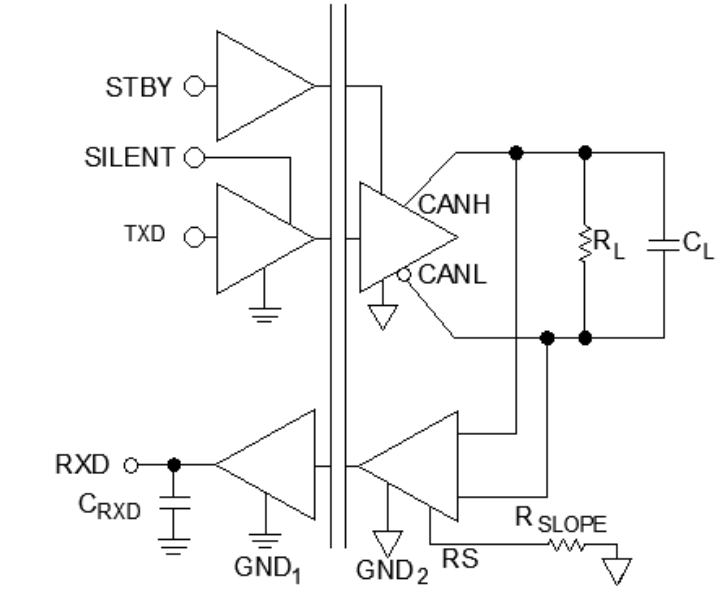


FIGURE 6. Transceiver timing diagram.



NOTES
1. 1% TOLERANCE FOR ALL RESISTORS AND CAPACITORS.

FIGURE 7 Switching characteristics measurements.

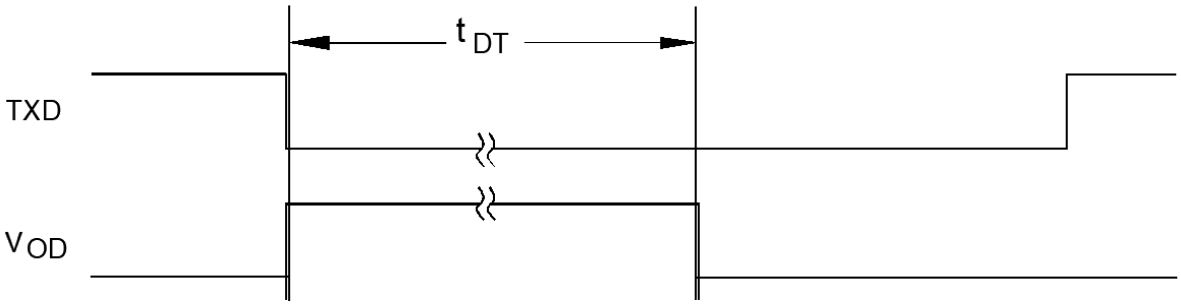


FIGURE 8. Dominant timeout.

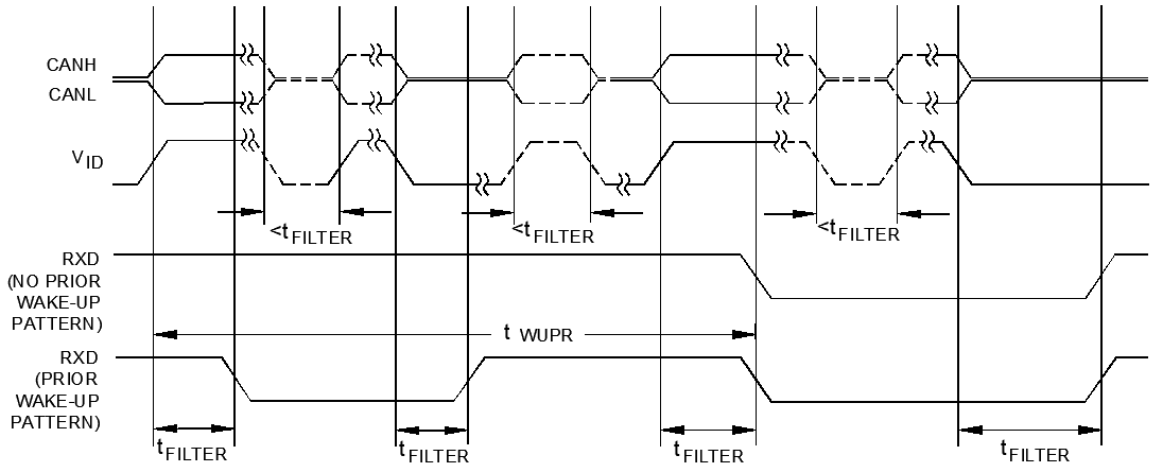


FIGURE 9. Wake up pattern detection and filtered RXD in standby mode timing diagram.

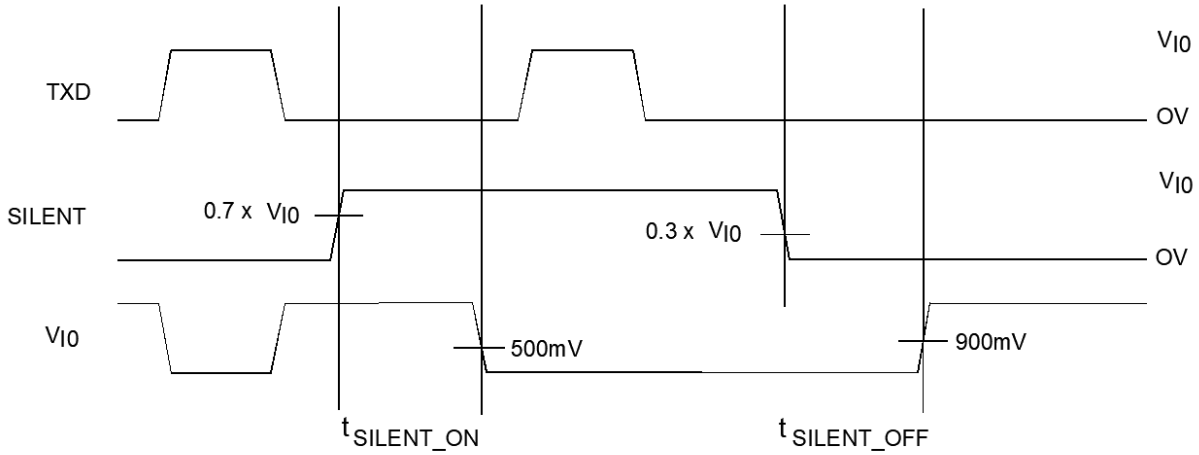


FIGURE 10. Silent mode timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/19604-01XE	24355	Tube, 37 units	ADM3057ETRWZ-EP
		Reel, 1000 units	ADM3057ETRWZ-EP-RL

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123