



AD9577 EVALUATION BOARD APPLICATION NOTE

1.0 Introduction:

This application note describes the AD9577 Evaluation board and its graphical user interface. It includes a board description, software installation and user guide.

The AD9577 evaluation board uses RoHS-compliant FR-4 material. The 4 output differential transmission line pairs use 50 Ω single ended characteristic impedance. The 4 differential output lines are connected to standard edge launch SMA connectors. Each output pair is ac coupled using a 0.1 μ F capacitor. The board can easily be converted to dc coupled traces by replacing the capacitor with a zero Ohm surface-mount resistor.

Some parts of the operation of the AD9577 are described in this document. See the AD9577 datasheet for complete details. In the event that this note contradicts the datasheet, the datasheet information should be used.

The evaluation kit includes:

- Evaluation board
- ADI USB-to-I2C controller board
- USB cable
- Ribbon cable
- Software installation CD

Also required, but not included:

- PC with Microsoft Windows 2000/XP or newer
- DC power supply (3.3V)

AD9577 Evaluation Board:

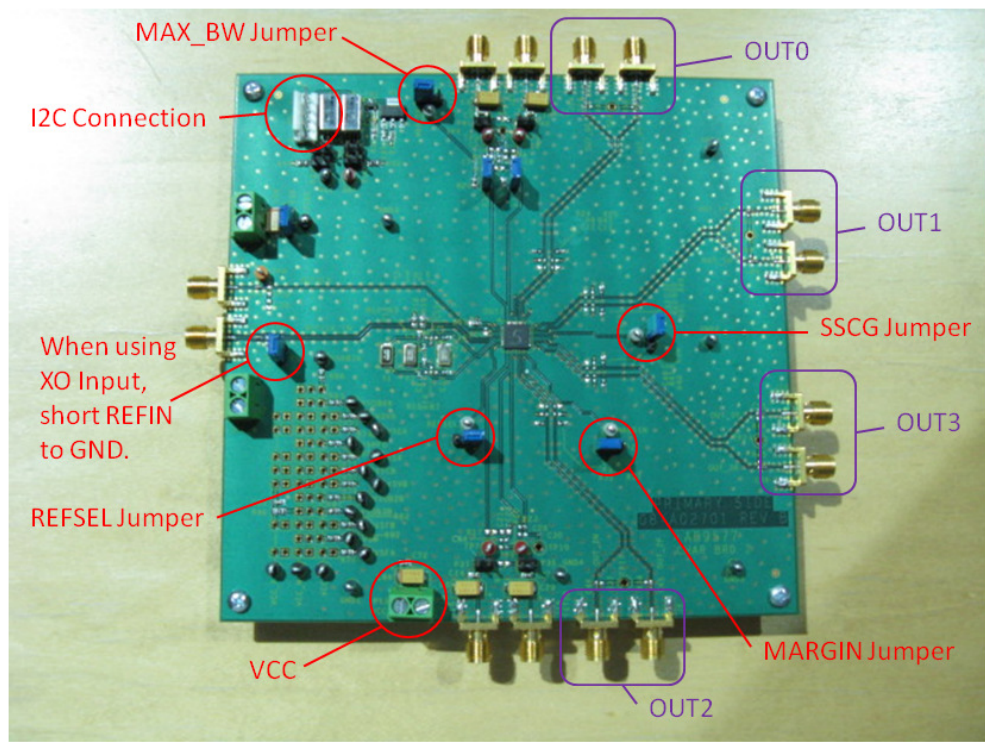


Figure 1. AD9577 evaluation board.

2.0 AD9577 Evaluation Board Outlines:

Power Supply

The AD9577 evaluation board requires a 3.3V, +/- 10% nominal power supply. Please bring this supply to the board through connector P53 labeled VCC in Figure 1.

XO Input

When the REFSEL pin is driven high, a crystal oscillator is used as the REFCLK input. The AD9577 evaluation board has three oscillators on board. The oscillation frequencies are 19.44, 25, and 27MHz. The 25MHz crystal is the default setting.

Reference Designator	Crystal Frequency	Populate Resistors
Y1	19.44MHz	R12, R15
Y2	25MHz	R13, R14
Y3	27MHz	R3,R7

Note: R3, R12, and R13 share a pad.
Note: R7, R14, and R15 share a pad.

REFCLK Input

The AD9577 gets a single-ended REFCLK through the SMA connectors J6. The REFCLK input is selected when the REFSEL pin is driven low. The board’s default state is REFSEL driven high. To change the state of the REFSEL pin, adjust the REFSEL jumper in Figure 1.

Differential Output Ports

The AD9577 has 4 differential output ports. These ports are labeled as OUT0 through OUT3 in Figure 1. The output formats of these ports are controllable over the I2C bus. The output can be differential LVPECL, differential LVDS, or single ended CMOS. The default setting is AC coupled LVPECL. Switching from LVPECL termination to LVDS or CMOS is possible by removing R49, R50, R55, R56, R57, R67, R72, and R73.

Default Evaluation Board Setup

- REFSEL pin set HIGH. This selects the XO inputs.
- MARGIN pin is set low.
- SSCG pin is set low. This sets spread spectrum to off.
- MAX_BW pin is set low.

- 25MHz crystal oscillator connected to the XO inputs.
- REFCLK input shorted to ground.

- OUT0 -> LVPECL -> 156.25MHz
- OUT1 -> LVPECL -> 125.00MHz
- OUT2 -> LVPECL -> 100.00MHz
- OUT3 -> LVPECL -> 33.33MHz

3.0 AD9577 Customer Software

Software Installation

1. Insert the AD9577 software CD into your CD drive.
2. Run setup.exe which is in the cvidistkit_ad9577_customer_gui_rev7\volume directory to install.

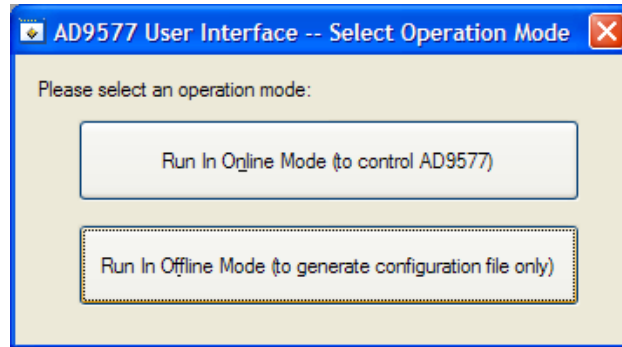


Figure 2. Dialog shown at start up

At start up, the graphical user interface (GUI) displays the dialog shown in Figure 2. The software allows the user to work online with an evaluation board or to work offline without an evaluation board. When working offline, the user can adjust all of the AD9577 settings and create configuration files for later use when an evaluation board is available.

Online Mode

When **Run In Online Mode** is selected, the main panel is displayed as in Figure 3. The title bar displays “Online Mode”. Most of the interface is disabled until I2C communication is verified by clicking the **Check Connection** button in the upper-left corner.

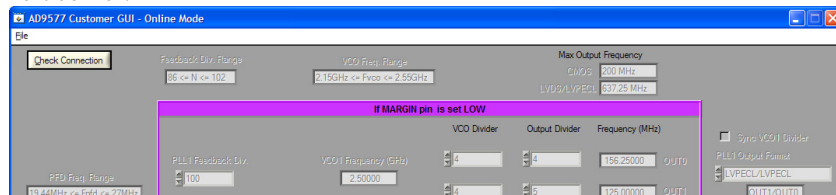


Figure 3. Portion of the GUI panel when first opened in Online mode

After clicking **Check Connection** and I2C communication is working, the GUI panel is fully enabled and loaded with the default values for the part. The software is now ready to change the AD9577 settings and features such as output frequencies, output formats, and spread spectrum settings.

Offline Mode

When **Run In Offline Mode** is selected, the panel loads with default values and all controls enabled except the **Acquire** button. The title bar displays “Offline Mode”. The same controls are available as in online mode; however, they do not actually perform any I2C writes. The Check Connection button is not present.

User Interface Overview

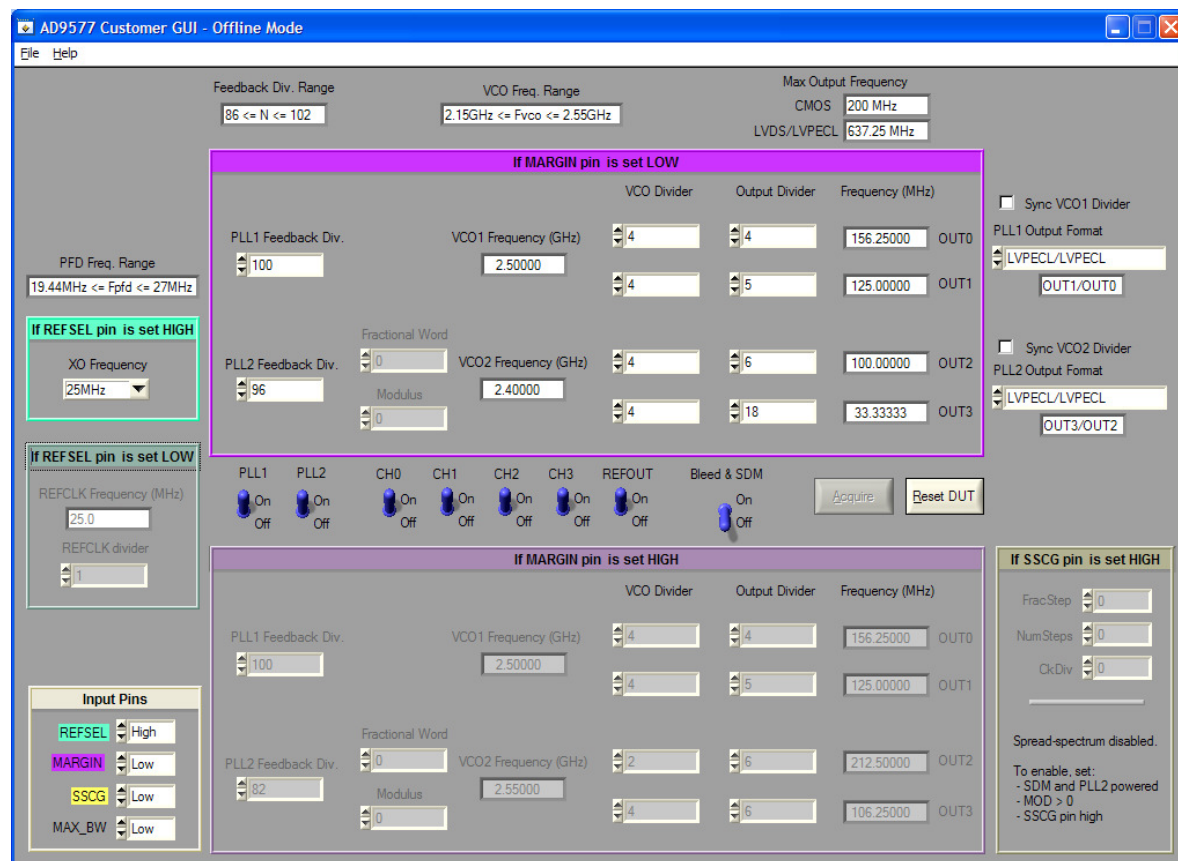


Figure 4. Initial View of the User Interface

Active/Inactive Controls

Many controls are active only under certain conditions, depending on input pin states and power switches. Active controls are displayed with a white background, while inactive controls have a grey background. See Figure 5.



Figure 5. Active Control vs. Inactive Control

Unlike many Windows programs, inactive controls can still be edited and still cause the registers to be changed in the AD9577 (in Online mode). This is to support applications where the part configuration may be switched dynamically (such as when MARGIN or REFSEL are controlled by a microcontroller).

Input Pin Section

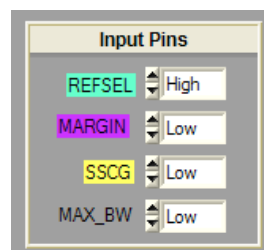


Figure 6. Input Pin Configuration

The input pin controls are located in the lower-left corner of the GUI (Figure 6). They only affect the appearance of the GUI. To change the state of these pins, you **must adjust the jumpers** on the evaluation board. See Figure 1 for the location of each jumper. Setting the input pin controls to match the evaluation board setup allows the proper controls to be displayed as active.

Input Frequency Section



Figure 7. The two states of the input frequency configuration

The input frequency section of the window will look like the left side of Figure 7 in the default configuration. The XO Frequency drop-down is used to select which crystal is connected to the AD9577. Selecting a different crystal from the menu does not actually change the crystal connected to the AD9577. It only lets the software know the correct value of the input frequency. To actually change the crystal, refer to the XO Input section of the evaluation board outline earlier in this document.

When the REFSEL Jumper is adjusted so that REFSEL is low and the REFSEL control is set to Low in the GUI, the panel will look like the right hand side of Figure 7. The software expects that a reference clock between 19.44 and 27MHz is externally given to the AD9577. There is a space to type in the reference frequency being applied. It is also possible to apply a reference frequency between 38.88 and 54MHz. In this case, the REFCLK divider should be set to 2. When the REFCLK divider = 1 the REFCLK is applied directly to the PLLs, and when it is set to 1 the REFCLK is divided by two before being applied to the PLLs. It is important to remember to remove the jumper that shorts the REFCLK input to ground when it is in use. It is also important to know that the CMOS REFCLK output of the AD9577 will be a copy of the applied REFCLK and not the divided down REFCLK.

PLL and Output Divider Section

By default, MARGIN is low, and only the top central section (labeled “If MARGIN pin is set LOW”) is active. The other section can be edited, but it will not have any effect on the operation of the AD9577 until the MARGIN pin jumper is adjusted.

Figure 8. Display when MARGIN is low

The top half of each group contains the PLL1 controls. PLL1 is an integer-N PLL, and the VCO1 frequency is the product of the input frequency and the feedback divider:

$$\text{VCO1 Frequency} = \text{REFCLK frequency} \cdot \text{PLL1 Feedback Divider}$$

PLL2 powers up as an integer-N PLL but it is possible to use it as a Frac-N PLL. In Int-N mode, VCO2 frequency is calculated the same as VCO1 frequency.

$$\text{VCO2 Frequency} = \text{REFCLK frequency} \cdot \text{PLL2 Feedback Divider}$$

When PLL2 is run in fractional-N PLL, the effective feedback divider is adjusted by the fractional word and the modulus registers:

$$\text{VCO2 Frequency} = \text{REFCLK frequency} \cdot (\text{PLL2 Feedback Divider} + (\text{FRAC}/\text{MOD}))$$



Figure 9. Bleed & SDM Switch

To set PLL2 to fractional-N mode, the **BLEED & SDM** switch shown in Figure 9 must be turned on. When it is turned off, the FRAC and MOD boxes are grayed out.

It is important to note that the PLL1 and PLL2 feedback dividers should not be set equal to each other. This could cause reduced performance due to injection locking between the two VCOs. The output frequencies are calculated by dividing the VCO frequency by the product of the VCO divider and the Output Divider.

$$\text{OUT0 frequency} = \text{VCO1 frequency} / (\text{OUT0 VCO Divider} * \text{OUT0 Output Divider})$$

$$\text{OUT1 frequency} = \text{VCO1 frequency} / (\text{OUT1 VCO Divider} * \text{OUT1 Output Divider})$$

$$\text{OUT2 frequency} = \text{VCO2 frequency} / (\text{OUT2 VCO Divider} * \text{OUT2 Output Divider})$$

$$\text{OUT3 frequency} = \text{VCO2 frequency} / (\text{OUT3 VCO Divider} * \text{OUT3 Output Divider})$$

Margining

If MARGIN pin is set LOW

		VCO Divider	Output Divider	Frequency (MHz)	
PLL1 Feedback Div.	VCO1 Frequency (GHz)	<input type="text" value="4"/>	<input type="text" value="4"/>	<input type="text" value="156.25000"/>	OUT0
<input type="text" value="100"/>	<input type="text" value="2.50000"/>	<input type="text" value="4"/>	<input type="text" value="5"/>	<input type="text" value="125.00000"/>	OUT1
PLL2 Feedback Div.	VCO2 Frequency (GHz)	<input type="text" value="4"/>	<input type="text" value="6"/>	<input type="text" value="100.00000"/>	OUT2
<input type="text" value="96"/>	<input type="text" value="2.40000"/>	<input type="text" value="4"/>	<input type="text" value="18"/>	<input type="text" value="33.33333"/>	OUT3
Fractional Word <input type="text" value="0"/> Modulus <input type="text" value="0"/>					

If MARGIN pin is set HIGH

		VCO Divider	Output Divider	Frequency (MHz)	
PLL1 Feedback Div.	VCO1 Frequency (GHz)	<input type="text" value="4"/>	<input type="text" value="4"/>	<input type="text" value="156.25000"/>	OUT0
<input type="text" value="100"/>	<input type="text" value="2.50000"/>	<input type="text" value="4"/>	<input type="text" value="5"/>	<input type="text" value="125.00000"/>	OUT1
PLL2 Feedback Div.	VCO2 Frequency (GHz)	<input type="text" value="2"/>	<input type="text" value="6"/>	<input type="text" value="212.50000"/>	OUT2
<input type="text" value="82"/>	<input type="text" value="2.55000"/>	<input type="text" value="4"/>	<input type="text" value="6"/>	<input type="text" value="106.25000"/>	OUT3
Fractional Word <input type="text" value="0"/> Modulus <input type="text" value="0"/>					

Figure 10. Display when MARGIN is high

The Margin pin can be switched from low to high by adjusting the MARGIN Jumper shown in Figure 1. It is important to know that there is only one Bleed & SDM register. It is a good idea if you are using PLL2 as a Frac-N PLL when MARGIN is high that PLL2 is also being used as a Frac-N PLL when MARGIN is low.

Output format and SYNC

☐ Sync VCO1 Divider
PLL1 Output Format
LVPECL/LVPECL
OUT1/OUT0

☐ Sync VCO2 Divider
PLL2 Output Format
LVPECL/LVPECL
OUT3/OUT2

Figure 11. Output format and SYNC registers

Adjusting the PLL1 or PLL2 output format is achieved by selecting the output formats from the drop-downs. The available options are:

Output Formats
LVPECL/LVPECL
LVDS/LVDS
2xCMOS/LVPECL
2xCMOS/2xCMOS
2xCMOS/LVDS
LVPECL/LVDS
LVPECL/2xCMOS
*2xCMOS/2xCMOS

Format is specified as: OUT1/OUT0 or OUT3/OUT2

*all 4 CMOS output per PLL are in phase

This only adjusts the output drivers of the AD9577. The LVPECL termination resistors need to be removed for LVDS or CMOS operation. It is important to note that it is not possible to have different output formats for the different states of the MARGIN pin.

When the SYNC check boxes are selected, the display will appear as in shown in Figure 12. The **VCO Divider** boxes for OUT1 and OUT3 become shaded. This is because when SYNC is checked, OUT0 and OUT1 share a VCO divider and OUT2 and OUT3 share a VCO divider. It is important to note that when SYNC is checked, the sync occurs for both states of the MARGIN pin.

VCO Divider	Output Divider	Frequency (MHz)	
4	4	156.25000	OUT0
4	5	125.00000	OUT1
2	6	212.50000	OUT2
4	6	212.50000	OUT3

Figure 12. Display when both SYNC options are checked

Power on and off PLLs and Output Ports



Figure 13. On/Off Switches

This section of the GUI panel allows the user to turn sections of the AD9577 off and on. There are switches for the following: PLL1, PLL2, CH0 Output, CH1 Output, CH2 Output, CH3 Output, and the REFCLK Output. When each switch is turned off, the GUI display also updates to indicate which controls will not have any effect. For example, if PLL1 and CH3 are both turned off, the display will look like Figure 14, indicating that only OUT2 will have a signal.

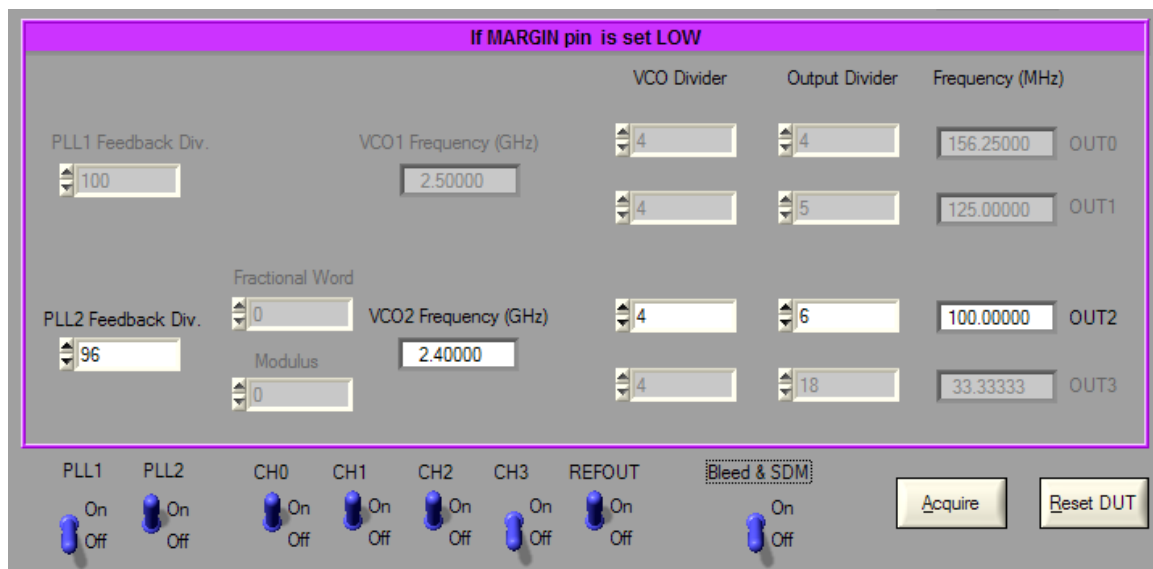


Figure 14. Effect of On/Off Switches on Display

Spread Spectrum

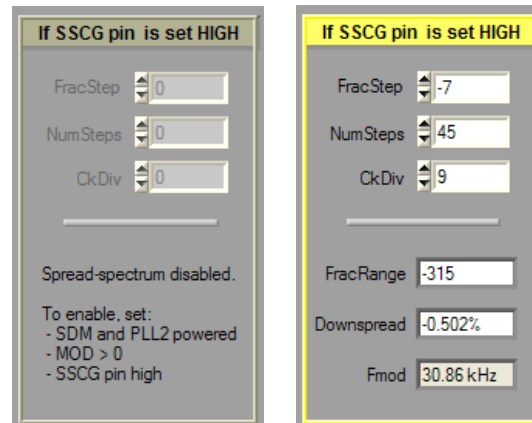


Figure 15. Spread Spectrum Register Display

Spread spectrum mode can be enabled on PLL2 by adjusting the SSCG Jumper in Figure 1 so that the SSCG pin is high. PLL2 must be in Fractional-N mode for spread spectrum operation to function. The output frequency is modulated with a triangular profile and the peak power is reduced. The tri-wave modulation is implemented by controlling the divide ratio of the feedback divider. This is achieved by ramping the fractional word to the SDM. The key parameters that define the frequency modulation profile are:

- FracRange: The maximum change in the modulated FRAC value from the initial FRAC value.
- Downspread: The maximum percent reduction in output frequency for OUT2 and OUT3.
- Fmod: The frequency of the modulation waveform

The following equations determine the value of these parameters:

$$\begin{aligned}\text{FracRange} &= \text{FracStep} * \text{NumSteps} \\ \text{Downspread} &= \text{FracRange} / (\text{MOD} * (\text{Nb} + \text{FRAC}/\text{MOD})) \\ \text{Fmod} &= \text{REFCLK frequency} / (2 * \text{NumSteps} * \text{CkDiv})\end{aligned}$$

Where the following are programmable registers

- FracStep: The value of the fractional word decrement whilst traversing the tri-wave. Only negative values are supported.
- NumSteps: The number of fractional word steps in half the tri-wave period.
- CkDiv: The refclk frequency is divided by this integer value to determine the update rate of the tri-wave generator, i.e. the step update rate.

The default values are all 0 and must be modified before spread-spectrum operation will function.

Acquire and Reset

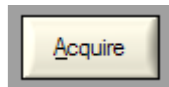


Figure 16. The Acquire button

Pressing the **Acquire** button in the GUI forces the AD9577 to perform a new acquisition.

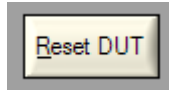


Figure 17. The Reset DUT button

Pressing the **Reset DUT** button resets the AD9577 back to its default power up state. The feedback dividers, VCO dividers, output dividers, output format, output sync, SSCG registers and on/off switches all get reset.

Invalid Value Indication

Certain combinations of values can cause the AD9577 operating parameters to exceed the valid ranges, as specified in the datasheet. In some of these cases, the GUI will highlight invalid values in red.

The following conditions are checked:

- Fpfd must be between 19.44MHz and 27MHz
- Feedback dividers (N) must be chosen so that the VCO frequency is valid
- Feedback dividers should not equal each other for the same value of MARGIN (injection locking)
- VCO frequencies must be between 2.15GHz and 2.55GHz
- CMOS output frequency must not be greater than 200MHz
- LVDS/LVPECL output frequency must not be greater than 637.5MHz
- REFCLK divider must be set to 1 when using the crystal (when REFSEL is high)
- SSCG must not cause FRAC/MOD to roll over more than 4 times, i.e., $|\text{FracRange}| < \text{FRAC} + 4 * \text{MOD}$
- SSCG downspread only supported from -0.5% to 0.0%.
-

For example, Figure 18 shows the results when several invalid values have been selected. The invalid values and the constraints that have been violated are highlighted in red. Note that there may be additional requirements specified on the datasheet that are not validated by the user interface.

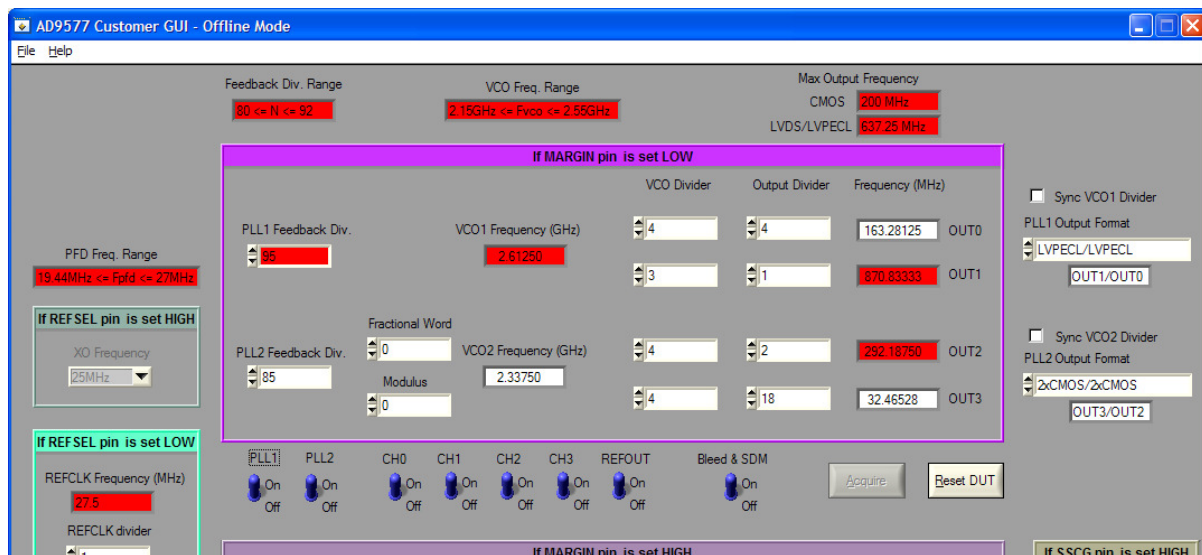


Figure 18. View Showing Invalid Data

File Menu

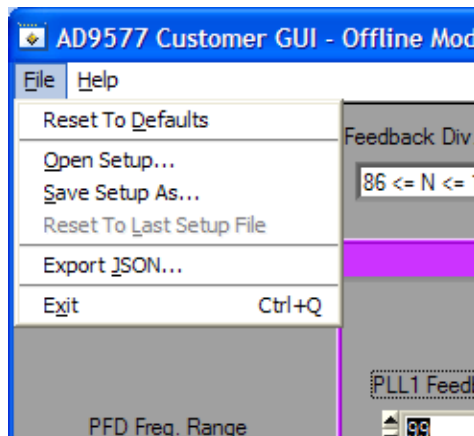


Figure 19. File Menu Display

The File menu provides the following commands:

- **Reset To Defaults:** Reset the AD9577 to its default power-up state. Same as the Reset DUT button.
- **Open Setup:** Read a setup (.stp) file and apply the saved register settings to the AD9577.
- **Save Setup As:** Write a setup (.stp) file containing all of the register settings.
- **Reset To Last Setup File:** Only valid after performing one of the previous two actions. This sets the registers of the AD9577 back to the last opened or saved configuration.
- **Export JSON:** Create a file used for automatic programming in certain applications. Not typically used.
- **Exit:** Quit the program. The normal X button in the upper right can also be used.

Setup Files

The AD9577 software allows the user to write a file containing all of the current settings and then read back this file and set the AD9577 registers back to those settings.

This is accomplished by the following:

1. Start the software in online mode and verify I2C communication
-OR-
Start the software in offline mode
2. Adjust the AD9577 settings to fit your needs.
3. Select the **File/Save Setup As** menu item. Select an output filename and the file will be written.
4. If the AD9577 power is cycled, the **Reset DUT** button is clicked, or the program is re-launched from offline to online mode, the saved settings can be recalled by using the **File/Open Setup** menu item. The settings in the file will be written to the AD9577.