

Evaluating the AD7450A/51

Full-featured evaluation board for the AD7450A/51
PC control in conjunction with the System Demonstration
Platform (EVAL-SDP-CB1Z)
PC software for control and data analysis (time and
frequency domain)
Standalone capability

EVAL-AD7450A/51SDZ KIT CONTENTS

EVAL-AD7450A/51SDZ Evaluation Board
Evaluation Software CD for the AD7450A/51
9V Mains power supply adapter

ADDITIONAL EQUIPMENT NEEDED

System Demonstration platform (EVAL-SDP-CB1Z)
Precision Analog signal source
SMB cables
USB Cables

EVALUATION BOARD DESCRIPTION

The EVAL-AD7450A/51SDZ is a full-featured evaluation board, designed to allow the user to easily evaluate all features of the AD7450A/51. The evaluation board can be controlled via the system demonstration platform (SDP) connector (J8). The EVAL-SDP-CB1Z board allows the evaluation board to be controlled via the USB port of a PC using the AD7450A/51 evaluation software.

The EVAL-AD7450A/51SDZ generates all required power supplies on board and supplies power to the EVAL-SDP-CB1Z controller board.

On-board components include the:

- AD8599: Ultralow Distortion, Ultralow Noise Op Amp (Dual)
- ADP1613: Step-Up PWM DC-to-DC Switching Converter,

- ADP3303-5: High Accuracy anyCAP™ 200 mA Low Dropout Linear Regulator
- ADP1720: 50 mA, High Voltage, Micropower Linear Regulator
- ADP7104: 20 V, 500 mA, Low Noise, CMOS LDO
- ADM1185: Quad Voltage Monitor and Sequencer
- ADG3308: Low Voltage, 1.15 V to 5.5 V, 8-Channel Bidirectional Logic Level Translator
- ADR431: Ultralow Noise XFET® Voltage References with Current Sink and Source Capability

Various link options are described in the Evaluation Board Hardware section.

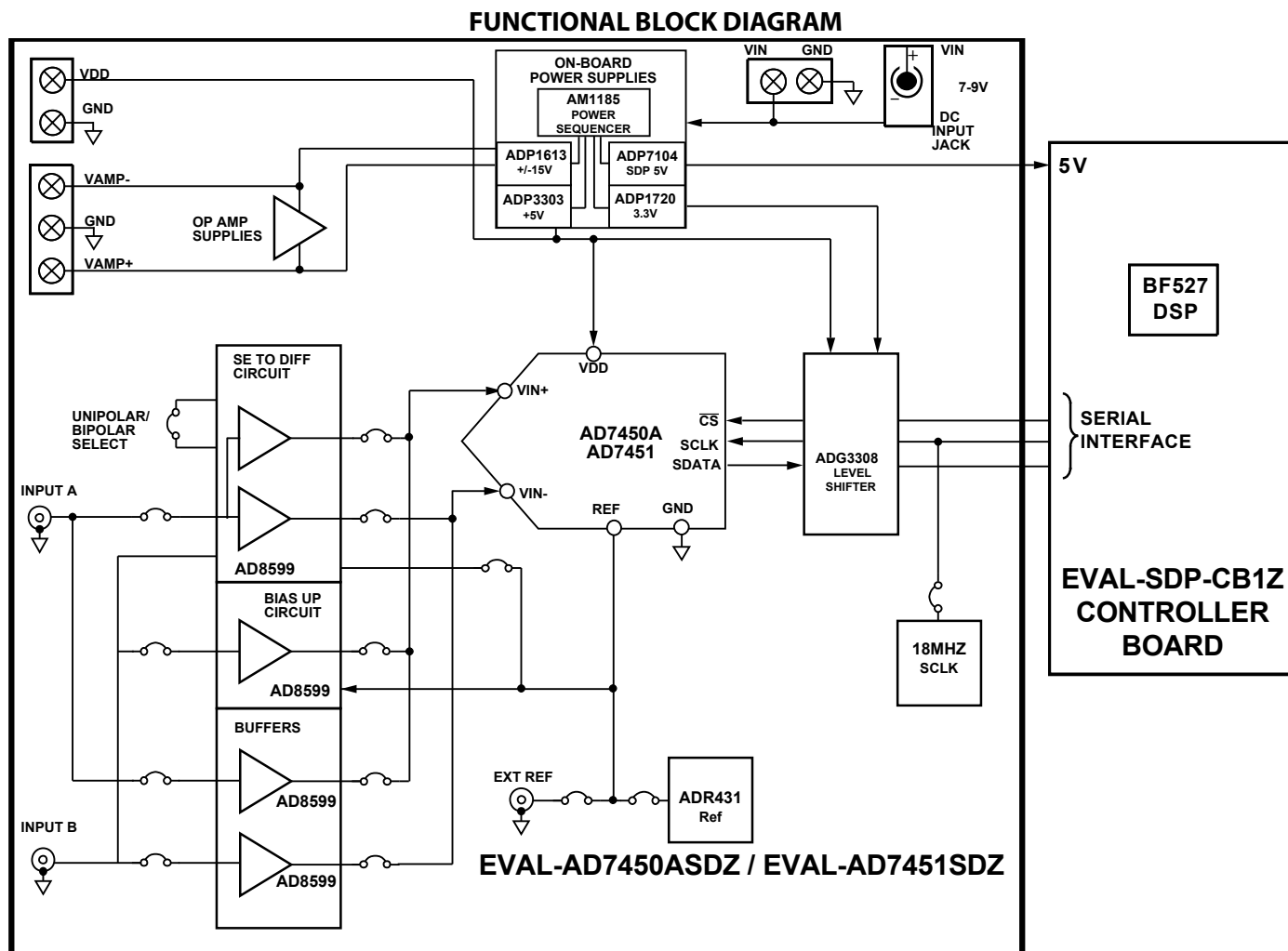


Figure 1 Functional Block Diagram

TABLE OF CONTENTS

EVAL-AD7450A/51SDZ KIT Contents	1	Sockets/Connectors	9
Additional Equipment Needed.....	1	EVAL-AD7450A/51SDZ Basic Hardware Setup	10
Evaluation Board Description	1	Evaluation Board Software.....	11
Functional Block Diagram	2	Software Installation	11
Revision History	3	Launching The Software	13
EVAL-AD7450A/51SDZ Quickstart Guide.....	4	Software Operation.....	13
Recommended Quick Start GUIDE.....	4	Description of User Software panel.....	14
Evaluation Board Hardware.....	5	WaveForm Capture.....	16
AD7450A Device description.....	5	AC Testing - Histogram	17
AD7451 Device description.....	5	DC Testing - Histogram	17
Hardware Link Options.....	6	AC Testing - FFT Capture.....	18
Power Supplies.....	8	Summary Tab.....	19
Serial Interface.....	8	Save File.....	20
Stand-alone mode	8	Load File.....	20
Analog Inputs	8	Evaluation Board Schematics and Artwork.....	21
Reference Options.....	9		

REVISION HISTORY

04/12—Revision PrA

EVAL-AD7450A/51SDZ QUICKSTART GUIDE

RECOMMENDED QUICK START GUIDE

To install the software do the following:

- (1) Install the AD7450A/51 Software from the enclosed CD. Ensure the EVAL-SDP-CB1Z board is **disconnected** from the USB port of the PC while installing the software. The PC must be restarted after the installation.
- (2) Connect the EVAL-SDP-CB1Z board to the EVAL-AD7450A/51SDZ board as shown in Figure 2.
- (3) Screwing the two boards together with the enclosed nylon screw-nut set will ensure the boards connect firmly together.
- (4) Connect the 9V power supply adapter included in the kit to connector J702 on the EVAL-AD7450A/51SDZ board.
- (5) Connect the EVAL-SDP-CB1Z board to the PC via the USB cable. For Windows XP you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.
- (6) Launch the EVAL-AD7450A/51SDZ software from the Analog Devices subfolder in the Programs menu.

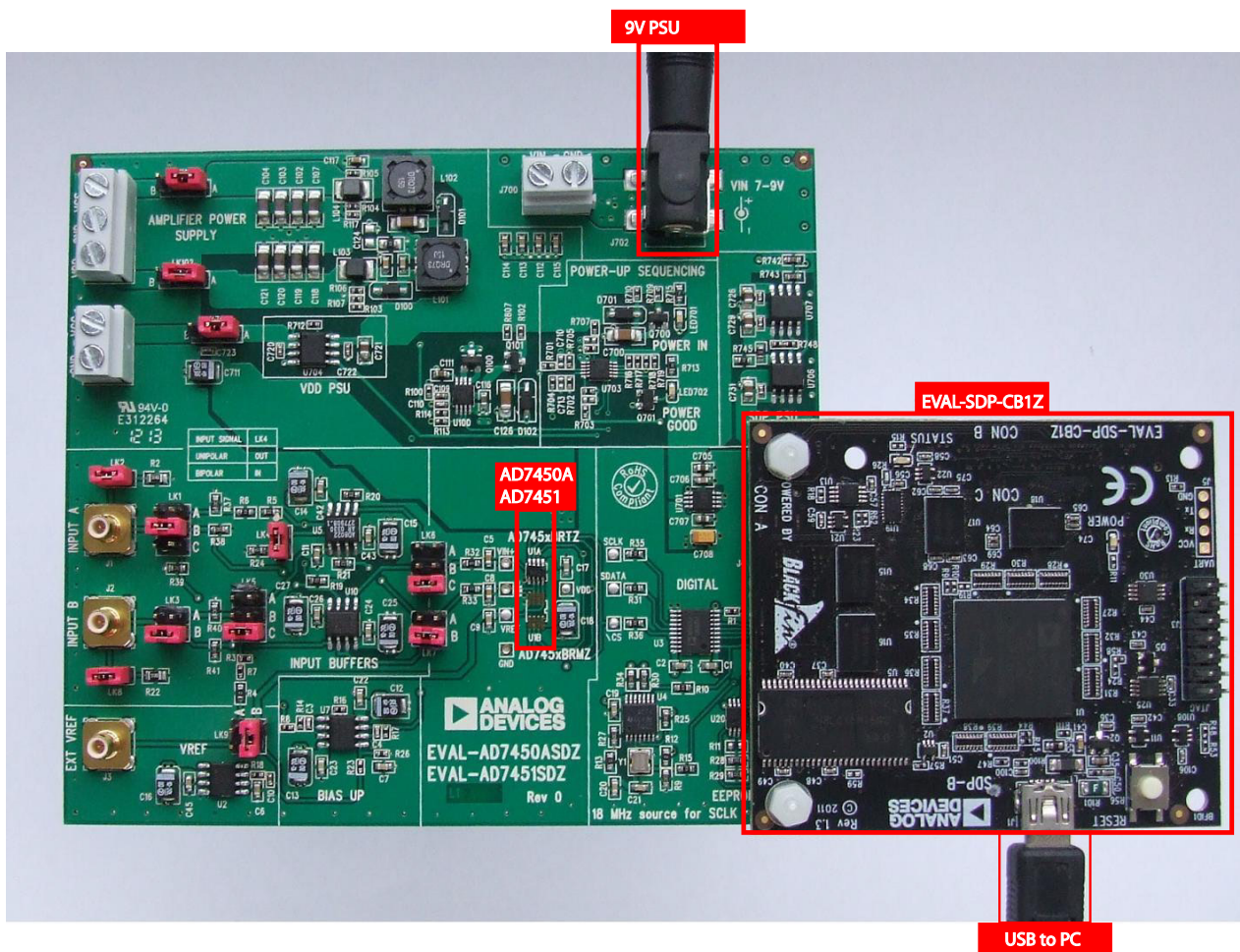


Figure 2. Hardware Configuration – Setting up the EVAL-AD7450A/51SDZ.

EVALUATION BOARD HARDWARE

AD7450A DEVICE DESCRIPTION

The AD7440/AD7450A1 are 10-bit and 12-bit high speed, low power, successive approximation (SAR) analog-to-digital converters with a fully differential analog input. These parts operate from a single 3 V or 5 V power supply and use advanced design techniques to achieve very low power dissipation at throughput rates up to 1 MSPS. The SAR architecture of these parts ensures that there are no pipeline delays.

The parts contain a low noise, wide bandwidth, differential track-and-hold amplifier (T/H) that can handle input frequencies up to 3.5 MHz. The reference voltage is applied externally to the VREF pin and can be varied from 100 mV to 3.5 V depending on the power supply and what suits the application. The value of the reference voltage determines the common-mode voltage range of the part. With this truly differential input structure and variable reference input, the user can select a variety of input ranges and bias points.

The conversion process and data acquisition are controlled using CS and the serial clock, allowing the device to interface with microprocessors or DSPs. The input signals are sampled on the falling edge of CS; the conversion is also initiated at this point. The SAR architecture of these parts ensures that there are no pipeline delays. The AD7440 and the AD7450A use advanced design techniques

AD7451 DEVICE DESCRIPTION

The AD7441/AD7451 are, respectively, 10-/12-bit high speed, low power, single-supply, successive approximation (SAR), analog-to-digital converters (ADCs) that feature a pseudo differential analog input. These parts operate from a single 2.7 V to 5.25 V power supply and achieve very low power dissipation at high throughput rates of up to 1 MSPS.

The AD7441/AD7451 contain a low noise, wide bandwidth, differential track-and-hold (T/H) amplifier that handles input frequencies up to 3.5 MHz. The reference voltage for these devices is applied externally to the V_{REF} pin and can range from 100 mV to V_{DD} , depending on the power supply and what suits the application.

The conversion process and data acquisition are controlled using CS and the serial clock, allowing the device to interface with microprocessors or DSPs. The input signals are sampled on the falling edge of CS when the conversion is initiated. The SAR architecture of these parts ensures that there are no pipeline delays.

HARDWARE LINK OPTIONS

There are 12 link options, which must be set for the required operating setup before using the evaluation board. The functions of these options are outlined in Table 1. Shows the position in which all the links are set when the evaluation board is packaged. Jumper and solder link (LKx) options must be set correctly to select the appropriate operating setup before using the evaluation board. The default link positions are shown in Table 2 and the functions of these options are outlined in Table 1

Table 1 Link Options

Link No.	Function
LK1	INPUT A Destination Selection. This selects which buffer input A is connected to. Position A: INPUT_A is connected to single ended to differential buffer Position B: INPUT_A is connected to single ended buffer (U10-A) Position C: INPUT_A is connected to bias up circuit (U7-A/B)
LK2	INPUT_A input impedance selection. INSERT: INPUT_A input impedance is 51Ω
LK3	INPUT B Destination Selection. This selects which buffer input A is connected to. Position A: INPUT_B is connected to LK5 position B Position B: INPUT_B is connected to single ended buffer (U10-B)
LK4	Input signal selection INSERT when input signal at INPUT_A is bipolar REMOVE when input signal at INPUT_A is unipolar
LK5	INPUT A Destination Selection. This selects which buffer input A is connected to. Position A: ½ VREF is supplied to U5-B Position B: INPUT_B is supplied to U5-B Position C: 0V is supplied to U5-B
LK6	VIN+ Source Selection. Select which buffered signal is routed to AD7540A/51 Pin VIN+ Position A: Signal is sourced from single ended to differential buffer putput (U5-A) Position B: Signal is sourced from single ended buffer (U10-A) Position C: Signal is sourced from bias up circuit (U7-B)
LK7	VIN- Source Selection. Select which buffered signal is routed to AD7540A/51 Pin VIN+ Position A: Signal is sourced from single ended to differential buffer output (U5-B) Position B: Signal is sourced from single ended buffer (U10-B)
LK8	INPUT_B input impedance selection. INSERT: INPUT_B input impedance is 51Ω
LK9	VREF source selection Position A: VREF Is sourced from U2 ADR431: Ultralow Noise XFET® Voltage Reference Position B: VREF Is sourced externally via SMB connector EXT_VREF
LK101 ¹	Amplifier negative voltage supply Selection Position A: Amplifier negative voltage supplied from on board supply Position B: Amplifier negative voltage supplied from external source via J100 terminal 1. Labeled VSS
LK102 ¹	Amplifier Positive voltage Selection Position A: Amplifier Positive voltage supplied from on board supply Position B: Amplifier Positive voltage supplied from external source via J100 terminal 3. Labeled VDD ²
LK701	VDD supply for AD7540A/51. Position A: VDD supplied from on board supply (5V) Position B: VDD supplied from external source via J100 terminal. Labeled VCC ²

¹ Both LK101 and LK102 should always be in corresponding positions.

² Be aware of labelling on current version of Evaluation Board

Table 2 Link Options -Setup condition for AD7450A

Link No.	Position	Function
LK1	B	INPUT_A is connected to single ended buffer (U10-A)
LK2	INSERTED	INPUT_A input impedance is 51Ω
LK3	B	INPUT_B is connected to single ended buffer (U10-B)
LK4	INSERTED	Input signal at INPUT_A is bipolar
LK5	A	VREF/2 is supplied to U5-B
LK6	C	Signal is sourced from bias up circuit (U7-B)
LK7	B	Signal is sourced from single ended buffer (U10-B)
LK8	INSERTED	INPUT_B input impedance is 51Ω
LK9	A	VREF Is sourced from U2
LK101 ¹	A	Amplifier negative voltage supplied from on board supply
LK102 ¹	A	Amplifier Positive voltage supplied from on board supply
LK701	A	VDD supplied from on board supply (5V)

Table 3 Link Options - Setup conditions for AD7451

Link No.	Position	Function
LK1	C	INPUT_A is connected to bias up circuit (U7)
LK2	INSERTED	INPUT_A input impedance is 51Ω
LK3	B	INPUT_B is connected to single ended buffer (U10-B)
LK4	INSERTED	Input signal at INPUT_A is bipolar
LK5	C	0V is supplied to U5-B
LK6	C	Signal is sourced from bias up circuit (U7-B)
LK7	A	Signal is sourced from (U5-B)
LK8	INSERTED	INPUT_B input impedance is 51Ω
LK9	A	VREF Is sourced from U2
LK101 ¹	A	Amplifier negative voltage supplied from on board supply
LK102 ¹	A	Amplifier Positive voltage supplied from on board supply
LK701	A	VDD supplied from on board supply (5V)

POWER SUPPLIES

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode.

When using the EVAL-AD7450A/51SDZ in conjunction with the EVAL-SDP-CB1Z board, connect the AC transformer to connector J702. VCC, VDD, VSS and VDRIVE are generated on-board. Alternatively a bench power supply may be connected to J700 to supply 7V to 9V

Table 4. External Power Supply Required

POWER SUPPLY	VOLTAGE RANGE	PURPOSE
VIN ¹ J700 or J702	7V to 9V	Supplies all onboard power supplies which generate all required voltages to run the evaluation board
VDD J100	+12V to +16.5V	Amplifier positive supply
VSS J100	-12V to - 16.5V	Amplifier negative supply
VCC J703	4.75V to 5.25V	VDD digital supply.

1. When this is supplied all other power supplies are available onboard. If this supply is not used then all other supplies must be sourced from an external source.

SERIAL INTERFACE

The AD7450A/51 uses a high speed serial interface which allows sampling rates up to 1MSPS. For details on the operation of the serial bus, refer to the AD7450A/51 datasheet.

The EVAL-AD7450A/51SDZ communicates with the EVAL-SDP-CB1Z board using level shifters. The EVAL-SDP-CB1Z operates at a 3.3V logic level. This allows VDRIVE voltages to exceed 3.3V to be used without damaging the SDP interface.

Details of the serial interface can be found in the AD7450A/51 Datasheets.

STAND-ALONE MODE

The EVAL-AD7450A/51SDZ may also be used without the EVAL-SDP-CB1Z. In this case, connection to the digital interface is made via the test-point connectors. **Remove R31, R35 and R36** to isolate the AD7450A/51 from the SDP interface circuitry

ANALOG INPUTS

3 buffer circuits are available as outlined below.

Single ended to Differential

A single input signal applied to INPUT_A SMB socket can be used to generate a differential signal.

For bipolar signals the input range should be +0.5VREF to -0.5VREF. LK4 is inserted.

For unipolar signals the input should be 0 to VREF. LK4 is removed.

Individual channel Buffers

INPUT_A and INPUT_B are used in this configuration. Both inputs are buffered individually. The outputs from these amplifiers are available to the AD7450A/51 VIN+ and VIN- inputs via low pass RC filter networks.

Level Shifter.

The analog inputs on the EVAL-AD7450A/51SDZ are filtered and buffered by an AD8599. The outputs from this amplifier is available to the AD7450A/51 VIN+ input via low pass RC filter network.

REFERENCE OPTIONS

the reference source can be from an ADR431: Ultralow Noise XFET® Voltage References with Current Sink and Source Capability (U2). An external reference voltage may also be applied to J3 EXT_REF

SOCKETS/CONNECTORS

Table 5 Socket connector functions

Socket	Function
J1 INPUT_A	Input. This is routed to a selection of input buffers
J2 INPUT_B	Input. This is routed to a selection of input buffers
J3 EXT_REF	External reference connection point
J4	EVAL-SDP-CB1Z Eval board controller socket
J100 VSS & VDD	Screw terminal connectors for external amplifier power supplies.
J700	7V to 9V bench supply screw terminal connector.
J702	7V to 9V DC transformer power connector.
J703 VCC	External power supply for VDD of the AD7450A/51.

EVAL-AD7450A/51SDZ BASIC HARDWARE SETUP

The AD7450A/51 evaluation board connects to the (EVAL-SDP-CB1Z) System Demonstration Board. The EVAL-SDP-CB1Z Board is the controller board, which is the communication link between the PC and the main evaluation board. Figure 2 shows a photograph of the connections made between the AD7450A/51 daughter board and the EVAL-SDP-CB1Z board.

Before connecting power, connect the EVAL-AD7450A/51SDZ board to connector A or connector B on the EVAL-SDP-CB1Z board. Nylon screws are included in the EVAL-AD7450A/51SDZ evaluation kit and can be used to ensure the EVAL-AD7450A/51SDZ board and the EVAL-SDP-CB1Z board are connected firmly together.

Evaluation Board Software section.

Finally connect the EVAL-SDP-CB1Z board to the PC via the USB cable enclosed in the EVAL-SDPCB1Z kit. If using Windows XP platform, you may need to search for the EVAL-

Once the EVAL-AD7450A/51SDZ board and the EVAL-SDP-CB1Z board are connected securely, connect the power supplies on the EVAL-AD7450A/51SDZ board. The EVAL-AD7450A/51SDZ requires an external power supply which is included in the evaluation board kit. Connect this power supply to the connector J702 on the EVAL-AD7450A/51SDZ board. Alternatively a bench power supply may be used to power the EVAL-AD7450A/51SDZ via J700. Further details on the required power supplies connections and options are detailed in Table 5 Socket connector functions.

Before connecting the EVAL-SDP-CB1Z board to your PC, ensure that the AD7450A/51 software has been installed from the enclosed CD. The full software installation procedure is detailed in the

SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The EVAL-AD7450A/51SDZ evaluation kit includes software on a CD. Click the **setup.exe** file from the CD to run the install. The default location for the software is
C:\Program Files\Analog Devices\AD7450A/51

Note:

Install the evaluation software before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

There are two parts to the install:

1. AD7450A/51 Evaluation board software Install.
2. EVAL-SDP-CB1Z System Demonstration Platform Board Drivers install

Figure 3 to Figure 7 show the separate stages of the AD7450A/51 evaluation software. Figure 8 to Figure 12 show the separate steps to install the EVAL-SDP-CB1Z drivers. Proceed through all of the installation steps allowing the software and drivers to be placed in the appropriate locations. Only after the software and drivers have been installed should you connect the EVAL-SDP-CB1Z board to the PC.

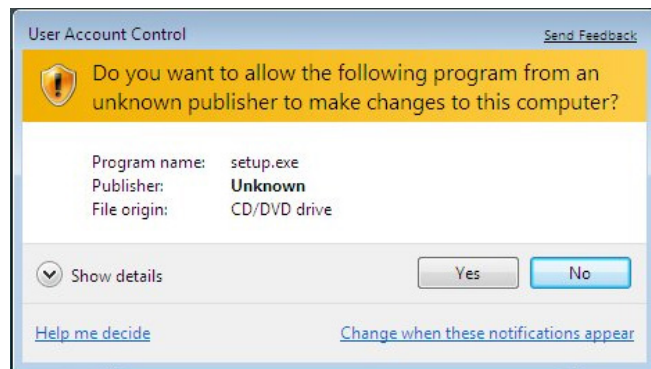


Figure 3. AD7450A/51 Install Window 1

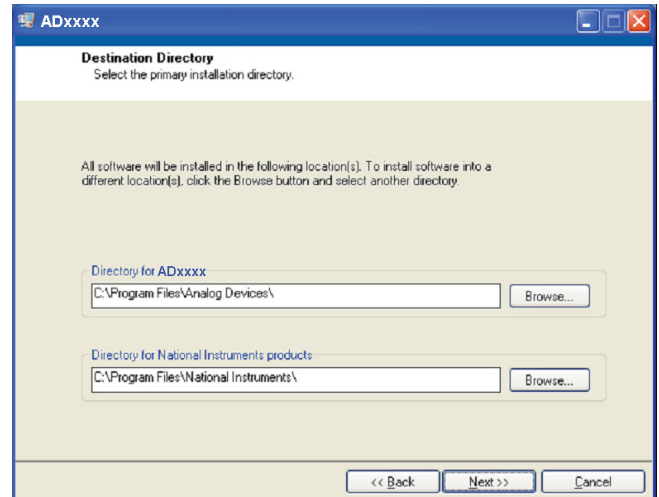


Figure 4 AD7450A/51 Install Window 2

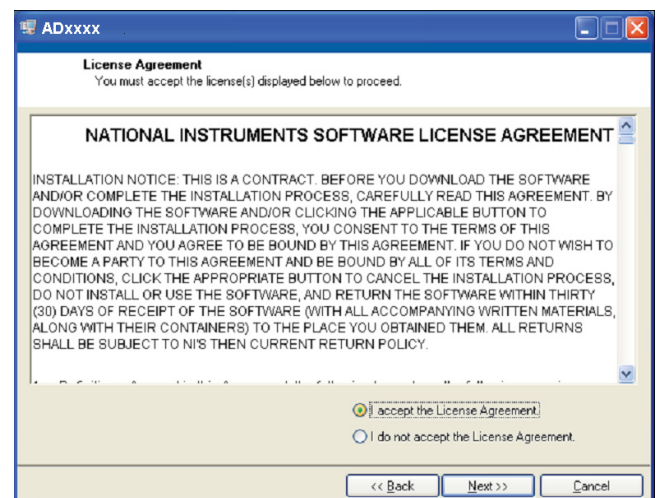


Figure 5 Install Window 3

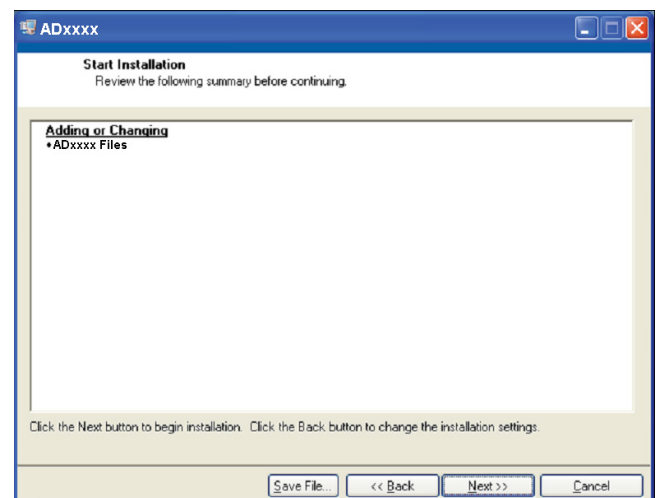


Figure 6. AD7450A/51 Install Window 4

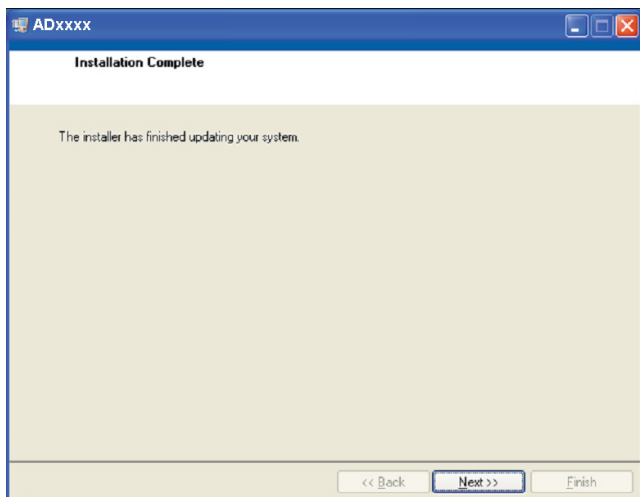


Figure 7. AD7450A/51 Install Window 5.



Figure 8. ADI EVAL-SDP-CB1Z Drivers Setup Window 1.

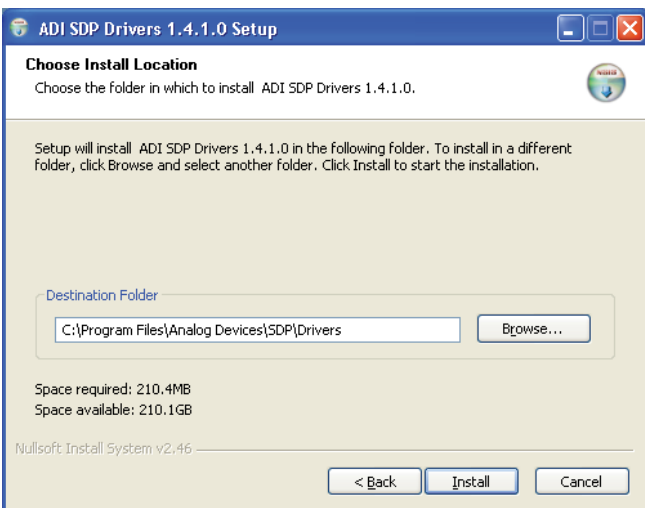


Figure 9. ADI EVAL-SDP-CB1Z Drivers Setup Window 2.

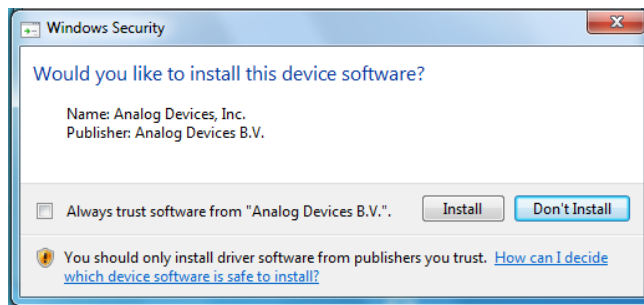


Figure 10. ADI EVAL-SDP-CB1Z Drivers Setup Window 3

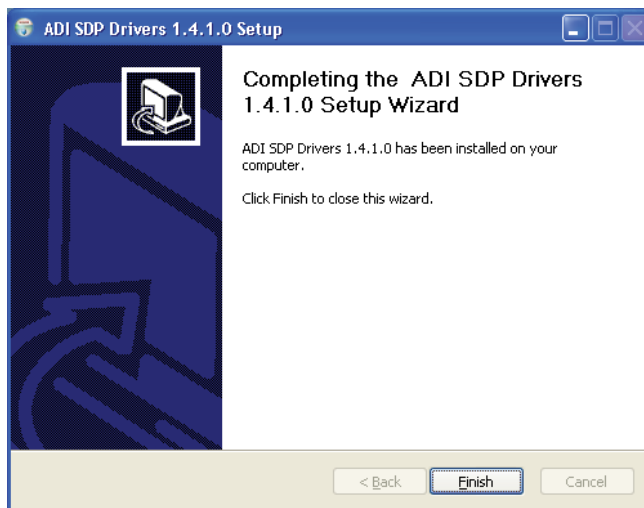


Figure 11. ADI EVAL-SDP-CB1Z Drivers Setup Window 4

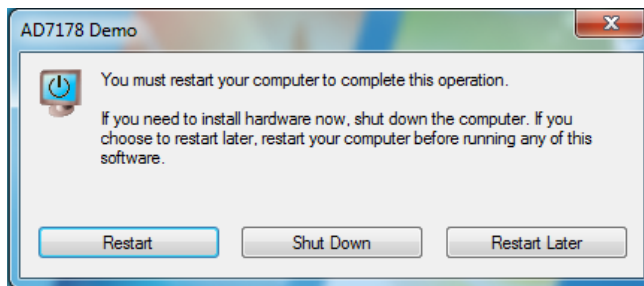


Figure 12. ADI EVAL-SDP-CB1Z Drivers Setup Window 5

After installation from CD is complete, connect the EVAL-AD7450A/51SDZ to the EVAL-SDP-CB1Z as described in the Evaluation Board Hardware section.

When you first plug in the EVAL-SDP-CB1Z board via the USB cable provided, allow the new Found Hardware Wizard to run. Once the drivers are installed, you may check that the board has connected correctly by looking at the Device Manager of the PC. The Device Manager can be found by right clicking on My Computer->Manage->Device Manager from the list of System Tools as shown below. The EVAL-SDP-CB1Z Board should appear under ADI Development Tools. This completes the installation.

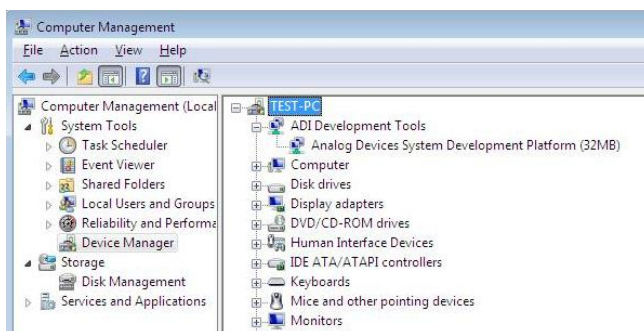


Figure 13. Device Manager

LAUNCHING THE SOFTWARE

Once the EVAL-AD7450A/51SDZ and EVAL-SDP-CB1Z are correctly connected to your PC, the AD7450A/51 software can be launched.

To launch the software, complete the following steps:

1. From the **Start** menu, select **Programs -> Analog Devices -> AD7450A/51**. The main window of the software then displays.
2. If the AD7450A/51 evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, a connectivity error displays (see Figure 14). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

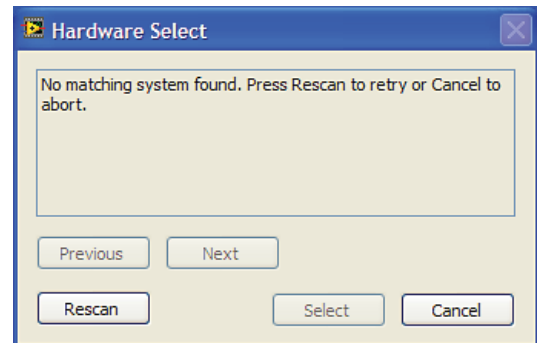


Figure 14. Connectivity Error Alert

SOFTWARE OPERATION

When the software is launched, the panel will open and the software will look for hardware connected to the PC. The software will detect the generic attached to the PC and return this in a user dialog box.

The user software panel will then launch as shown in Figure 15.

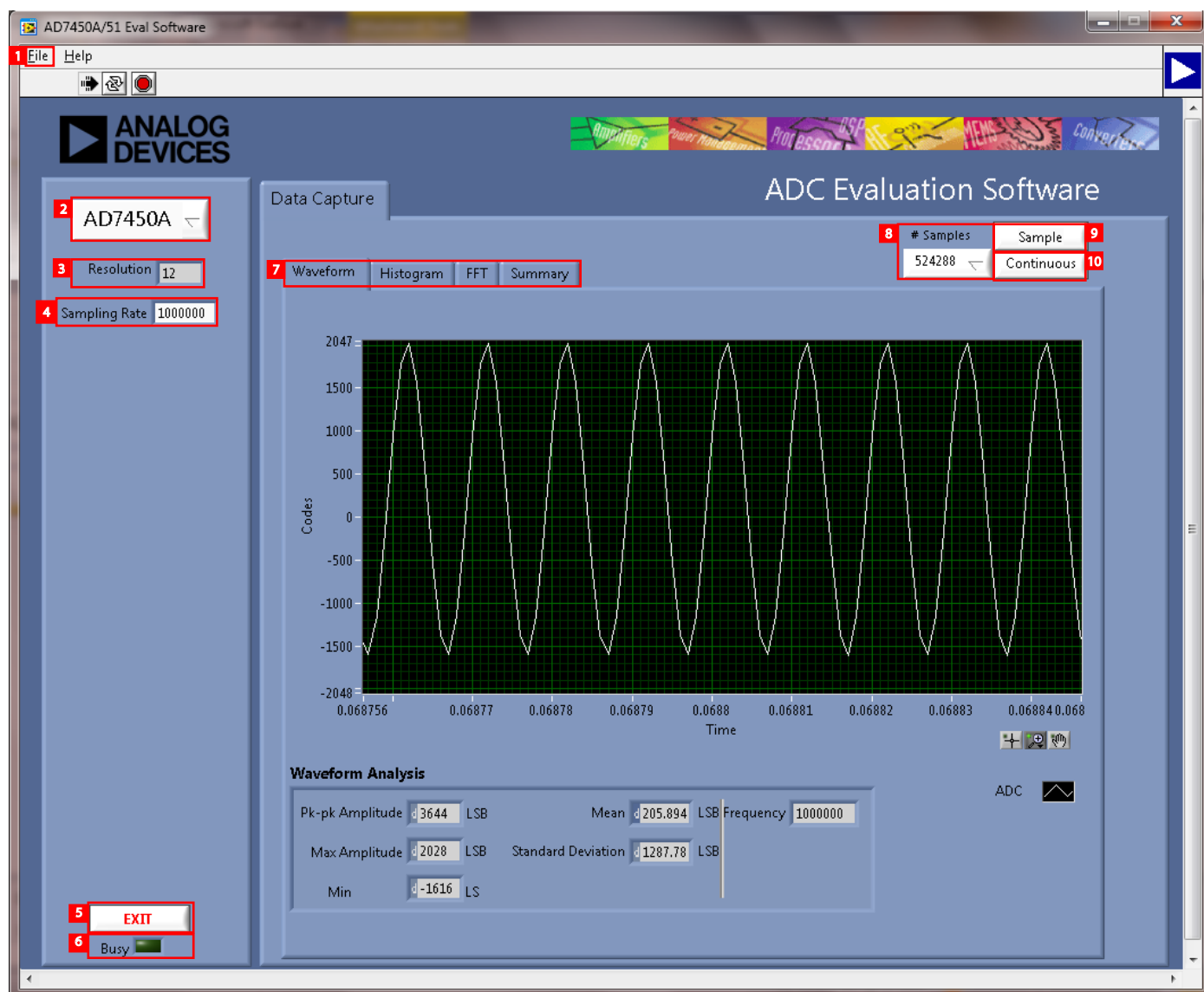


Figure 15. Setup Screen

DESCRIPTION OF USER SOFTWARE PANEL

The user software panel as shown in Figure 15 has the following features:

1. File menu with choice of;
 - a. Load data: load previously captured data in tsv (tab separated values) format for analysis
 - b. Save Data as .tsv: Save captured data in tsv (tab separated values) format for future analysis
 - c. Print Front Panel Picture. Use to print the front panel to your default printer.
 - d. Save Picture: Use to save the current screen capture
 - e. Exit
2. Use this drop down menu to select the generic AD7450A or AD7451.
3. Resolution of selected part is displayed
4. Sampling Rate. The default sampling frequency will match the max sample rate of the ADC selected from the drop down menu. User can adjust the sampling frequency, however there are limitations around the sample frequency where unusable sample frequencies are input, the software will automatically adjust the sample frequency accordingly. Units can be entered such as 10k for 10,000Hz etc. As the max sample frequency possible is device dependent, with some of the ADCs capable of operating up to 250ksps, while others can run to 1.3MSPS, the software will match the particular ADC ability. If the user enters a value larger

than the ability of the existing device, the software will indicate this and revert to the max Sample frequency.

5. Exit Button. Use this to exit the software. Alternatively , go to File->Exit
6. This LED indicates when a read is in progress from the EVAL-SDP-CB1Z board
7. There are four tabs available displaying the data in different formats, this are listed here and described in more detail later.
 - a. Waveform tab
 - b. Histogram
 - c. FFT

d. Summary

8. Select the number of samples to analyze.
9. “Sample” : to perform a single capture.
10. “Continuous” : to perform a continuous capture from the ADC. Press a second time to stop sampling

Within any of the Chart panels, the following tools allow user control of the different chart displays.



Is used for controlling the cursor if present



Is used for zooming in and out.



Is used for panning.

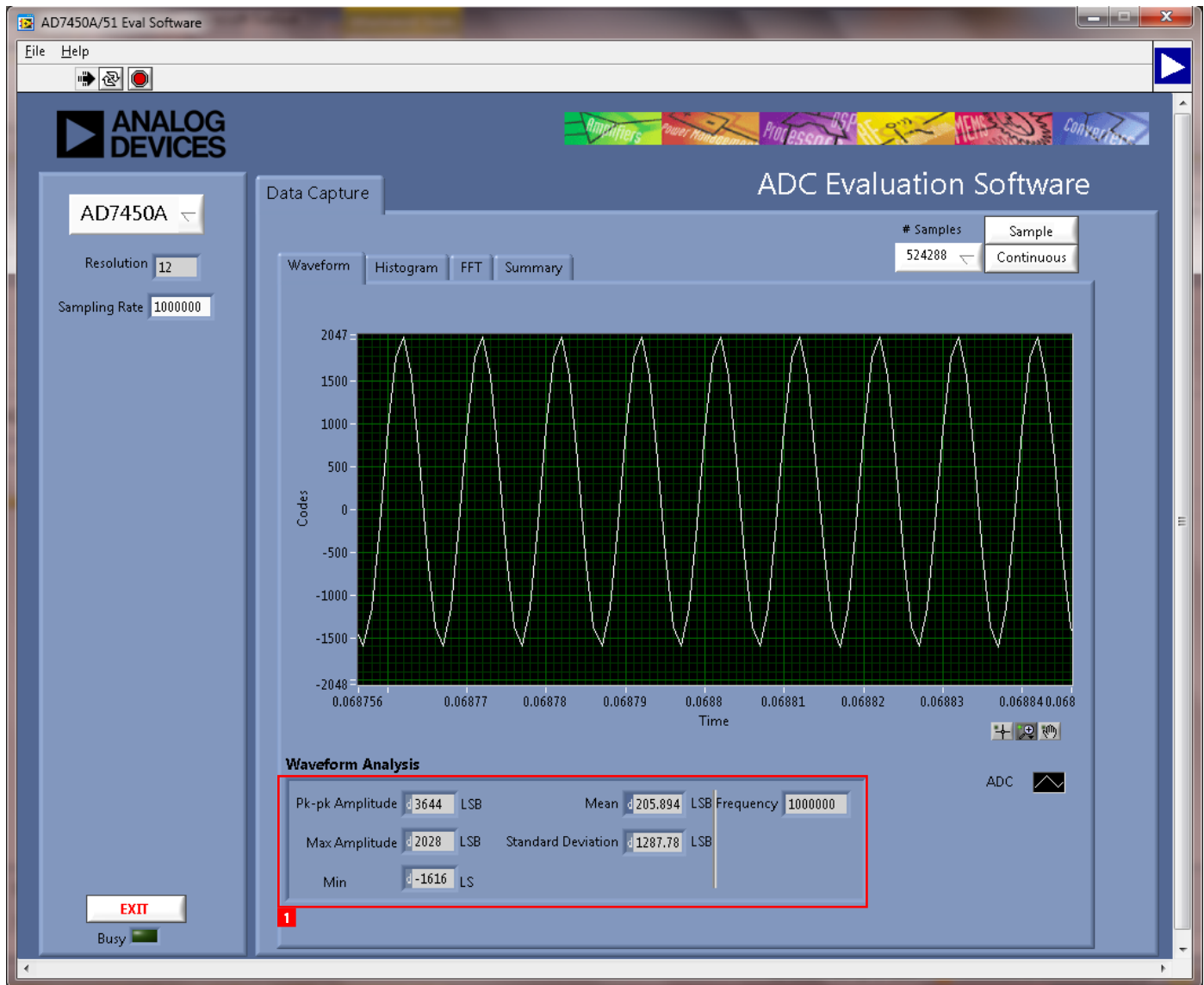


Figure 16. Waveform Capture Tab

WAVEFORM CAPTURE

Figure 16 illustrates the waveform capture tab. The input signal here is a 100kHz sine-wave.

The waveform analysis reports back the amplitudes recorded from the captured signal in addition to the frequency of the signal tone.

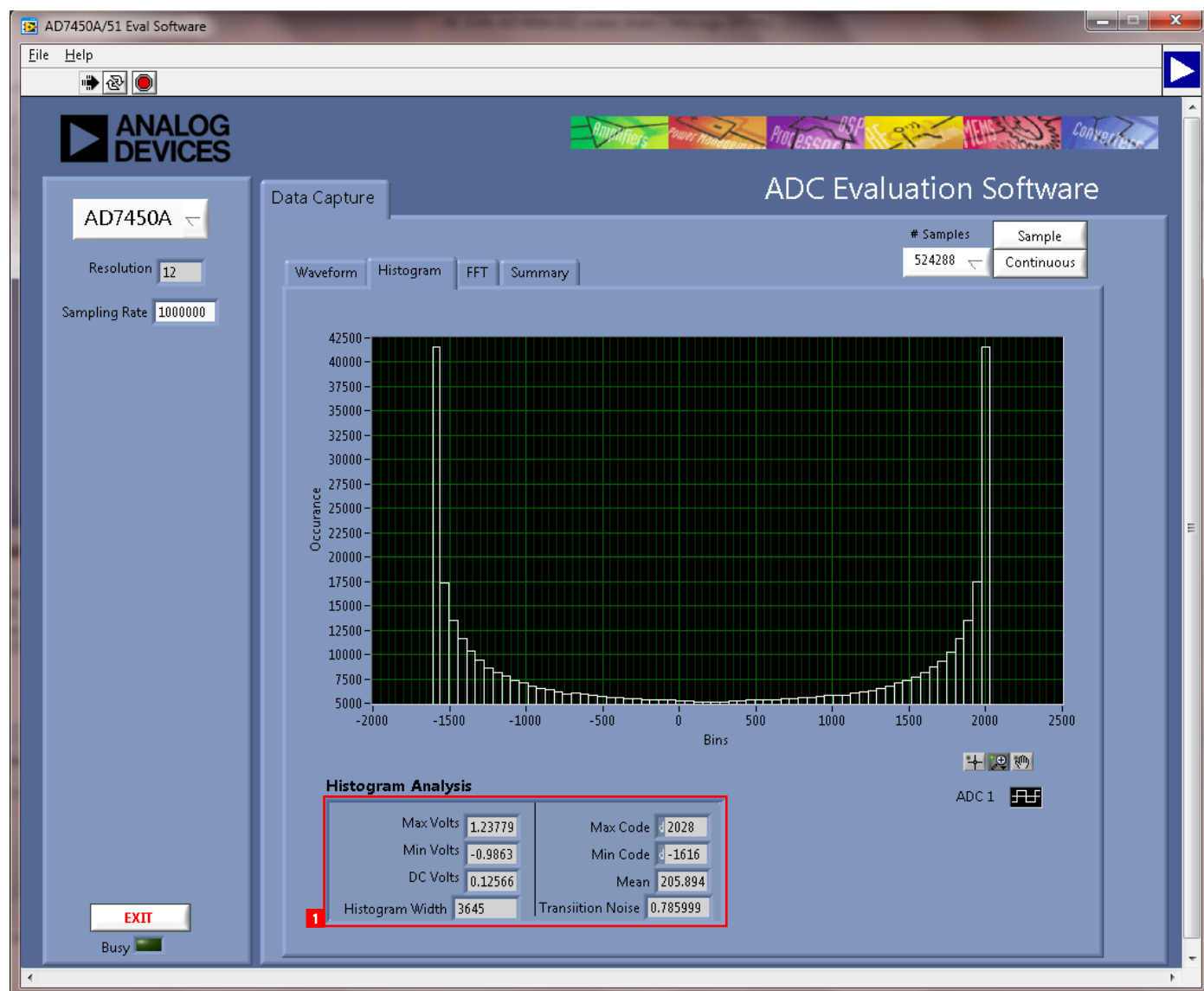


Figure 17. Histogram Capture Tab

AC TESTING - HISTOGRAM

Figure 17 shows the histogram capture tab. This tests the ADC for the code distribution for AC input and computes the mean and standard deviation, or transition noise of the converter and displays the results.

Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select "Histogram" tab from the test selection window and click on the "Start" button.

Note: an AC histogram needs a quality signal source applied to the input SK1/SK3 connectors. Figure 17 shows the histogram for a 50kHz sinewave applied to the ADC input and the results calculated.

1. Illustrates the different measured values for the data captured.

DC TESTING - HISTOGRAM

More commonly, the histogram would be used for DC testing. Where user tests the ADC for the code distribution for DC input and computes the mean and standard deviation, or transition noise of the converter and displays the results. Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select "Histogram" tab from the test selection window and click on the "Start" button.

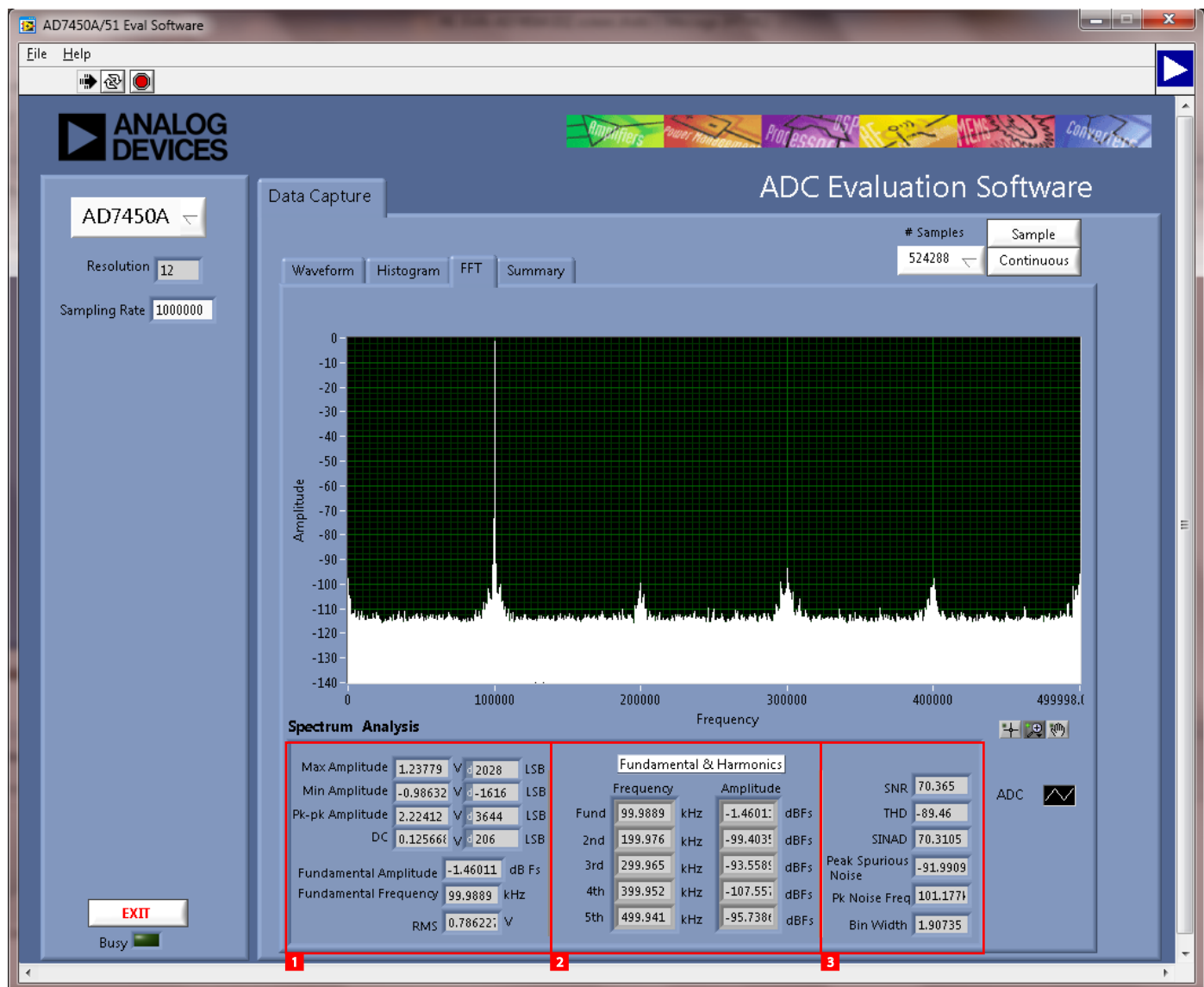


Figure 18. FFT Capture Tab

AC TESTING - FFT CAPTURE

Figure 18 shows the FFT capture tab. This tests the traditional AC characteristics of the converter and displays a Fast Fourier Transform (FFT) of the results. As in the histogram test, raw data is captured and passed to the PC where the FFT is performed displaying SNR, SINAD, THD and SFDR. To perform an AC test, apply a sinusoidal signal to the evaluation board at the SMB inputs J4/63. Low distortion, better than 115dB, is required to allow true evaluation of the part. One possibility is to filter the input signal from the AC source. There is no suggested band-pass filter but consideration should be taken in the choice. Furthermore, if using a low frequency

band-pass filter when the full-scale input range is more than a few Vpp, it is recommended to use the on board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

Figure 18 displays the results of the captured data.

1. Shows the input signal information
2. Displays the fundamental frequency and amplitude in addition to the 2nd to 5th harmonics.
3. Displays the performance data. SNR, Dynamic Range, THD, SINAD, Noise performance.

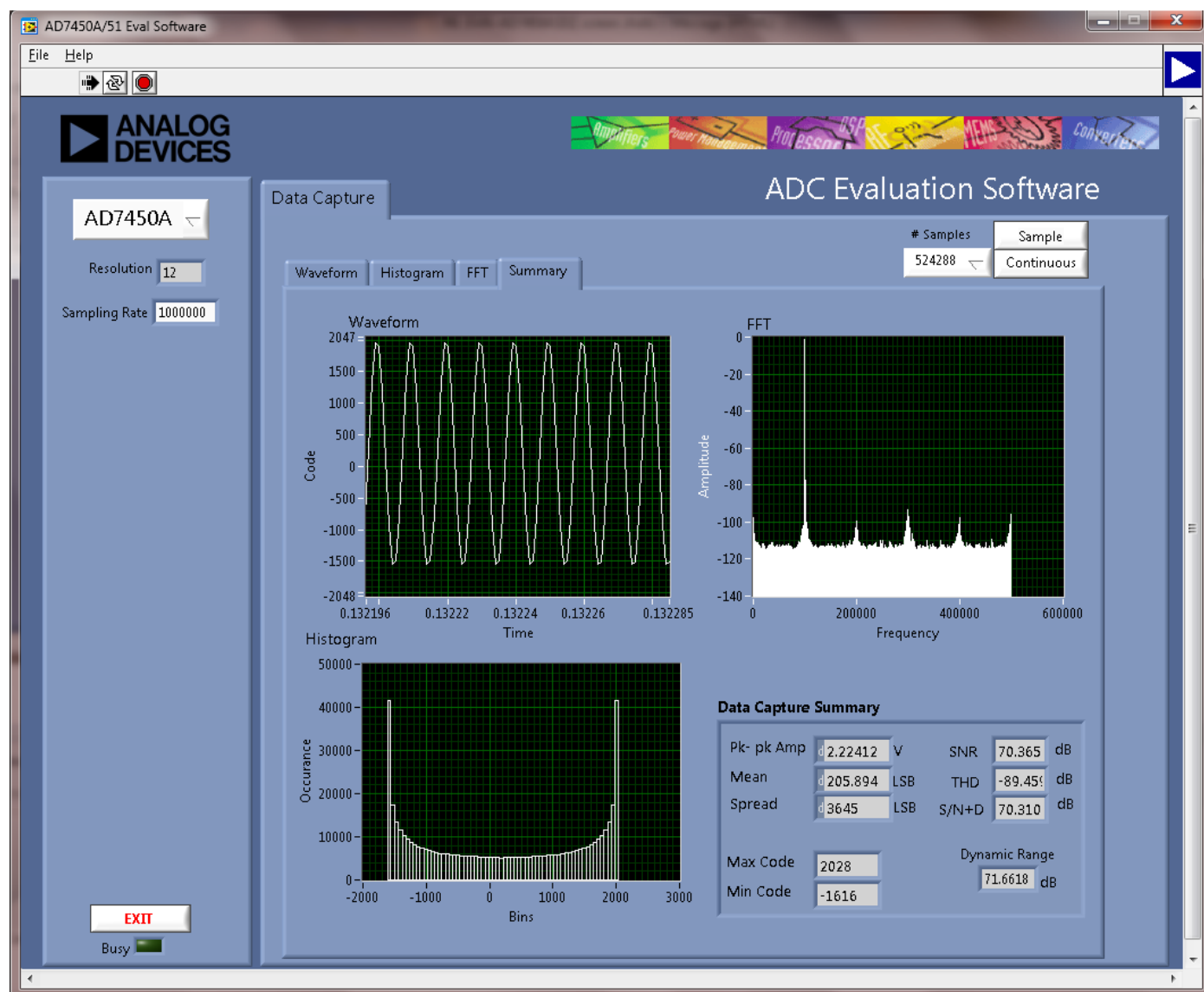


Figure 19. Summary Tab

SUMMARY TAB

Figure 19 shows the summary tab. The summary tab captures all the display information and provides them in one panel with a synopsis of the information including key performance parameters such as SNR and THD.

SAVE FILE

See Figure 20 The software can save the current captured data for later analysis; the file format is .tsv (tab-separated values).

User will be prompted with a Save dialog box and should save to an appropriate folder location

LOAD FILE

See Figure 21 User is prompted with a load dialog box. User may have to navigate to find these example files. The default location for the example files is C:\Program Files\Analog Devices\EVAL-AD7450A_51SDZ

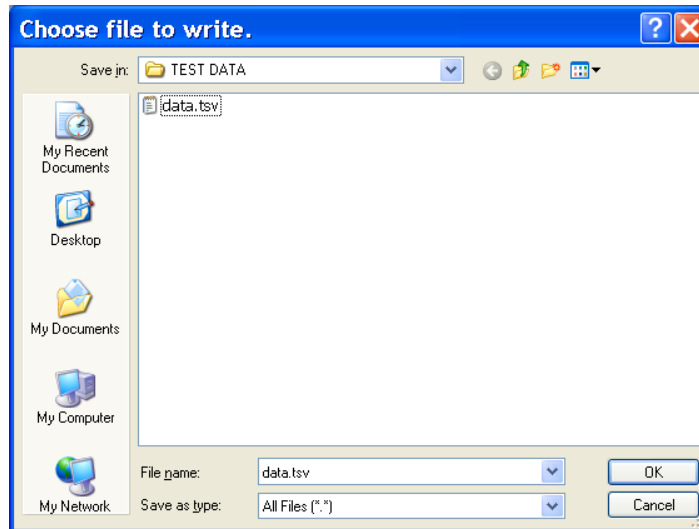


Figure 20 Save File dialog Box

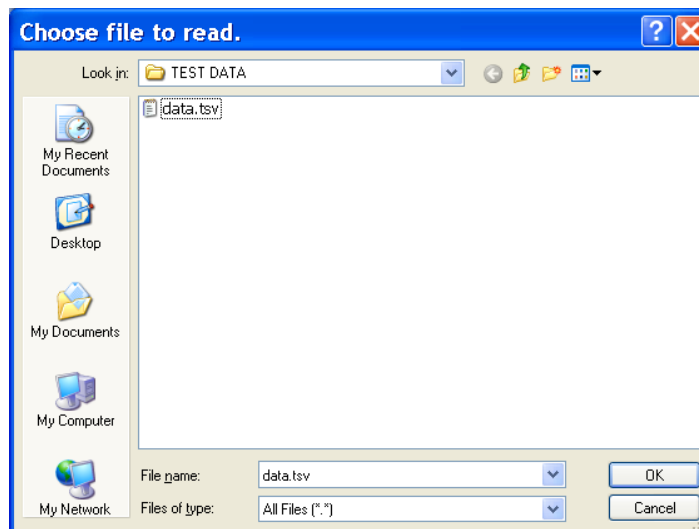
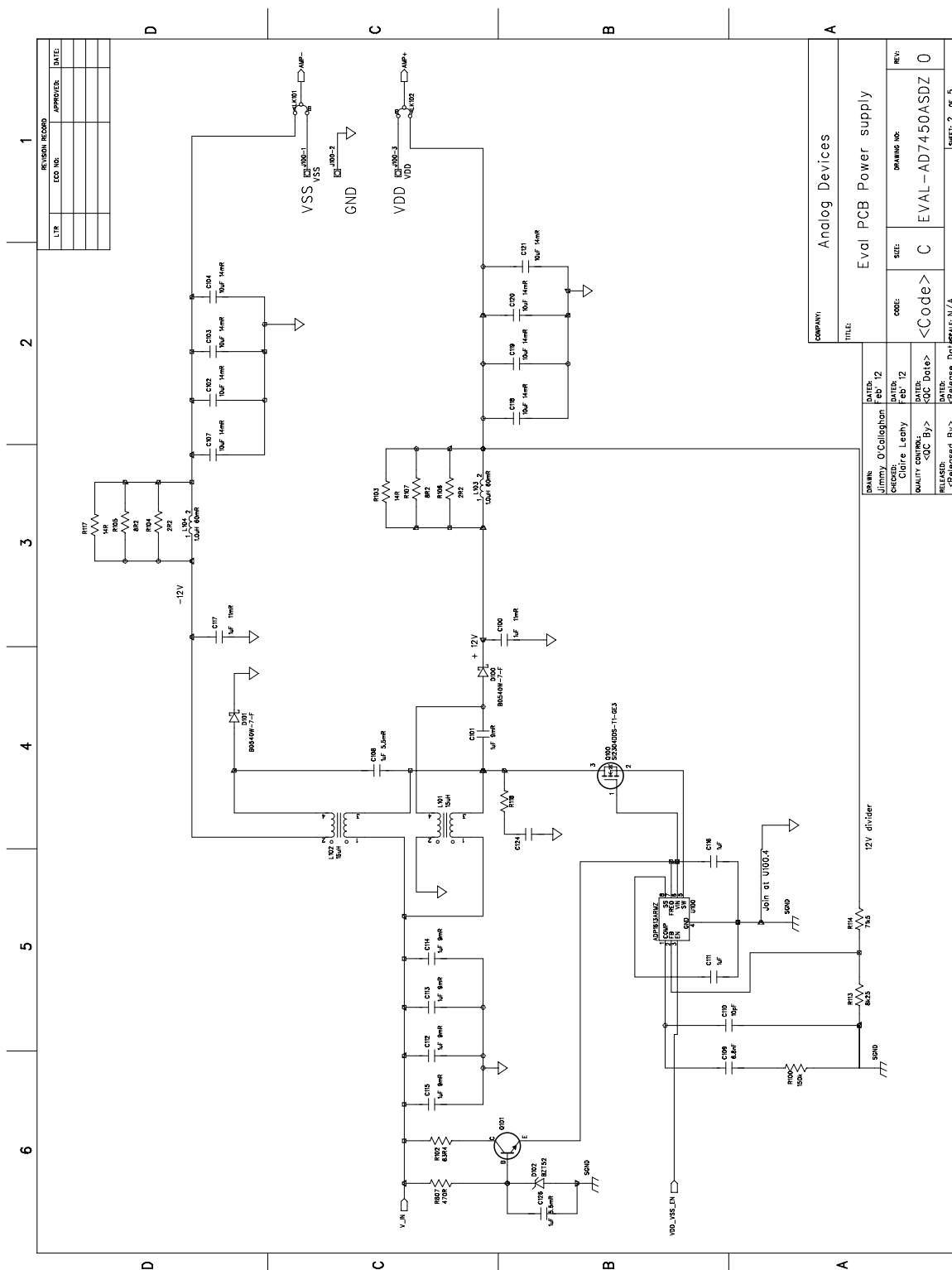
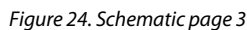


Figure 21 Load File Dialog Box





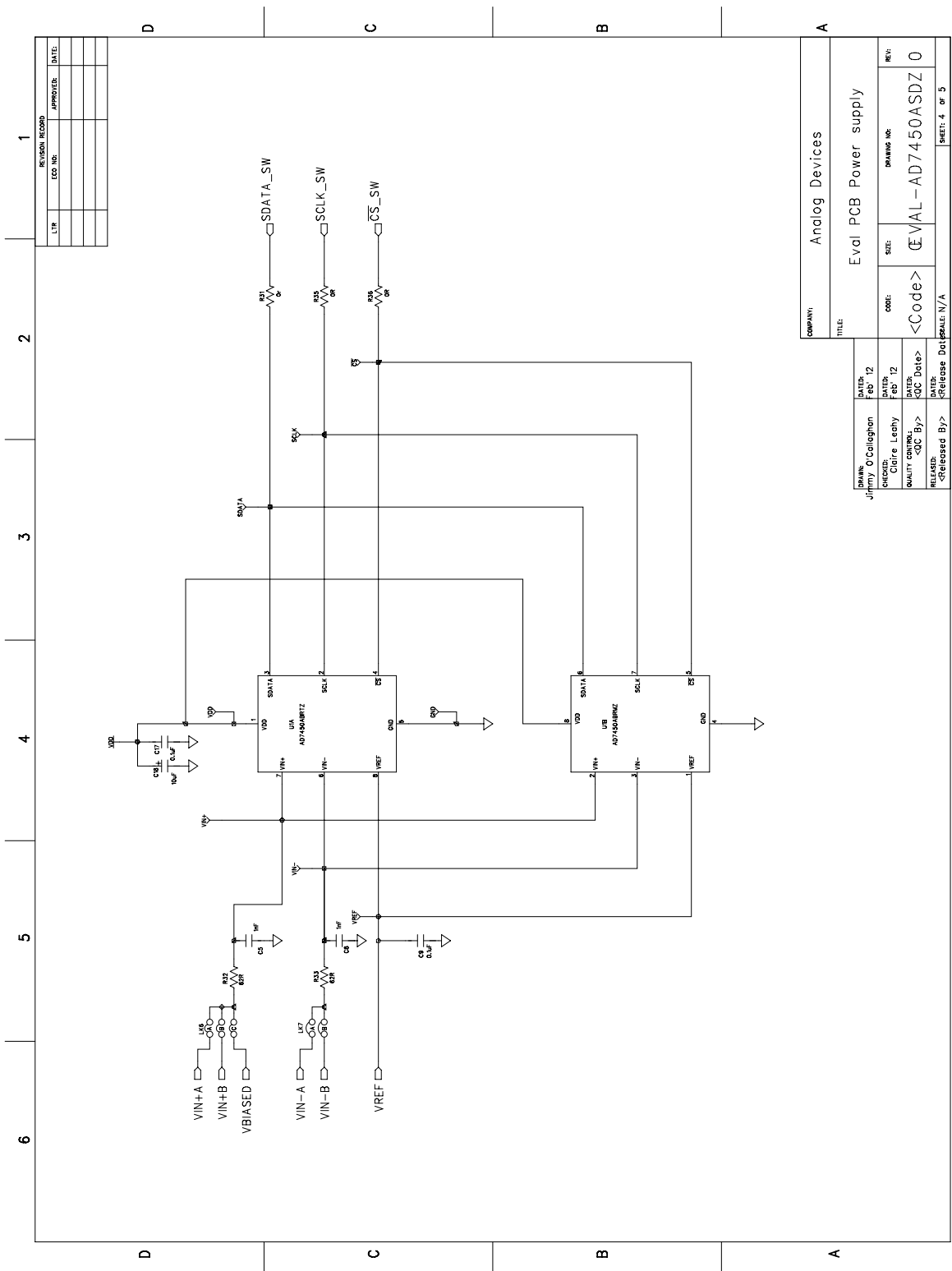


Figure 25 Schematic page 4

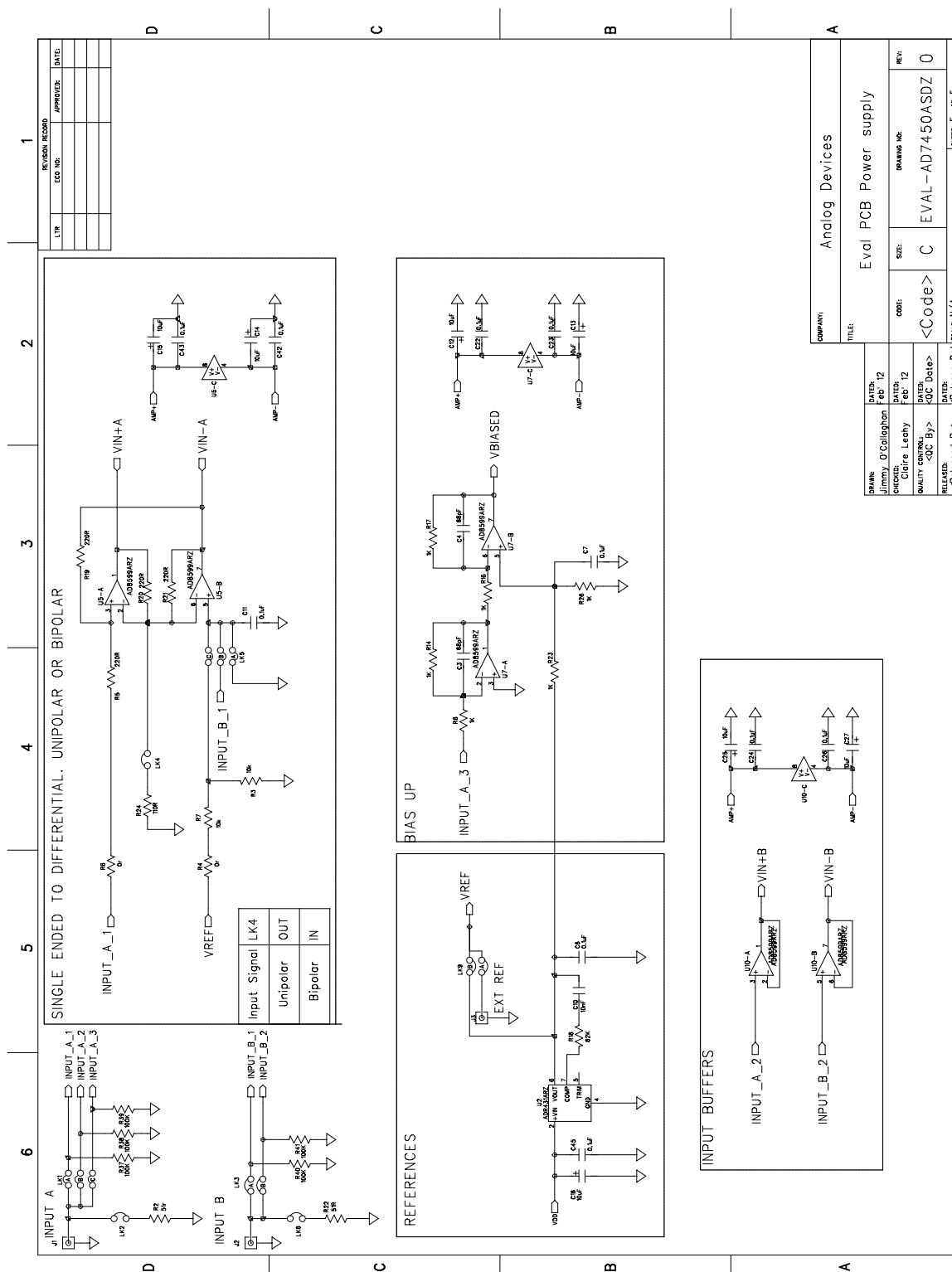
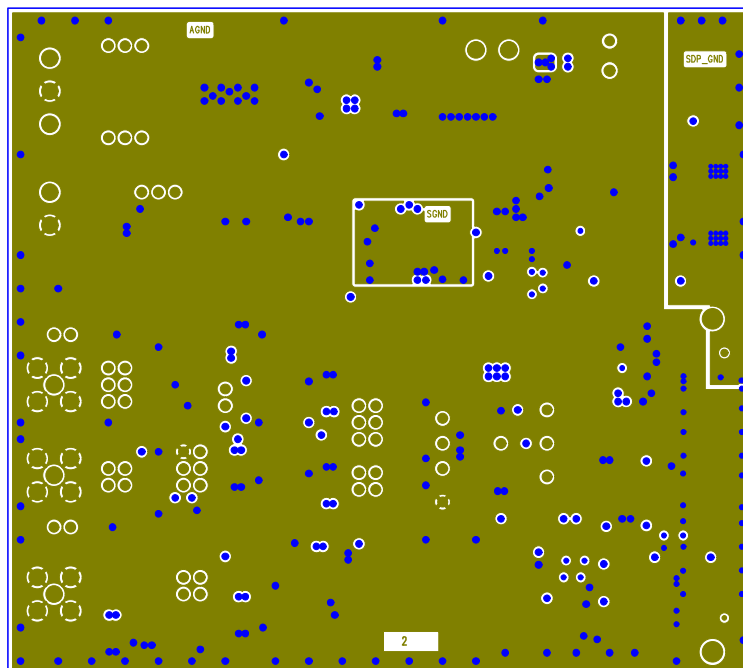
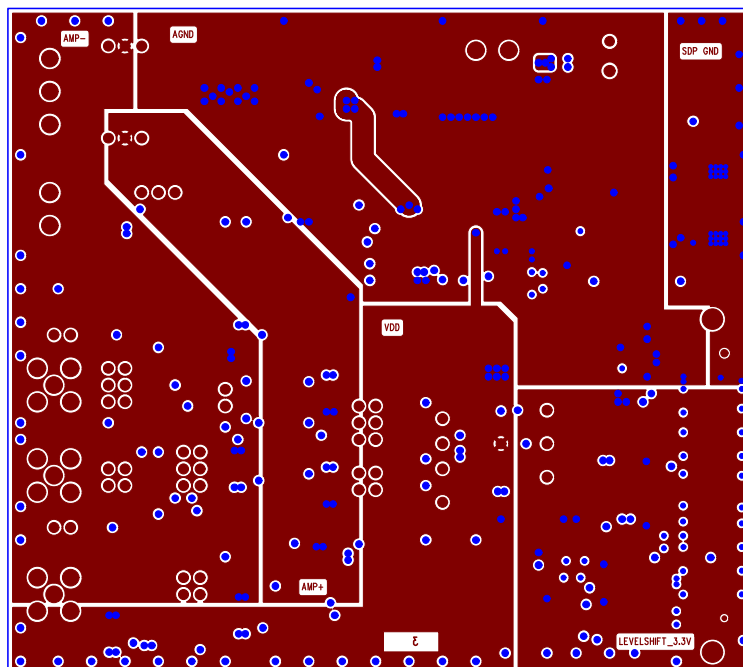


Figure 26 Schematic page 5



Eval-AD7450ASDZ (Rev. 0) Top Side View.
Layer 2 - Ground

Figure 29. Layer 2 Component Side view



Eval-AD7450ASDZ (Rev. 0) Top Side View.
Layer 3 - Power

Figure 30 Layer 3 Component side view

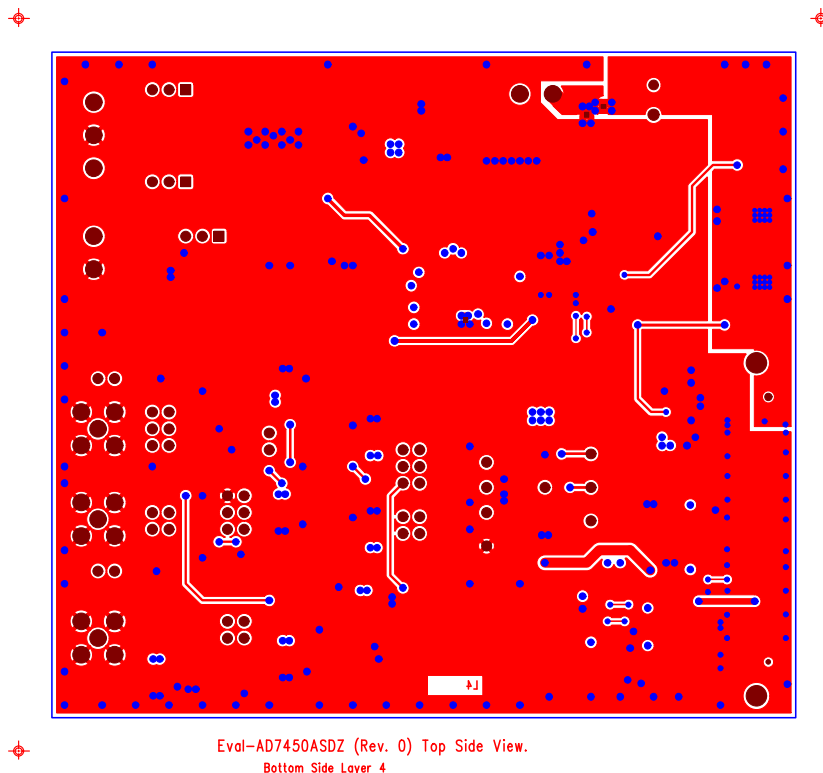


Figure 31 Layer 4 Component side view

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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