

	8	7	6	5	4	3	2	1																													
D	<div>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.</div>					<div>JUMPER TABLE</div> <table><tr><td>JP#</td><td>ON</td><td>OFF</td></tr><tr><td>1</td><td></td><td></td></tr><tr><td>2</td><td></td><td></td></tr><tr><td>3</td><td></td><td></td></tr><tr><td>4</td><td></td><td></td></tr><tr><td>5</td><td></td><td></td></tr></table>			JP#	ON	OFF	1			2			3			4			5			<div>REVISIONS</div> <table><tr><td>REV</td><td>DESCRIPTION</td><td>DATE</td><td>APPROVED</td></tr><tr><td>C</td><td>CHANGE AS PER ECR-099043</td><td>02/10/20</td><td>H.MIRONCZUK</td></tr></table>			REV	DESCRIPTION	DATE	APPROVED	C	CHANGE AS PER ECR-099043	02/10/20	H.MIRONCZUK
	JP#	ON	OFF																																		
	1																																				
	2																																				
	3																																				
	4																																				
	5																																				
	REV	DESCRIPTION	DATE	APPROVED																																	
	C	CHANGE AS PER ECR-099043	02/10/20	H.MIRONCZUK																																	
RELAY CONTROL CHART																																					
CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR																																	
C																																					
B																																					
A						<div>TEMPLATE ENGINEER -</div> <div>HARDWARE SERVICES -</div> <div>HARDWARE SYSTEMS -</div> <div>TEST ENGINEER -</div> <div>COMPONENT ENGINEER -</div> <div>TEST PROCESS -</div> <div>HARDWARE RELEASE</div> <div>DESIGNER -</div> <div>PTD ENGINEER &lt;PTD_ENGINEER&gt;</div> <div>CHECKER -</div>			<div>DATE</div>	<div>SCHEMATIC</div> <div>HW TYPE : Customer Evaluation Product(s): ADRV9002 : NAVASSA  PACKAGE : LeadCount-lead BodySize BGA-family : Pitch-pitch StyleVendor Style  &lt;User Define&gt; &lt;User Define&gt; &lt;User Define&gt;</div>		<div>ANALOG DEVICES</div>																									
						<div>MASTER PROJECT TEMPLATE TBD</div> <div>TESTER TEMPLATE no_template</div> <div>DRAWING NO. 02_063978-02</div> <div>REV. C</div>																															
	P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER	<div>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES</div> <div>TOLERANCES DECIMALS X.XX +0.010 X.XXX +-0.005 FRACTIONS +-1/32 ANGLES +-2</div>			<div>SIZE D</div> <div>SCALE 1:1</div> <div>CODE ID NO. CodeID</div>	SHEET 1 OF 11																											
	8	7	6	5	4	3	2	1																													

8 7 6 5 4 3 2 1

OVERVIEW

1.8V ANALOG  
1.8V DIGITAL  
1.3V ANALOG  
1.0V ANALOG  
1.0V DIGITAL  
3.3V CLOCK

POWER MANAGEMENT

ADCLK944BCPZ  
MCS FANOUT BUFFER

MCS ->  
3.3V CLOCK

PAGE 9-12

PAGE 6

<- TX1  
<- TX2  
RX 1A ->  
RX 1B ->  
RX 2A ->  
RX 2B ->  
EXT LO 1 ->  
EXT LO 2 ->

BALUN

AD9001  
INTEGRATED TRANSCEIVER

SWITCH

<- MCS\_EXT  
<- MCS

INTERFACE <->

ANALOG GPIO/AUX ADC/AUX DAC/MODEA  
TX/RX ENABLE/MODE/INT  
DIGITAL GPIO  
ARM JTAG  
SPI

HEADER  
HEADER  
HEADER  
HEADER  
HEADER

PAGE 7

FMC  
CONNECTOR

EEPROM  
BOARD ID

PAGE 8

3.3V CLOCK

ADCLK944BCPZ  
CLOCK FANOUT BUFFER

<- DEVICE CLK  
FPGA CLK ->  
TCXO/VCTCXO  
<- REF CLK

PAGE 6

ZYNQ FAN CONNECTOR  
VADJ MONITORING

PAGE 8

PAGE 3, 4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
C	CHANGE AS PER ECR-099043	02/10/20	H.MIRONCZUK

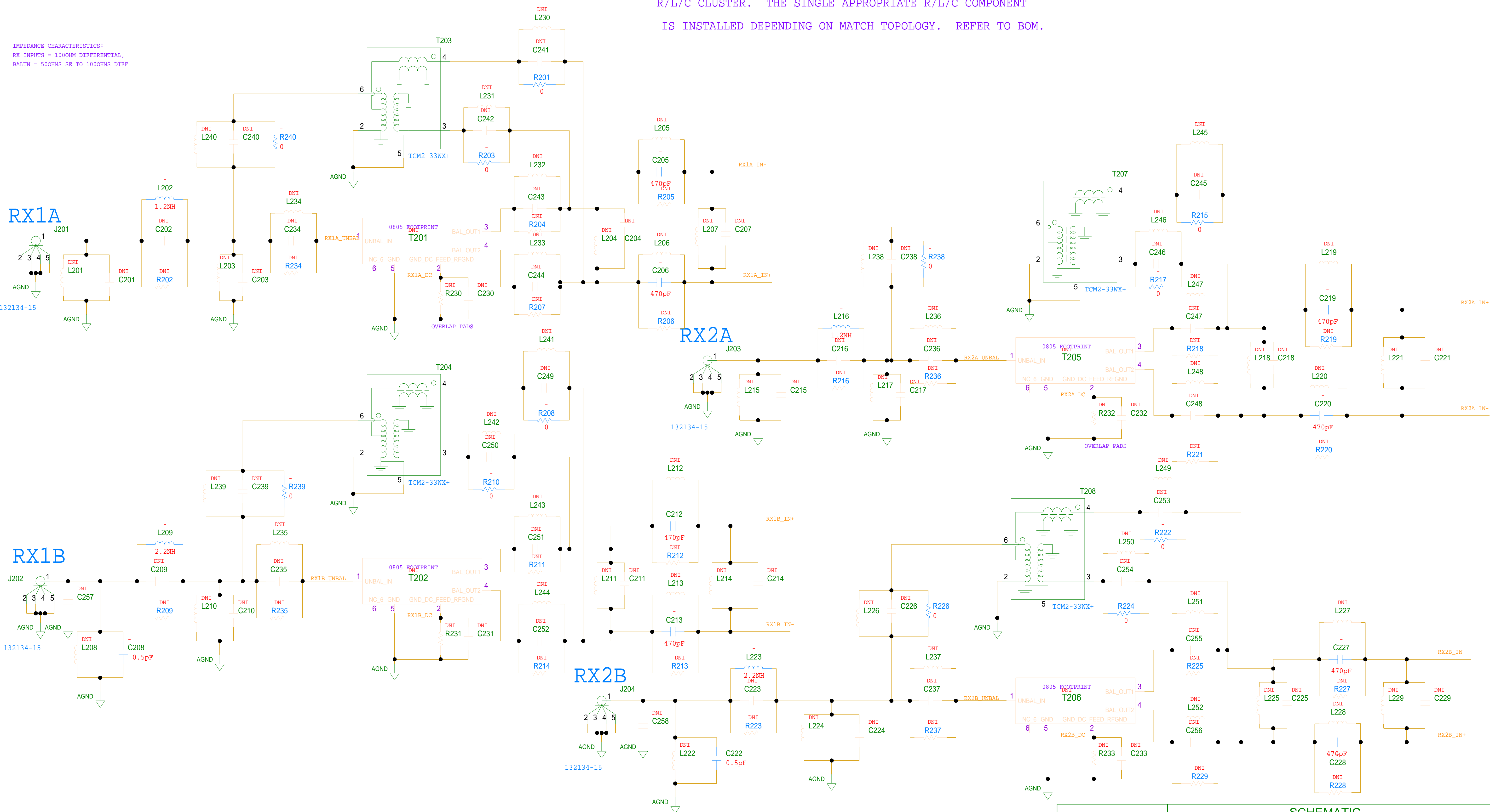
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HW TYPE : Customer Evaluation Product(s) : ADRV9002 : NAVASSA				
DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_063978-02	REV C	
PTD ENGINEER <PTD_ENGINEER>		SIZE D	SCALE 1:1	SHEET 2 OF 11

8 7 6 5 4 3 2 1

# RF IO

IMPEDANCE CHARACTERISTICS:  
RX INPUTS = 100OHM DIFFERENTIAL,  
BALUN = 50OHMS SE TO 100OHMS DIFF

ONLY 1 SET OF MOUNTING PADS EXISTS ON THE PCB PER  
R/L/C CLUSTER. THE SINGLE APPROPRIATE R/L/C COMPONENT  
IS INSTALLED DEPENDING ON MATCH TOPOLOGY. REFER TO BOM.



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
C	CHANGE AS PER ECR-099043	02/10/20	H.MIRONCZUK

SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : ADRV9002 : NAVASSA			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_063978-02	REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 3 OF 11

# RF IO

## RF OUTPUT 1

## RF OUTPUT 2

## LO1 INPUT

## LO2 INPUT

### TOP SIDE

### BOTTOM SIDE

### TOP SIDE

### BOTTOM SIDE

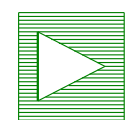
ONLY 1 SET OF MOUNTING PADS EXISTS ON THE PCB PER R/L/C CLUSTER. THE SINGLE APPROPRIATE R/L/C COMPONENT IS INSTALLED DEPENDING ON MATCH TOPOLOGY. REFER TO BOM.

IMPEDANCE CHARACTERISTICS:  
EXTERNAL LO INPUTS = 100OHM DIFFERENTIAL,  
BALUN = 50OHMS SE TO 100OHMS DIFF

### REVISIONS

REV	DESCRIPTION	DATE	APPROVED
C	CHANGE AS PER ECR-099043	02/10/20	H.MIRONCZUK

IMPEDANCE CHARACTERISTICS:  
TX OUTPUTS = 50OHM DIFFERENTIAL,  
BALUN = 50OHMS SE TO 50OHMS DIFF



ANALOG  
DEVICES

### SCHEMATIC

HW TYPE : Customer Evaluation  
Product(s): ADRV9002  
: NAVASSA

DESIGN VIEW

<DESIGN\_VIEW>

PTD ENGINEER  
<PTD\_ENGINEER>

DRAWING NO.

02\_063978-02

REV

C

SIZE

D

SCALE

1:1

SHEET

4

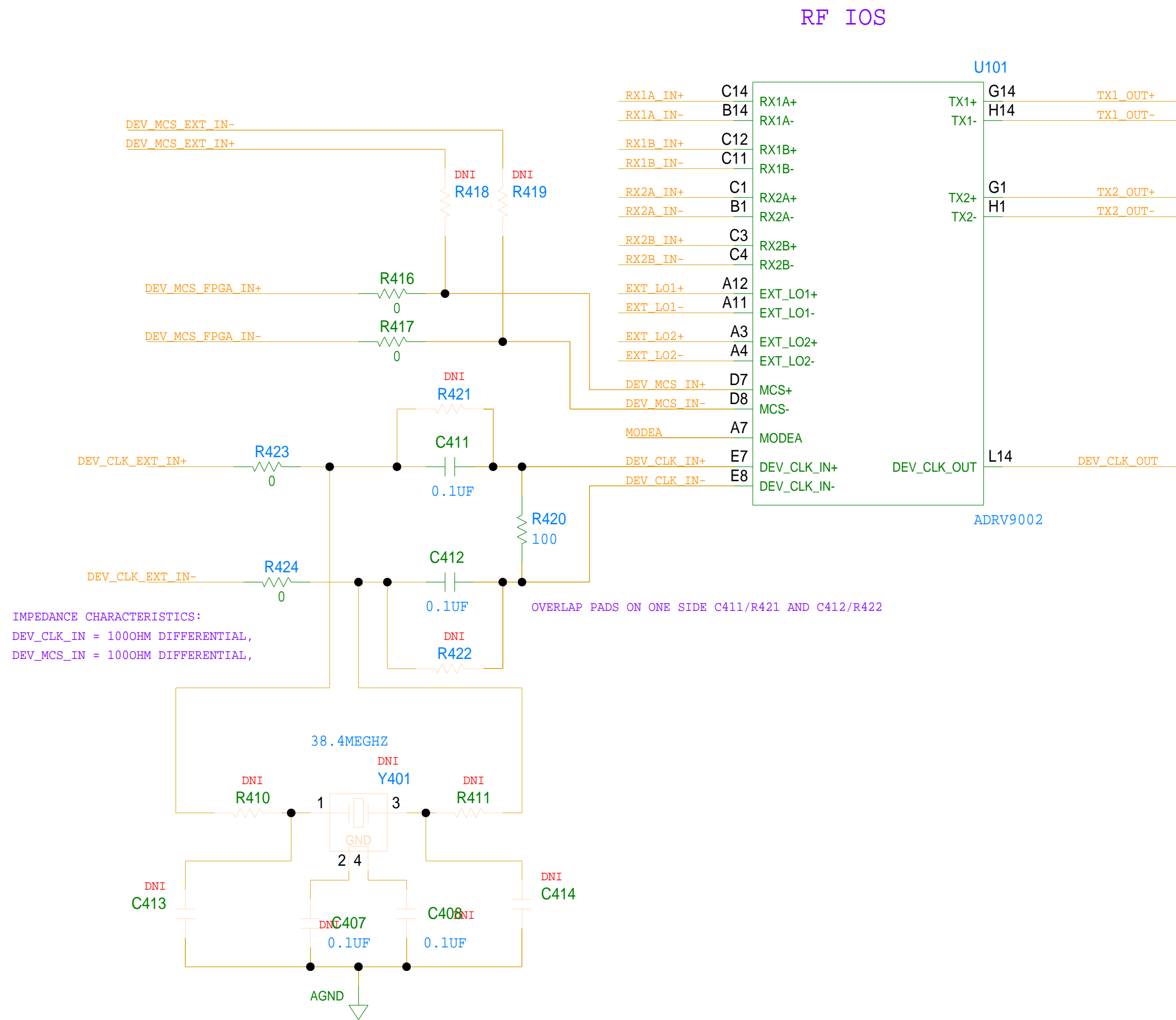
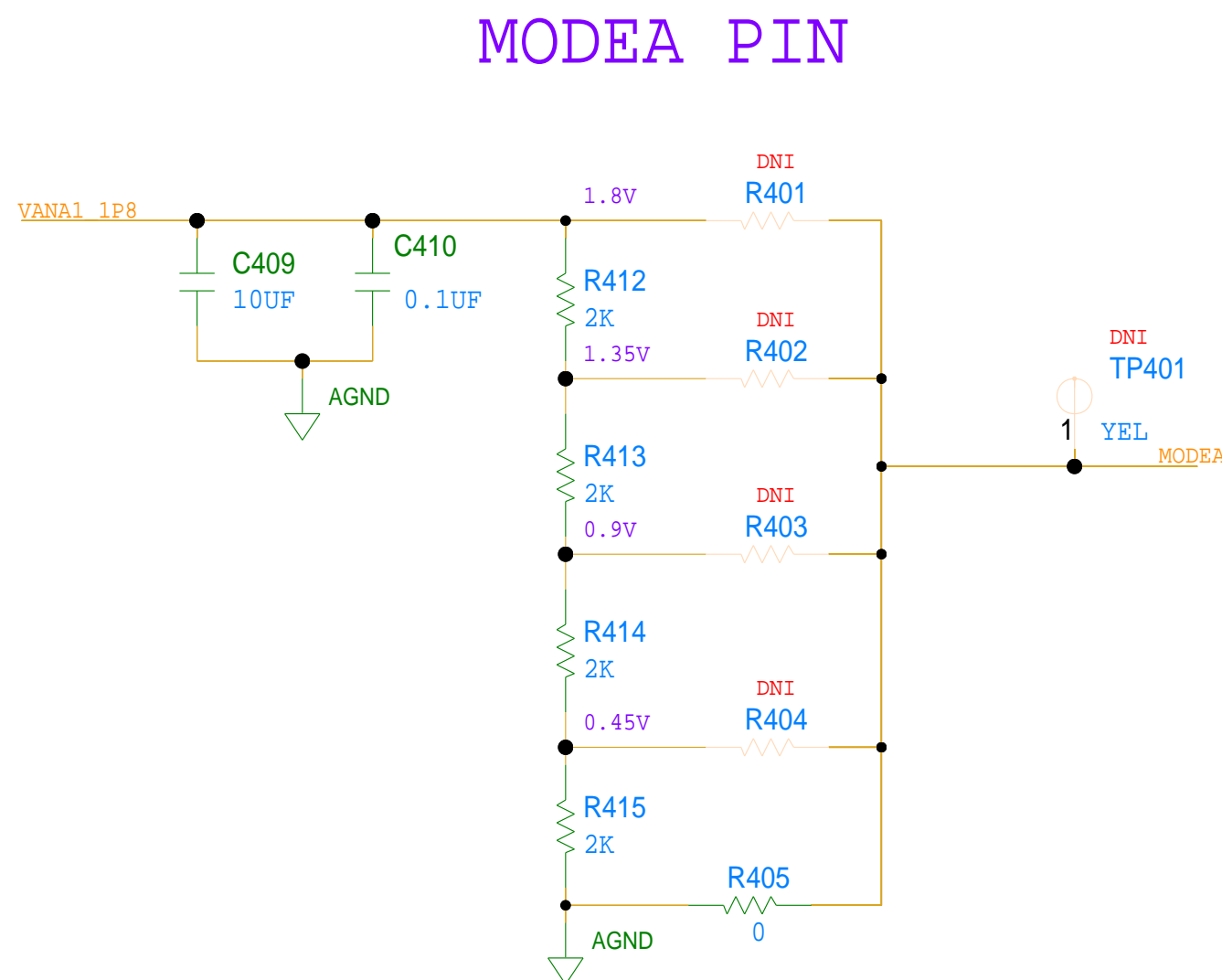
OF

11



DEVICE CLOCK INPUT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
C	CHANGE AS PER ECR-099043	02/10/20	H.MIRONCZUK



XTAL CONNECTION

SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : ADRV9002 : NAVASSA			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_063978-02	REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 5 OF 11

# DEVICE CLOCK/MCS DISTRIBUTION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
C	CHANGE AS PER ECR-099043	02/10/20	H.MIRONCZUK

## DEVICE CLK FANOUT

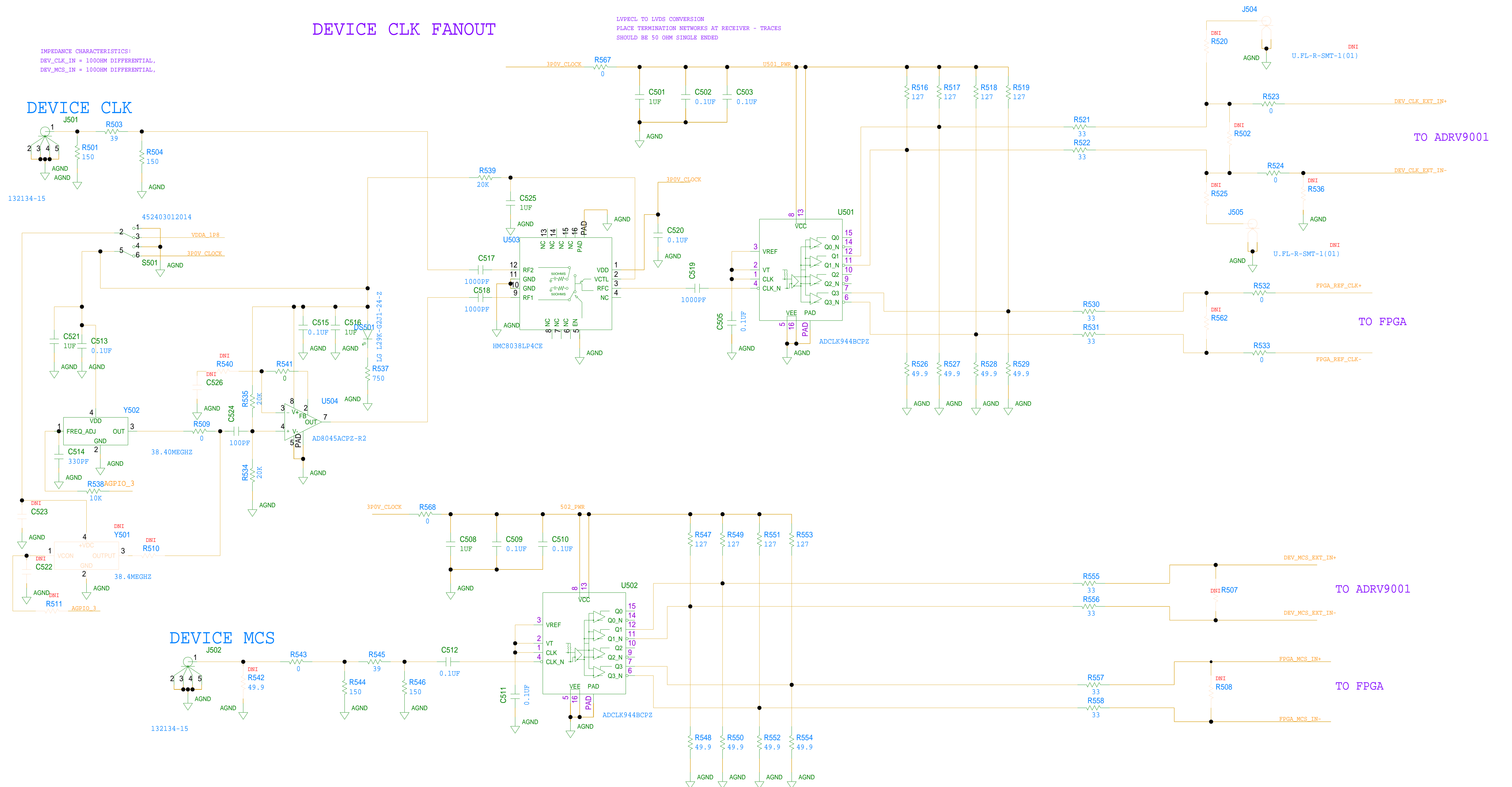
LVPECL TO LVDS CONVERSION  
PLACE TERMINATION NETWORKS AT RECEIVER - TRACES  
SHOULD BE 50 OHM SINGLE ENDED

DEVICE CLK


```

IMPEDANCE CHARACTERISTICS:
DEV_CLK_IN = 100OHM DIFFERENTIAL,
DEV_MCS_IN = 100OHM DIFFERENTIAL,

```

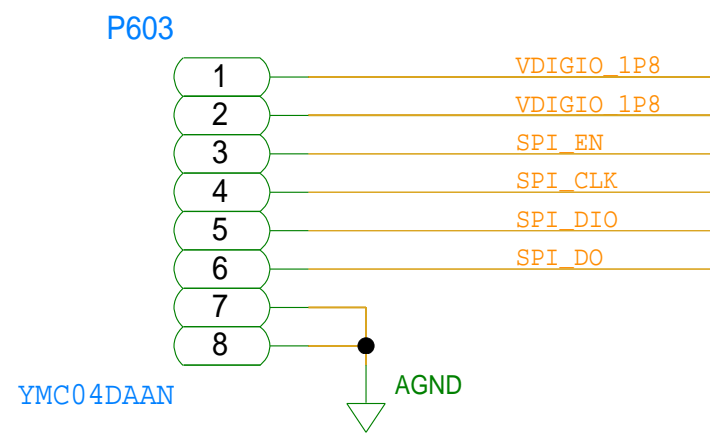


## DEVICE MCS FANOUT

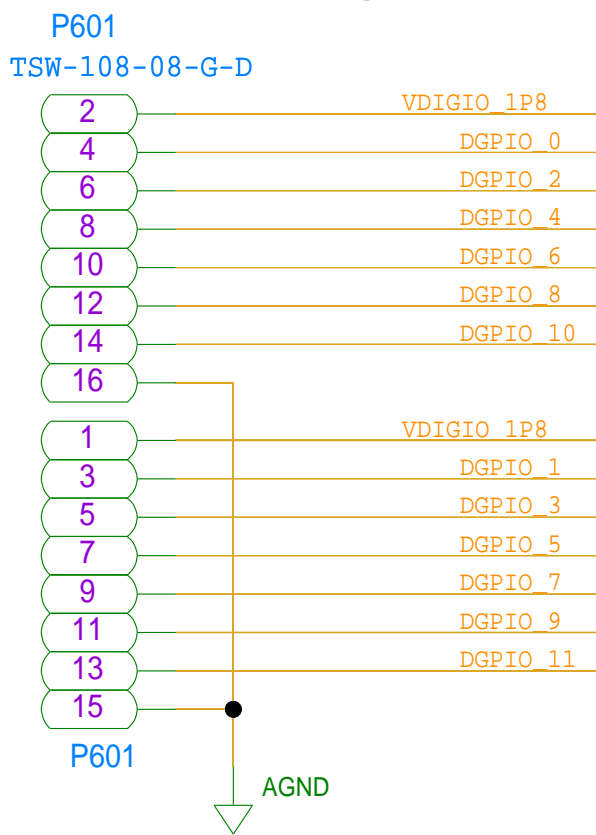
 <b>ANALOG DEVICES</b>	<h1 style="text-align: center;">SCHEMATIC</h1>			
	<p>HW TYPE : Customer Evaluation          Product(s) : ADRV9002          : NAVASSA</p>			
<small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.          IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR          IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,          OR FOR ANY OTHER UNLAWFUL PURPOSES, TO THE EXTENTS          OF ANALOG DEVICES.          THE SCHEMATIC SYMBOLS, DESIGN MAY BE PROTECTED BY PATENTS          OWNED OR CONTROLLED BY ANALOG DEVICES.</small>	<b>DESIGN VIEW</b> <b>&lt;DESIGN_VIEW&gt;</b>	<b>DRAWING NO.</b> <b>02_063978-02</b>		<b>REV</b> <b>C</b>
	<b>PTD ENGINEER</b> <b>&lt;PTD_ENGINEER&gt;</b>	<b>SIZE</b> <b>D</b>	<b>SCALE</b> <b>1:1</b>	<b>SHEET 6 OF 11</b>

# GPIO

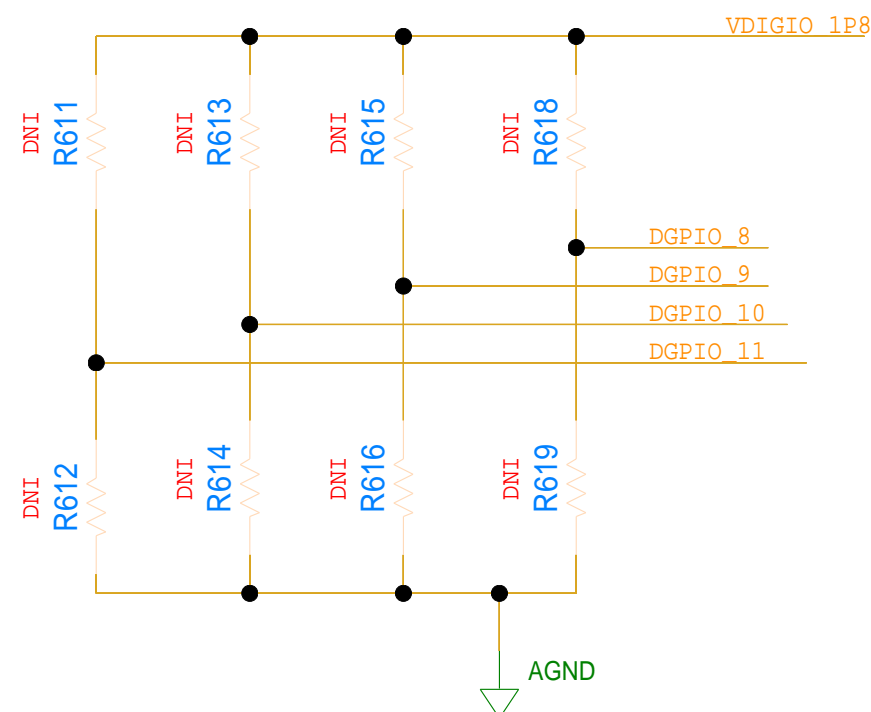
## SPI INTERFACE



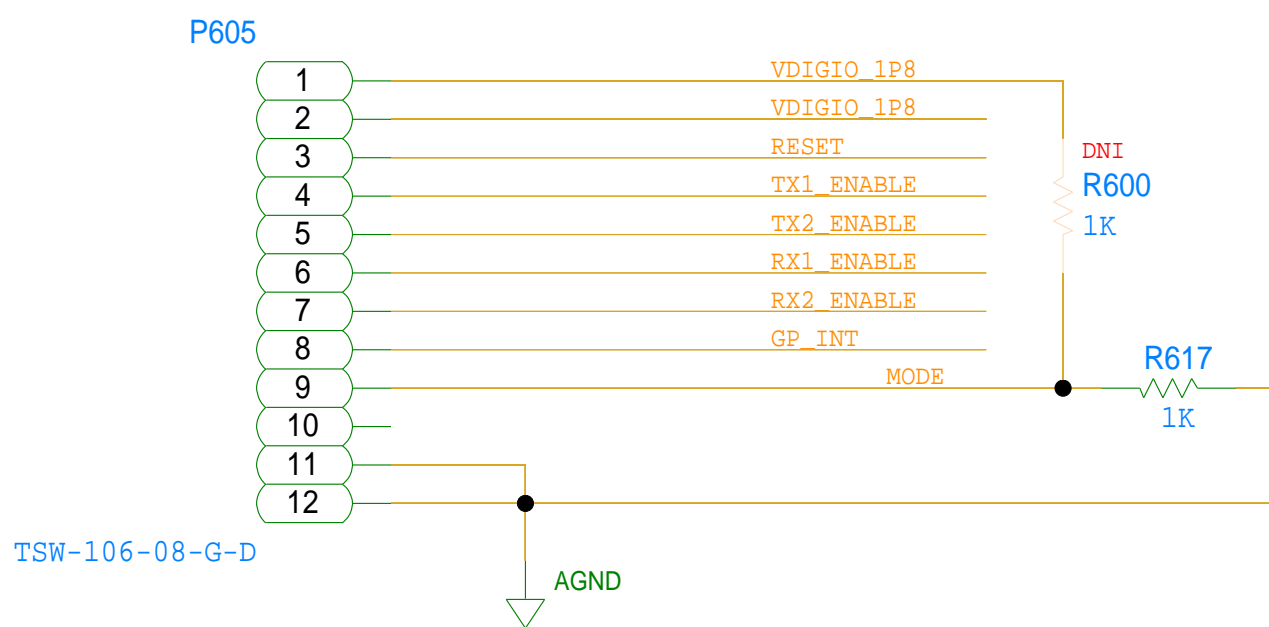
## DIGITAL GPIO



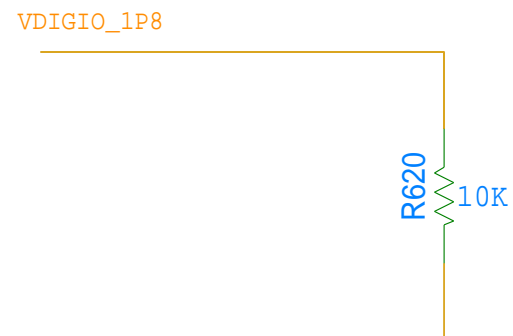
## ANALOG GPIO



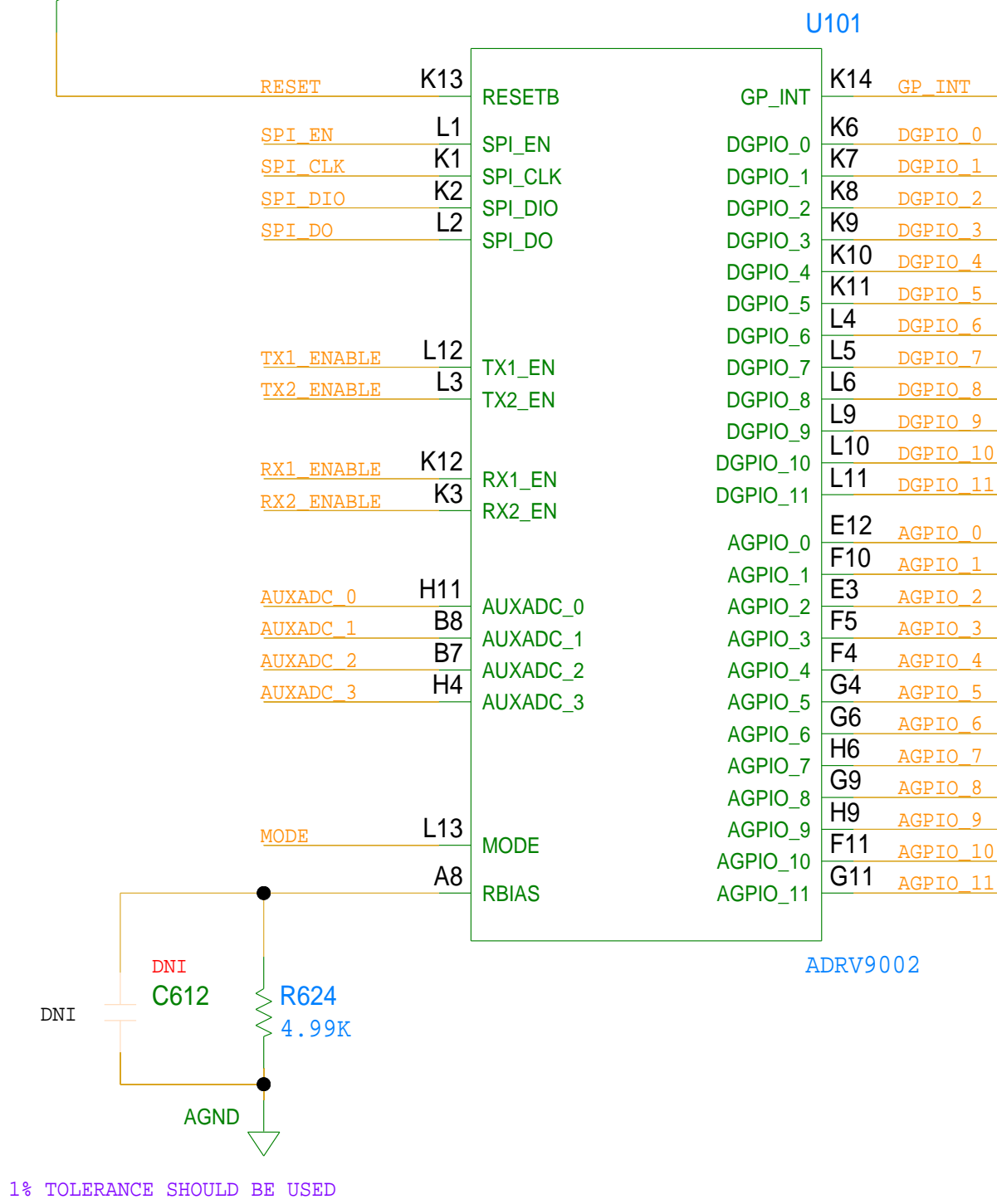
## ENABLES/GPINT/RESETB



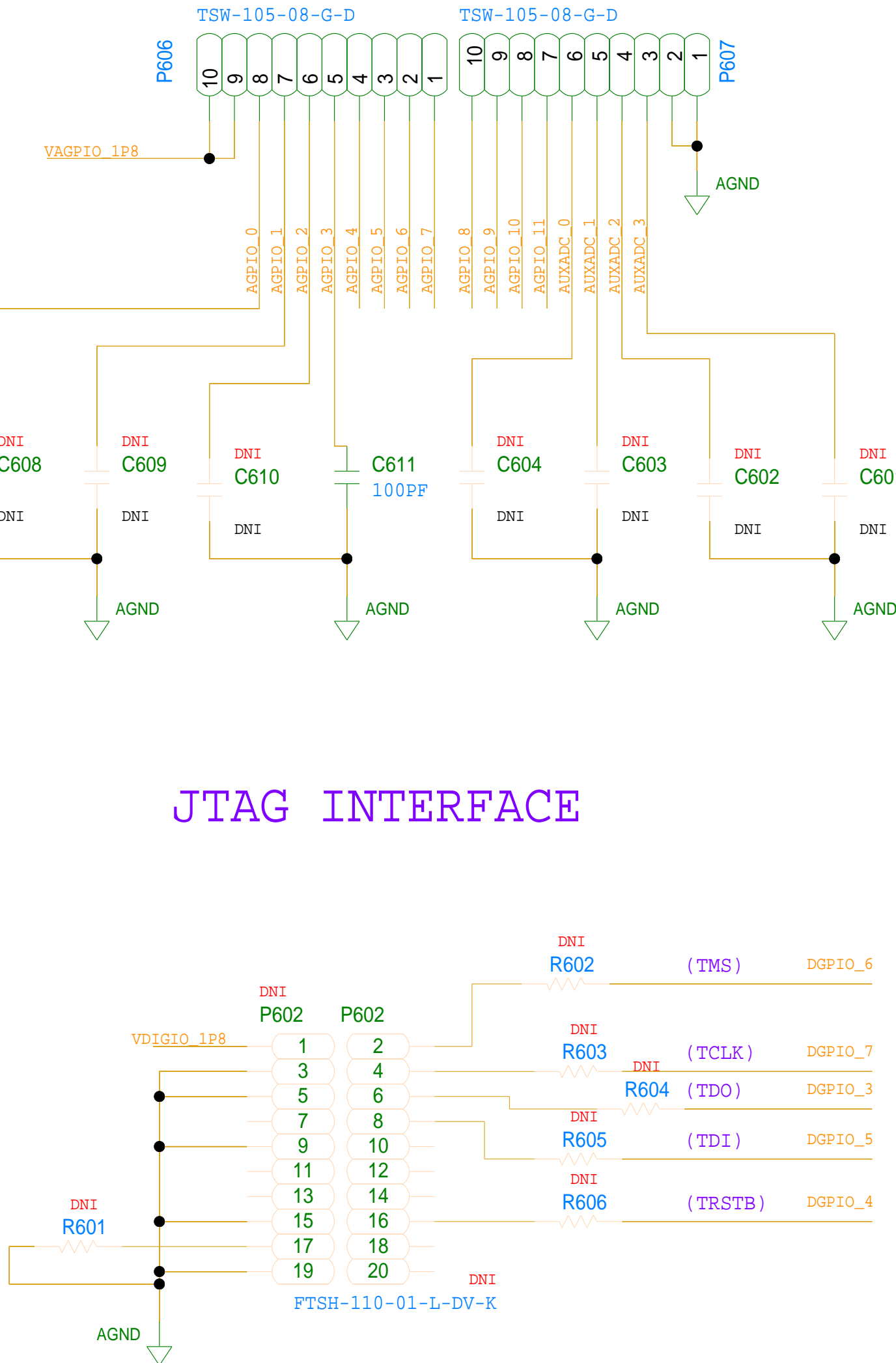
## RESETB



## CONTROL AND GPIOs



## JTAG INTERFACE



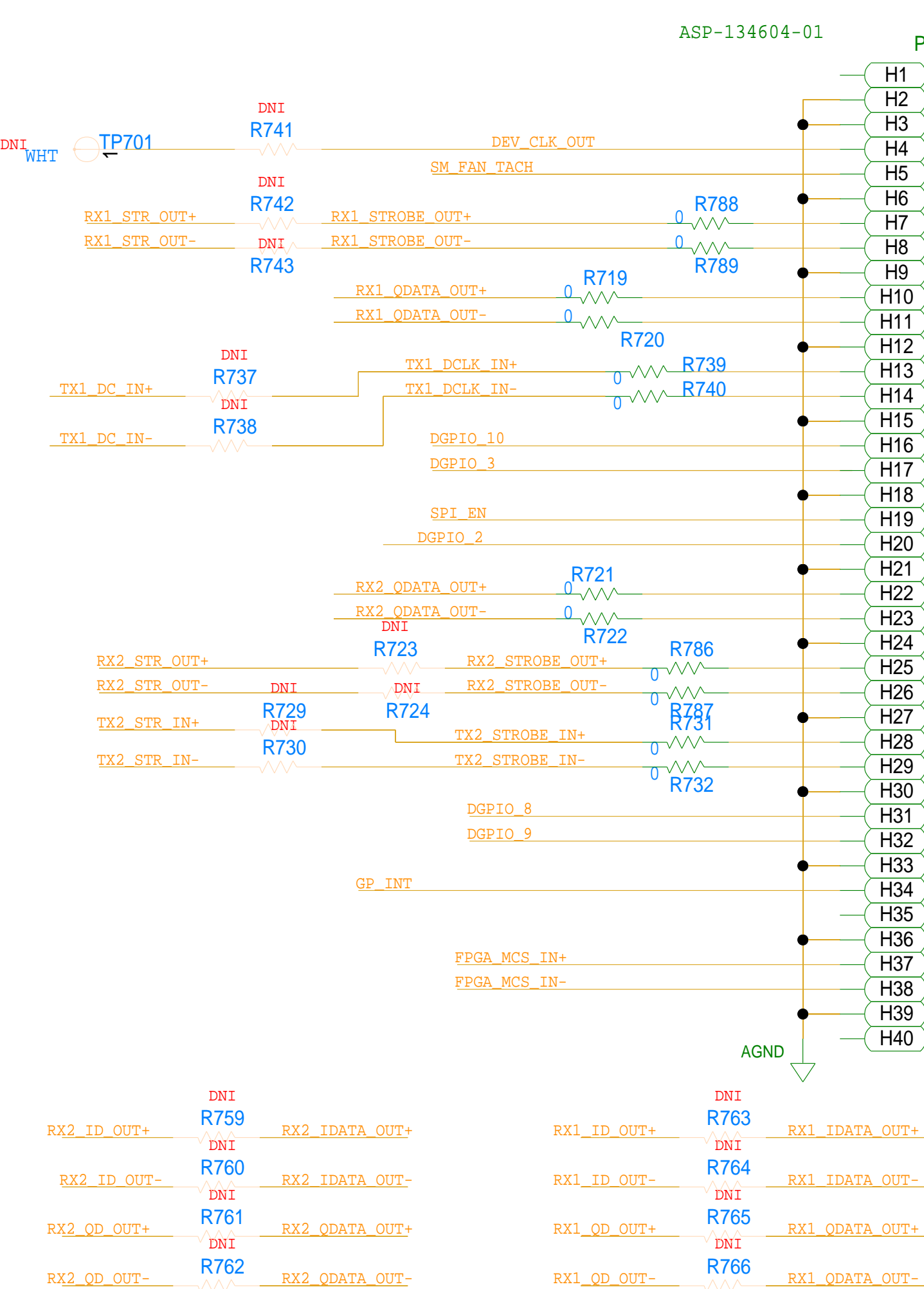
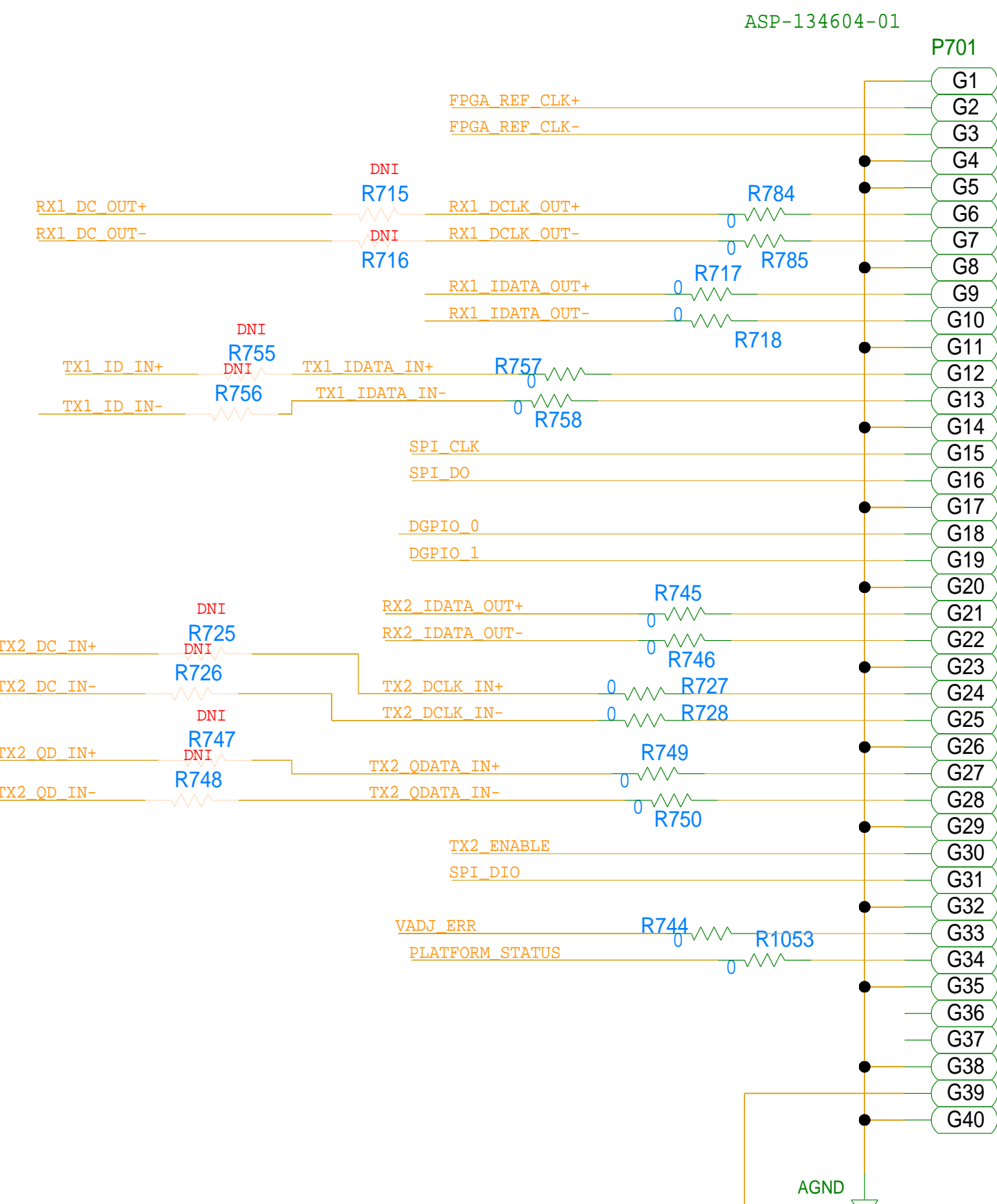
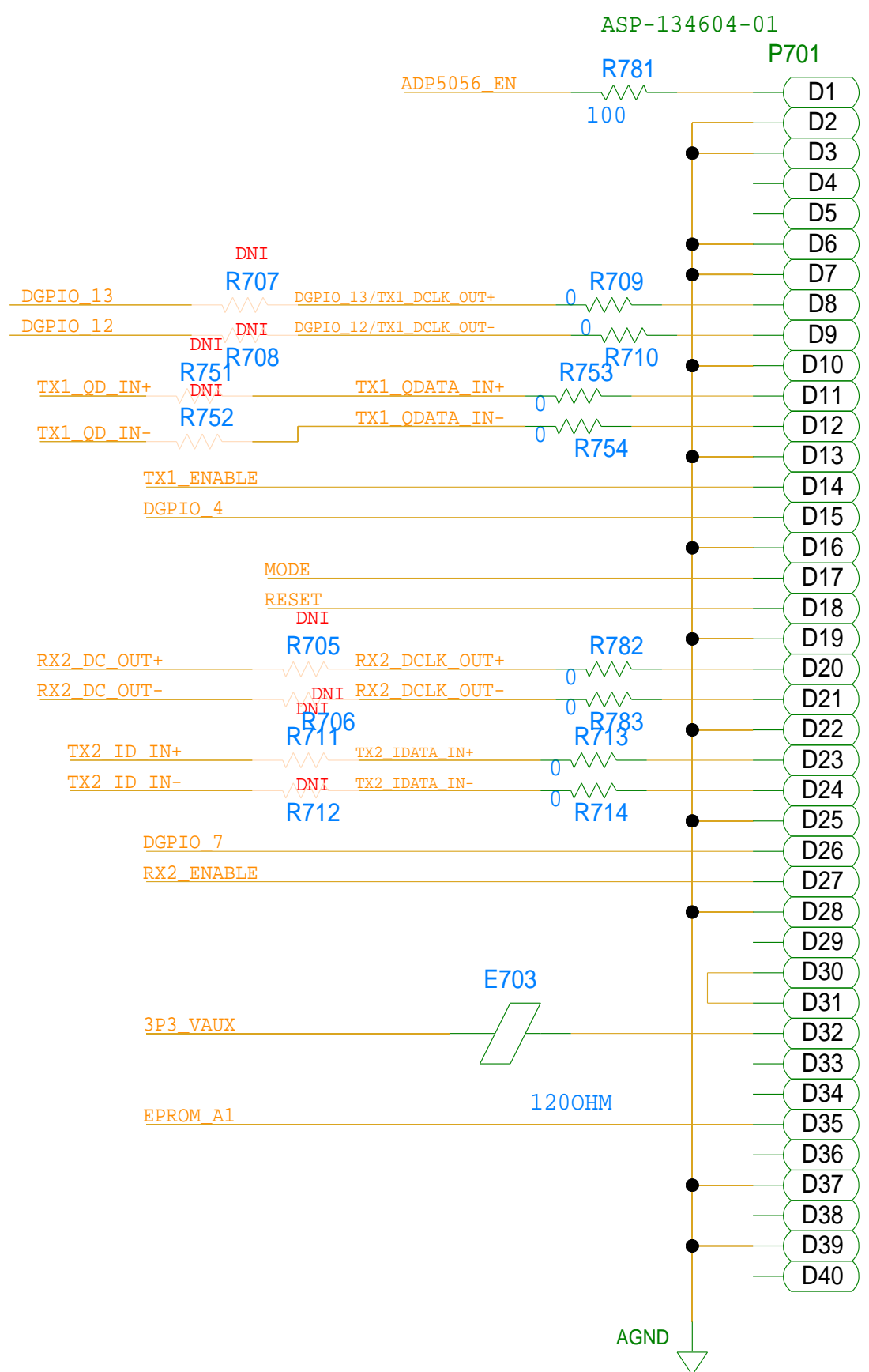
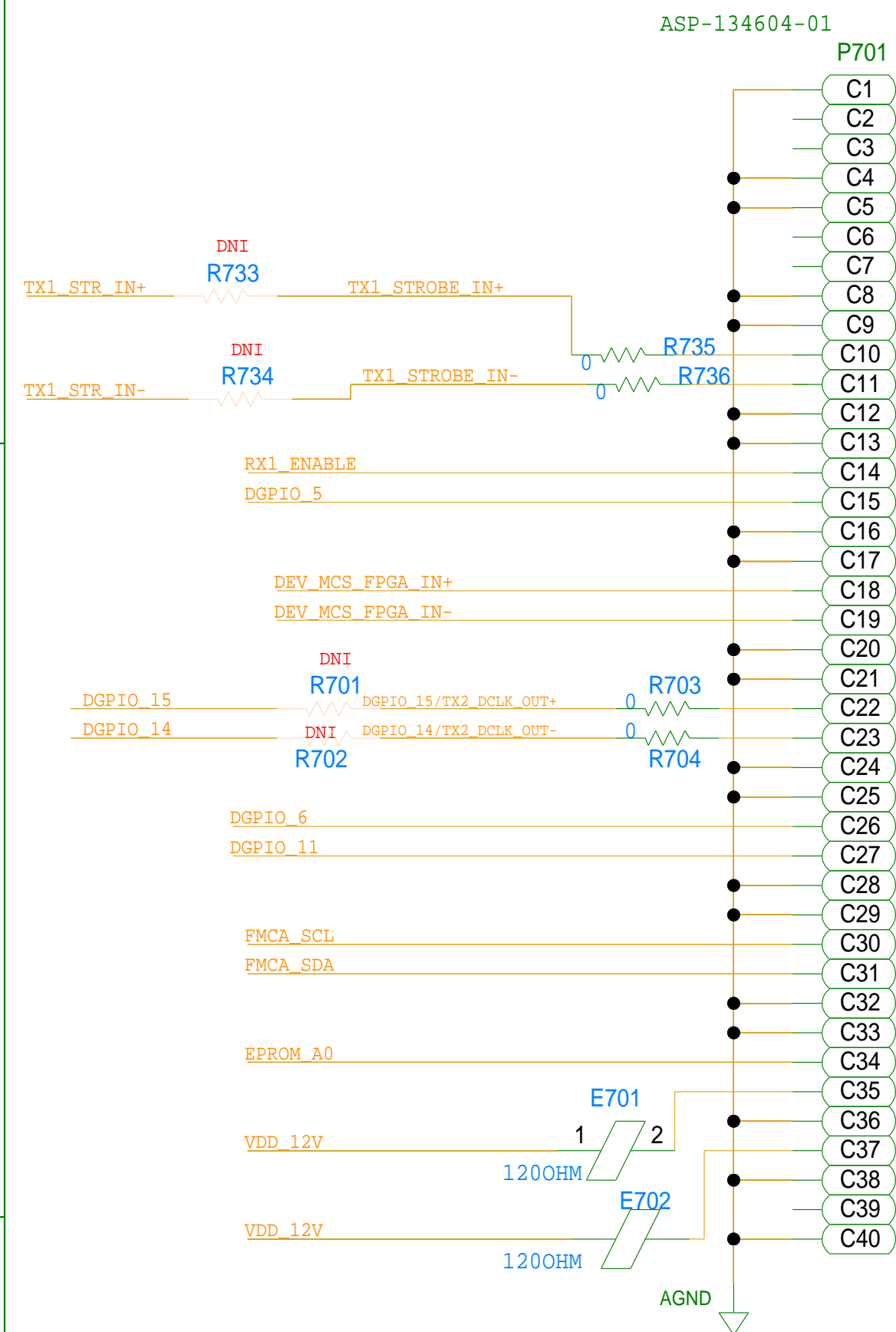
ANALOG DEVICES		SCHEMATIC			
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		DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_063978-02	REV C	
		PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 7 OF 11



# FPGA CONNECTIONS

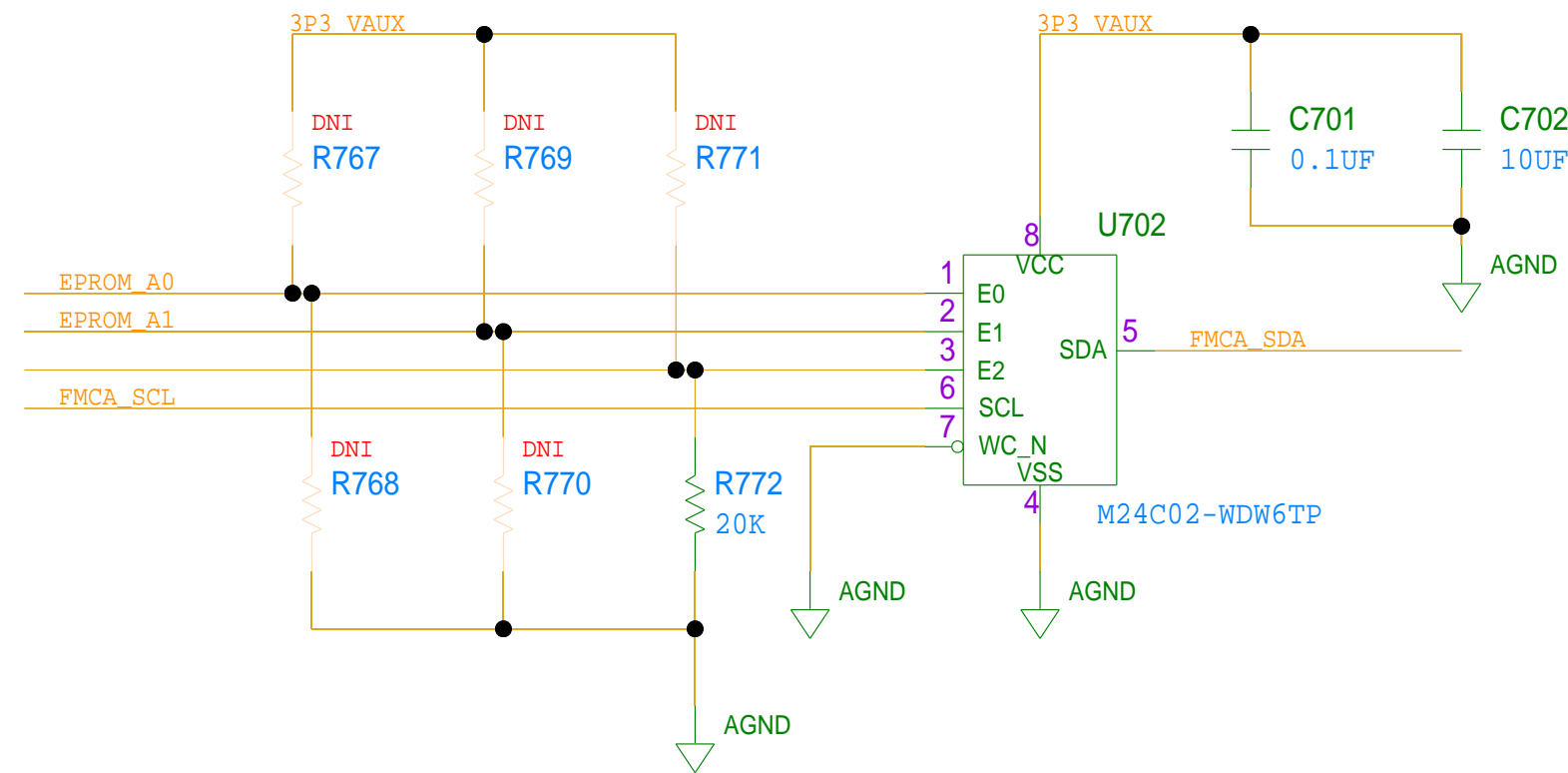
IMPEDANCE CHARACTERISTICS:  
ALL DATA PORT DIFFERENTIAL PAIRS = 100OHM DIFFERENTIAL,

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
C	CHANGE AS PER ECR-099043	02/10/20	H.MIRONCZUK

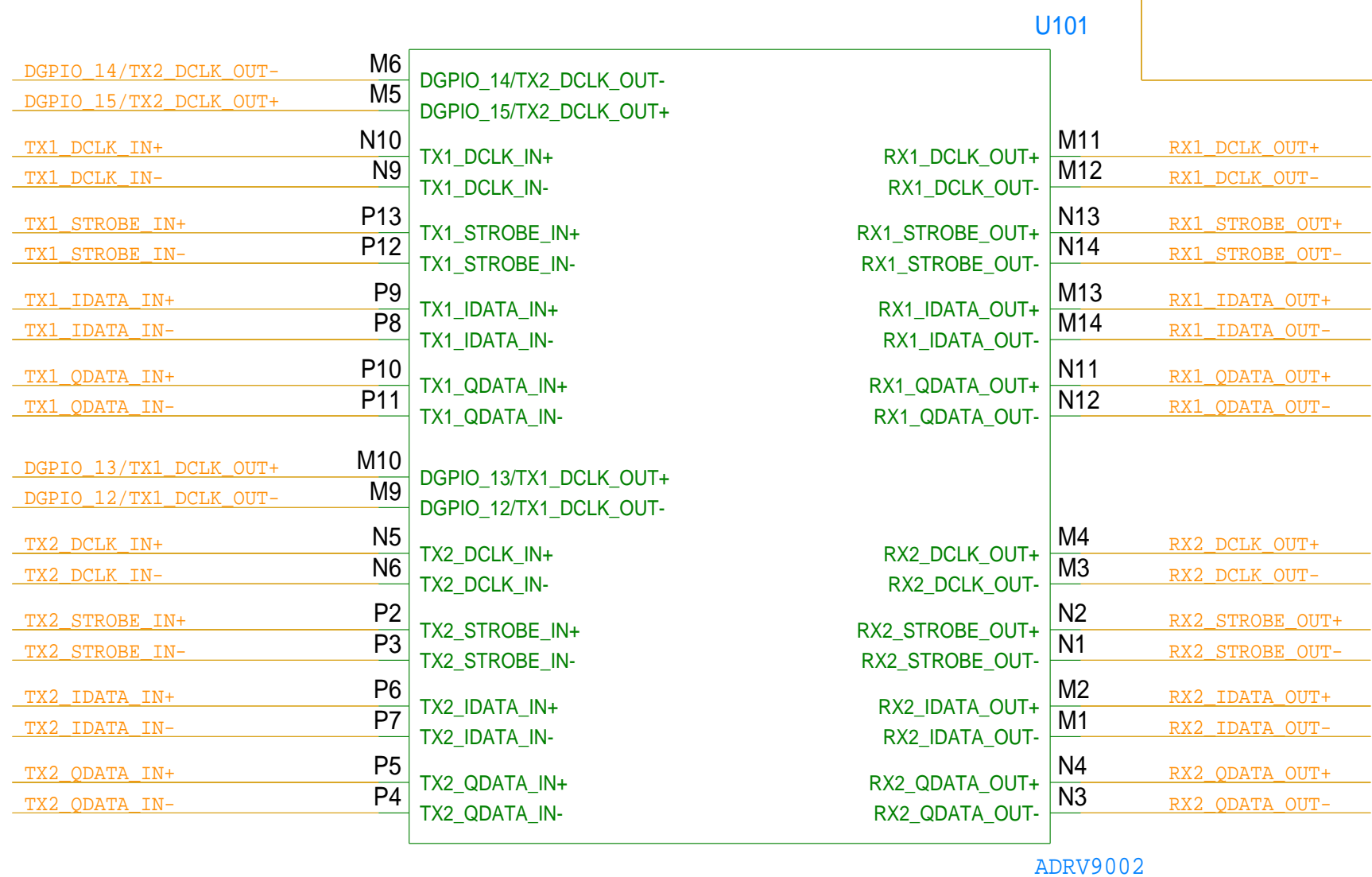


TX1_ID_IN-	DNI P704	1
TX1_ID_IN+		2
TX1_QD_IN-		3
TX1_QD_IN+		4
TX1_DC_IN-		5
TX1_DC_IN+		6
TX1_STR_IN-		7
TX1_STR_IN+		8
RX1_QD_OUT+		9
RX1_QD_OUT-		10
RX1_STR_OUT+		11
RX1_STR_OUT-		12
TSW-106-08-G-D		
RX2_QD_OUT-	DNI P705	1
RX2_QD_OUT+		2
TX2_ID_IN-		3
TX2_ID_IN+		4
TX2_DC_IN-		5
TX2_DC_IN+		6
RX1_DC_OUT+		7
RX1_DC_OUT-		8
DGPI0_12		9
DGPI0_13		10
RX1_ID_OUT+		11
RX1_ID_OUT-		12
TSW-106-08-G-D		
RX2_DC_OUT-	DNI P706	1
RX2_DC_OUT+		2
RX2_ID_OUT-		3
RX2_ID_OUT+		4
TX2_STR_IN-		5
TX2_STR_IN+		6
RX2_STR_OUT-		7
RX2_STR_OUT+		8
DGPI0_15		9
DGPI0_14		10
TX2_QD_IN-		11
TX2_QD_IN+		12
TSW-106-08-G-D		

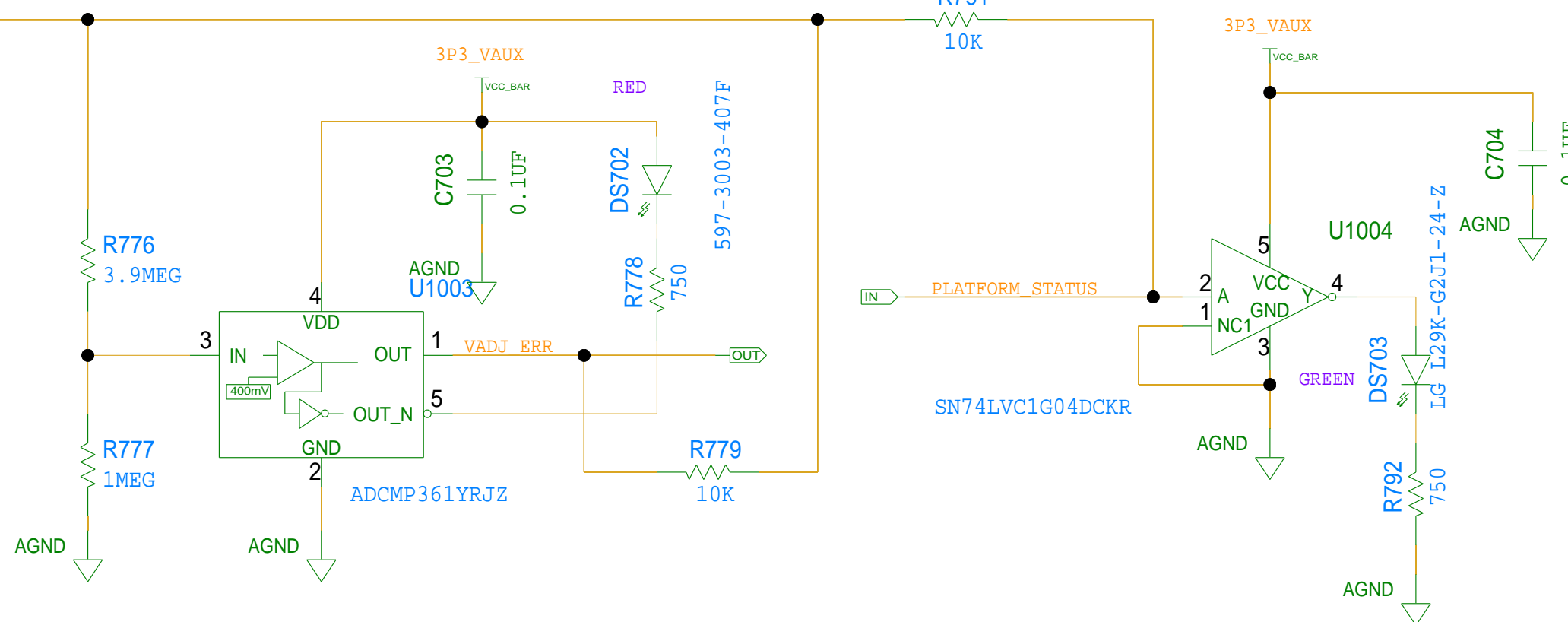
## BOARD ID EEPROM



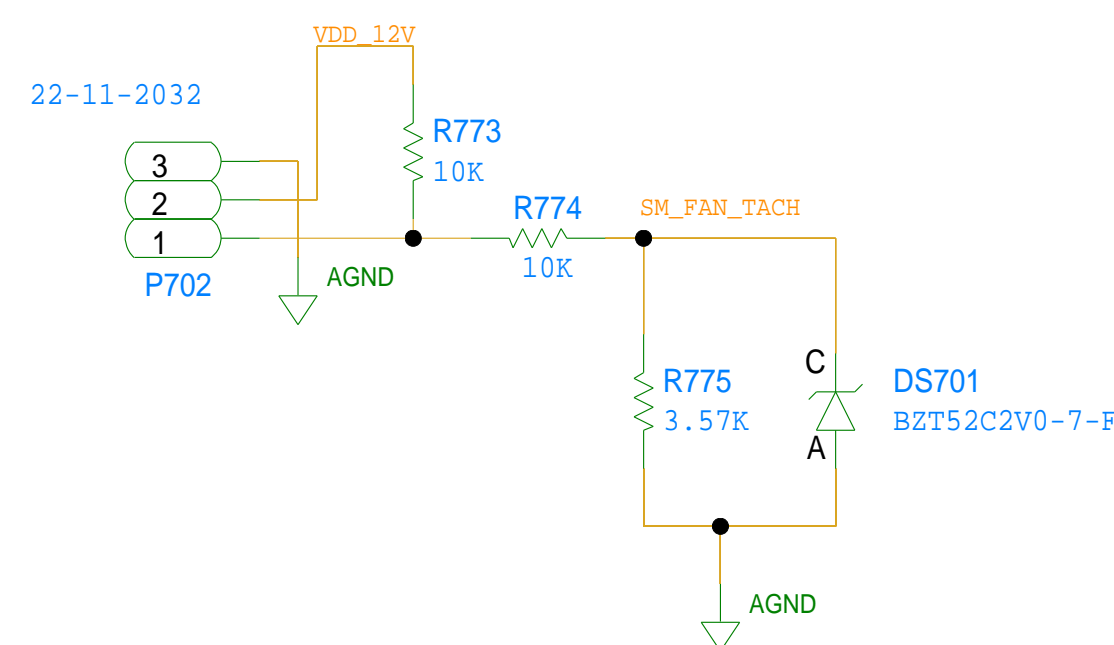
## DATA PORTS



## VADJ MONITORING



## KEYED FAN HEADER

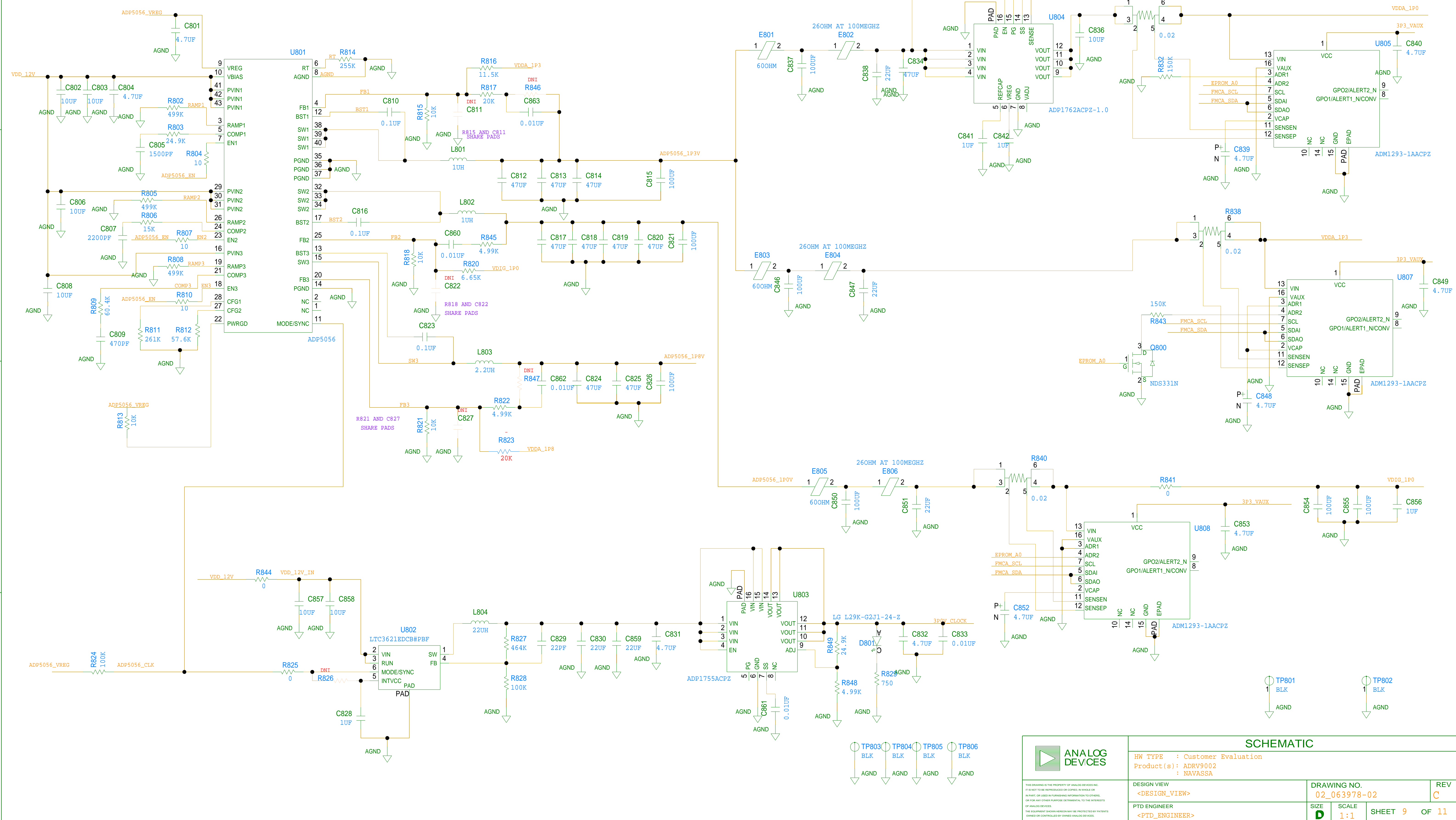


SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : ADRV9002 : NAVASSA			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_063978-02	REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 8 OF 11

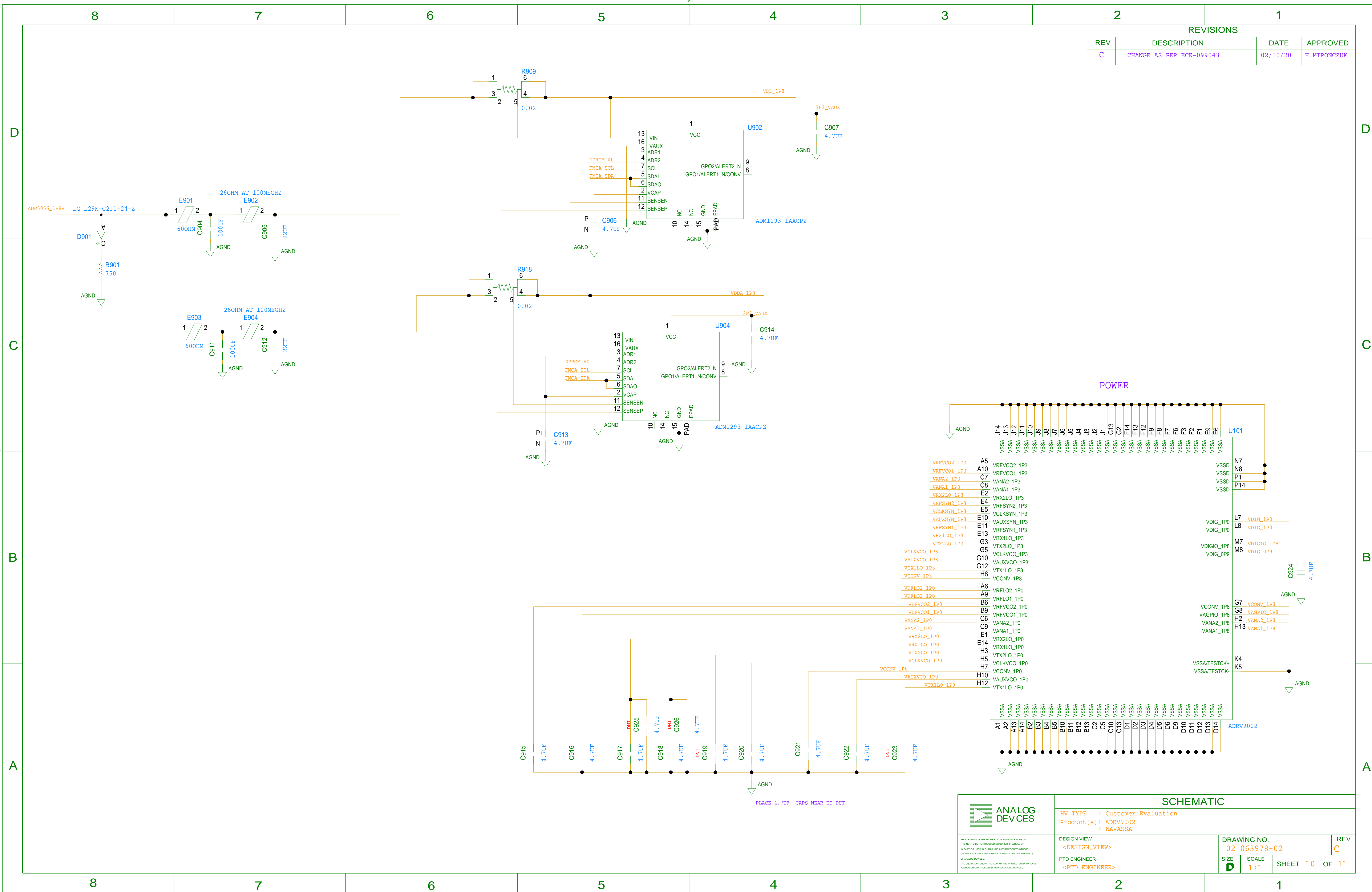


POWER SUPPLY

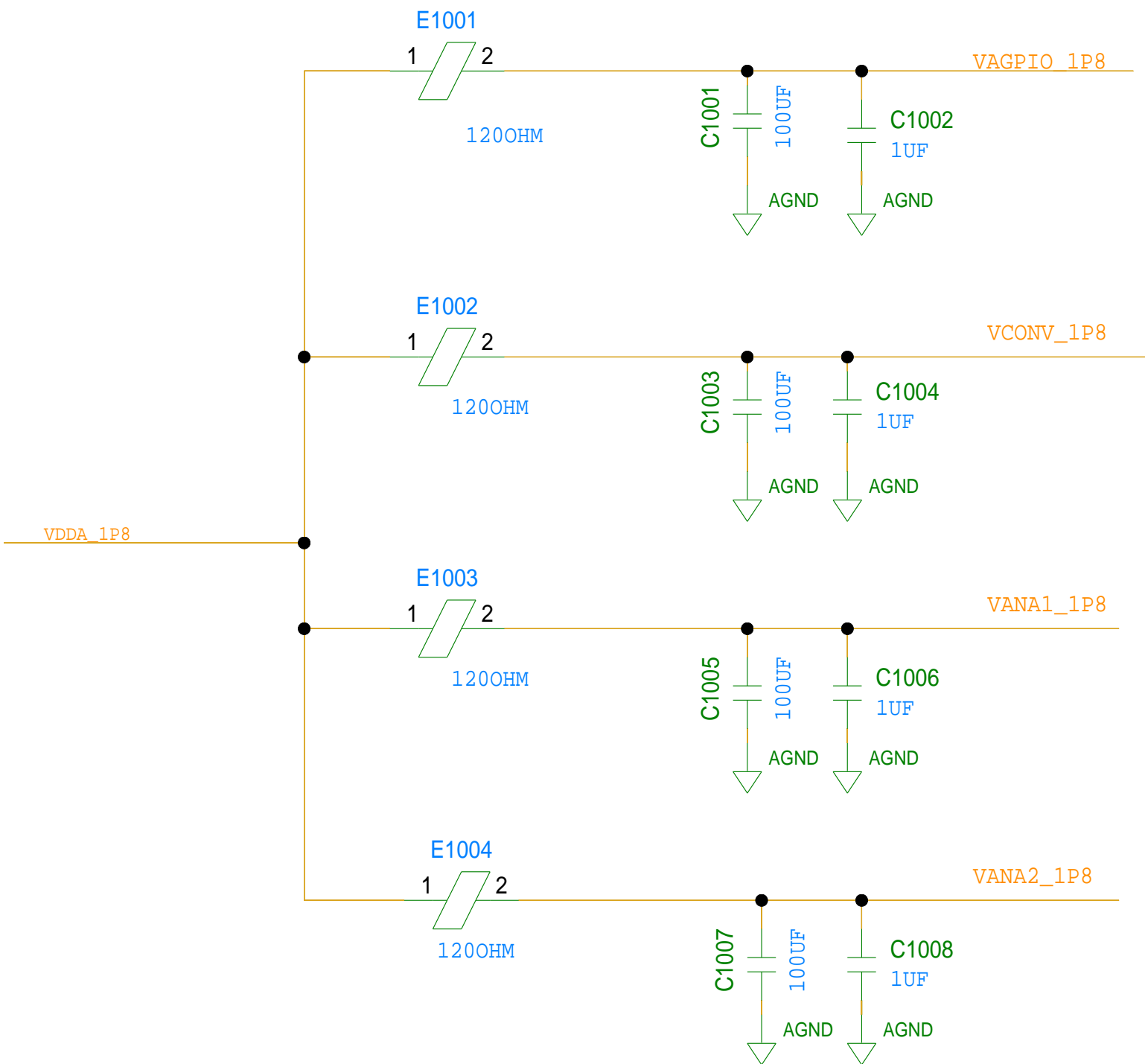
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
C	CHANGE AS PER ECR-099043	02/10/20	H.MIRONCZUK



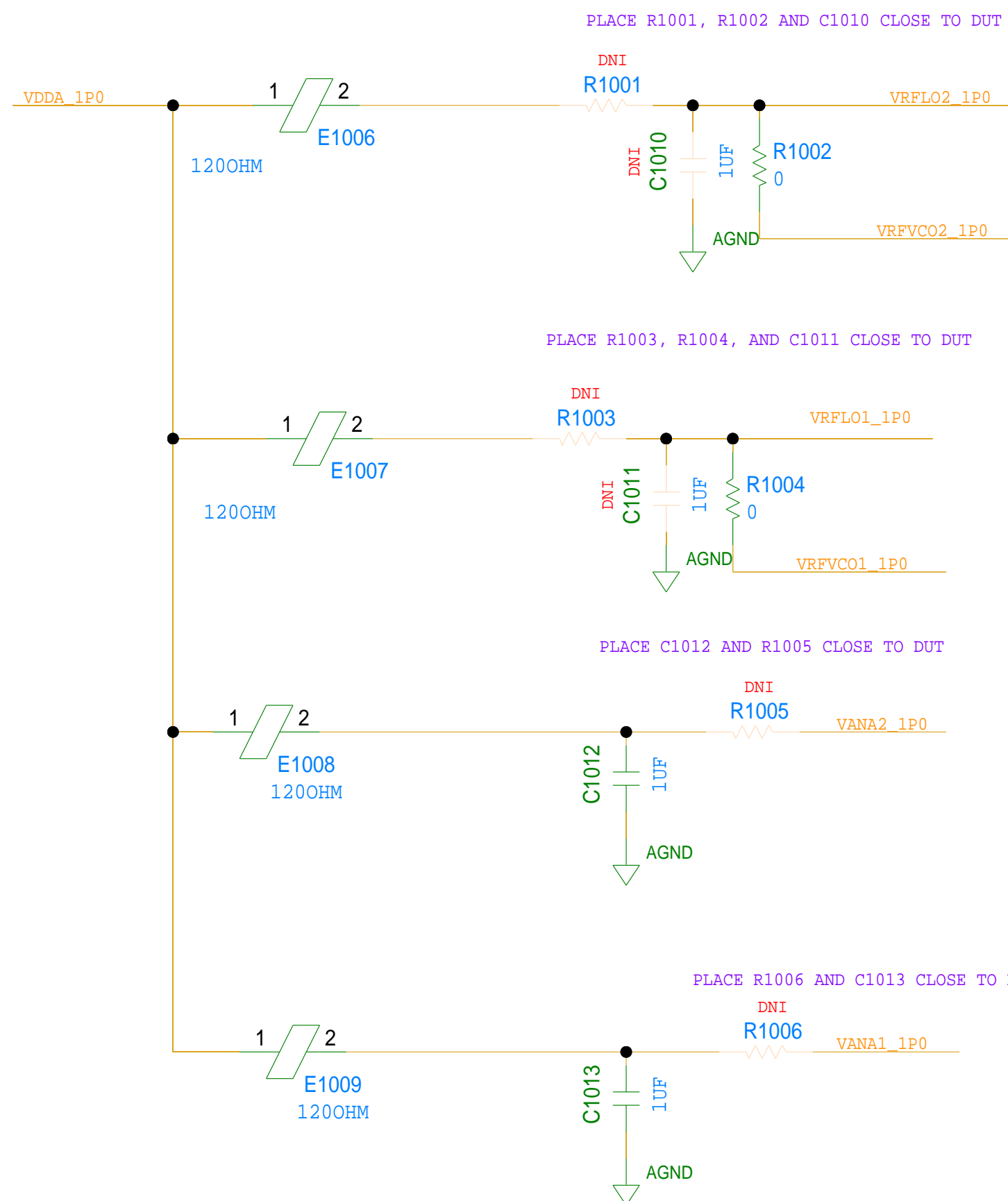
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HW TYPE : Customer Evaluation Product(s) : ADRV9002 : NAVASSA			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_063978-02	REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 9 OF 11



# POWER INPUT



PLACE 1UF CAPS NEAR TO DUT

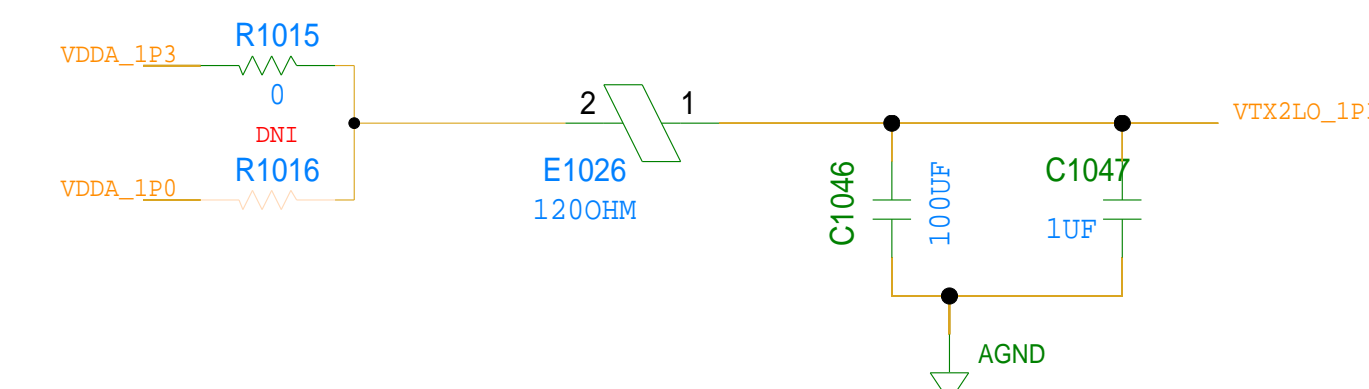
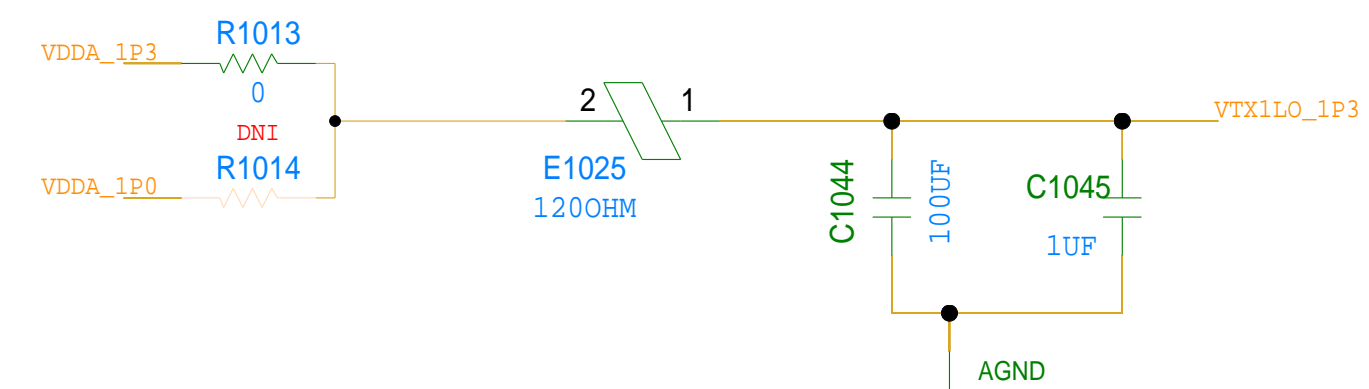
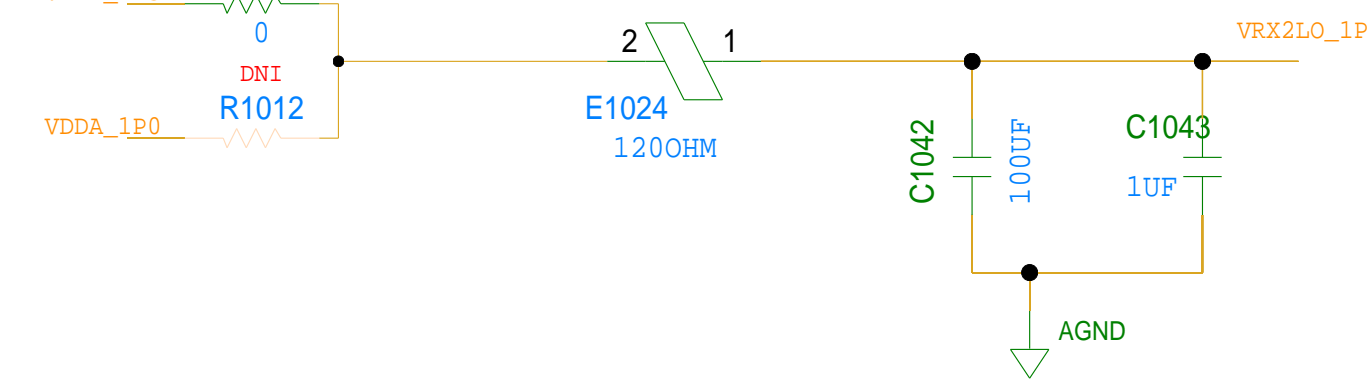
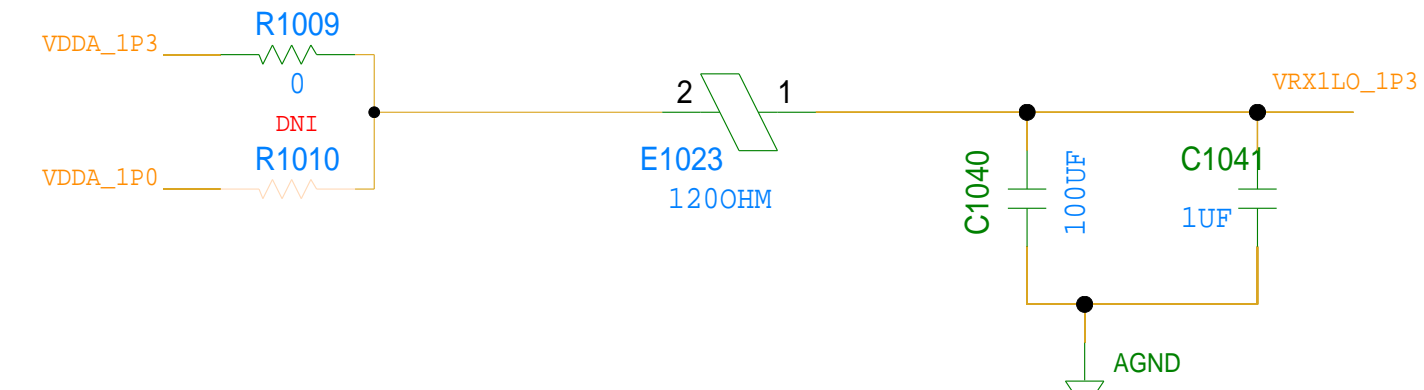
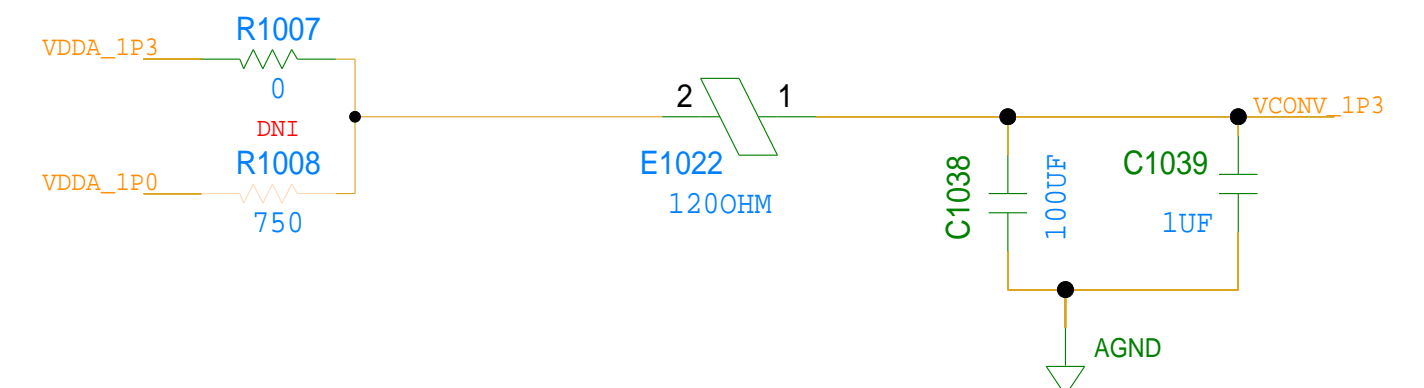
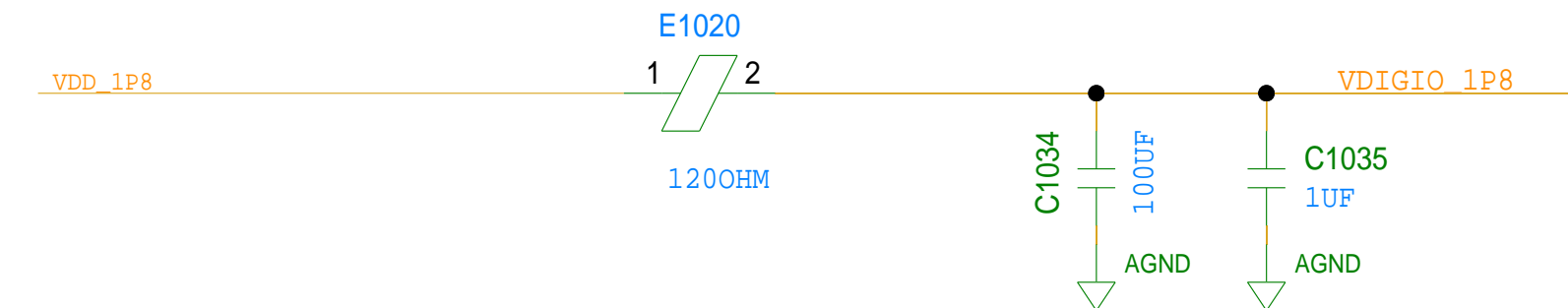
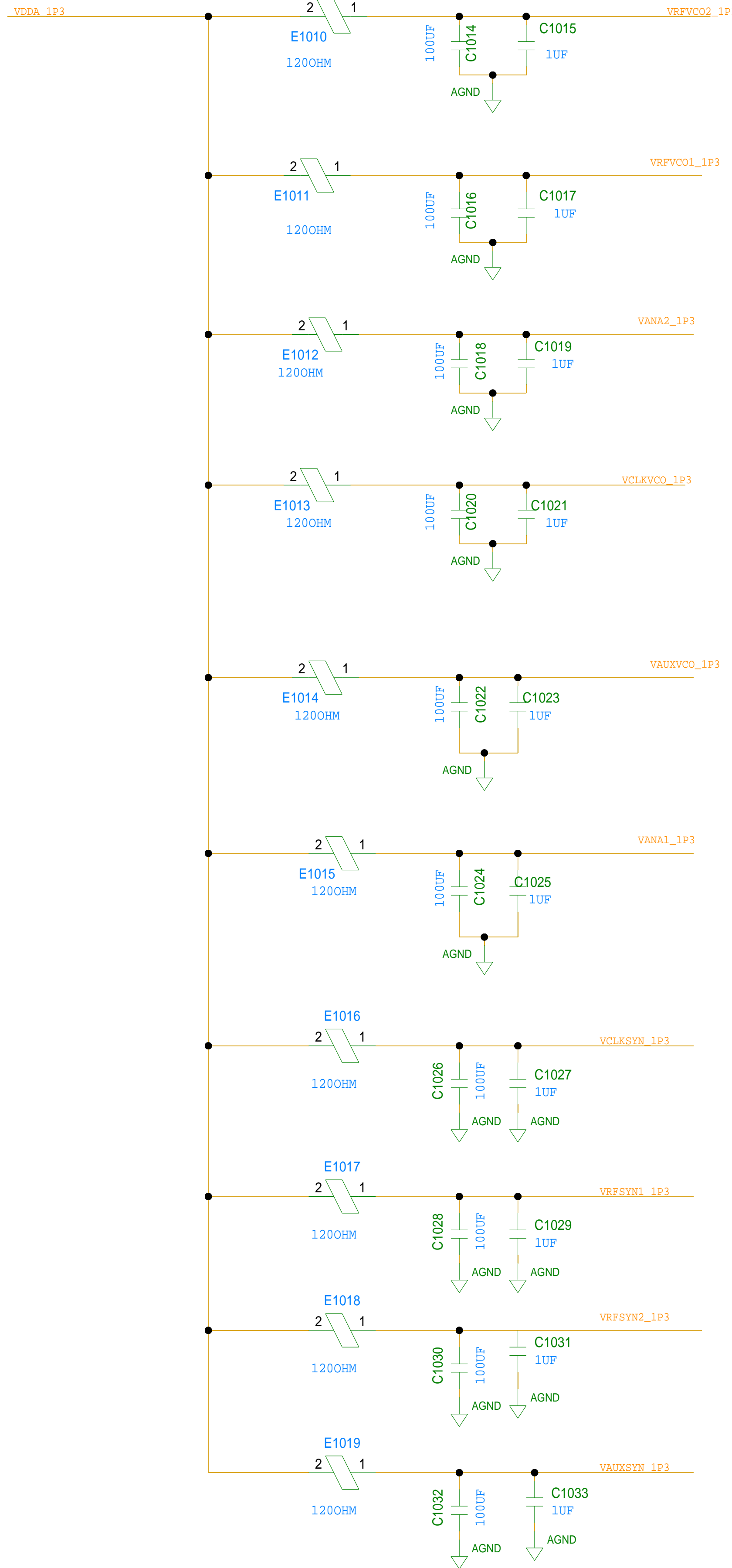


PLACE R1001, R1002 AND C1010 CLOSE TO DUT

PLACE R1003, R1004, AND C1011 CLOSE TO DUT

PLACE C1012 AND R1005 CLOSE TO DUT

PLACE R1006 AND C1013 CLOSE TO DUT



ANALOG DEVICES		SCHEMATIC			
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		DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_063978-02		REV C
		PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 11 OF 11