

Release Note

Thank you for purchasing the **EZ-Board™** product.

Software Requirements for BF526 EZ-Board use:

- **VisualDSP++ 5.0 Update 4 or newer**

Manual: Please read the manual and familiarize yourself with the board before applying power.

The manual can be found:

- <http://www.analog.com/>

Audio Interface:

J3 and J4 are audio connectors which allow use of MIC and LINEIN (J4), as well as HEADPHONE and LINOUT (J3). Left and right signals are swapped in the layout for LINEIN, HEADPHONE, and LINEOUT ports. The schematics are correct, but the layout is inverted. The MIC port is also swapped causing the port to only work with standard PC electret microphones. **DO NOT** use dynamic and active microphones, they will not work and may cause damage. A PC sound card may need a jumper moved to use a MIC with connector J4. In the BF526 EZ-Board design, MICBIAS signal is actually on the tip, and MICIN signal is on the ring of a standard 3.5mm audio connector. This applies to the current revision 1.1 and all previous revisions of the BF526.

Signal Termination:

Signal termination, series or parallel, is recommended for EBIU signals in custom board designs.

Boost Regulator for Expansion Interface:

When using the lithium ion battery to power the BF526 EZ-Board (JP9 OFF, JP25 ON, JP8 5&6, 7&8), SW22 must remain ON when plugging in USB (P8) or the wall (P14).

VDDINT Programmable Regulator

By default, the EZ-Board has VDDINT programmed to 1.4V. This board contains a programmable regulator that supplies the processor's core with a voltage between 1.1V and 1.4V. For silicon revisions 0.0 and 0.1, do not run the VDDINT at less than 1.2V. For information on programming the regulator refer to the Power On Self Test (POST) example for the ADSP-BF526 in the VDSP++ installation directory. Acceptable settings for silicon revision 0.0 and 0.1 are found in the table below.

| Step Value | Voltage |
|------------|---------|
| 36 | 1.2V |
| 27 | 1.25V |
| 18 | 1.3V |
| 10 | 1.35V |
| 3 | 1.4V |