

A

B

C

D

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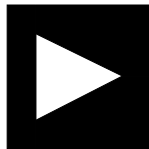
3

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# ADSP-BF526 EZ-BOARD SCHEMATIC



**ANALOG  
DEVICES**

20 Cotton Road  
Nashua, NH 03063  
PH: 1-800-ANALOGD

Title ADSP-526 EZ-BOARD  
TITLE

Size C	Board No. A0212-2007	Rev 0.2A
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Date 8-15-2008_13:19	Sheet 1 of 14
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A

B

C

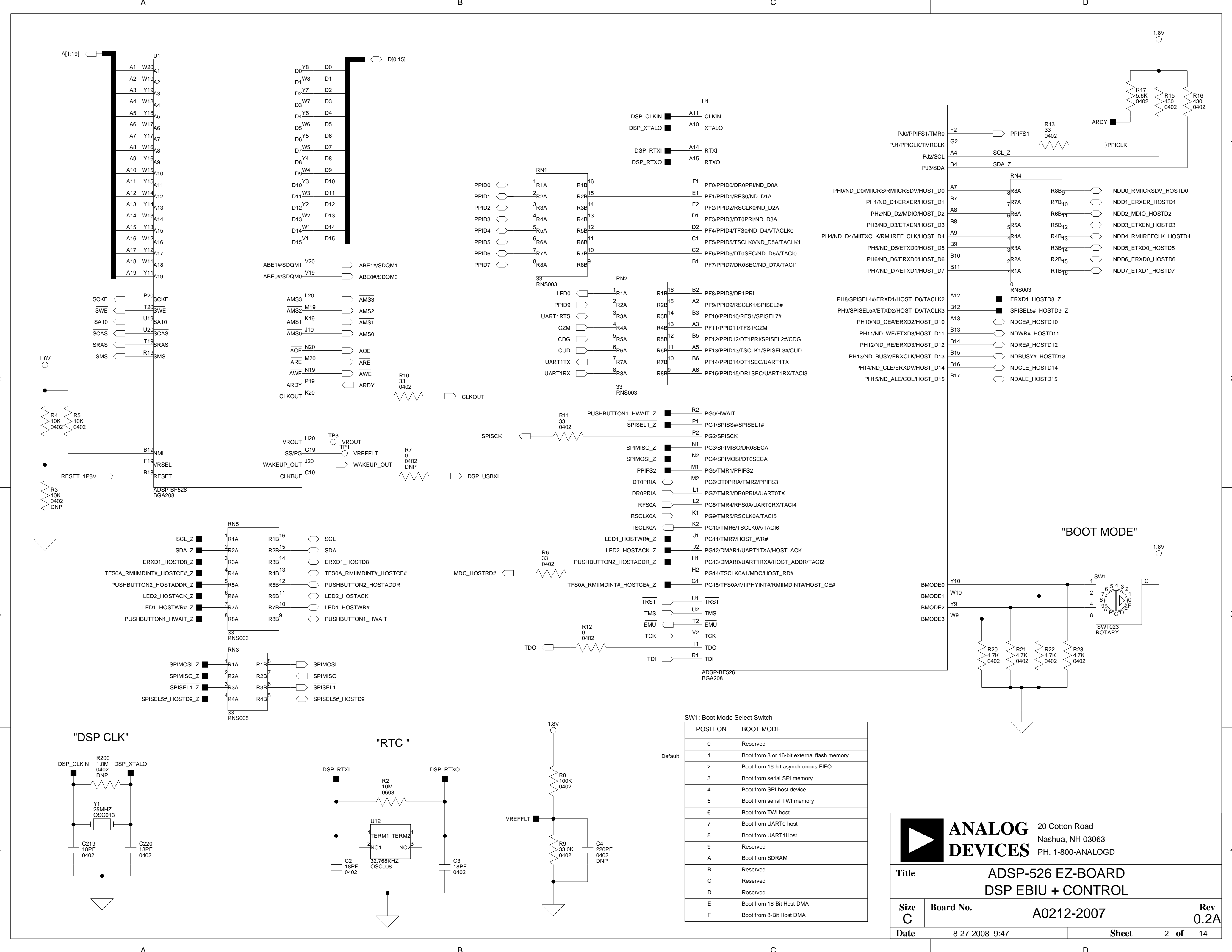
D

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1

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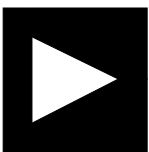
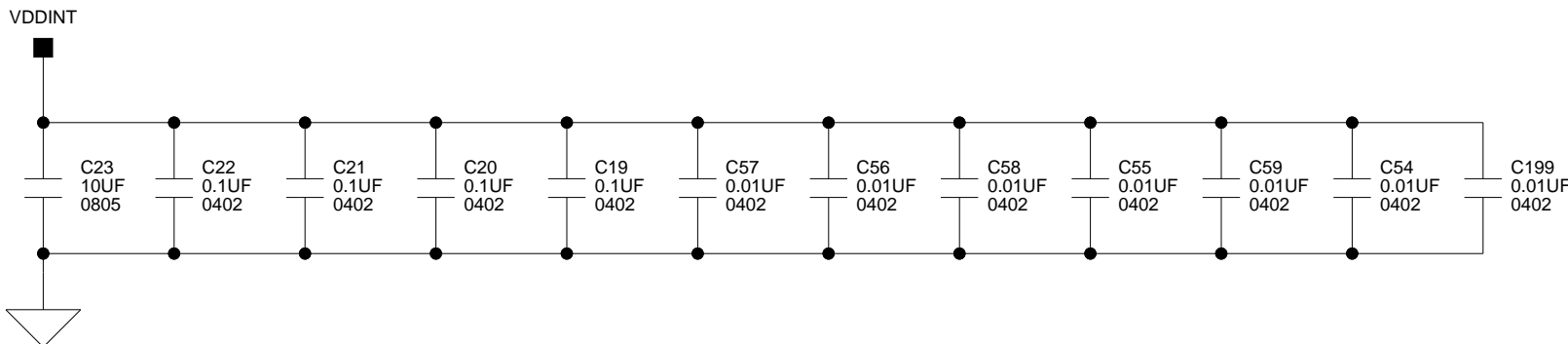
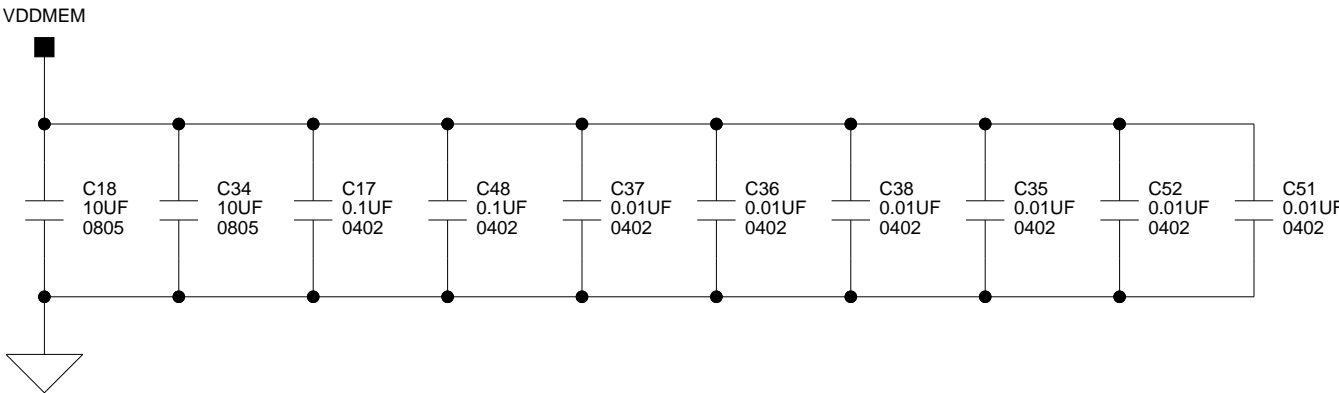
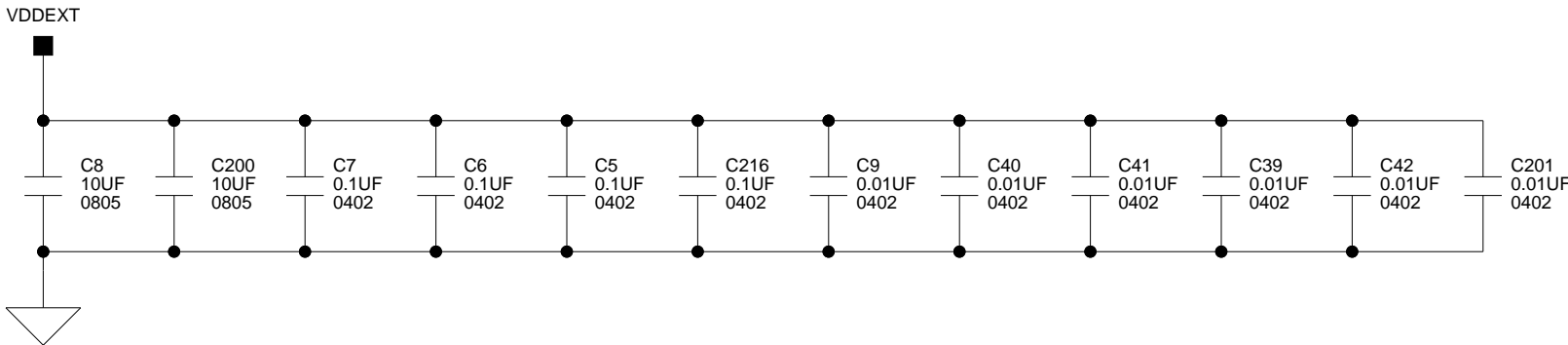
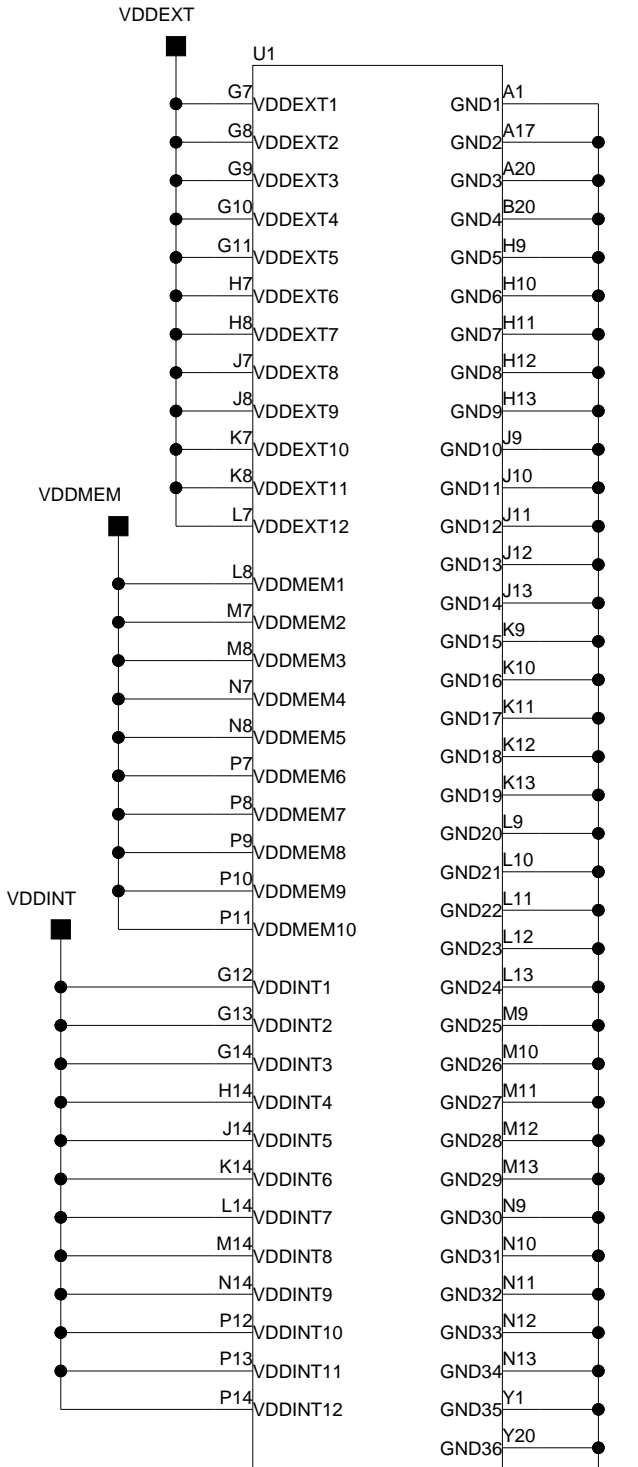
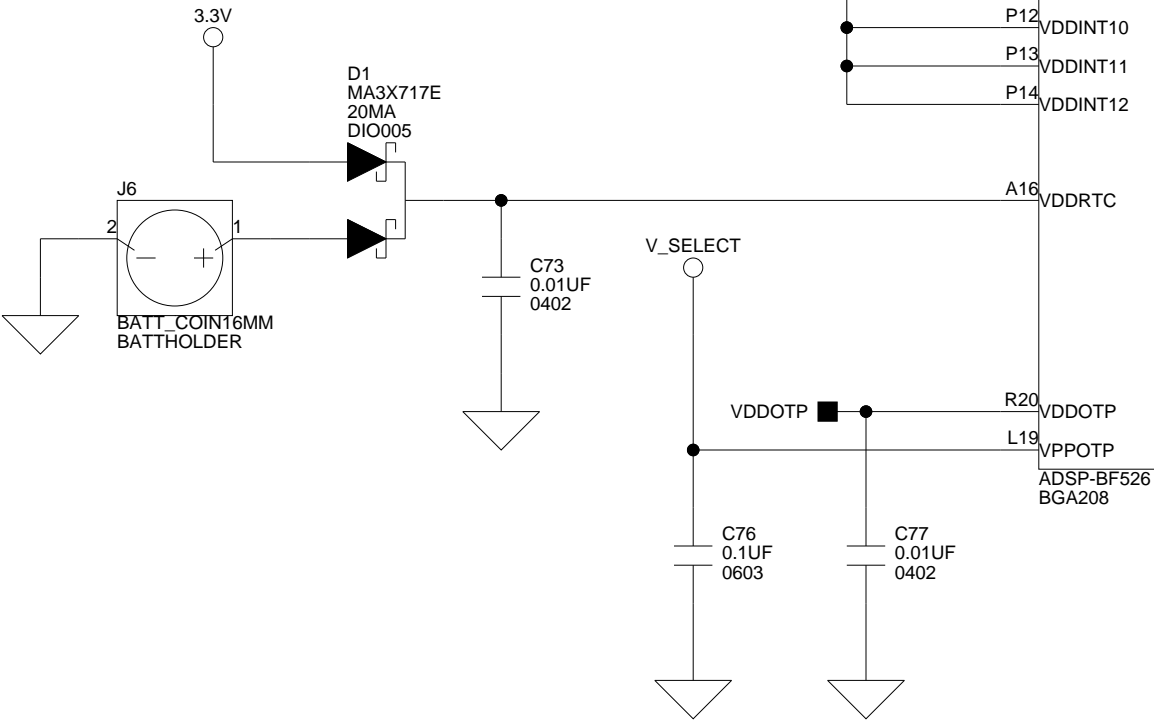
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"RTC BATTERY"



**ANALOG  
DEVICES**

20 Cotton Road  
Nashua, NH 03063  
PH: 1-800-ANALOGD

Title **ADSP-526 EZ-BOARD  
DSP POWER, BYPASS CAPS**

Size **C** Board No. **A0212-2007**

Rev **0.2A**

Date **8-15-2008\_13:19**

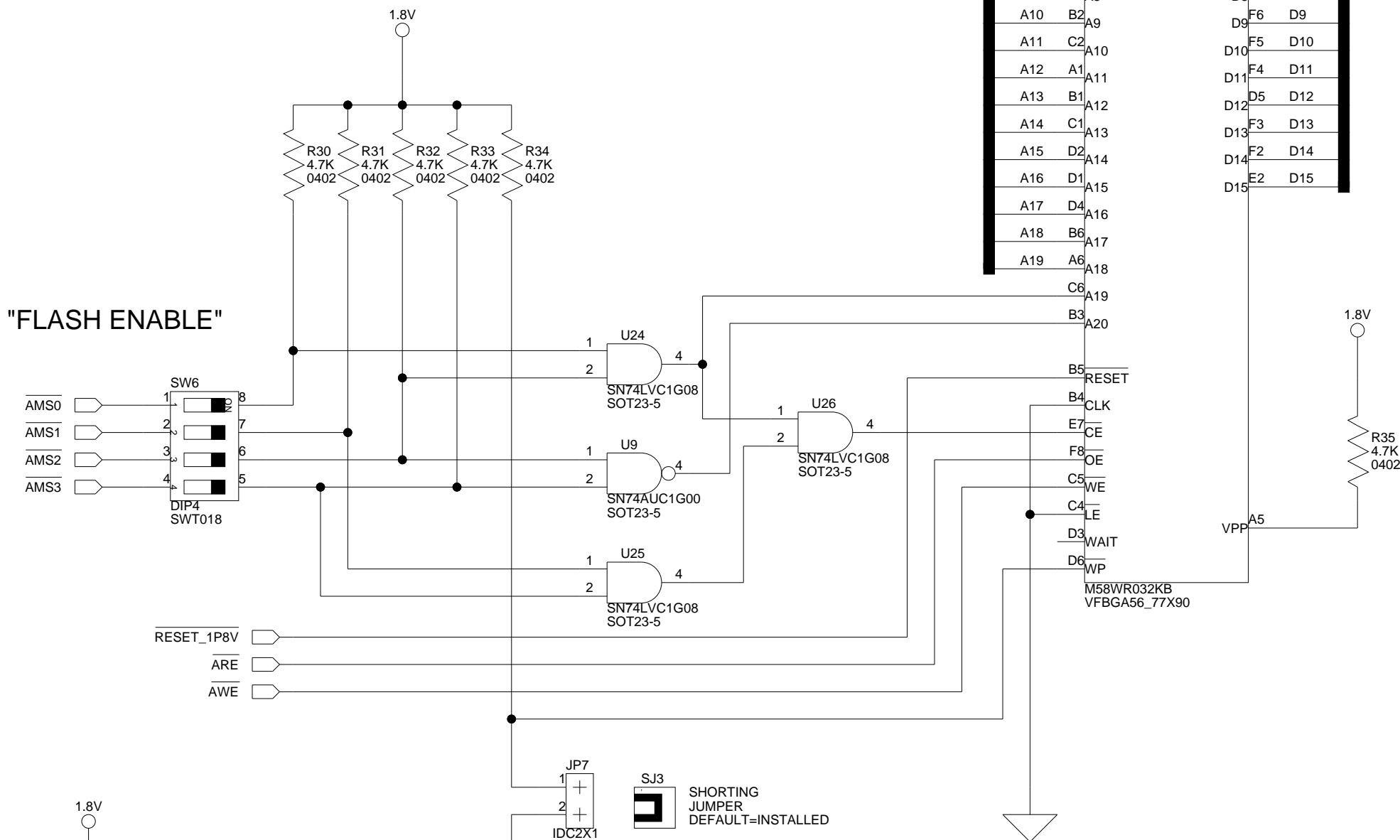
Sheet **3 of 13**

SW6: FLASH Enable

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
SW6.1	DSP (U1)	FLASH (U16)	ON	(Expansion Interface)
SW6.2	DSP (U1)	FLASH (U16)	ON	(Expansion Interface)
SW6.3	DSP (U1)	FLASH (U16)	ON	(Expansion Interface)
SW6.4	DSP (U1)	FLASH (U16)	ON	(Expansion Interface)

4 MB FLASH  
(2M x 16)

64MB SDRAM (32M x 16)

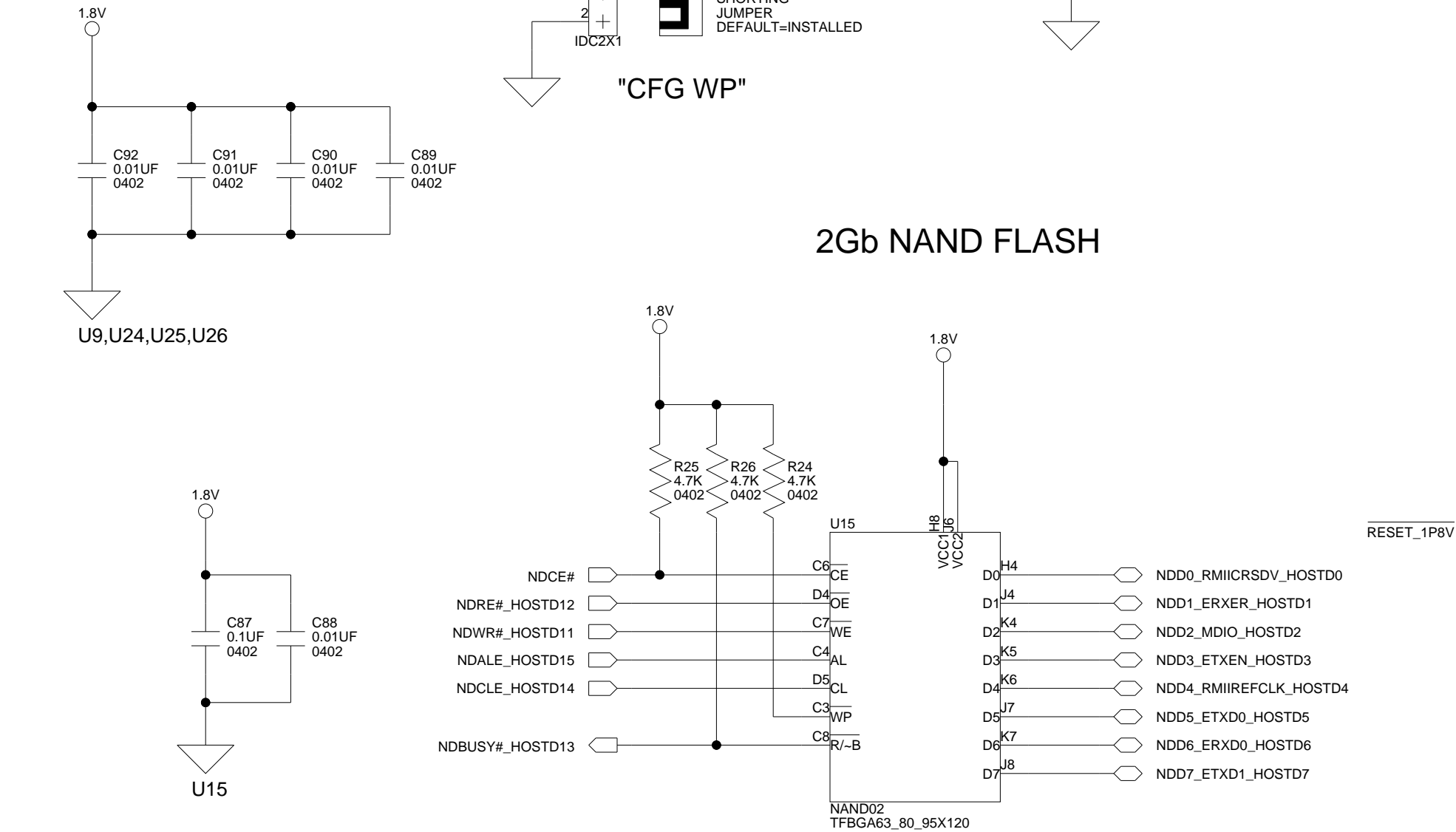


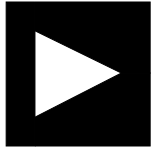
MEMORY MAP

ADDRESS RANGE	SELECT LINE	TYPE
0x2030 0000 - 0x203F FFFF	ASYNC BANK 3	FLASH
0x2020 0000 - 0x202F FFFF	ASYNC BANK 2	FLASH
0x2010 0000 - 0x201F FFFF	ASYNC BANK 1	FLASH
0x2000 0000 - 0x200F FFFF	ASYNC BANK 0	FLASH
0x0000 0000 - 0x03FF FFFF	NONE	SDRAM

2Gb NAND FLASH

4 Mb SPI FLASH



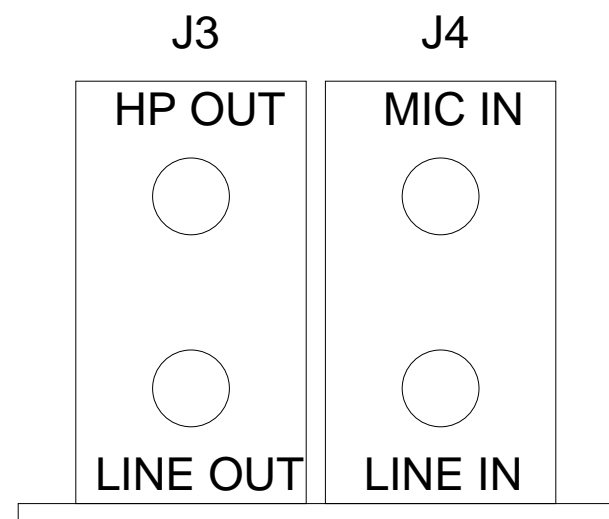
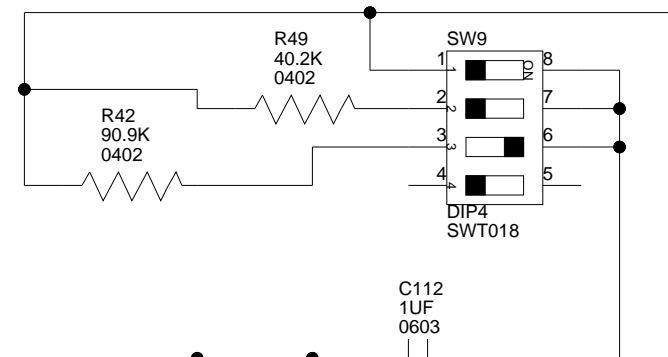


**ANALOG  
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20 Cotton Road  
Nashua, NH 03063  
PH: 1-800-ANALOGD

Title ADSP-526 EZ-BOARD MEMORY		
Size C	Board No. A0212-2007	Rev 0.2A
Date	8-15-2008_13:19	Sheet 4 of 14

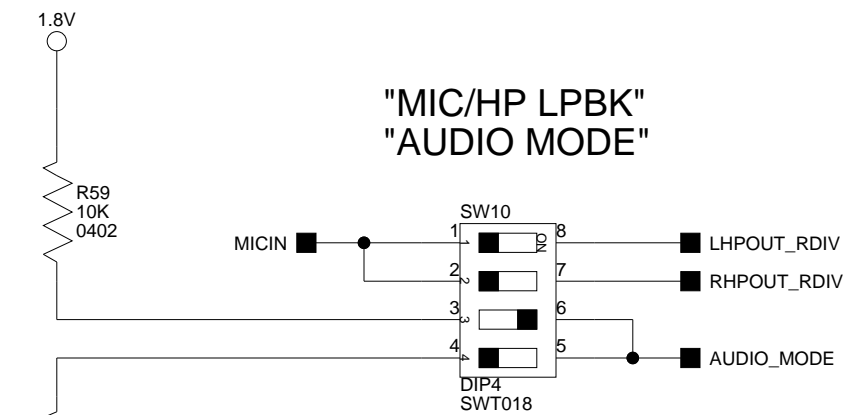
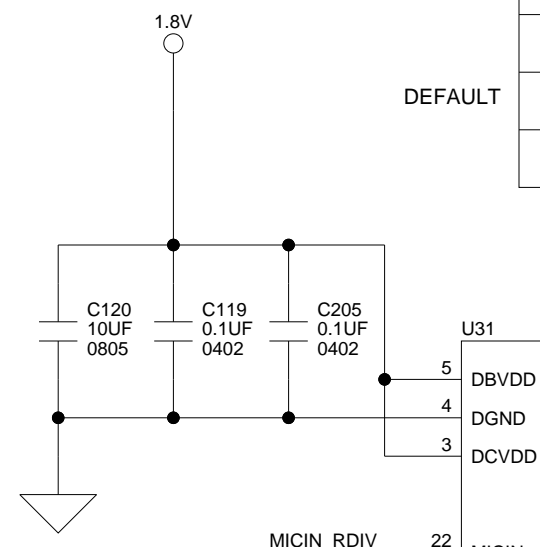


**"MIC GAIN"****SW9: MIC GAIN**

POS.	GAIN
1	5 (14dB)
2	1 (0dB)
3	0.5 (-6dB)
4	NC

Table shows the gain if switch position in left column is ON, all others OFF.

DEFAULT

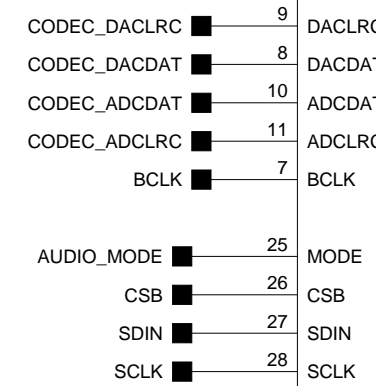
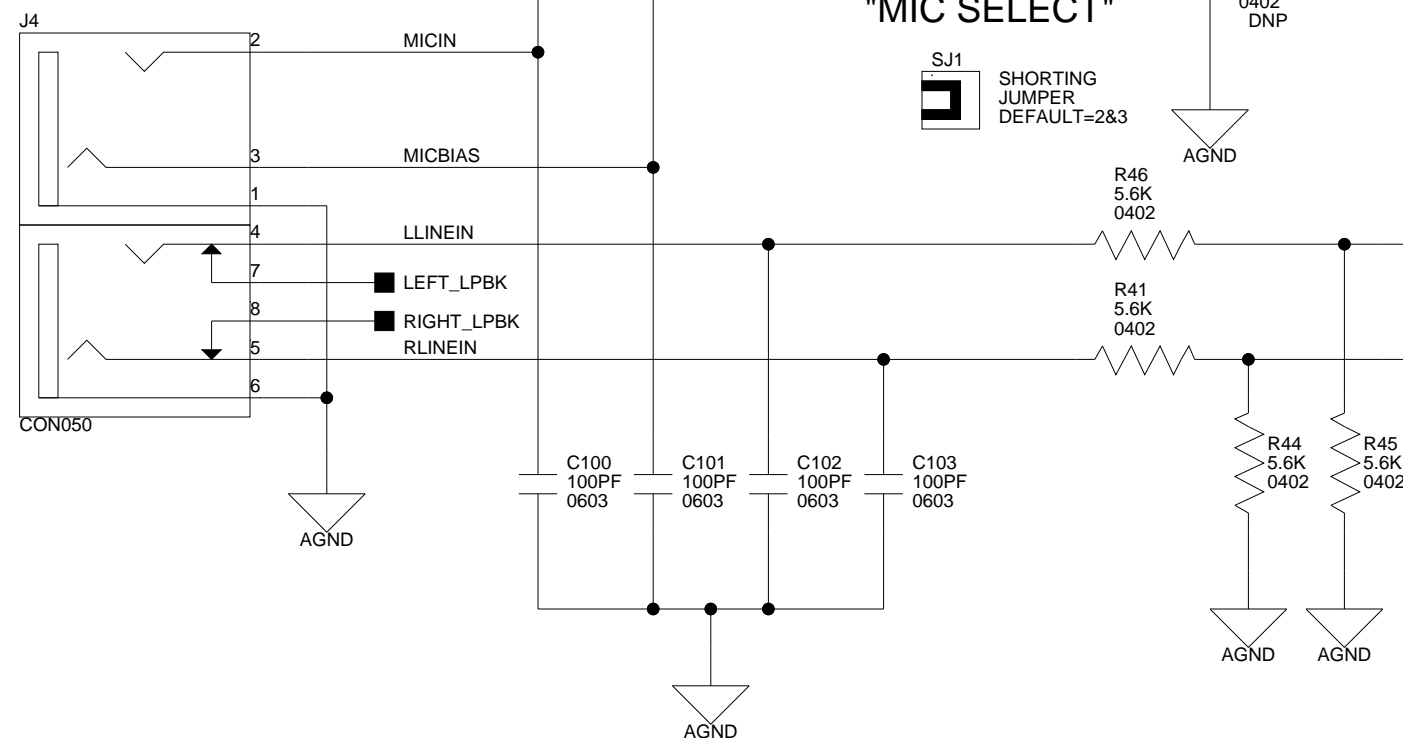
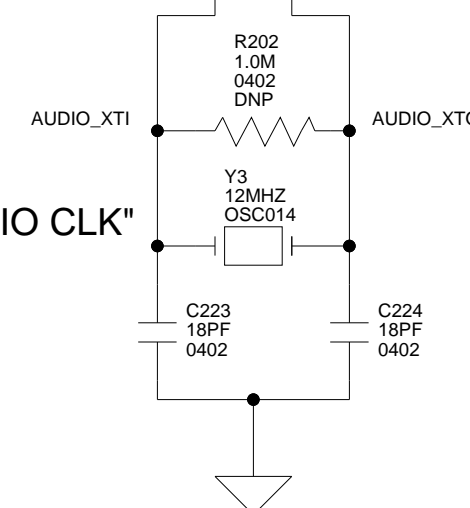
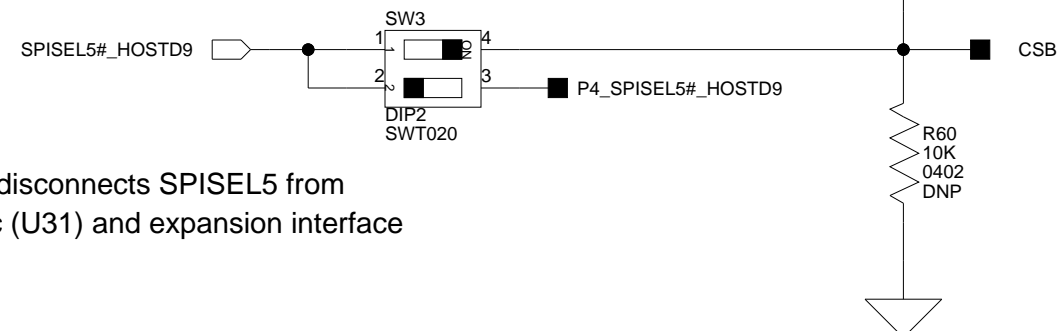
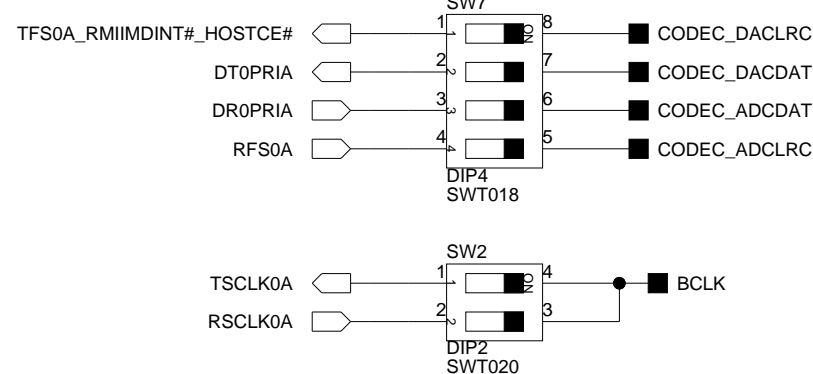


SW10 allows the MICIN signal to be looped back, for test purposes, to the Left and Right headphone. DO NOT switch positions 1 & 2 ON at the same time. Ensure that JP6 is on 2&3 or OFF when using SW10.

AUDIO CODEC INTERFACE MODE:

SW10.3 ON and SW10.4 OFF = SPI MODE

SW10.3 OFF and SW10.4 ON = TWI MODE

**"MIC"****"LINE IN"****"AUDIO CLK"****"CODEC CS"****"SPORT"****"OA"****"ENBL"**

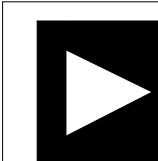
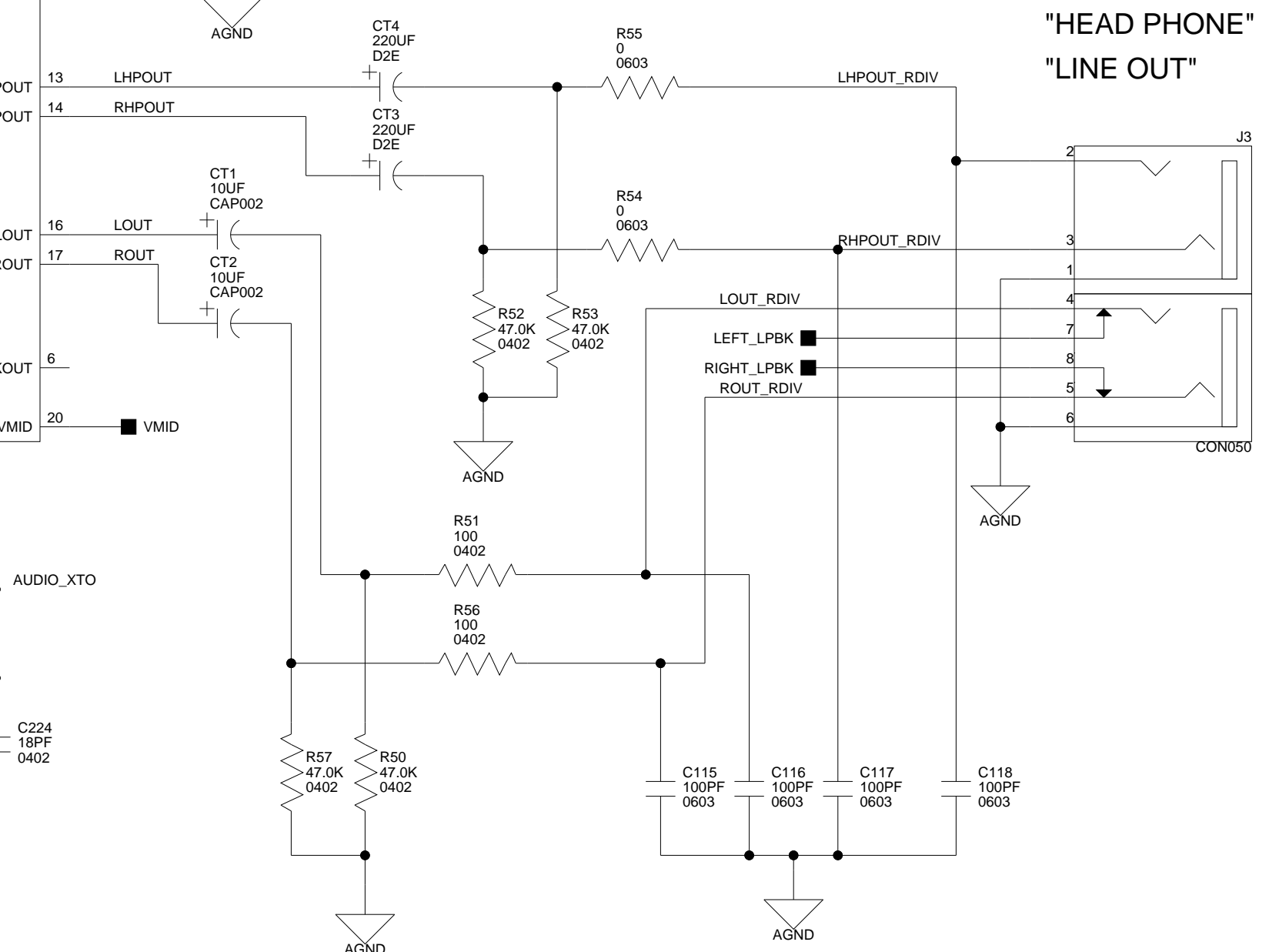
SW7 and SW2 disconnect DSP from AUDIO CODEC

**"SPI/TWI"**

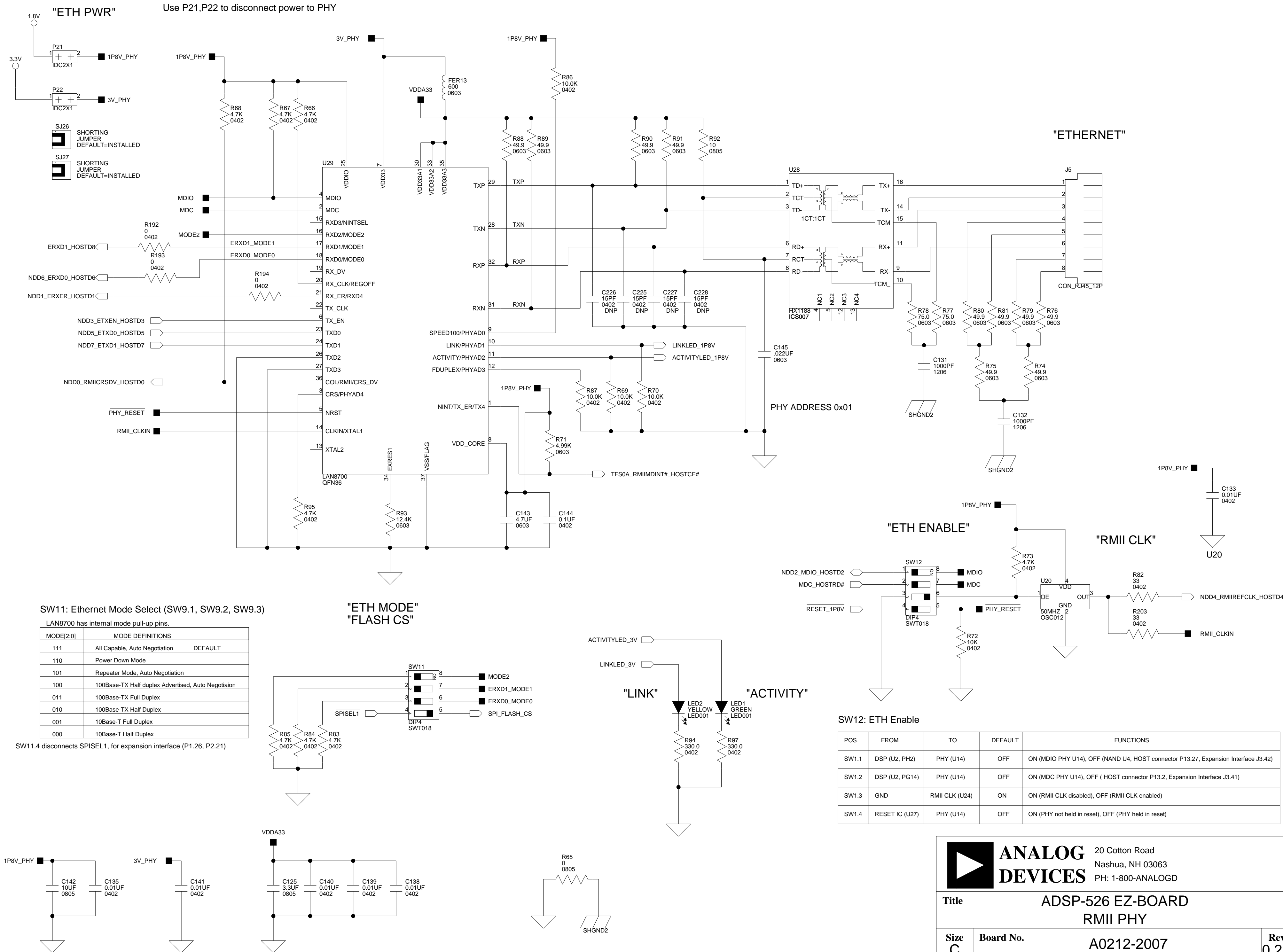
AUDIO CODEC MODE INTERFACE:

SPI MODE: ON, OFF, ON, OFF

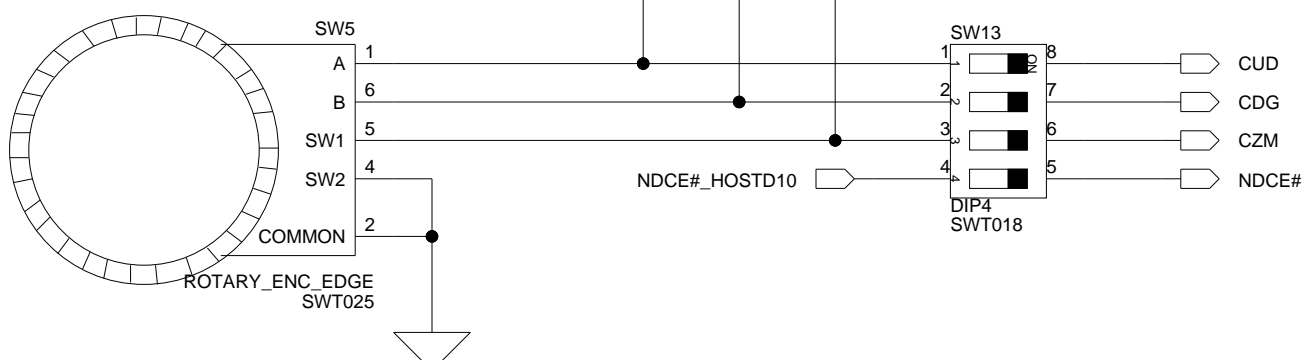
TWI MODE: OFF, ON, OFF, ON

**"HEAD PHONE"****"LINE OUT"****ANALOG  
DEVICES**20 Cotton Road  
Nashua, NH 03063  
PH: 1-800-ANALOGD

Title			ADSP-526 EZ-BOARD AUDIO CODEC		
Size C	Board No.		A0212-2007		Rev 0.2A
Date	8-28-2008_15:18		Sheet	6 of 14	

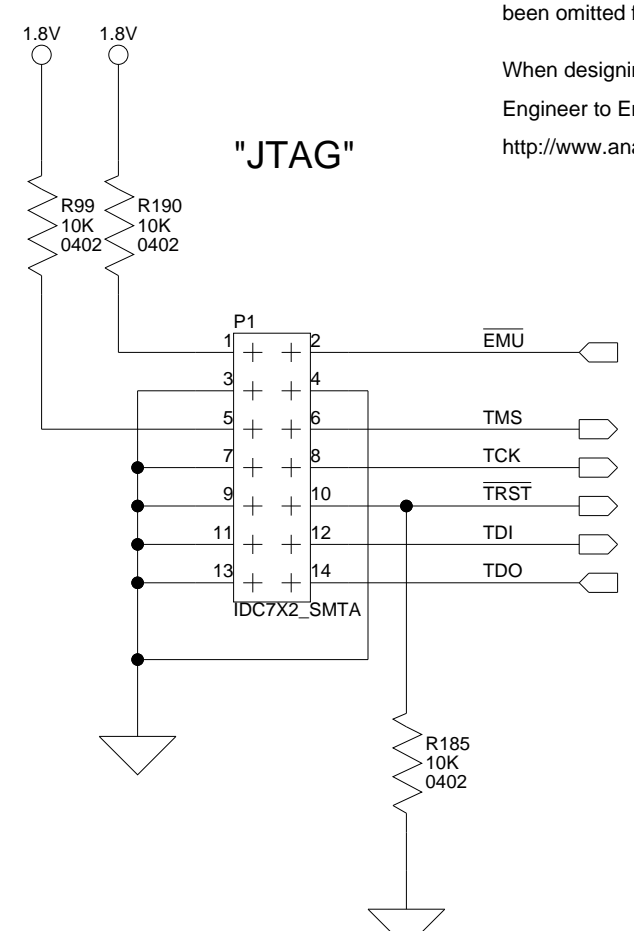


"ENCODER"



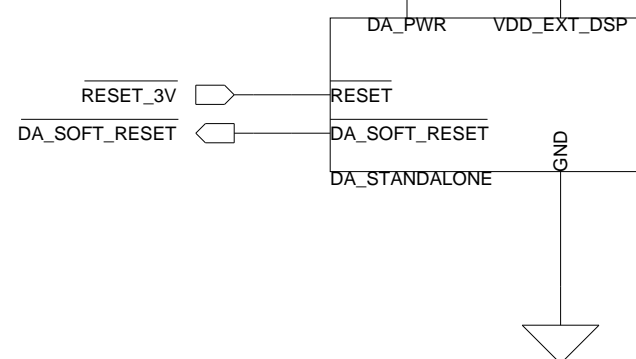
"ROTARY"  
"NAND"  
"ENABLE"

"JTAG"



All USB interface circuitry is considered proprietary and has been omitted from this schematic.

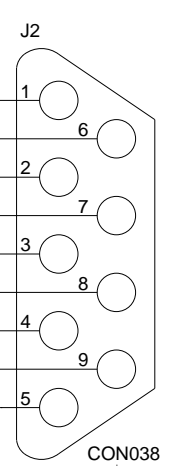
When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at <http://www.analog.com>



"UART SD"



"UART 1"

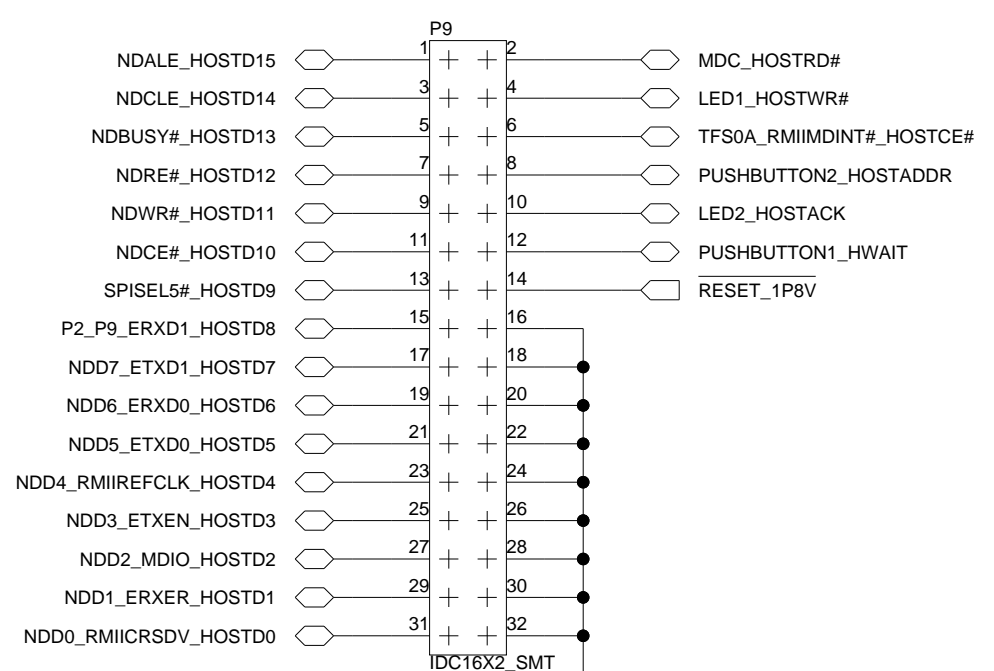


"UART SETUP"

SERIAL PORT  
(UART 1)

"UART LPBK"

"HOST"

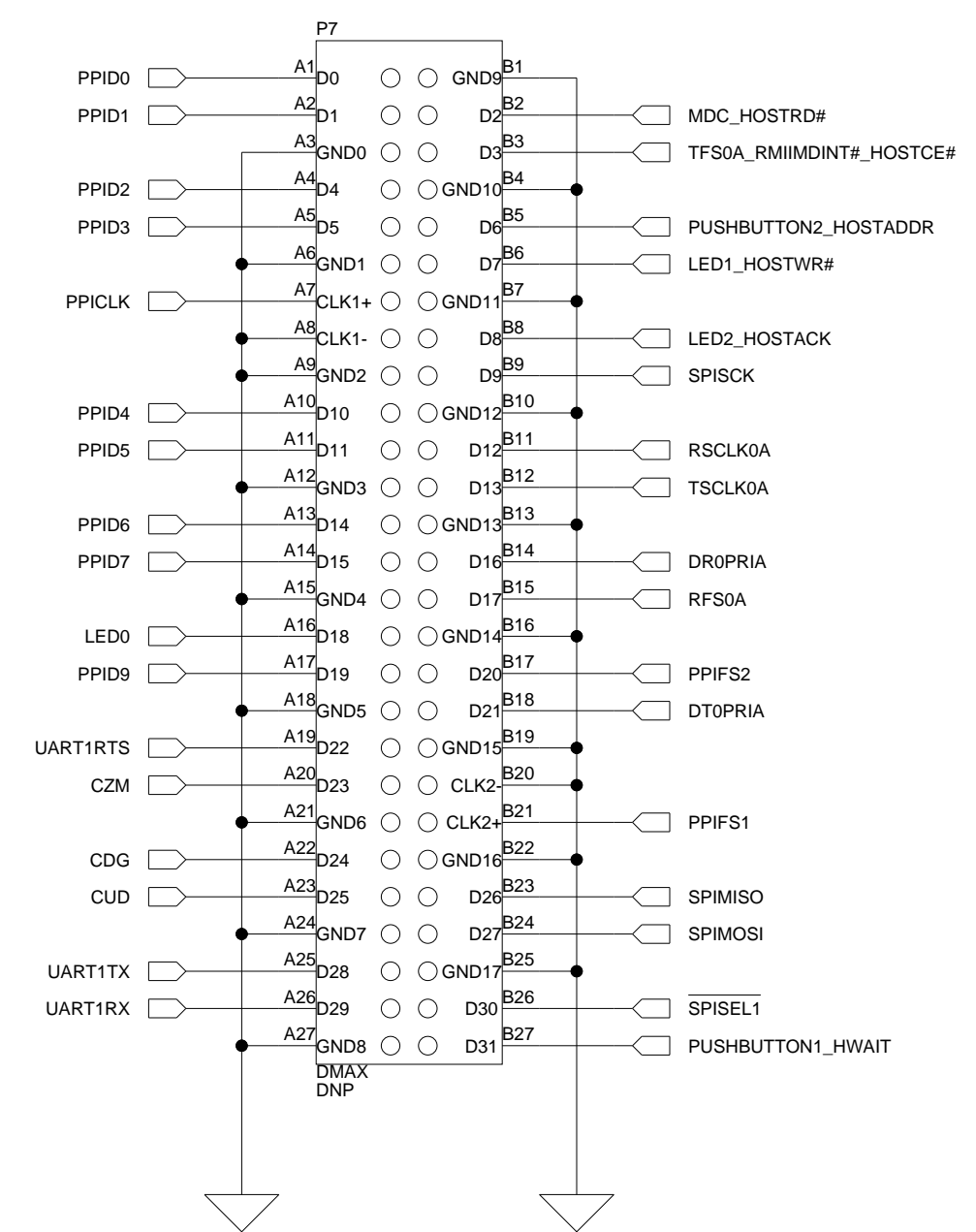
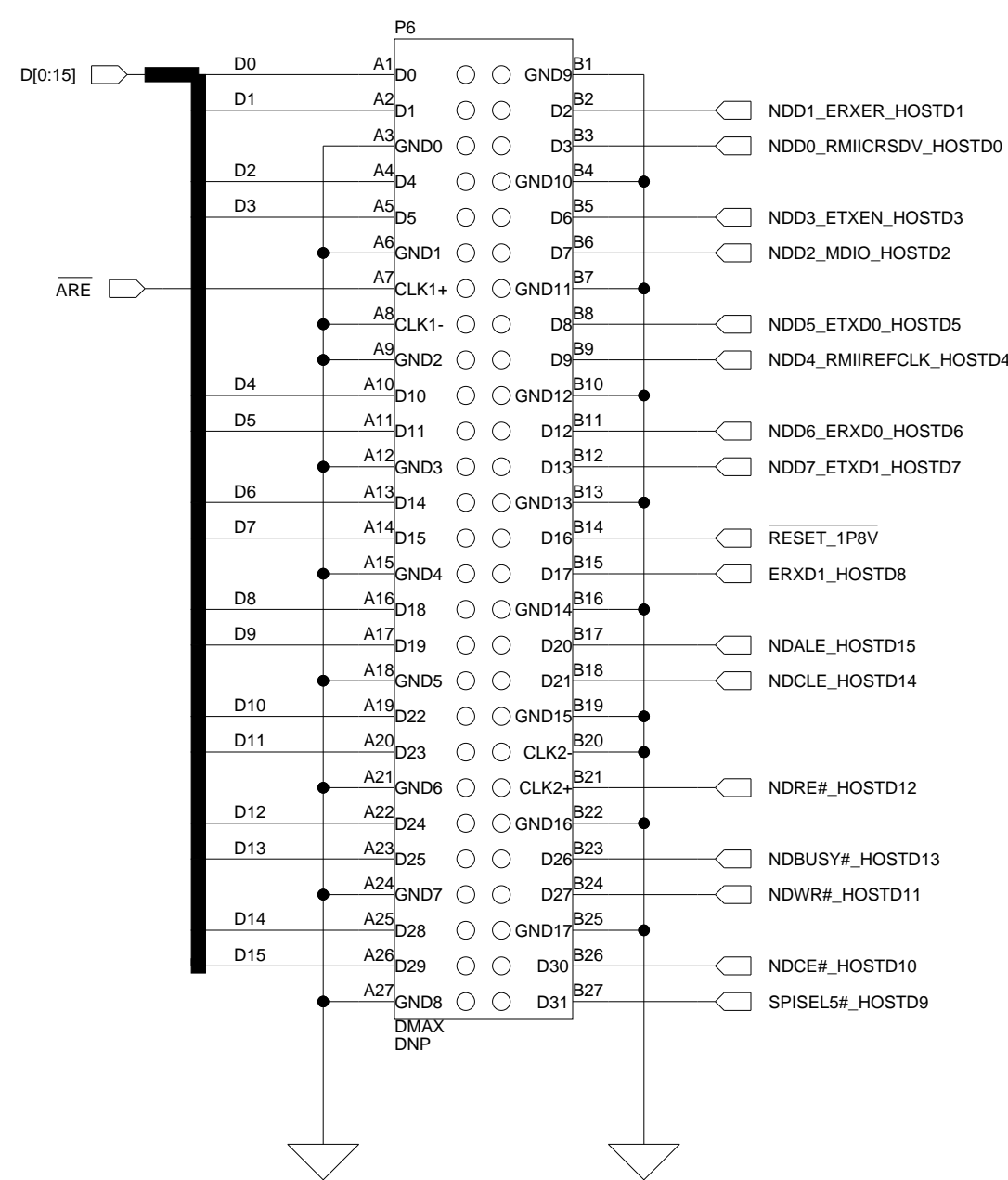
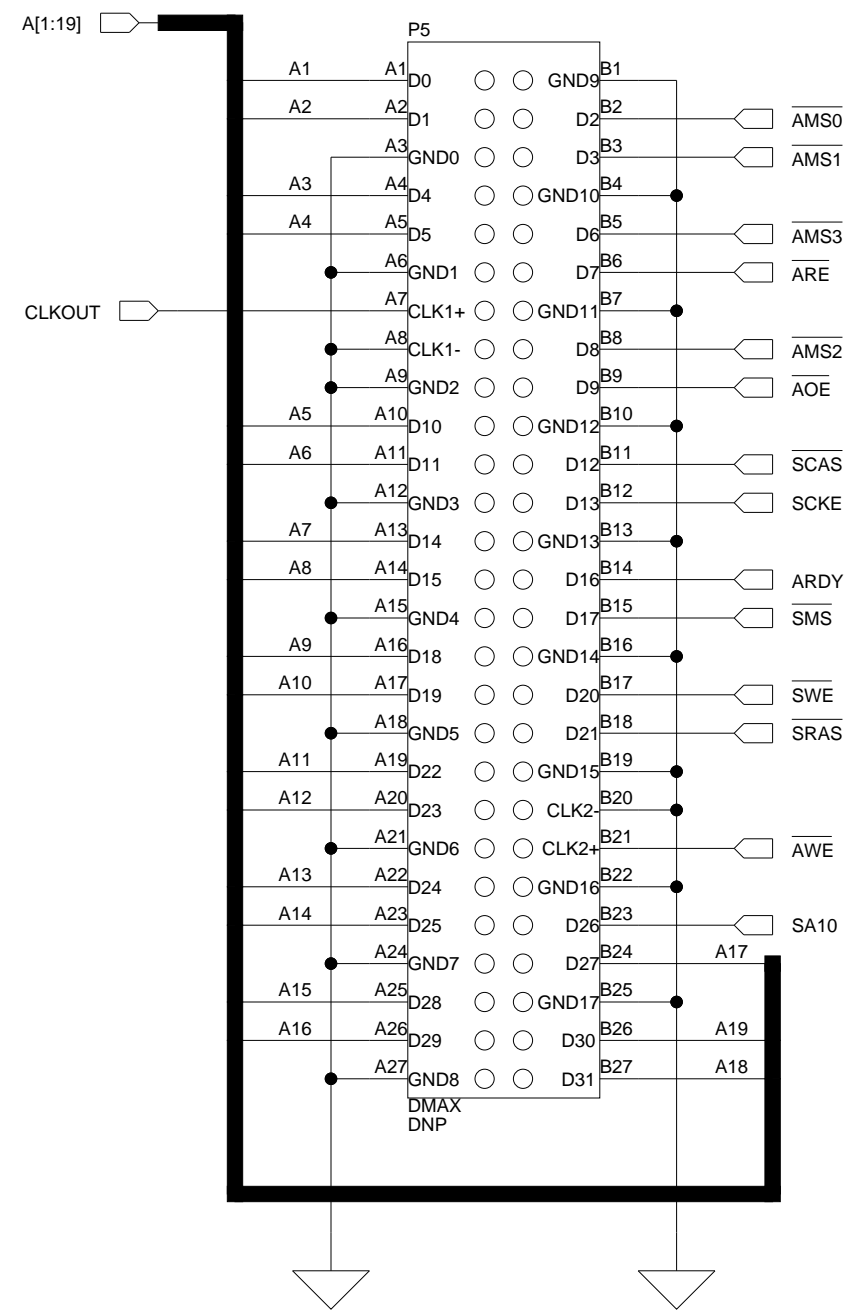


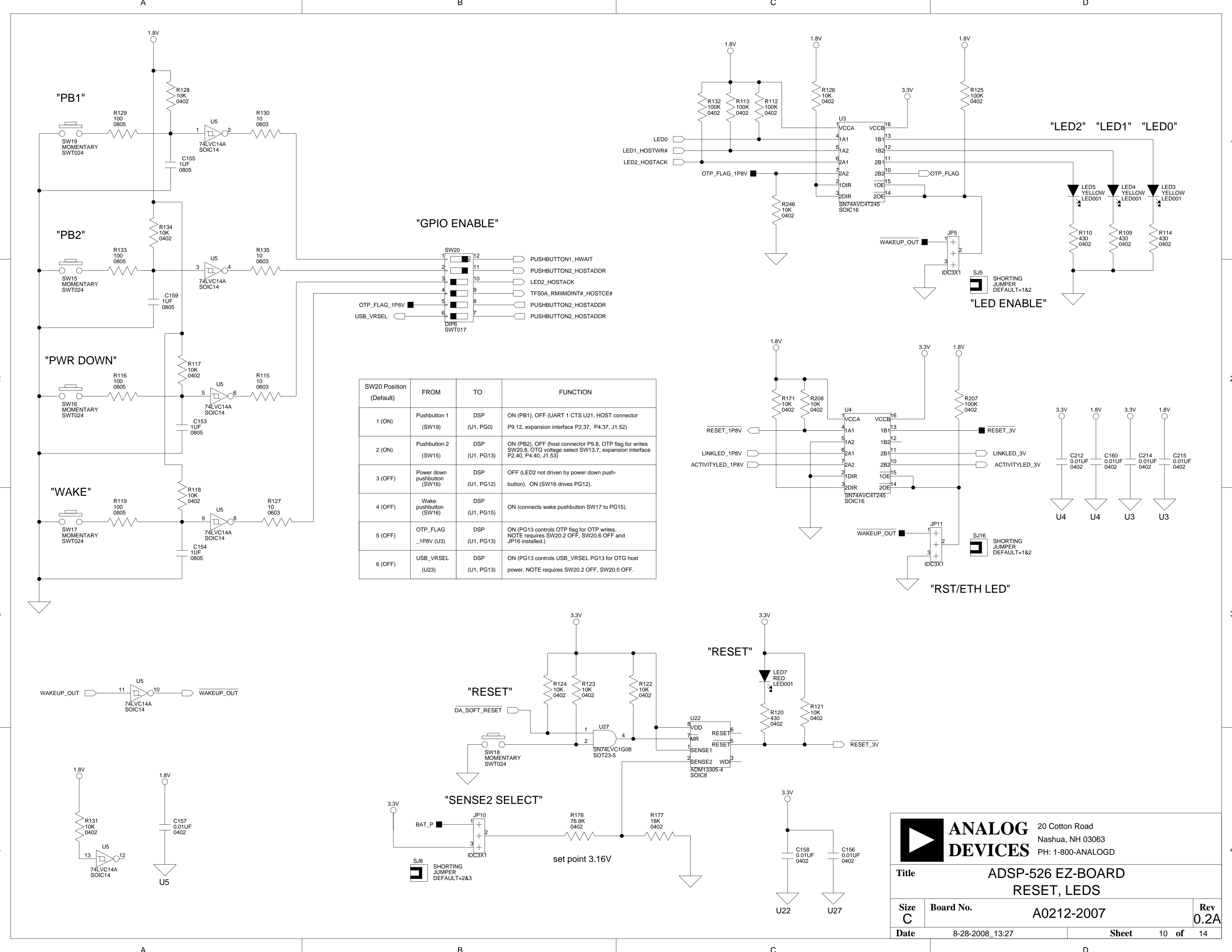
**ANALOG  
DEVICES**

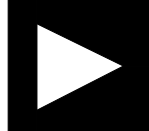
20 Cotton Road  
Nashua, NH 03063  
PH: 1-800-ANALOGD

Title		ADSP-526 EZ-BOARD ROTARY ENCODER, JTAG, RS232, HOST	
Size C	Board No.	A0212-2007	Rev 0.2A
Date	8-28-2008_11:59	Sheet	8 of 14









**ANALOG  
DEVICES**

20 Cotton Road  
Nashua, NH 03063  
PH: 1-800-ANALOGD

Title <b>ADSP-526 EZ-BOARD RESET, LEDS</b>		
Size <b>C</b>	Board No. <b>A0212-2007</b>	Rev <b>0.2A</b>
Date <b>8-28-2008_13:27</b>	Sheet <b>10</b>	of <b>14</b>



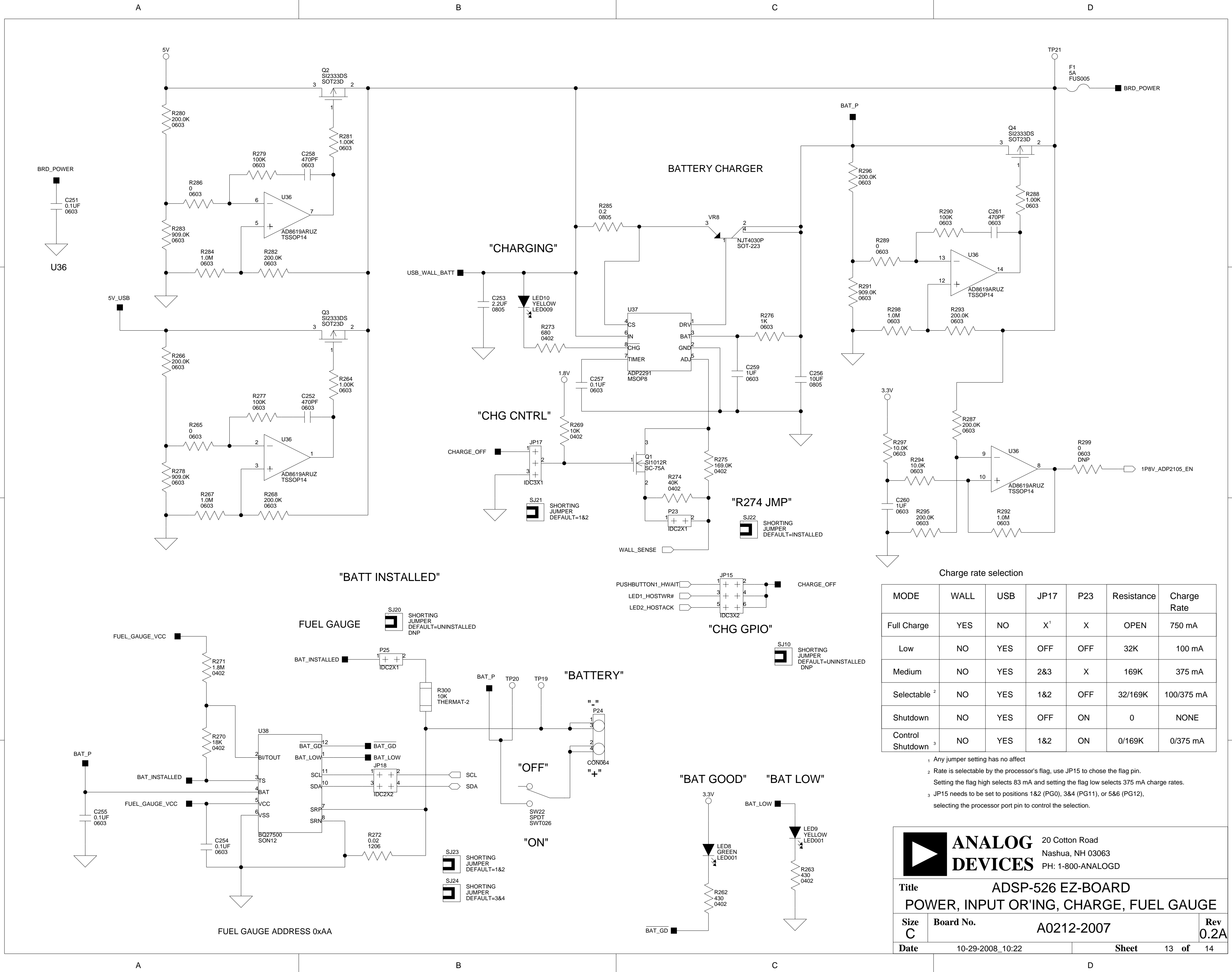


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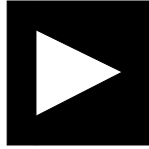
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Charge rate selection						
MODE	WALL	USB	JP17	P23	Resistance	Charge Rate
Full Charge	YES	NO	X <sup>1</sup>	X	OPEN	750 mA
Low	NO	YES	OFF	OFF	32K	100 mA
Medium	NO	YES	2&3	X	169K	375 mA
Selectable <sup>2</sup>	NO	YES	1&2	OFF	32/169K	100/375 mA
Shutdown	NO	YES	OFF	ON	0	NONE
Control Shutdown <sup>3</sup>	NO	YES	1&2	ON	0/169K	0/375 mA

- <sup>1</sup> Any jumper setting has no affect
- <sup>2</sup> Rate is selectable by the processor's flag, use JP15 to chose the flag pin.  
Setting the flag high selects 83 mA and setting the flag low selects 375 mA charge rates.
- <sup>3</sup> JP15 needs to be set to positions 1&2 (PG0), 3&4 (PG11), or 5&6 (PG12), selecting the processor port pin to control the selection.



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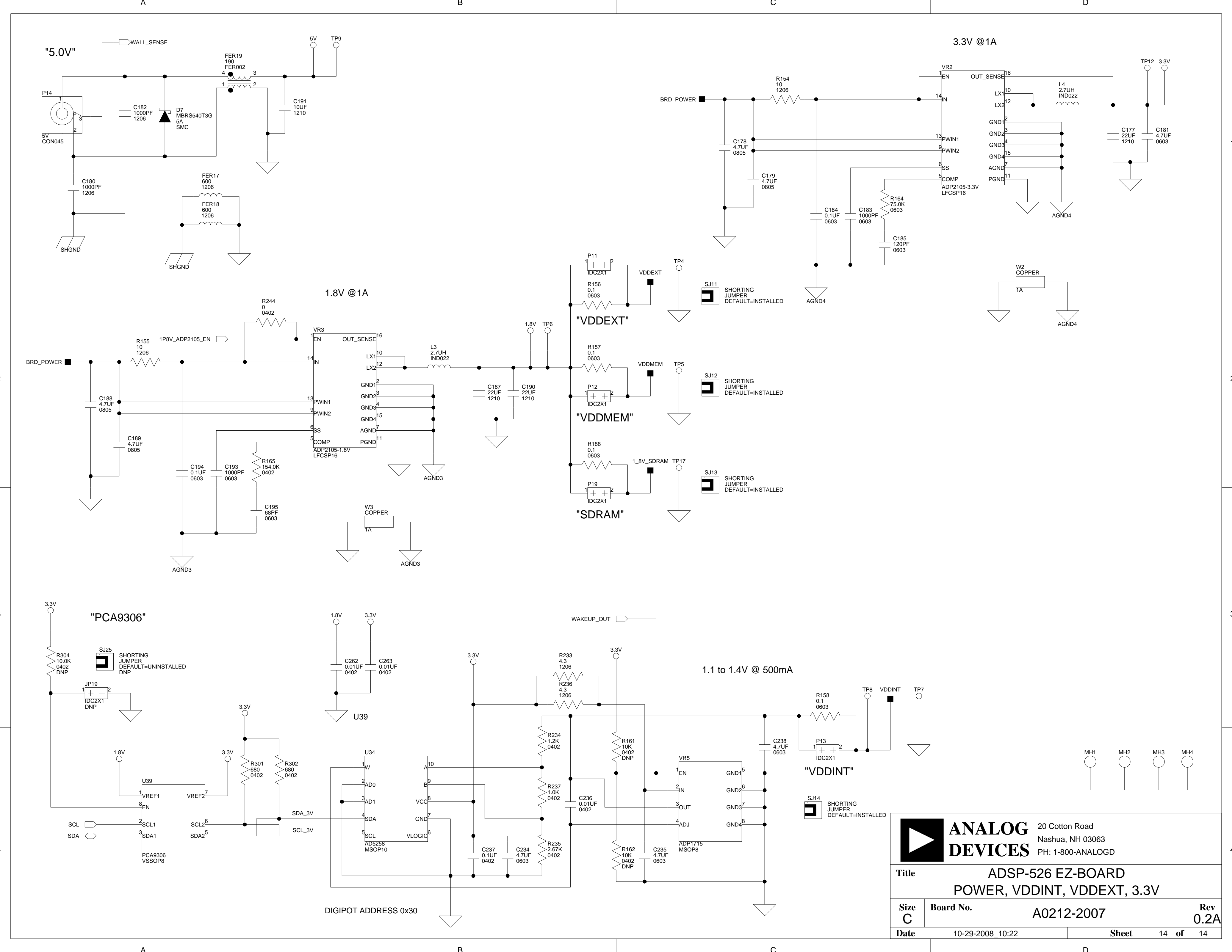
Title			ADSP-526 EZ-BOARD		
POWER, INPUT OR'ING, CHARGE, FUEL GAUGE					
Size C	Board No.		A0212-2007		Rev 0.2A
Date	10-29-2008_10:22		Sheet	13 of	14

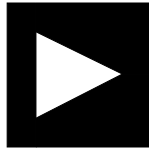
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**ANALOG  
DEVICES**

20 Cotton Road  
Nashua, NH 03063  
PH: 1-800-ANALOGD

Title ADSP-526 EZ-BOARD POWER, VDDINT, VDDEXT, 3.3V		
Size C	Board No. A0212-2007	Rev 0.2A
Date 10-29-2008_10:22	Sheet 14 of 14	