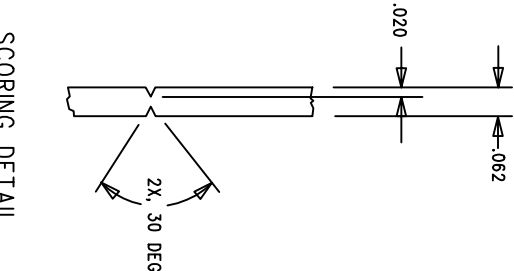
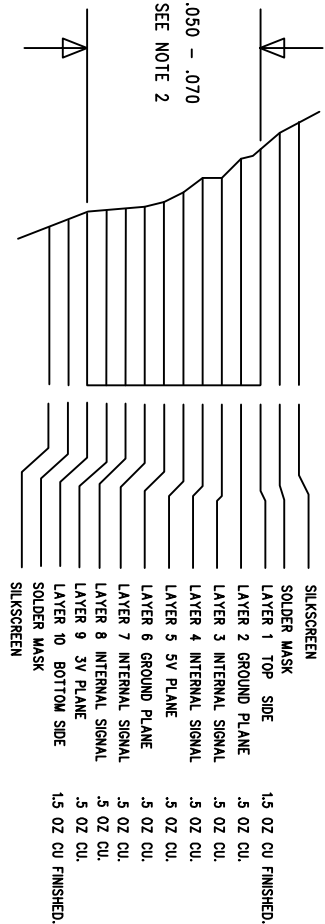
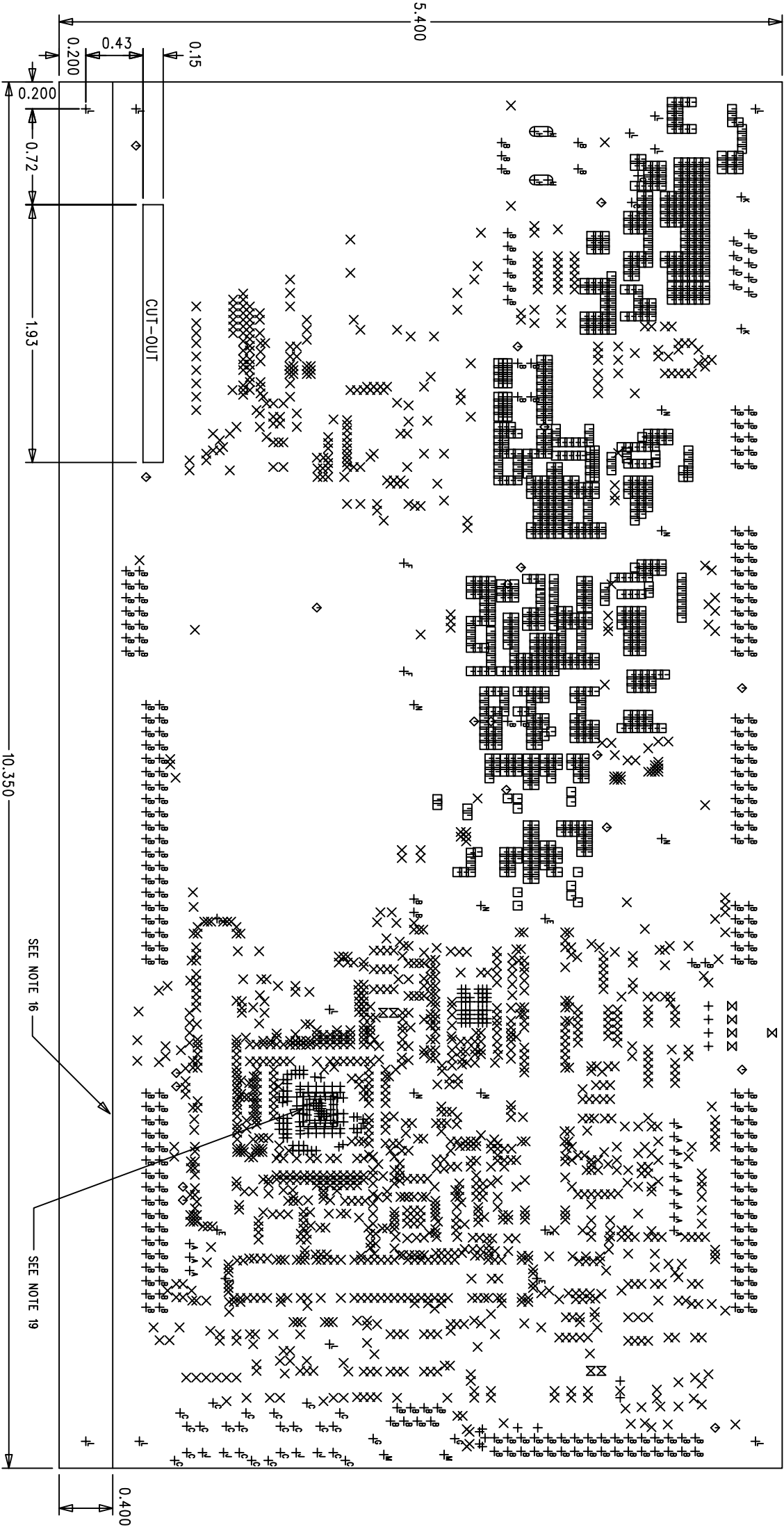


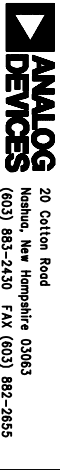
REVISIONS			
REV	DESCRIPTION OF CHANGE	DRTFR	DATE
1.0	NEW RELEASE	C.C.D.	03/06/07
1.1	REFER TO ECO2007-020	C.C.D.	06/05/07
1.2	REFER TO ECO2007-044	C.C.D.	06/22/07
1.3	REFER TO ECO2007-059	C.C.D.	08/06/07
1.4	REFER TO ECO2007-094	C.C.D.	10/10/07
2.0	REFER TO ECO2008-091	C.C.D.	11/17/08
2.1	REFER TO ECO2009-030	C.C.D.	07/31/09
2.2	REFER TO ECO2009-093	C.C.D.	07/14/10

- UNLESS OTHERWISE SPECIFIED
- BOARD TO BE FABRICATED PER IPC-6012A, CLASS 2.
 - MATERIAL: POLYGLAD FR-370HR OR EQUIVALENT, OUTER LAYERS 1/2 OZ/SQFT CU INNER LAYERS 1/2 OZ/SQFT CU FINISHED .062 (.050 MIN .070 MAX SEE DETAIL), VENDOR MAY ADJUST THICKNESS TO FULFILL NOTE 9.
 - PLATING: ADDITIONAL CU PLATING 1 OZ/SQFT
ALL HOLES PLATED THROUGH, EXCEPT AS NOTED IN HOLE LEGEND.
MINIMUM PTH BARREL THICKNESS = 0.0008" MINIMUM AVERAGE PER IPC-6012A WITH AMENDMENT 1, CLASS 2 REQUIREMENTS.
WITH NO SINGLE MEASUREMENT LESS THAN 0.00071 IN THE PLATED HOLES.
 - FINISH: SURFACES TO BE COATED BY ENIG OF 2 TO 10 MICRONS OVER A MINIMUM OF 60-200 MICRONS OF LOW STRESS NICKEL.
 - SOLDERMASK: SOLDER MASK TO BE TRANSPARENT GREEN LPI BOTH SIDES PER GERBER FILES.
 - SILKSCREEN: WHITE EPOXY INK, APPLY TO BOTH SIDES PER GERBER FILES.
MINIMUM FEATURE SIZE = 0.00492
MINIMUM AIR GAP = 0.00449
 - ARTWORK: MINIMUM AIR GAP = 0.00449
 - ALL DIMENSIONS ARE IN INCHES.
 - CONTROLLED IMPEDANCE: BOARD TO BE BUILT TO YIELD CONTROLLED IMPEDANCE OF 60 OHMS +/-10% (SINGLE ENDED) ON ALL .005" LINE WIDTHS. ALL .007" LINE WIDTHS TO BE 50 OHMS SINGLE ENDED AND 100 OHMS DIFFERENTIAL +/-10%. ALL .0079" LINE WIDTHS TO BE 45 OHMS SINGLE ENDED AND 90 OHMS DIFFERENTIAL +/-10%.
 - DO NOT ADD NON-FUNCTIONAL COPPER THEIVING ON OPEN AREAS OF OUTER LAYERS. THEIVING IS ALLOWED ON INNER LAYERS, UNLESS OTHERWISE SPECIFIED.
 - VIAS SHOULD BE COVERED ACCORDING TO ONE OF THE FOLLOWING METHODS.
METHOD 1: VIAS MUST BE FILLED WITH SOLDERMASK MATERIAL AFTER ELECTROLESS NICKEL/IMMERSION GOLD AND BEFORE PRIMARY LPI MASK. AFTER THE FILL IS CURED, THE PRIMARY MASK IS THEN APPLIED WITH NO VIA APERTURES BOTH SIDES.
METHOD 2: AFTER APPLICATION OF FULL BODY ELECTROLESS NICKEL/IMMERSION GOLD, APPLY PRIMARY MASK WITH REDUCED VIA APERTURES THAT ARE 6 MILS LARGER THAN DRILLED HOLE DIAMETER BOTH SIDES. THEN APPLY SOLDER MASK PLUG ON COMPONENT SIDE.
 - VIA HOLES (.006, .010, .012, & .014) REQUIRE TANGENCY ONLY, INSTEAD OF ANNULAR RING.
 - TEARDROP PADS ARE ACCEPTABLE WHERE NEEDED.
 - REMOVAL OF NON-FUNCTIONAL PADS ON LAYERS 3, 4, 7, AND 8 IS ACCEPTABLE.
 - USE IPC-D-356A NETLIST AS SUPPLIED FOR CHECKING.
 - V SCORE 1 LINE ON BOTH SIDES OF THE BOARD. SEE DETAIL.
 - BUILD AS 1-UP PCB.
 - THE FOLLOWING NETS ARE INTENTIONALLY SHORTED AND RESULT IN IPC NETLIST ERRORS: AT W1 : GND & AGND (LAYER 10)
AT W3 : GND & PGND (LAYERS 1 & 10)
AT W4 : GND & PGND2 (LAYERS 1 & 10)
AT W5 : GND & AGND2 (LAYER 10)
 - HOLES/VIAS IN AREA SHOWN TO BE FILLED AND LEVELLED IN AREAS SHOWN WITH NON-CONDUCTIVE PASTE.



SIZE	QTY	SYM	PLATED	TOL.
0.006	87	+	YES	+ .003/- .006
0.01	1993	X	YES	+ .003/- .010
0.014	934	□	YES	+ .003/- .012
0.028	20	◇	YES	+ .003/- .014
0.032	5	×	YES	+/- .0003
0.035	4	×	YES	+/- .0003
0.037	12	+	YES	+/- .0003
0.038	243	+	YES	+/- .0003
0.043	24	+	YES	+/- .0003
0.047	9	+	YES	+/- .0003
0.053	6	+	NO	+/- .0003
0.055	2	+	YES	+/- .0003
0.063	2	+	YES	+/- .0003
0.071 ± 0.173	2	+	YES	+/- .0003
0.117	4	+	NO	+/- .0003
0.125	2	+	NO	+/- .0005
0.125	11	+	YES	+/- .0003
0.128	2	+	NO	+/- .0005
0.167	7	+	YES	+/- .0005

UNLESS OTHERWISE SPECIFIED		CONTRACT NO.	
DIMENSIONS ARE IN INCHES		APPROVALS	
TOLERANCES ARE : XX +/- .010 XXX +/- .005		DATE	
MATERIAL		C.C.D.	
SEE NOTES		01/14/10	
CHECKED			
ENGINEERING			
QUALITY			
FINISH			
SEE NOTES			
DO NOT SCALE THIS DRAWING			



FABRICATION DRAWING

ADSP-BF527 EZ-KIT LITE

SIZE B DWG. NO. A0208-2006-REF REV. 2.2

SCALE 1 : 1 SHEET 1 OF 1