LTP88XX Operations Reference Manual

INTRODUCTION

This reference manual lists the functionality of the standard PMBus commands and the Analog Devices manufacturer-specific commands that are supported by the LTP88XX power µModule® (micromodule) regulators, including the *LTP8800-1A*, *LTP8800-4A*, *LTP8800-2*, *LTP8803-1A*, *LTP8802A-1B*, and *LTP8813*. The operational information of the LTP88XX is also described.

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SUPPORTED COMMANDS LIST

Table 1 and *Table 2* list the supported PMBus commands and the Analog Devices manufacturer-specific commands. A complete description of the supported PMBus commands is found in the *PMBus Power System Management Protocol Specification, Revision 1.2, dated September 6, 2010*. All the PMBus commands that are not listed in *Table 1* are implicitly reserved or not supported by the LTP88XX modules. The users must avoid blind writes and attempts to access the unsupported or reserved commands to prevent undesired operation results for the LTP88XX modules.

The user must not assume the compatibility of commands between different devices based upon command names. Refer to the LTP88XX data sheets for a complete definition of the function of the command. Analog Devices strives to keep command functionality compatible between all Analog Devices products. However, differences can be introduced to address specific product design requirements.

See the *Operation and Application Information* section for detailed information and for the application of each supported register.

Table 1. Supported Standard PMBus Commands

COMMAND CODE	COMMAND NAME	COMMAND CODE	COMMAND NAME
0x01	OPERATION	0x59	VIN_UV_FAULT_LIMIT
0x02	ON_OFF_CONFIG	0x5A	VIN_UV_FAULT_RESPONSE
0x03	CLEAR_FAULTS	0x5B	IIN_OC_FAULT_LIMIT
0x10	WRITE_PROTECT	0x5C	IIN_OC_FAULT_RESPONSE
0x15	STORE_USER_ALL	0x5E	POWER_GOOD_ON
0x16	RESTORE_USER_ALL	0x5F	POWER_GOOD_OFF
0x1B	SMBALERT_MASK	0x60	TON_DELAY
0x20	VOUT_MODE	0x61	TON_RISE
0x21	VOUT_COMMAND	0x62	TON_MAX_FAULT_LIMIT
0x22	VOUT_TRIM	0x63	TON_MAX_FAULT_RESPONSE
0x23	VOUT_CAL_OFFSET	0x64	TOFF_DELAY
0x24	VOUT_MAX	0x65	TOFF_FALL
0x27	VOUT_TRANSITION_RATE	0x66	TOFF_MAX_WARN_LIMIT
0x28	VOUT_DROOP	0x68	POUT_OP_FAULT_LIMIT
0x29	VOUT_SCALE_LOOP	0x69	POUT_OP_FAULT_RESPONSE
0x2A	VOUT_SCALE_MONITOR	0x78	STATUS_BYTE
0x35	VIN_ON	0x79	STATUS_WORD
0x36	VIN_OFF	0x7A	STATUS_VOUT
0x37	INTERLEAVE	0x7B	STATUS_IOUT
0x38	IOUT_CAL_GAIN	0x7C	STATUS_INPUT
0x39	IOUT_CAL_OFFSET	0x7D	STATUS_TEMPERATURE
0x40	VOUT_OV_FAULT_LIMIT	0x7E	STATUS_CML
0x41	VOUT_OV_FAULT_RESPONSE	0x7F	STATUS_OTHER
0x42	VOUT_OV_WARN_LIMIT	0x80	STATUS_MFR_SPECIFIC
0x43	VOUT_UV_WARN_LIMIT	0x88	READ_VIN
0x44	VOUT_UV_FAULT_LIMIT	0x89	READ_IIN
0x45	VOUT_UV_FAULT_RESPONSE	0x8B	READ_VOUT
0x46	IOUT_OC_FAULT_LIMIT	0x8C	READ_IOUT
0x47	IOUT_OC_FAULT_RESPONSE	0x8E	READ_TEMPERATURE_2
0x4A	IOUT_OC_WARN_LIMIT	0x94	READ_DUTY_CYCLE
0x4B	IOUT_UC_FAULT_LIMIT	0x95	READ_FREQUENCY
0x4C	IOUT_UC_FAULT_RESPONSE	0x96	READ_POUT
0x4F	OT_FAULT_LIMIT	0x9A	MFR_MODEL
0x50	OT_FAULT_RESPONSE	0xD0	SLV_ADDR_SELECT
0x51	OT_WARN_LIMIT	0xF2	READ_BLACKBOX_CURR
0x55	VIN_OV_FAULT_LIMIT	0xF3	READ_BLACKBOX_PREV
0x56	VIN_OV_FAULT_RESPONSE		

Table 2. Supported Analog Devices Manufacturer-Specific Commands

COMMAND CODE	COMMAND NAME	COMMAND CODE	COMMAND NAME
0xFE00	GO_CMD	0xFE43	PGOOD_FAULT_DEB
0xFE01	NM_DIGFILT_LF_GAIN_SETTING	0xFE44	PGOOD1_FAULT_SELECT
0xFE02	NM_DIGFILT_ZERO_SETTING	0xFE45	PGOOD2_FAULT_SELECT
0xFE03	NM_DIGFILT_POLE_SETTING	0xFE46	SOFT_START_BLANKING
0xFE04	NM_DIGFILT_HF_GAIN_SETTING	0xFE47	SOFT_STOP_BLANKING
0xFE09	SS_DIGFILT_LF_GAIN_SETTING	0xFE48	BLACKBOX_SETTING
0xFE0A	SS_DIGFILT_ZERO_SETTING	0xFE4A	FILTER_TRANSITION
0xFE0B	SS_DIGFILT_POLE_SETTING	0xFE4D	OVP_FAULT_CONFIG
0xFE0C	SS_DIGFILT_HF_GAIN_SETTING	0xFE51	SOFT_START_SETTING
0xFE2C	IIN_OC_FAST_SETTING	0xFE55	SYNC
0xFE2D	IOUT_OC_FAST_SETTING	0xFE5B	AUTO_GO_CMD
0xFE2E	IOUT_UC_FAST_SETTING	0xFE5F	SR_SETTING
0xFE2F	VOUT_OV_FAST_SETTING	0xFE65	VOUT_DROOP_SETTING
0xFE30	DEBOUNCE_SETTING_1	0xFE8C	FAULT_VOUT
0xFE31	DEBOUNCE_SETTING_2	0xFE8D	FAULT_IOUT
0xFE32	DEBOUNCE_SETTING_3	0xFE8E	FAULT_INPUT
0xFE34	VOUT_OV_FAST_FAULT_RESPONSE	0xFE8F	FAULT_TEMPERATURE
0xFE35	IOUT_OC_FAST_FAULT_RESPONSE	0xFE90	FAULT_CML
0xFE36	IOUT_UC_FAST_FAULT_RESPONSE	0xFE91	FAULT_OTHER
0xFE37	IIN_OC_FAST_FAULT_RESPONSE	0xFE92	FAULT_MFR_SPECIFIC
0xFE3E	DELAY_TIME_UNIT	0xFE93	FAULT_UNKNOWN
0xFE3F	WDT_SETTING	0xFE94	STATUS_UNKNOWN
		0xFE95	FIRST_FAULT_ID

OPERATION AND APPLICATION INFORMATION

Power-Up and Power-Down

Power-Up and Power-Down Sequence

When the 3.3V supply is applied to the devices, a certain time elapses before the internal controller can regulate the power supply. It is recommended to turn on the 3.3V auxiliary power supply before turning on the 7V auxiliary power supply and/or the input main power supply and reverse sequence for power-down.

ON/OFF Control

The PMBus commands OPERATION (Register 0x01) and ON_OFF_CONFIG (Register 0x02) control the power-up and power-down behavior.

Table 3. Register 0x01 — OPERATION

BITS	NAME	R/W	DESCRIPTION
[7:6]	Enable	R/W	00 = immediate off 01 = soft off 10 = device on 11 = reserved
[5:0]	Reserved	N/A	N/A

Table 4. Register 0x02 — ON_OFF_CONFIG

BITS	NAME	R/W	DESCRIPTION
[7:5]	Reserved	N/A	N/A
4	Power-up control	R/W	0 = device powers up when power is present 1 = device powers up only when commanded by the CTRL pin and the OPERATION command
3	Command enable	R/W	0 = ignores OPERATION command 1 = the OPERATION command must be set to 1 to enable the device (in addition to setting Bit 2)
2	CTRL pin enable	R/W	0 = ignores the CTRL pin 1 = CTRL pin must be asserted to enable the device (in addition to setting Bit 3)
1	CTRL pin polarity	R/W	0 = active low 1 = active high
0	CTRL pin power-down action	R/W	Actions to take on power-down when it is activated by the CTRL pin. 0 = soft off 1 = turns off the output immediately

The VIN_ON (Register 0x35) command sets the value of the input voltage (V_{RMS}) at which the device starts power conversion. Setting the VIN_ON = 0 effectively disables this function.

Table 5. Register 0x35 — VIN_ON

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in linear data format ($X = Y \times 2^N$)

The VIN_OFF (Register 0x36) command sets the value of the input voltage (V_{RMS}) at which the device stops power conversion. The VIN_OFF register is not checked until the device reaches the regulation voltage or TON_MAX has expired.

Table 6. Register 0x36 — VIN_OFF

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in linear data format ($X = Y \times 2^N$)

Soft Start

The soft-start proceeds as follows:

- Upon power-up, the LTP88XX modules wait for the programmed TON_DELAY (Register 0x60).
- The soft start begins to ramp up the internal digital reference. The total duration of the soft-start ramp is programmed using the TON_RISE (Register 0x61).

The delays for the turn-on command TON_DELAY (Register 0x60) and the soft-start ramp-up time TON_RISE (Register 0x61) can each be programmed in steps of 1ms. The maximum ramp-up time [in ms] = 100 × V_{REF} [in V]. See *VOUT Commands Related Registers* for the internal reference voltage V_{REF} programming. The maximum delay time is 1024ms.

Table 7. Register 0x60 — TON_DELAY

BITS	NAME	R/W	DESCRIPTION
[15:0]	TON_DELAY	R/W	Unsigned integer with steps of 1ms

Table 8. Register 0x61 — TON_RISE

BITS	NAME	R/W	DESCRIPTION
[15:0]	TON_RISE	R/W	Unsigned integer with steps of 1ms

If the soft start from a precharge function is enabled (Register 0xFE51[0] = 1), the soft-start ramp starts from the current value of the output voltage sensed on the V_S^+ and V_S^- pins, therefore, the soft-start ramp-up time is reduced proportionally.

Table 9. Register 0xFE51 — SOFT_START_SETTING

BITS	NAME	R/W	DESCRIPTION
7	Soft stop enable for current faults	R/W	0 = disable 1 = enable
6	Soft stop enable for other faults	R/W	0 = disable 1 = enable
[5:3]	SR phase-in speed up factor during soft stop	R/W	During the soft-stop process, these bits increase the SR edge transition speed specified by Register 0xFE5F[7:4]. The speed-up factor is 2^x, where x is this 3-bit number. The maximum speed of the SR edge is 40ns per t_{SW}. For example, if Register 0xFE5F specifies 5ns per $4t_{SW}$, setting these three bits to 2 increases the SR speed to 5ns per t_{SW} (5ns/4 t_{SW} × 2^2). Setting these bits to 3 increases the SR speed to 10ns per t_{SW} (5ns/4t_{SW} × 2^3). Setting these bits to 7 increases the SR speed to 40ns per t_{SW}, the maximum rate. A smaller value means slower SR transitioning.
[2:1]	Reserved	N/A	N/A
0	Soft start from precharge	R/W	1 = enables the soft start from precharge function

During soft start, use Register 0xFE46 to mask various faults.

Table 10. Register 0xFE46 — SOFT_START_BLANKING

BITS	NAME	R/W	DESCRIPTION
15	VOUT_OV_FAULT	R/W	1 = this flag is ignored during soft start
14	Reserved	N/A	N/A
13	TON_MAX_FAULT	R/W	1 = this flag is ignored during soft start
12	VIN_OV_FAULT	R/W	1 = this flag is ignored during soft start
11	VIN_UV_FAULT	R/W	1 = this flag is ignored during soft start
10	IIN_OC_FAULT	R/W	1 = this flag is ignored during soft start
9	IOUT_OC_FAULT	R/W	1 = this flag is ignored during soft start
8	IOUT_UC_FAULT and IOUT_UC_FAST_FAULT	R/W	1 = this flag is ignored during soft start
7	POUT_OP_FAULT	R/W	1 = this flag is ignored during soft start
6	IIN_OC_FAST_FAULT	R/W	1 = this flag is ignored during soft start
5	IOUT_OC_FAST_FAULT	R/W	1 = this flag is ignored during soft start
4	VOUT_OV_FAST	R/W	1 = this flag is ignored during soft start
3	Reserved	N/A	N/A
2	Reserved	N/A	N/A
1	Reserved	N/A	N/A
0	OT_FAULT	R/W	1 = this flag is ignored during soft start

Soft Stop

Soft stop can be enabled normal shutdown of the power supply using the OPERATION and ON_OFF_CONFIG commands. It can also be enabled during a fault triggered condition using Register 0xFE51[7:6].

The soft-stop process occurs in the same manner as the soft start process. The delays for the turn-off command TOFF_DELAY (Register 0x64) and the ramp-down time TOFF_FALL (Register 0x65) can each be programmed in steps of 1ms.

Table 11. Register 0x64 — TOFF_DELAY

BITS	NAME	R/W	DESCRIPTION
[15:0]	TOFF_DELAY	R/W	Unsigned integer with steps of 1ms

Table 12. Register 0x65 — TOFF_FALL

BITS	NAME	R/W	DESCRIPTION
[15:0]	TOFF_FALL	R/W	Unsigned integer with steps of 1ms

During soft-stop, use Register 0xFE47 to mask various faults.

Table 13. Register 0xFE47 — SOFT_STOP_BLANKING

BITS	NAME	R/W	DESCRIPTION
15	VOUT_OV_FAULT	R/W	1 = this flag is ignored during soft stop
14	Reserved	N/A	N/A
13	TON_MAX_FAULT	R/W	1 = this flag is ignored during soft stop
12	VIN_OV_FAULT	R/W	1 = this flag is ignored during soft stop
11	VIN_UV_FAULT	R/W	1 = this flag is ignored during soft stop
10	IIN_OC_FAULT	R/W	1 = this flag is ignored during soft stop
9	IOUT_OC_FAULT	R/W	1 = this flag is ignored during soft stop
8	IOUT_UC_FAULT and IOUT_UC_FAST_FAULT	R/W	1 = this flag is ignored during soft stop
7	POUT_OP_FAULT	R/W	1 = this flag is ignored during soft stop
6	IIN_OC_FAST_FAULT	R/W	1 = this flag is ignored during soft stop
5	IOUT_OC_FAST_FAULT	R/W	1 = this flag is ignored during soft stop
4	VOUT_OV_FAST	R/W	1 = this flag is ignored during soft stop
3	Reserved	N/A	N/A
2	Reserved	N/A	N/A
1	Reserved	N/A	N/A
0	OT_FAULT	R/W	1 = this flag is ignored during soft stop

SR Phase In

Synchronous rectification (SR) is used for the output rectifiers. When SR is enabled, an abrupt change in the SR outputs may cause the output voltage to dip momentarily. An optional SR transition process, during which the pulse width of the SR pulse-width modulation (PWM) outputs is increased slowly, can be applied to the SR outputs. The speed at which the SR edges move from zero duty cycle to maximum duty cycle (as determined by the control loop) can be programmed from 5ns per t_{SW} to 5ns per $1024t_{SW}$ (t_{SW} = switching cycle) using Register 0xFE5F[7:4].

Table 14. Register 0xFE5F — SR_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:4]	SR phase-in speed	R/W	SR edges move by 5ns every switching cycle 0000 = $1t_{SW}$ 0001 = $2t_{SW}$ 0010 = $4t_{SW}$ 0011 = $8t_{SW}$ 0100 = $16t_{SW}$ 0101 = $32t_{SW}$ 0110 = $64t_{SW}$ 0111 = $128t_{SW}$ 1000 = $256t_{SW}$ 1001 = $384t_{SW}$ 1010 = $512t_{SW}$ 1011 = $640t_{SW}$ 1100 = $768t_{SW}$ 1101 = $832t_{SW}$ 1110 = $960t_{SW}$ 1111 = $1024t_{SW}$
[3:1]	Reserved	N/A	N/A
0	Blank SR during soft start	R/W	1 = blank SR during soft start

During the soft-stop process, the register 0xFE51[5:3] bits increase the SR edge transition speed specified by Register 0xFE5F[7:4]. The speed-up factor is 2^x, where x is this 3-bit number. The maximum speed of the SR edge is 40ns per t_{SW}. For example, if Register 0xFE5F specifies 5ns per $4t_{SW}$, setting these three bits to 2 increases the SR speed to 5ns per t_{SW} ($5ns/4t_{SW} \times 2^2$). Setting these bits to 3 increases the SR speed to 10ns per t_{SW} ($5ns/4t_{SW} \times 2^3$). Setting these bits to 7 increases the SR speed to 40ns per t_{SW} (the maximum rate). A smaller value means slower SR transitioning.

VOUT Commands

VOUT Commands Related Registers

The VOUT_MODE (Register 0x20) command sets the data format for the output voltage related data. The 5-bit parameter sets the exponent value for a linear format.

Table 15. Register 0x20 — VOUT_MODE

BITS	NAME	R/W	DESCRIPTION
[7:5]	Mode	R	Fixed at 000, which means that only the linear data format is supported
[4:0]	Exponent−N	R/W	Two's complement N-exponent used in the output voltage related commands in a linear data format ($V = Y \times 2^N$)

The VOUT_COMMAND (Register 0x21) command sets the output voltage. The exponent N is set using VOUT_MODE[4:0]. The setting or adjusting of this register is gated by the GO Bit in Register 0xFE00.

Table 16. Register 0x21 — VOUT_COMMAND

BITS	NAME	R/W	DESCRIPTION
[15:0]	Mantissa−Y	R/W	16-bit unsigned integer Y value for the linear data format ($V = Y \times 2^N$). The N is defined using the VOUT_MODE[4:0].

VOUT_TRIM and VOUT_CAL_OFFSET can be used to apply a fixed offset voltage to the VOUT_COMMAND value. The value of VOUT_COMMAND is summed with the value of VOUT_TRIM and VOUT_CAL_OFFSET, and the result is sent to the control loop as the output voltage setpoint.

Table 17. Register 0x22 — VOUT_TRIM

BITS	NAME	R/W	DESCRIPTION
[15:0]	Offset trim	R/W	Two's complement integer used to apply a fixed offset voltage to the VOUT_COMMAND value

Table 18. Register 0x23 — VOUT_CAL_OFFSET

BITS	NAME	R/W	DESCRIPTION
[15:0]	Offset trim	R/W	Two's complement integer used to apply a fixed offset voltage to the VOUT_COMMAND value

The VOUT_MAX command sets an upper limit on the output voltage.

Table 19. Register 0x24 — VOUT_MAX

BITS	NAME	R/W	DESCRIPTION
[15:0]	Mantissa−Y	R/W	Set the output voltage upper limit. The 16-bit unsigned integer Y value for a linear data format ($V = Y \times 2^N$). The N is defined using the VOUT_MODE[4:0].

The VOUT_DROOP command sets the rate, in mV/A, at which the output voltage decreases or increases with increasing or decreasing output current. For VOUT_DROOP, the output current is continuously sampled with a selectable rate (set in Register 0xFE65[1:0]) before the droop is applied.

Table 20. Register 0x28 — VOUT_DROOP

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 21. Register 0xFE65 — VOUT_DROOP_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:3]	Reserved	N/A	N/A
2	Disable VOUT_TRANSITION_RATE	R/W	1 = changes the internal voltage reference at the fastest internal supported rate 0 = the output voltage changes from one value to another as programmed by the VOUT_TRANSITION_RATE command
[1:0]	VOUT_DROOP sampling rate	R/W	00 = 82µs 01 = 164µs 10 = 327µs 11 = 655µs

The V_S^+ and V_S^- pins are used to monitor and protect the remote load voltage. The differential V_S^+ and V_S^- input pins are the main feedback sense point for the power supply control loop. The V_S^+ and V_S^- pins sense point on the power rail requires an external resistor divider to bring the nominal common-mode signal to the range from 0V to 1.6V. This resistor divider is programmed into VOUT_SCALE_LOOP and VOUT_SCALE_MONITOR, accordingly.

The VOUT_SCALE_LOOP command sets the gain (K_R) by which the commanded voltage (V_{OUT}) is scaled to generate the internal reference voltage (V_{REF}). The $V_{REF} = V_{OUT} \times K_R$, where $K_R = Y \times 2^N$.

Table 22. Register 0x29 — VOUT_SCALE_LOOP

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

The VOUT_SCALE_MONITOR command sets the gain (K_{VOUT}) by which the sensed output voltage at the DUT (V_{SENSE}) is scaled to generate the reading for the READ_VOUT command. READ_VOUT = V_{SENSE} / K_{VOUT}, where $K_{VOUT} = Y \times 2^N$.

Table 23. Register 0x2A — VOUT_SCALE_MONITOR

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Usually it is recommended that VOUT_SCALE_LOOP = VOUT_SCALE_MONITOR = $R_{BOT}/(R_{TOP} + R_{BOT})$, where R_{TOP} and R_{BOT} are top and bottom resistors of the external resistor divider.

Soft Transition

When the device receives a VOUT_COMMAND or OPERATION command that causes the output voltage to change, this command sets the output transition rate (or slew rate), in mV/µs, at which the V_S^+ and V_S^- pins change voltage. The output voltage slew rate (or transition rate) can be set using the PMBus VOUT_TRANSITION_RATE command (Register 0x27). The slew rate determines how quickly the output voltage is adjusted in response to a change in the digital reference. The fastest slew rate supported by the LTP88XX modules is 1kV/sec, and the slowest rate is 14.3V/sec. A PMBus command setting of 0 sets the slew rate to the slowest setting. This slew rate is the rate at which the internal setpoint reference can change; the actual output voltage change depends on the control loop bandwidth and its ability to track the reference.

If a fault occurs at any time during the soft-start process with an action set to a value other than shutdown, the remainder of the soft-start ramp continues at the transition rate specified by the PMBus command VOUT_TRANSITION_RATE.

Table 24. Register 0x27 — VOUT_TRANSITION_RATE

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Go and Auto Go Command

When reprogramming more than one of the following outputs, it is important to first update all the registers and then latch the information into the controller at the same time. The GO command (Register 0xFE00) facilitates this simultaneous update. It acts as a gate to apply all functions related to the commands at the same time. The GO command gates the following functions.

Table 25. Register 0xFE00 — GO_CMD

BITS	NAME	R/W	DESCRIPTION
7	Reserved	N/A	N/A
6	SYNC GO	W	This bit latches Register 0xFE55
[5:4]	Reserved	N/A	N/A
3	Filter GO	W	This bit latches Register 0xFE4A, Register 0xFE01 to Register 0xFE04, and Register 0xFE09 to Register 0xFE0C
[2:1]	Reserved	N/A	N/A
0	Voltage Reference GO	W	Update reference voltage commanded by the VOUT_COMMAND (Register 0x21)

During reprogramming, the outputs are temporarily disabled. The auto GO command (Register 0xFE5B) is an added level of protection that restricts the user from making a change to certain commands.

Table 26. Register 0xFE5B — AUTO_GO_CMD

BITS	NAME	R/W	DESCRIPTION
[7:1]	Reserved	N/A	N/A
0	V_{REF} auto-go enable	R/W	0 = GO_CMD[0] (Register 0xFE00 Bit 0) is required to latch the programmed reference voltage in VOUT_COMMAND into the internal loop frequency 1 = write to any commands affecting the reference voltage is automatically latched into the internal loop reference voltage, commands that affect the reference voltage include VOUT_COMMAND, VOUT_MODE, VOUT_MAX, VOUT_TRIM, VOUT_CAL_OFFSET, VOUT_SCALE_LOOP, and VOUT_DROOP

Control Loop

Operation Mode

The LTP88XX modules are designed to operate under forced continuous mode (FCM).

Compensation

The loop response of the power supply can be changed using the internal programmable digital filter. The transfer function of the digital filter in the z-domain is resolved by Equation *1*,

$$H(z) = \frac{D}{LFG} \times \frac{1}{1-z^{-1}} + \frac{C}{HFG} \times \frac{1-\frac{B}{256}\times z^{-1}}{1-\frac{A}{256}\times z^{-1}} \quad (1)$$

where

LFG = $5.968 \times m \times 10^6/f_{SW}$,

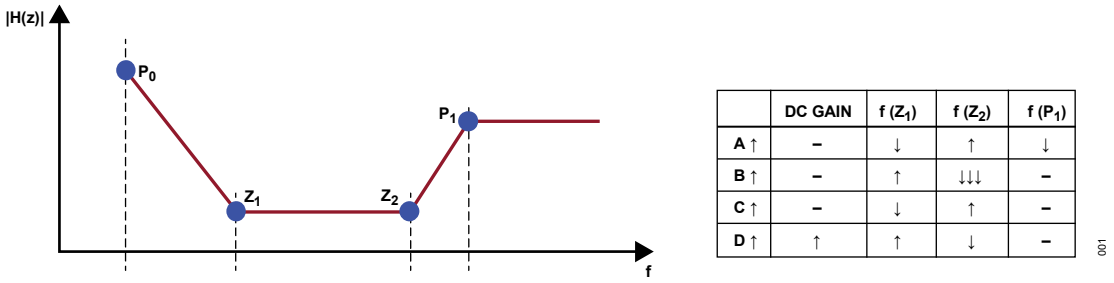
HFG = $3.73 \times m \times 10^5/f_{SW}$,

m = 8 when $390.625kHz \le f_{SW} < 781.250kHz$,

m = 16 when $781.250kHz \le f_{SW} < 1MHz$.

To tailor the loop response to a specific application, set parameters A, B, C, and D in the corresponding registers See *Figure 1*. This filter provides one low-frequency integration pole, P_0; two zeros, Z_1 and Z_2; and one high-frequency pole, P_1.

- The DC gain is adjusted by the parameter D: larger D provides higher DC gain.
- The high-frequency pole P_1's location is adjusted by parameter A: larger A moves P_1 to a lower frequency.
- Zero Z_2's location is mainly determined by parameter B: larger B moves Z_2 to a lower frequency.



	DC GAIN	f (Z_1)	f (Z_2)	f (P_1)
A ↑	–	↓	↑	↓
B ↑	–	↑	↓↓↓	–
C ↑	–	↓	↑	–
D ↑	↑	↑	↓	–

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Figure 1. Programmable Digital Filter of the LTP88XX

It is recommended that *LTpowerCAD*® be used to facilitate deciding the filter parameters. The software's graphical user interface (GUI) displays the filter response in a Bode plot format and calculates all stability criteria for the power supply.

Filter Transition

Two sets of registers allow programming of two different filters.

- Normal mode filter (configured in Register 0xFE01 to Register 0xFE04)
- Soft-start filter (configured in Register 0xFE09 to Register 0xFE0C)

The setting or adjusting of these registers is gated by the GO Bit in Register 0xFE00. See the *Go and Auto Go Command* section for more details.

Table 27. Register 0xFE01 — NM_DIGFILT_LF_GAIN_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:0]	D	R/W	Decimal value is used in Equation *1*.

Table 28. Register 0xFE02 — NM_DIGFILT_ZERO_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:0]	B	R/W	Decimal value is used in Equation *1*.

Table 29. Register 0xFE03 — NM_DIGFILT_POLE_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:0]	A	R/W	Decimal value is used in Equation *1*.

Table 30. Register 0xFE04 — NM_DIGFILT_HF_GAIN_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:0]	C	R/W	Decimal value is used in Equation *1*.

Table 31. Register 0xFE09 — SS_DIGFILT_LF_GAIN_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:0]	D	R/W	Decimal value is used in Equation *1*.

Table 32.Register 0xFE0A — SS_DIGFILT_ZERO_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:0]	B	R/W	Decimal value is used in Equation 1.

Table 33. Register 0xFE0B — SS_DIGFILT_POLE_GAIN_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:0]	A	R/W	Decimal value is used in Equation *1*.

Table 34. Register 0xFE0C — SS_DIGFILT_HF_GAIN_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:0]	C	R/W	Decimal value is used in Equation *1*.

To avoid output voltage glitches and to provide a seamless transition from one filter to another, the LTP88XX modules support programmable filter transitions. This feature allows a gradual transition from one filter to another. The filter transitions are programmed using Register 0xFE4A[2:0]. When the controller switches filters, the switching action is changed in 32 steps. The step size can be programmed over several cycles ($1t_{SW}$ to $32t_{SW}$) to avoid glitches in the output. The setting or adjusting of these registers is gated by the GO Bit in Register 0xFE00. See the *Go and Auto Go Command* section for more details.

Table 35. Register 0xFE4A — FILTER_TRANSITION

BITS	NAME	R/W	DESCRIPTION
[7:3]	Reserved	N/A	N/A
2	Enable soft transition	R/W	Enables soft transition between filter settings to minimize output transients. All the four parameters of each filter are linearly transitioned to the new value.
[1:0]	Transition speed	R/W	The filter changes in 32 steps, with one step applied at the interval specified by these bits. 00 = 32 × t_{sw} (total transition time = 32 ×32 × t_{sw}) 01 = 8 × t_{sw} (total transition time = 8 × 32 × t_{sw}) 10 = 2 × t_{sw} (total transition time = 2 × 32 × t_{sw}) 11 = 1 × t_{sw} (total transition time = 1 × 32 × t_{sw})

External Frequency Synchronization

A SYNC pin is used for frequency synchronization. The internal digital phase-locked loop (DPLL) determines the master frequency on the SYNC pin (f_{SYNC}) and locks the internal switching frequency to the external frequency. The lock or capture range is ±10% of the pre-programmed switching frequency.

Synchronization is disabled by default. To enable synchronization, set 0xFE55[6] = 0 and then set 0xFE00 = 0b0100000 for the value to take effect. It is recommended to disable this input when not in use. To disable, set 0xFE55[6] = 1 and then set 0xFE00 = 0b0100000 for the value to take effect.

Table 36. Register 0xFE55 — SYNC

BITS	NAME	R/W	DESCRIPTION
7	Reserved	N/A	N/A
6	PLL disable	R/W	0 = enable SYNC function 1 = disable SYNC function
[5:2]	Reserved	N/A	N/A
1	Jitter enable	R/W	1 = enable jitter on clock (to randomize frequency components)
0	5ns resolution enable	R/W	0 = t_{SW} varies in multiples of 10ns (50% point is synchronized with 5ns) 1 = t_{SW} varies in multiples of 5ns

Using the INTERLEAVE command (Register 0x37), a phase shift in steps of 22.5° can be added. Additional functions that are part of the standard PMBus INTERLEAVE command include the group ID number and the respective number in the group, both programmable using Register 0x37.

Table 37. Register 0x37 — INTERLEAVE

BITS	NAME	R/W	DESCRIPTION
[15:12]	Reserved	N/A	N/A
[11:8]	Group ID number	R/W	Group identification number
[7:4]	Number in group	R/W	Number of units in the group
[3:0]	Interleave order	R/W	Interleave order for this unit 0000 = 0 × 22.5° (0 × t_{SW}/16) 0001 = 1 × 22.5° (1 × t_{SW} /16) 0010 = 2 × 22.5° (2 × t_{SW} /16) 0011 = 3 × 22.5° (3 × t_{SW} /16) … 1111 = 15 × 22.5° (15 × t_{SW} /16)

Due to the PWM programming resolution of 5ns for programming the minimum and maximum PWM modulation limits, the switching frequency and the main device clock frequency may not be exact multiples of each other. Although the DPLL can detect f_{SYNC} exactly, due to the quantization of the internal frequency settings, there is a possibility that f_{SYNC} and f_{SW} may not be the same and may differ by a small amount. To prevent the frequency from jumping from one value of f_{SW} to another (which causes the switching period to change) due to the quantization of f_{SW}, f_{SW} is set to the closest quantized value to f_{SYNC}, rounded down. Due to this effect or due to a non-ideality (jitter) of the main device clock, a dither can be added to the clock frequency (using Register 0xFE55[1]) of 5ns or 10ns. Using this dither, f_{SW} is equal to f_{SYNC} on average. For LTP88XX modules, it is recommended that Register 0xFE55[0] = 0, so that half the switching period is an exact multiple of 5ns.

After synchronization, if the main device clock suddenly changes to 0Hz, the LTP88XX modules continue to operate at the last known main device frequency. However, if the device is power cycled through a soft start, the main device frequency is not retained, and the LTP88XX modules default to the internal frequency preset. If the device is off and the main device frequency is already present on the SYNC pin, the switching frequency is set to the main device frequency when the LTP88XX modules turn on. It is recommended that the synchronization function be disabled when not in use because switching noise may be coupled into the SYNC pin. The switching frequency can be read back using the PMBus command READ_FREQUENCY (Register 0x95).

Table 38. Register 0x95 — READ_FREQUENCY

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

PolyPhase Configuration

Refere to the LTP88XX data sheets for hardware configuration details on how to configure a PolyPhase rail with multiple LTP88XX modules.

Firmware Setup

Enable synchronization and command the INTERLEAVE command if needed. See the *External Frequency Synchronization* section for more details. For the LTP88XX modules, the output ripple frequency is two times the primary switching frequency, when commanding phase shift ϕ in Register 0x37, 2ϕ phase shift is applied for the output side. For example, if 180° phase interleaving is desired for two paralleled LTP88XX modules, 4 × 22.5° should be programmed in INTERLEAVE command (0x37[3:0] = 0100) for the second phase.

Current Sharing

The LTP88XX modules support analog current sharing, which can provide excellent current sharing among phases during both steady state and transient conditions. The current sharing accuracy is affected by the values of R_{TOP} and R_{BOT}. Larger R_{TOP} and R_{BOT} values provide stronger current-sharing influence, which means better current sharing accuracy. Besides the current-sharing accuracy, the values of R_{TOP} and R_{BOT} also affect the DC voltage droop and loop stability. Therefore, there will be a tradeoff when selecting the R_{TOP} and R_{BOT} value.

Telemetry and Protection

Input Current

The sensed input current signal is fed into an analog-to-digital converter (ADC), and the READ_IIN (Register 0x89) command reports the average input current. The READ_IIN register is updated every 10.5ms. This reading of the ADC is compared around every 0.7ms to the threshold set using the command IIN_OC_FAULT_LIMIT (Register 0x5B) to make a fault decision. The fault response is set by the IIN_OC_FAULT_ RESPONSE command (Register 0x5C). The IIN_OC_FAULT_RESPONSE command instructs the device on actions to take due to an input overcurrent (OC) fault condition. The device notifies the main device and sets the OTHER bit in the STATUS_BYTE register, the INPUT bit in the STATUS_WORD register, and the IIN_OC_FAULT bit in the STATUS_INPUT register. The debounce time for the IIN_OC fault can be set by 0xFE31[11:8].

Table 39. Register 0x89 — READ_IIN

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 40. Register 0x5B — IIN_OC_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 41. Register 0x5C — IIN_OC_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	Default: 11. The OC response of the LTP88XX modules is set as shut down, disable the output, and respond as programmed by the retry setting (Bits [5:3]).
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

The sensed input current signal is also fed into a comparator for pulse-by-pulse overcurrent protection (OCP). The fast OCP comparator is used to limit the primary current within each switching cycle. The maximum fast OCP comparator latency is 80ns. When the fast OCP comparator is crossed, the PWM outputs are immediately terminated for the remainder of the switching cycle to disable power transfer. The fast OCP comparator provides programmable debounce time using Register 0xFE2C. The IIN_OC_FAST_FAULT_RESPONSE command instructs the device on the actions to take due to an input fast OC fault condition. The device notifies the main device and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the IIN_OC_FAST_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 42. Register 0xFE2C — IIN_OC_FAST_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:2]	Reserved	N/A	N/A
[1:0]	Debounce time	R/W	00 = 0ns 01 = 40ns 10 = 80ns 11 = 120ns

Table 43. Register 0xFE37 — IIN_OC_FAST_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	Default: 11. The OC response of the LTP88XX modules is set as shut down, disable the output, and respond as programmed by the retry setting (Bits [5:3]).
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

Output Current

The Read_IOUT (Register 0x8C) reports the average output current. The reading is updated every 2.6ms. This reading is compared to the threshold set in IOUT_OC_FAULT_LIMIT (Register 0x46), IOUT_OC_WARN_LIMIT (Register 0x4A), and IOUT_UC_FAULT_LIMIT (Register 0x4B) to make a warning or fault decision.

The IOUT_OC_WARN_LIMIT command sets the current (in amperes) measured that causes an OC warning condition. The device notifies the main device and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the IOUT bit in the STATUS_WORD register, and the IOUT_OC_WARNING bit in the STATUS_IOUT register.

The IOUT_OC_FAULT_LIMIT command sets the threshold value (in amperes) measured at the sense pins that cause an OC fault condition. The IOUT_OC_FAULT_RESPONSE command instructs the device on actions to take due to an output OC fault condition. The device notifies the main device and sets the IOUT_OC_FAULT bit in the STATUS_BYTE register, the IOUT bit in the STATUS_WORD register, and the IOUT_OC_FAULT bit in the STATUS_IOUT register. The fault response is programmable in IOUT_OC_FAULT_RESPONSE (Register 0x47). The debounce time for the IOUT_OC fault can be set by 0xFE31[3:0].

The IOUT_UC_FAULT_LIMIT command sets the current (in amperes) measured at the sense/output pin that causes an undercurrent (UC) fault condition. The IOUT_UC_FAULT_RESPONSE command instructs the device on actions to take due to an output UC fault condition. The device notifies the main device and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the IOUT bit in the STATUS_WORD register, and the IOUT_UC_FAULT bit in the STATUS_IOUT register. The debounce time for the IOUT_UC fault can be set by 0xFE31[7:4].

Table 44. Register 0x8C — READ_IOUT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 45. Register 0x46 — IOUT_OC_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 46. Register 0x4A — IOUT_OC_WARN_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 47. Register 0x4B — IOUT_UC_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 48. Register 0x47 — IOUT_OC_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	Default: 11. The OC response of the LTP88XX modules is set as shut down, disable the output, and respond as programmed by the retry setting (Bits [5:3]).
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

Table 49. Register 0x4C — IOUT_UC_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	00 = Do nothing 11 = Shut down, disable the output, and respond as programmed by the retry setting (Bits [5:3])
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E inDebounce *Time and Delay Time Unit*)

The output current signal is also fed into two comparators for fast OCP. One comparator is used to limit the instantaneous secondary current. The IOUT_OC_FAST_FAULT_RESPONSE command instructs the device on the actions to take due to an output fast OC fault condition. The device notifies the main device and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the IOUT_OC_FAST_FAULT bit in STATUS_MFR_SPECIFIC register. The maximum fast OCPcomparator latency is 80ns.

Table 50. Register 0xFE2D — IOUT_OC_FAST_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:2]	Reserved	N/A	N/A
[1:0]	Debounce time	R/W	00 = 0ns 01 = 40ns 10 = 200ns 11 = 400ns

Table 51. Register 0xFE35 — IOUT_OC_FAST_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	Default: 11. The OC response of the LTP88XX modules is set as shut down, disable the output, and respond as programmed by the retry setting (Bits [5:3]).
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E inDebounce *Time and Delay Time Unit*)

The other programmable comparator is used to detect reverse current. The IOUT_UC_FAST fault is set when the reverse comparator is asserted. After it is set, the IOUT_UC_FAST fault is cleared between 328µs and 656µs after the de-assertion of the reverse comparator. The debounce is programmed in Register 0xFE2E[0]. The IOUT_UC_FAST_FAULT_RESPONSE command instructs the device on the actions to take due to an output fast UC fault condition. The device notifies the main device and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the IOUT_UC_FAST_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 52. Register 0xFE2E — IOUT_UC_FAST_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:1]	Reserved	N/A	N/A
0	Debounce time	R/W	The debounce setting is set by Register 0xFE2D [1:0]. For example, if Register 0xFE2D [1:0] = 10, the IOUT_OC_FAST_SETTING is 200ns and the IOUT_UC_FAST_SETTING is 800ns. 00 = 40ns 01 = 200ns 10 = 800ns 11 = 1200ns

Table 53. Register 0xFE36 — IOUT_UC_FAST_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	Default: 11. The OC response of the LTP88XX modules is set as shut down, disable the output, and respond as programmed by the retry setting (Bits [5:3]).
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

Input Voltage

The READ_VIN (Register 0x88) reports the average input voltage. The READ_VIN is updated every 10.5ms. The input voltage is monitored and compared to the threshold to make a fault decision every 328µs.

Fault limits and their responses can be set using PMBus commands such as VIN_UV_FAULT_LIMIT (Register 0x59), VIN_OV_FAULT_LIMIT (Register 0x55), VIN_UV_FAULT_RESPONSE (Register 0x5A), and VIN_OV_FAULT_RESPONSE (Register 0x56). The debounce time for the VIN_OV fault can be set by 0xFE30[7:4]. The debounce time for the VIN_UV fault can be set by 0xFE30[13:11].

The VIN_OV_FAULT_RESPONSE command instructs the device on the actions to take due to an input OV fault condition. The device notifies the main device and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the INPUT bit in the STATUS_WORD register, and the VIN_OV_FAULT bit in the STATUS_INPUT register.

The VIN_UV_FAULT_RESPONSE command instructs the device on the actions to take due to an input UV fault condition. The device notifies the main device and sets the VIN_UV_FAULT bit in the STATUS_BYTE register, the INPUT bit in the STATUS_WORD register, and the VIN_UV_FAULT bit in the STATUS_INPUT register.

Table 54. Register 0x88 — READ_VIN

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 55. Register 0x55 — VIN_OV_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 56. Register 0x56 — VIN_OV_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	00 = Do nothing 01 = Continue operation for the delay time (Bits[2:0]), if the fault persists, retry the number of times specified by Bits[5:3] 10 = Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]) 11 = Disable the output while the fault is present, operation resumes, and the output is enabled when the fault condition no longer exists
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

Table 57. Register 0x59 — VIN_UV_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 58. Register 0x5A — VIN_UV_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	00 = Do nothing 01 = Continue operation for the delay time (Bits[2:0]), if the fault persists, retry the number of times specified by Bits[5:3] 10 = Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]) 11 = Disable the output while the fault is present, operation resumes, and the output is enabled when the fault condition no longer exists
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

Output Voltage

The V_S^+ and V_S^- pins of the LTP88XX modules are used to monitor, control, and protect the power supply output. Typically, the output voltage is divided using a resistive divider. The READ_VOUT (Register 0x8B) command reports the average output voltage; this reading is updated every 10.5ms.

Accurate overvoltage protection (OVP) is provided by the PMBus commands VOUT_OV_FAULT_LIMIT (Register 0x40), VOUT_OV_FAULT_RESPONSE (Register 0x41), and VOUT_OV_WARN_LIMIT (Register 0x42). Similarly, accurate undervoltage protection (UVP) is provided by the PMBus commands VOUT_UV_WARN_LIMIT (Register 0x43), VOUT_UV_FAULT_LIMIT (Register 0x44), and VOUT_UV_ FAULT_RESPONSE (Register 0x45). The debounce time for the VOUT_OV fault can be set by 0xFE30[3:0]. The debounce time for the VOUT_UV fault can be set by 0xFE30[10:8]. The accurate OVP fault decision is made after a sampling interval of 82µs. For OVP, an additional sampling time of up to a maximum of 320µs can be programmed in steps of 82µs using Register 0xFE4D[3:2]. If additional sampling time is enabled, the OV fault condition must be present for the number of additional samples programmed before the VOUT_OV flag is set. For UVP, the output voltage is converted into the PMBus format and compared with the output UV fault limit threshold every 328 µs.

The VOUT_OV_WARN_LIMIT command sets the upper voltage threshold (in volts) measured at the sense/output pin that causes an OV warning condition. The device notifies the main device and sets the NONE_OF_THE_ ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the VOUT_OV_WARNING bit in the STATUS_VOUT register. The VOUT_OV_FAULT_LIMIT command sets the upper voltage threshold (in volts) measured at the sense/output pin that causes an OV fault condition. The VOUT_OV_FAULT_RESPONSE command instructs the device on the actions to take due to an output OV fault. The device notifies the main device and sets the VOUT_OV_FAULT bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the VOUT_OV_FAULT bit in the STATUS_VOUT register.

The VOUT_UV_WARN_LIMIT command sets the lower voltage threshold (in volts) measured at the sense/output pin that causes an UV warning condition. The device notifies the main device and sets the NONE_OF_ THE_ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the VOUT_UV_WARNING bit in the STATUS_VOUT register. The VOUT_UV_FAULT_LIMIT command sets the threshold value (in volts) measured at the sense/output pin that causes an UV fault condition. The VOUT_UV_FAULT_RESPONSE command instructs the device on actions to take due to an output UV fault condition. The device notifies the main device and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the VOUT_UV_FAULT bit in the STATUS_VOUT register. The system does not start monitoring for UVP fault until after the soft-start ramp-up.

Table 59. Register 0x8B — READ_VOUT

BITS	NAME	R/W	DESCRIPTION
[15:0]	Mantissa−Y	R	Unsigned Y-mantissa used in output voltage related commands in a linear data format ($V = Y \times 2^N$). The exponent N is set using VOUT_MODE[4:0].

Table 60. Register 0x42 — VOUT_OV_WARN_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:0]	Mantissa−Y	R/W	Unsigned Y-mantissa used in output voltage related commands in a linear data format ($V = Y \times 2^N$). The exponent N is set using VOUT_MODE[4:0].

Table 61. Register 0x40 — VOUT_OV_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:0]	Mantissa−Y	R/W	Unsigned Y-mantissa used in output voltage related commands in a linear data format ($V = Y \times 2^N$). The exponent N is set using VOUT_MODE[4:0].

Table 62. Register 0x41 — VOUT_OV_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	00 = Do nothing 01 = Continue operation for the delay time (Bits[2:0]), if the fault persists, retry the number of times specified by Bits[5:3] 10 = Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]) 11 = Disable the output while the fault is present, operation resumes, and the output is enabled when the fault condition no longer exists
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

Table 63. Register 0x43 — VOUT_UV_WARN_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:0]	Mantissa−Y	R/W	Unsigned Y-mantissa used in output voltage related commands in a linear data format ($V = Y \times 2^N$). The exponent N is set using VOUT_MODE[4:0].

Table 64. Register 0x44 — VOUT_UV_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:0]	Mantissa−Y	R/W	Unsigned Y-mantissa used in output voltage related commands in a linear data format ($V = Y \times 2^N$). The exponent N is set using VOUT_MODE[4:0].

Table 65. Register 0x45 — VOUT_UV_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	00 = Do nothing 01 = Continue operation for the delay time (Bits[2:0]), if the fault persists, retry the number of times specified by Bits[5:3] 10 = Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]) 11 = Disable the output while the fault is present, operation resumes, and the output is enabled when the fault condition no longer exists
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

The local output voltage is also sensed for fast protection, where a comparator compares the fractional output voltage by means of resistive dividers to the voltage set by a DAC. The fast OVP threshold is programmable using Register 0xFE2F[7:2]. A debounce time, ranging from 40ns to 10µs, can be added using Register 0xFE2F[1:0] before the fault response is taken. The fault response is set using the manufacturer-specific command VOUT_OV_FAST_FAULT_RESPONSE (Register 0xFE34). The device notifies the main device and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the VOUT_OV_FAST_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 66. Register 0xFE2F — VOUT_OV_FAST_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:2]	Threshold	R/W	64 steps: Threshold = 0.8 + (Register 0xFE2F[7:2]) × 0.8/63
[1:0]	Debounce	R/W	00 = 40ns 01 = 2µs + 1µs 10 = 5µs + 1µs 11 = 10µs + 1µs

Table 67. Register 0xFE34 — VOUT_OV_FAST_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	00 = Do nothing 01 = Continue operation for the delay time (Bits[2:0]), if the fault persists, retry the number of times specified by Bits[5:3] 10 = Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]) 11 = Disable the output while the fault is present, operation resumes, and the output is enabled when the fault condition no longer exists
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

Temperature

The temperature can be read in READ_TEMPERATURE_2 (Register 0x8E). The reading is updated every 130ms. Overtemperature protection (OTP) can be set using OT_FAULT_LIMIT (Register 0x4F), OT_FAULT_RESPONSE (Register 0x50), and OT_WARN_LIMIT (Register 0x51).

The OT_WARN_LIMIT command sets the threshold value (in °C) for an overtemperature (OT) warning condition. The device notifies the main device and sets the TEMPERATURE bit in the STATUS_BYTE register and the OT_WARNING bit in the STATUS_TEMPERATURE register.

The OT_FAULT_LIMIT command sets the threshold value (in °C) that causes an overtemperature (OT) fault condition. The OT_FAULT_RESPONSE command instructs the device on actions to take due to an OT fault condition. The device notifies the main device and sets the TEMPERATURE bit in the STATUS_BYTE register and the OT_FAULT bit in the STATUS_TEMPERATURE register.

The hysteresis for OTP is the difference between the OT_FAULT_LIMIT and OT_WARN_ LIMIT values. For example, if OT_FAULT_LIMIT is set to disable all PWM outputs at 125°C and OT_WARN_LIMIT is set to 115°C, the LTP88XX modules stop switching at 125°C and begins switching again only when the temperature falls below 115°C.

Table 68. Register 0x8E — READ_TEMPERATURE_2

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 69. Register 0x51 — OT_WARN_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 70. Register 0x4F — OT_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 71. Register 0x50 — OT_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	00 = Do nothing 01 = Continue operation for the delay time (Bits[2:0]), if the fault persists, retry the number of times specified by Bits[5:3] 10 = Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]) 11 = Disable the output while the fault is present, operation resumes, and the output is enabled when the fault condition no longer exists
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

Maximum On and Off Time

The TON_MAX_FAULT_LIMIT (Register 0x62) command specifies the maximum on-time (in ms) before the output voltage must exceed the VOUT_UV_FAULT_LIMIT (Register 0x44). If the VOUT_UV_FAULT_LIMIT is set to 0, the TON_MAX value is ignored. The TON_MAX_FAULT_RESPONSE command instructs the device on the actions to take due to a TON_MAX fault condition. The device notifies the main device and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the TON_MAX_FAULT bit in the STATUS_VOUT register.

Table 72. Register 0x62 — TON_MAX_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two-complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 73. Register 0x63 — TON_MAX_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	00 = Do nothing 01 = Continue operation for the delay time (Bits[2:0]), if the fault persists, retry the number of times specified by Bits[5:3] 10 = Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]) 11 = Disable the output while the fault is present, operation resumes, and the output is enabled when the fault condition no longer exists
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

The TOFF_MAX_WARN_LIMIT command sets the upper time threshold (in ms) that causes a TOFF_MAX warning condition, that is, the time it takes to power down the output voltage from V_{OUT} to 12.5% of V_{OUT}. The device notifies the main device and sets the NONE_OF_THE_ ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the TOFF_MAX_WARNING bit in the STATUS_VOUT register.

Table 74. Register 0x66 —TOFF_MAX_WARN_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Output Power

The multiplication of output voltage and output current ADCs averaged every 2.6ms is compared with the POUT_OP_FAULT_LIMIT to set the flag. The READ_POUT command returns the output power (W) in a linear data format ($X = Y \times 2^N$).

The POUT_OP_FAULT_RESPONSE command instructs the device on the actions to take due to an output overpower (OP) fault condition. The device notifies the main device and sets the IOUT_OC_FAULT bit in the STATUS_BYTE register, the IOUT/POUT bit in the STATUS_WORD register, and the POUT_OP_FAULT bit in the STATUS_IOUT register.

Table 75. Register 0x96 — READ_POUT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 76. Register 0x68 — POUT_OP_FAULT_LIMIT

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 77. Register 0x69 — POUT_OP_FAULT_RESPONSE

BITS	NAME	R/W	DESCRIPTION
[7:6]	Response	R/W	00 = Do nothing 01 = Continue operation for the delay time (Bits[2:0]), if the fault persists, retry the number of times specified by Bits[5:3] 10 = Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]) 11 = Disable the output while the fault is present, operation resumes, and the output is enabled when the fault condition no longer exists
[5:3]	Number of retries	R/W	000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E in *Debounce Time and Delay Time Unit*)

Debounce Time and Delay Time Unit

Table 78. Register 0xFE30 — DEBOUNCE_SETTING_1

BITS	NAME	R/W	DESCRIPTION
[15:14]	Reserved	N/A	N/A
[13:11]	VIN_UV_DEB	R/W	000 = 0 001 = 1ms + 10µs 010 = 2.5ms + 10µs 011 = 5ms + 10µs 100 = 10ms + 10µs 101 = 50ms + 10µs 110 = 100ms + 10µs 111 = 250ms + 10µs
[10:8]	VOUT_UV_DEB	R/W	000 = 0 001 = 1ms + 10µs 010 = 2.5ms + 10µs 011 = 5ms + 10µs 100 = 10ms + 10µs 101 = 50ms + 10µs 110 = 100ms + 10µs 111 = 250ms + 10µs
[7:4]	VIN_OV_DEB	R/W	0000 = 0 0001 = 100µs + 1µs 0010 = 250µs + 1µs 0011 = 500µs + 1µs 0100 = 750µs + 10µs 0101 = 1ms + 10µs 0110 = 2.5ms + 10µs 0111 = 5ms + 10µs 1000 = 7.5ms + 100µs 1001 = 10ms + 100µs 1010 = 25ms + 100µs 1011 = 50ms + 100µs 1100 = 75ms + 1ms 1101 = 100ms + 1ms 1110 = 250ms + 1ms 1111 = 500ms + 1ms
[3:0]	VOUT_OV_DEB	R/W	0000 = 0 0001 = 100µs + 1µs 0010 = 250µs + 1µs 0011 = 500µs + 1µs 0100 = 750µs + 10µs 0101 = 1ms + 10µs 0110 = 2.5ms + 10µs 0111 = 5ms + 10µs 1000 = 7.5ms + 100µs 1001 = 10ms + 100µs

BITS	NAME	R/W	DESCRIPTION
			1010 = 25ms + 100µs 1011 = 50ms + 100µs 1100 = 75ms + 1ms 1101 = 100ms + 1ms 1110 = 250ms + 1ms 1111 = 500ms + 1ms

Table 79. Register 0xFE31 — DEBOUNCE_SETTING_2

BITS	NAME	R/W	DESCRIPTION
[15:12]	Reserved	N/A	N/A
[11:8]	IIN_OC_DEB	R/W	0000 = 0 0001 = 1ms + 10µs 0010 = 2.5ms + 10µs 0011 = 5ms + 10µs 0100 = 7.5ms + 100µs 0101 = 10ms + 100µs 0110 = 25ms + 100µs 0111 = 50ms + 100µs 1000 = 75ms + 1ms 1001 = 100ms + 1ms 1010 = 250ms + 1ms 1011 = 500ms + 1ms 1100 = 750ms + 10ms 1101 = 1sec + 10ms 1110 = 2.5sec + 10ms 1111 = 5sec + 10ms
[7:4]	IOUT_UC_DEB	R/W	0000 = 0 0001 = 1ms + 10µs 0010 = 2.5ms + 10µs 0011 = 5ms + 10µs 0100 = 7.5ms + 100µs 0101 = 10ms + 100µs 0110 = 25ms + 100µs 0111 = 50ms + 100µs 1000 = 75ms + 1ms 1001 = 100ms + 1ms 1010 = 250ms + 1ms 1011 = 500ms + 1ms 1100 = 750ms + 10ms 1101 = 1sec + 10ms 1110 = 2.5sec + 10ms 1111 = 5sec + 10ms
[3:0]	IOUT_OC_DEB	R/W	0000 = 0 0001 = 1ms + 10µs 0010 = 2.5ms + 10µs

BITS	NAME	R/W	DESCRIPTION
			0011 = 5ms + 10µs 0100 = 7.5ms + 100µs 0101 = 10ms + 100µs 0110 = 25ms + 100µs 0111 = 50ms + 100µs 1000 = 75ms + 1ms 1001 = 100ms + 1ms 1010 = 250ms + 1ms 1011 = 500ms + 1ms 1100 = 750ms + 10ms 1101 = 1sec + 10ms 1110 = 2.5sec + 10ms 1111 = 5sec + 10ms

Table 80. Register 0xFE32 — DEBOUNCE_SETTING_3

BITS	NAME	R/W	DESCRIPTION
[15:12]	Reserved	N/A	N/A
[11:8]	POUT_OP_DEB	R/W	0000 = 0 0001 = 100µs + 1µs 0010 = 250µs + 1µs 0011 = 500µs + 1µs 0100 = 750µs + 10µs 0101 = 1ms + 10µs 0110 = 2.5ms + 10µs 0111 = 5ms + 10µs 1000 = 7.5ms + 100µs 1001 = 10ms + 100µs 1010 = 25ms + 100µs 1011 = 50ms + 100µs 1100 = 75ms + 1ms 1101 = 100ms + 1ms 1110 = 250ms + 1ms 1111 = 500ms + 1ms
[7:4]	TON_MAX_DEB	R/W	0000 = 0 0001 = 100µs + 1µs 0010 = 250µs + 1µs 0011 = 500µs + 1µs 0100 = 750µs + 10µs 0101 = 1ms + 10µs 0110 = 2.5ms + 10µs 0111 = 5ms + 10µs 1000 = 7.5ms + 100µs 1001 = 10ms + 100µs 1010 = 25ms + 100µs 1011 = 50ms + 100µs

BITS	NAME	R/W	DESCRIPTION
			1100 = 75ms + 1ms 1101 = 100ms + 1ms 1110 = 250ms + 1ms 1111 = 500ms + 1ms
[3:0]	OT_DEB	R/W	0000 = 0 0001 = 1ms + 10µs 0010 = 2.5ms + 10µs 0011 = 5ms + 10µs 0100 = 7.5ms + 100µs 0101 = 10ms + 100µs 0110 = 25ms + 100µs 0111 = 50ms + 100µs 1000 = 75ms + 1ms 1001 = 100ms + 1ms 1010 = 250ms + 1ms 1011 = 500ms + 1ms 1100 = 750ms + 10ms 1101 = 1sec + 10ms 1110 = 2.5sec + 10ms 1111 = 5sec + 10ms

Table 81. Register 0xFE3E — DELAY_TIME_UNIT

BITS	NAME	R/W	DESCRIPTION
7	Current fault delay time unit	R/W	0 = ms 1 = µs
[6:4]	Current fault delay time multiplier	R/W	000 = 1 001 = 4 010 = 16 011 = 64 100 = 128 101 = 256 110 = 512 111 = 1024
3	Voltage/other fault delay time unit	R/W	0 = ms 1 = µs
[2:0]	Voltage/other fault delay time multiplier	R/W	000 = 1 001 = 4 010 = 16 011 = 64 100 = 128 101 = 256 110 = 512 111 = 1024

3V3 OVLO

The LTP88XX modules have built-in overvoltage protection (OVP) on its internal controller 3V3 supply rail. When the 3V3 voltage rises above the overvoltage lockout (OVLO) threshold, the response can be programmed using Register 0xFE4D. The 3V3 OV is ignored when the device is downloading information from the EEPROM, even if the OV occurs during the initial power-up or due to the setting of Register 0xFE4D[6]. The 3V3 OV is recognized as a fault only after the EEPROM download completes. The internal controller has a 4ms idle time after an EEPROM download. If the 3V3 OV occurs during the ramp-up of 3V3 and the EEPROM download has not been initiated, the device responds according to the default setting of Bit 7 in Register 0xFE4D, which is to ignore V_{DD} OV.

Table 82. Register 0xFE4D — OVP_FAULT_CONFIG

BITS	NAME	R/W	DESCRIPTION
7	V_{DD}/V_{CORE} OV fault ignore	R/W	0 = V_{DD} OV and V_{CORE} OV flags are not ignored 1 = V_{DD} OV and V_{CORE} OV flags are ignored
6	V_{DD}/V_{CORE} OV restart	R/W	0 = Do not download EEPROM again following a fault shutdown 1 = Download EEPROM following a fault shutdown
5	V_{DD}/V_{CORE} OV debounce	R/W	0 = 2µs + 1µs debounce 1 = 500µs + 10µs debounce
4	V_{DD} UV debounce	R/W	0 = No debounce 1 = 120ns debounce
[3:2]	VOUT_OV sampling	R/W	00 = One sample sets the VOUT_OV flag (80µs sampling period) 01 = Two consecutive samples that read a value greater than the one set in VOUT_OV_FAULT_LIMIT set the VOUT_OV flag (160µs sampling period) 10 = Three consecutive samples that read a value greater than the one set in VOUT_OV_FAULT_LIMIT set the VOUT_OV flag (240µs sampling period) 11 = Four consecutive samples that read a value greater than the one set in VOUT_OV_FAULT_LIMIT set the VOUT_OV flag (320µs sampling period)
[1:0]	Reserved	N/A	N/A

Duty Cycle

The READ_DUTY_CYCLE command returns the duty cycle (%) in a linear data format ($X = Y \times 2^N$).

Table 83. Register 0x94 — READ_DUTY_CYCLE

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Flags, Faults, and Status

Flags, Faults, and Watchdog Timer

When a potentially abnormal condition occurs in the power supply that is regulated by the LTP88XX modules, a flag is asserted, and the system waits for a programmed debounce time. If the flag is continuously asserted until the end of the debounce time, it is latched as a fault. The fault is then processed according to the programmed fault response setting and cleared only when the flag condition is removed. The debounce circuitry resets when the flag condition is removed; until then, the fault remains set. The CLEAR_FAULTS command (Register 0x03) clears the latched fault registers and resets all flags. Register 0xFE8C to Register 0xFE93 have the same flags as the PMBus STATUS_x commands (Register 0x7A to Register 0x80).

Table 84. Register 0x03 — CLEAR_FAULTS

BITS	NAME	TYPE	DESCRIPTION
N/A	Exponent−N	Send	Clears all bits in the PMBus status registers (Register 0x78 to Register 0x7E) simultaneously

Table 85. Register 0xFE8C — FAULT_VOUT

BITS	NAME	R/W	DESCRIPTION
[7:0]	FAULT_VOUT	R	Unlatched fault conditions after debounce (see STATUS_VOUT for latched version in *Table 98*)

Table 86. Register 0xFE8D — FAULT_IOUT

BITS	NAME	R/W	DESCRIPTION
[7:0]	FAULT_IOUT	R	Unlatched fault conditions after debounce (see STATUS_IOUT for latched version in *Table 99*)

Table 87. Register 0xFE8E — FAULT_INPUT

BITS	NAME	R/W	DESCRIPTION
[7:0]	FAULT_INPUT	R	Unlatched fault conditions after debounce (see STATUS_INPUT for latched version in *Table 100*)

Table 88. Register 0xFE8F — FAULT_TEMPERATURE

BITS	NAME	R/W	DESCRIPTION
[7:0]	FAULT_TEMPERATURE	R	Unlatched fault conditions after debounce (see STATUS_TEMPERATURE for latched version in *Table 101*)

Table 89. Register 0xFE90 — FAULT_CML

BITS	NAME	R/W	DESCRIPTION
[7:0]	FAULT_CML	R	Unlatched fault conditions after debounce (see STATUS_CML for latched version in *Table 102*)

Table 90. Register 0xFE91 — FAULT_OTHER

BITS	NAME	R/W	DESCRIPTION
[7:0]	FAULT_OTHER	R	Unlatched fault conditions after debounce (see STATUS_OTHER for latched version in *Table 97*)

Table 91. Register 0xFE92 — FAULT_MFR_SPECIFIC

BITS	NAME	R/W	DESCRIPTION
[7:0]	FAULT_MFR_SPECIFIC	R	Unlatched fault conditions after debounce (see STATUS_MFR_SPECIFIC for latched version in *Table 103*)

Table 92. Register 0xFE93 — FAULT_UNKNOWN

BITS	NAME	R/W	DESCRIPTION
[7:0]	FAULT_UNKNOWN	R	Unlatched fault conditions after debounce (see STATUS_UNKNOWN for latched version in *Table 104*)

The first-fault ID (FFID) information is used to capture the first fault that caused the system to shut down. Register 0xFE95 contains the ID of the first fault that caused the system to shut down. Faults captured in the FFID register have configured actions of shutdown immediate, shutdown with retries, and disabling PWM outputs with watchdog timeout. The contents of Register 0xFE95 cannot be overwritten unless the information is first cleared. The FFID can be cleared by the CLEAR_FAULTS command (Register 0x03), by a power cycle of the device, or by a power sense on (PSON) signal using Register 0x01, Register 0x02, or both. If the black box feature is enabled, the FFID can also be cleared when the information is saved into the black box.

Table 93. Register 0xFE95 – FIRST_FAULT_ID

BITS	NAME	R/W	DESCRIPTION
[7:0]	First-fault ID (in hex)	R	0x00 = no fault 0x01 = VOUT_OV 0x02 = VOUT_OV_FAST 0x03 = VOUT_UV 0x04 Not supported 0x05 = VIN_OV 0x06 = VIN_UV 0x07 = OT 0x08 = TON_MAX 0x09 = POUT_OP 0x0A = Not supported 0x0B = Not supported 0x0C = Not supported 0x0D = Not supported 0x0E = IOUT_OC 0x0F = IOUT_OC_FAST 0x10 = IOUT_UC 0x11 = IOUT_UC_FAST 0x12 = IIN_OC 0x13 = IIN_OC_FAST 0x14 = Not supported

When the voltage fault response is set to disable the outputs and wait for the faults to clear, the LTP88XX modules disable the PWM outputs but do not immediately shut down and restart through a soft-start cycle. The LTP88XX modules keep the PWM outputs disabled until the fault is cleared, after which the PWM outputs are reenabled. If the fault is not cleared, the system can potentially remain in a dormant condition for an infinitely long time. To prevent this condition, a watchdog timer can be set to time out the fault condition. The WDT_SETTING command (Register 0xFE3F) is used to set a timeout of 0sec, 1sec, 5sec, or 10sec, after which the system shuts down, captures the FFID, and requires a power-up (CTRL pin or OPERATION command) to restart.

Table 94. Register 0xFE3F — WDT_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:2]	Reserved	N/A	N/A
[1:0]	Watchdog timeout	R/W	00 = disable 01 = 1sec 10 = 5sec 11 = 10sec

STATUS_x and SMBALERT_MASK

The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SMBALERT signal. The bits in the mask byte align with the bits in the corresponding status register. Refer to the *PMBus Power System Management Protocol Specification, Revision 1.2, dated September 6, 2010*, for the command format.

For example, to block (masking) an OT warning condition while unmasking the OT fault condition from asserting SMBALERT of a device with address 0x41, the command line should be: 0x41, WW, 0x1B, 0x407D.

Where 0x1B is the command code for SMBALERT_MASK, 0x40 (01000000b) is the mask byte, 0x7D is command code for STATUS_TEMPERATURE.

Table 95. Register 0x1B — SMBALERT_MASK

BITS	NAME	R/W	DESCRIPTION
[15:8]	Mask byte	W	Update mask register with this value
[7:0]	STATUS_x command code	W	Command code of the STATUS_x mask register to update

Table 96. Register 0x78 — STATUS_BYTE

BITS	NAME	R/W	DESCRIPTION
7	BUSY	R/W	This bit is asserted if the device is busy and unable to respond.
6	POWER_OFF	R	This bit is asserted if the unit is not providing power to the output.
5	VOUT_OV_FAULT	R	An output OV fault has occurred.
4	IOUT_OC_FAULT	R	An output OC fault has occurred
3	VIN_UV_FAULT	R	An input UV fault has occurred.
2	TEMPERATURE	R	A temperature fault or warning has occurred.
1	CML	R	A communications, memory, or logic fault has occurred.
0	NONE_OF_THE_ABOVE	R	A fault or warning not listed in Bits[7:1] has occurred.

Table 97. Register 0x79 — STATUS_WORD

BITS	NAME	R/W	DESCRIPTION
15	VOUT	R	Output voltage fault or warning, a bit in STATUS_VOUT is set
14	IOUT/POUT	R	Output current or output power fault or warning, a bit in STATUS_IOUT is set
13	INPUT	R	Input voltage, input current, or input power fault or warning, a bit in STATUS_INPUT is set
12	MFR	R	Manufacturer-specific fault or warning
11	$\overline{\text{POWER\_GOOD}}$	R	$\overline{\text{POWER\_GOOD}}$ is a negation of POWER_GOOD, which means that the output power is not good, this bit is set when the sensed VOUT is less than the limit programmed in the POWER_GOOD_OFF command
10	FANS	R	Not supported
9	OTHER	R	A bit in STATUS_OTHER is set
8	UNKNOWN	R	A fault or warning not listed in STATUS_WORD[15:1]
7	BUSY	R/W	This bit is asserted if the device is busy and unable to respond
6	POWER_OFF	R	This bit is asserted if the unit is not providing power to the output
5	VOUT_OV_FAULT	R	An output OV fault has occurred
4	IOUT_OC_FAULT	R	An output OC fault has occurred
3	VIN_UV_FAULT	R	An input UV fault has occurred
2	TEMPERATURE	R	A temperature fault or warning has occurred
1	CML	R	A communications, memory, or logic fault has occurred
0	NONE_OF_THE_ABOVE	R	A fault or warning not listed in Bits[7:1] has occurred

Table 98. Register 0x7A — STATUS_VOUT

BITS	NAME	R/W	DESCRIPTION
7	VOUT_OV_FAULT	R/W	An output OV fault has occurred.
6	VOUT_OV_WARN	R/W	An output OV warning has occurred.
5	VOUT_UV_WARN	R/W	An output UV warning has occurred.
4	VOUT_UV_FAULT	R/W	An output UV fault has occurred.
3	VOUT_MAX_WARN	R/W	An attempt was made to set the output voltage to a value greater than the VOUT_MAX command.
2	TON_MAX_FAULT	R/W	The device took too long to power up without reaching the VOUT_UV fault limit.
1	TOFF_MAX_WARN	R/W	The device took too long to power down to 12.5% of its output voltage.
0	Reserved	N/A	N/A

Table 99. Register 0x7B — STATUS_IOUT

BITS	NAME	R/W	DESCRIPTION
7	IOUT_OC_FAULT	R/W	This bit is asserted if the device is busy and unable to respond.
6	Reserved	N/A	N/A
5	IOUT_OC_WARN	R/W	An output OC warning has occurred.
4	IOUT_UC_FAULT	R/W	An output UC fault has occurred.
3	Reserved	N/A	N/A
2	Reserved	N/A	N/A
1	POUT_OP_FAULT	R/W	An output OP fault has occurred.
0	Reserved	N/A	N/A

Table 100. Register 0x7C — STATUS_INPUT

BITS	NAME	R/W	DESCRIPTION
7	VIN_OV_FAULT	R/W	This bit is asserted if the device is busy and unable to respond.
6	Reserved	N/A	N/A
5	Reserved	N/A	N/A
4	VIN_UV_FAULT	R/W	An input UV fault has occurred.
3	VIN_LOW	R/W	The device is off due to insufficient input voltage; that is, the input voltage is below the turn-off threshold.
2	IIN_OC_FAULT	R/W	An input OC fault has occurred.
1	Reserved	N/A	N/A
0	Reserved	N/A	N/A

Table 101. Register 0x7D — STATUS_TEMPERATURE

BITS	NAME	R/W	DESCRIPTION
7	OT_FAULT	R/W	An OT fault has occurred.
6	OT_WARN	R/W	An OT warning has occurred.
[5:0]	N/A	N/A	N/A

Table 102. Register 0x7E — STATUS_CML

BITS	NAME	R/W	DESCRIPTION
7	CMD_ERR	R/W	Invalid or unsupported command received.
6	DATA_ERR	R/W	Invalid or unsupported data received.
5	PEC_ERR	R/W	Packet error check failed.
4	CRC_ERR	R/W	Memory fault detected (for example, a CRC error).
3	Reserved	N/A	N/A
2	Reserved	N/A	N/A
1	COMM_ERR	R/W	Other communication fault not specified by Bits[7:2].
0	MEM_ERR	R/W	Other memory or logic fault not specified by Bits[7:2]. This bit is set if the black box record number has been reached.

Table 103. Register 0x80 — STATUS_MFR_SPECIFIC

BITS	NAME	R/W	DESCRIPTION
[7:4]	Reserved	N/A	N/A
3	IIN_OC_FAST_FAULT	R/W	Fast input OC fault received.
2	IOUT_UC_FAST_FAULT	R/W	Fast output reverse current fault received.
1	IOUT_OC_FAST_FAULT	R/W	Fast output OC fault received.
0	VOUT_OV_FAST_FAULT	R/W	Fast output OV fault received.

Table 104. Register 0xFE94 — STATUS_UNKNOWN

BITS	NAME	R/W	DESCRIPTION
15	EEPROM unlocked	R/W	The EEPROM is unlocked.
14	Reserved	N/A	N/A
13	Soft start filter	R/W	The soft start filter is in use.
12	Soft start ramp or soft stop ramp	R/W	The reference is being ramped up (soft start) or ramped down (soft stop).
[11:8]	Reserved	N/A	N/A
7	PGOOD2 fault	R/W	PGOOD2 fault. At least one of the flags listed in Register 0xFE45 has been set.
6	PGOOD1 fault	R/W	PGOOD1 fault. At least one of the flags listed in Register 0xFE44 has been set.
5	Sync unlock	R/W	Sync mode is enabled, but unit not locked to sync input frequency.
4	SR off	R/W	Synchronous rectifiers are disabled.
3	Address warning	R/W	I2C/PMBus address warning. The ADD resistor value out-of-range.
2	VCORE OV	R/W	2.5V VCORE is above limit. The action is set to immediate shutdown.
1	VDD OV	R/W	VDD is above limit. The I2C interface stays functional, but a unit power-off/power-on sequence is required to restart the power supply. The response to a VDD OV is programmable in Register 0xFE4D[6].
0	VDD UV	R/W	VDD is below limit. The response to a VDD UV immediate shutdown.

PGOOD and POWER_GOOD

Various flags can be programmed into PGOOD1 and PGOOD2 using Register 0xFE44 and Register 0xFE45. A delay (debounce) can be added to the PGOODx signals using Register 0xFE43. The same debounce applies to the PGOOD1_FAULT and PGOOD2_FAULT flags set in Register 0xFE93[6] (FAULT_UNKNOWN[6]) and Register 0xFE93[7] (FAULT_ UNKNOWN[7]) (where 0 means no fault).

Table 105. Register 0xFE43 — PGOOD_FAULT_DEB

BITS	NAME	R/W	DESCRIPTION
[7:6]	PGOOD2_OFF_DEB	R/W	00 = 0ms 01 = 150ms + 10ms 10 = 350ms + 10ms 11 = 550ms + 10ms
[5:4]	PGOOD2_ON_DEB	R/W	00 = 0ms 01 = 150ms + 10ms 10 = 350ms + 10ms 11 = 550ms + 10ms
[3:2]	PGOOD1_OFF_DEB	R/W	00 = 0ms 01 = 150ms + 10ms 10 = 350ms + 10ms 11 = 550ms + 10ms
[1:0]	PGOOD1_ON_DEB	R/W	00 = 0ms 01 = 150ms + 10ms 10 = 350ms + 10ms 11 = 550ms + 10ms

Table 106. Register 0xFE44 — PGOOD1_FAULT_SELECT

BITS	NAME	R/W	DESCRIPTION
15	TON_MAX_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
14	IOUT_UC_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
13	POUT_OP_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
12	IIN_OC_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
11	VIN_OV_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
10	VOUT_UV_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
9	VOUT_OV_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
8	IOUT_OC_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
7	VIN_UV_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
6	IIN_OC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
5	IOUT_OC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
4	VOUT_OV_FAST	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
3	SOFT_START_RAMP	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
2	OT_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
1	SR_OFF	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
0	OFF	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)

Table 107. Register 0xFE45 — PGOOD2_FAULT_SELECT

BITS	NAME	R/W	DESCRIPTION
15	VOUT (STATUS_WORD [15])	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
14	IOUT/POUT (STATUS_WORD [14])	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
13	INPUT (STATUS_WORD [13])	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
12	TEMPERATURE (STATUS_WORD [2])	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
11	Reserved	N/A	N/A
10	Reserved	N/A	N/A
9	TOFF_MAX_WARN	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
8	IOUT_UC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
7	Reserved	N/A	N/A
6	IIN_OC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
5	IOUT_OC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
4	VOUT_OV_FAST	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
3	SOFT_START_RAMP	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
2	SYNC_UNLOCK	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
1	Maximum black box record reached	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
0	Soft start filter	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)

The POWER_GOOD_ON register (Register 0x5E) sets the voltage that the output voltage must exceed before $\overline{\text{POWER\_GOOD}}$ can be set. Similarly, the output voltage must fall below the POWER_GOOD_OFF threshold (set in Register 0x5F) for $\overline{\text{POWER\_GOOD}}$ to be reset.

The PMBus signal $\overline{\text{POWER\_GOOD}}$ is accessible through STATUS_WORD (Register 0x79[11]). $\overline{\text{POWER\_GOOD}}$ is asserted (0 means power is good) only if all the following conditions are met.

- VOUT has exceeded POWER_GOOD_ON
- VOUT has not fallen below POWER_GOOD_OFF
- PGOOD1_FAULT is not set
- PGOOD2_FAULT is not set

The undervoltage protection (UVP) is not associated with this flag; however, the PGOOD1_ FAULT and PGOOD2_FAULT flags can be programmed to select UVP (VOUT_UV_FAULT). There is no debounce for $\overline{\text{POWER\_GOOD}}$.

Table 108. Register 0x5E — POWER_GOOD_ON

BITS	NAME	R/W	DESCRIPTION
[15:0]	Mantissa−Y	R/W	Unsigned Y-mantissa used in output voltage related commands in a linear data format ($V = Y \times 2^N$)

Table 109. Register 0x5F — POWER_GOOD_OFF

BITS	NAME	R/W	DESCRIPTION
[15:0]	Mantissa−Y	R/W	Unsigned Y-mantissa used in output voltage related commands in a linear data format ($V = Y \times 2^N$)

Output Current Readout Calibration

The IOUT reading is trimmable by the user. The IOUT_CAL_GAIN command sets the ratio of the voltage at the current sense pins to the sensed current (in mΩ). The IOUT_CAL_OFFSET command is used to null any offsets in the output current sensing circuit (in amperes).

Table 110. Register 0x38 — IOUT_CAL_GAIN

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Table 111. Register 0x39 — IOUT_CAL_OFFSET

BITS	NAME	R/W	DESCRIPTION
[15:11]	Exponent−N	R/W	Two's complement N-exponent used in a linear data format ($X = Y \times 2^N$)
[10:0]	Mantissa−Y	R/W	Two's complement Y-mantissa used in a linear data format ($X = Y \times 2^N$)

Other Commands

The WRITE_PROTECT command is used to protect the PMBus device from accidental writes. Reads to the device are allowed regardless of the setting of this command.

Table 112. Register 0x10 — WRITE_PROTECT

BITS	NAME	R/W	DESCRIPTION
7	WRITE_PROTECT 1	R/W	Setting this bit disables writes to all commands except WRITE_PROTECT
6	WRITE_PROTECT 2	R/W	Setting this bit disables writes to all commands except WRITE_PROTECT, OPERATION, and PAGE
5	WRITE_PROTECT 3	R/W	Setting this bit disables writes to all commands except WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND
[4:0]	Reserved	N/A	N/A

Table 113. Register 0x15 — STORE_ USER_ALL

BITS	NAME	TYPE	DESCRIPTION
N/A	STORE_DEFAULT_ALL	Send	This command copies the entire contents of operating memory into the EEPROM (Page 1 of the main block) as the user settings.

Table 114. Register 0x16 — RESTORE_ USER_ALL

BITS	NAME	TYPE	DESCRIPTION
N/A	RESTORE_USER_ALL	Send	This command downloads the stored user settings from EEPROM into operating memory.

Table 115. Register 0x9A — MFR_MODEL

BITS	NAME	R/W	DESCRIPTION
[7:0]	Model	Block read	Return the manufacturer's model number

Table 116. Register 0xFE48 — BLACKBOX_SETTING

BITS	NAME	R/W	DESCRIPTION
[7:3]	Reserved	N/A	N/A
2	Maximum record number	R/W	Sets the maximum record number at which the black box recording feature is disabled 0 = 150,000. Recommended when operating at <85°C 1 = 16,000. Recommended when operating at 125°C
[1:0]	Recording options	R/W	00 = No recording 01 = Record only telemetry just before the final shutdown 10 = Record telemetry of final shutdown and all retry attempts 11 = Record telemetry of final shutdown, all retry attempts, and normal unit-off per the CTRL pin and the OPERATION command

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/26	Initial release	—