PURPOSE OF THIS MANUAL

This document details the features and functions of the ADIN1140 transceiver and should be used in conjunction with the ADIN1140 datasheet.

WHAT'S NEW IN THIS REFERENCE

This revision (0) is the first version of the document.

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Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

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REVISION HISTORY

5/2026—Revision 0: Initial Version

PRODUCT OVERVIEW

The ADIN1140 is a low power, high performance, single port 10BASE-T1S MAC-PHY designed for multidrop Ethernet connectivity applications. The PHY complies with the IEEE 802.3™-2022 Ethernet standard for 10Mbps single-pair Ethernet. For point-to-point (half-duplex) configurations, the standard specifies up to 15m, but the ADIN1140 has been tested up to 200m under typical conditions using 18AWG solid copper twisted pair cable. For multidrop configurations, the standard allows up to at least eight nodes over 25m, while the ADIN1140 has been validated in setups with more than 40 nodes under typical lab conditions without noise injection.

ADDITIONAL RESOURCES

The following additional documents from Analog Devices are useful for understanding and using the transceiver:

- Product specific data sheet.
- Software documentation.

The following additional documents from other sources are also useful for understanding and using the transceiver:

- *IEEE Standard 802.3-2022 for Ethernet*.
- *OPEN Alliance 10BASET1x MAC-PHY Serial Interface V1.1*.
- *IEEE 802.1AS-2020 - Timing and Synchronization for Time-Sensitive Applications*.
- *OPEN Alliance TC10/TC14 10BASE-T1S Sleep/Wake-up version 1.0*.
- *OPEN Alliance TC10/TC14 10BASE-T1S Topology Discovery Specification version 1.0*.
- *10BASE-T1S System Implementation Specification, OPEN Alliance, 15 February 2023*.
- *OPEN Alliance TC14, Advanced Diagnostic Features for 10BASE-T1S PHYs, Version 1.1*.
- *OPEN Alliance, 10BASE-T1S Common Mode Choke (CMC) Test Specification*.
- *IEEE P802.1DG, TSN Profile for Ethernet Communications*.

TERMINOLOGY

To make the best use of the system, it is helpful to understand the following terms.

Table 1. Abbreviations, Terms, and Symbols

Acronym	Description	Acronym	Description
ADC	Analog to Digital Converter	MDC	MDIO Interface Clock
AN	Auto Negotiation	MDIO	Management Data Input/Output
CD	Collision Detection	MII	Media Independent Interface
CAN	Controller Area Network	MMD	MDIO Manageable Device
CRC	Cyclic Redundancy Check	NTC	Negative Temperature Coefficient
Clause 4	IEEE 802.3 Clause 4: MAC	OA-SPI	OPEN Alliance SPI
Clause 22	IEEE 802.3 Clause 22: RS and MII	OEM	System Manufacturer/Original Equipment Manufacturer
Clause 45	IEEE 802.3 Clause 45: MDIO Interface	OPEN Alliance	Special Interest Group: One-Pair Ether-Net
CM	Common Mode	OSC	Oscillator/Crystal
CMC	Common Mode Choke	OSI	Open Systems Interconnect
CMT	Common Mode Termination	OSR	Output Shift Register
CS	Chip Select	OTP	One Time Programmable
CSMA/CD	Carrier Sense Multiple Access/Collision Detection	PCS	Physical Coding Sublayer
DA	Destination Address	PCB	Printed Circuit Board
DC	Direct Current	PHY	Interface semiconductor circuit for implementation of the functions of the Ethernet physical layer
DET	Differential End Termination	PLCA	Physical Layer Collision Avoidance
DGND	Digital Ground	PMA	Physical Medium Attachment
DME	Differential Manchester Encoding	PMD	Physical Medium Device
DUT	Device under Test	PoDL	Power over Data Line
EBTP	E2B Transport Protocol	PoR	Power-on Reset
ECU	Electronic Control Unit	P2P	Point to Point
ECC	Error Correction code	QoS	Quality of Service
ED	Energy Detect	RefDes	Reference Designator
EMC	Electromagnetic Compatibility	RF	Radio Frequency
ESD	Electrostatic Discharge	RS	Reconciliation Sublayer
ET	End Termination	Rx	Receive
FCS	Frame Check Sequence	SAIF	Sensor Actuator Interface[1]
FIFO	First In, First Out	SDI	Serial Data Input
GND	Ground (0V Reference) connection in electrical circuits	SDO	Serial Data Output
gPTP	Generalized Precision Time Protocol	SECDED	Single Error Correction, Double Error Detection
gRS	Generic Reconciliation Sublayer	SNR	Signal to Noise Ratio
HV	High Voltage	SOC	System on Chip
IC	Integrated Circuit	SPI	Serial Peripheral Interface
IEEE	Institute of Electrical and Electronics Engineers	SSC	Safe State Controller
IP	Intellectual Property	SQI	Signal Quality Index
Switch	Network device that connects multiple devices within a local area network (LAN) and efficiently directs data between them based on their MAC addresses.	SRAM	Static Random Access Memory
ISO	International Organization for Standardization	TSC	Time Stamp Capture
ISR	Input Shift Register	TSN	Time Sensitive Networking
LPF	Low Pass Filter	Tx	Transmit
LUT	Look Up Table	UTP	Unshielded Twisted Pair
LV	Low Voltage	VBAT	Battery Voltage
MAC	Media Access Control	VCC	Pin for IC Voltage Supply

TERMINOLOGY

Table 1. Abbreviations, Terms, and Symbols (Continued)

Acronym	Description	Acronym	Description
MAC-PHY	A MAC-PHY solution integrates an IEEE Clause 4 MAC and a 10BASE-T1x PHY exposing a low pin count serial peripheral interface (SPI) to the host microcontroller.	VDD	Pin for IC Voltage SAupply
Mbps	Megabits per Second	WUD	Wake Up Detector
MCU	Micro Controller Unit	WUP/WUT/W US	Wake Up Pulse/Wake Up Tone/Wake Up Signal

[1] For more information on using SAIF pins, see the ADIN1140 data sheet.

ARCHITECTURE OVERVIEW

This section introduces the ADIN1140 10BASE-T1S transceiver technology. The ADIN1140 operates as a standard MAC-PHY product, enabling direct connectivity with a variety of host controllers via open alliance SPI (OA-SPI). The transceiver interfaces are shown in the Figure 1. The ADIN1140 transceiver has two dice—a high-voltage (HV) die, and a low-voltage (LV) die.

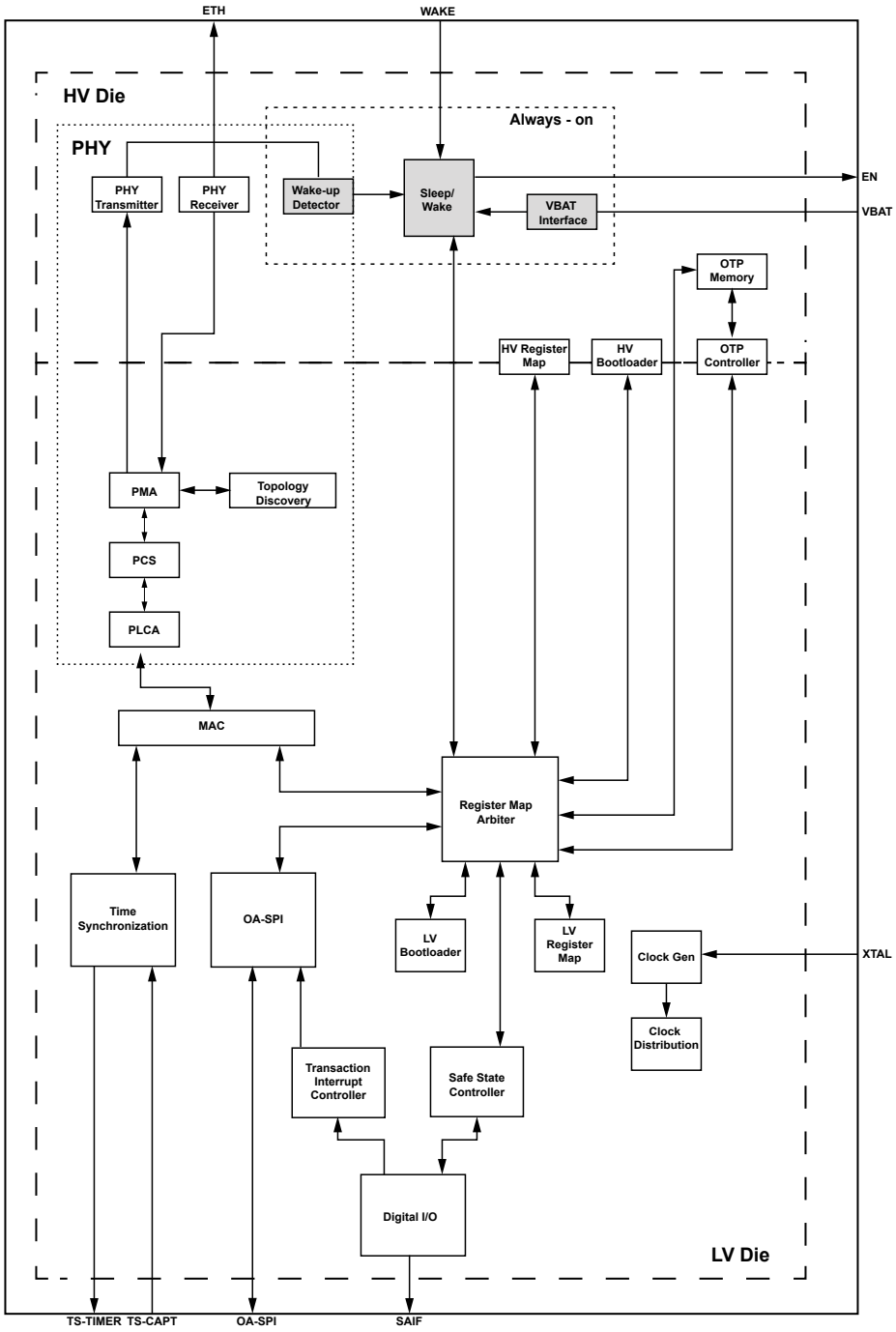

Figure 1. ADIN1140 Block Diagram

ARCHITECTURE OVERVIEW

10BASE-T1S INTERFACE

The ETH port interfaces to the 10BASE-T1S harness through an off-chip coupling circuit, which includes a common-mode choke and coupling capacitors. It interfaces to three blocks on the transceiver's 10BASE-T1S PHY module: the PHY transmitter, PHY receiver, and the wake-up detector.

PHYSICAL LAYER COLLISION AVOIDANCE (PLCA)

The physical layer collision avoidance (PLCA), physical coding sublayer (PCS), and the digital portion of the physical medium attachment (PMA) are implemented as per the 10BASE-T1S requirements and form the LV die portion of the PHY. The PHY block interfaces to the MAC.

MEDIA ACCESS CONTROLLER (MAC)

The PLCA block is connected to the integrated media access controller (MAC) which provides flow control, frame filtering, and data integrity checking.

TIME SENSITIVE NETWORKING (TSN)

The transceiver includes a time sync block for time sensitive networking (TSN). This block incorporates an IEEE 802.1AS engine and supports timestamping of incoming and outgoing frames. For more information, see the Time Synchronization section.

SAFE STATE CONTROLLER (SSC)

The transceiver features a safe state controller (SSC) that monitors faults and places the device into a predefined state if fault conditions are detected. The safe state controller can be configured to detect several fault conditions internally, and forward the fault externally using an SAIF output pin. For more information, see the Safe State Controller (SSC) section.

REGISTER MAP ARBITER

The register map arbiter routes access to the HV and LV die register maps as seen in the Bootloader section.

TRANSACTION INTERRUPT CONTROLLER

The transceiver includes an interrupt controller, which is used to output interrupts over the OA-SPI interface to the host controller. The interrupt controller can accept a configurable number of inputs from a range of internal triggers relating to, for example, sleep/wake, SSC, MAC, and PHY. For more information, see the Event Management section.

VBAT INTERFACE

The VBAT interface block serves two primary functions; it is used as an *always-on* supply for sleep/wake functionality that allows all other supplies to be set to 0V by inhibiting the external DC-DC converter. The VBAT interface block can monitor the VBAT voltage level for overvoltage (OV) and undervoltage (UV) events. For more information, see the Hardware Reset: Power-on Reset section.

OPERATING MODES

The 10BASE-T1S specification mandates half-duplex, point-to-point, 10Mbps, up to at least 15m cable.

Additionally, 10BASE-T1S PHYs may operate in a half-duplex multidrop mode. This operating mode is required to support up to at least eight PHYs and at least 25m cable. An overall effective data rate of 10Mbps is shared among the nodes.

The support of this multidrop topology with all nodes connected over the same twisted pair cable is a unique aspect of 10BASE-T1S differing from other Ethernet technologies. This bus implementation provides an optimized BOM, that only requires a single Ethernet PHY in each node. This means only one 10BASE- T1S port is required at the switch and removes the need for a star topology implementation associated with other Ethernet technologies.

The MDI and transmitter electrical specifications for a multidrop topology are different to those for a point to point topology. Requirements for the differential termination resistance connected across the MDI positive and negative terminals, depending on the network topology, are defined in IEEE 802.3-2022. The standard also defines the MDI return loss limits for a point to point topology and the minimum parallel impedance across the MDI attachment points for a multidrop topology.

10BASE-T1S TRANSCEIVER (PHY)

The transceiver includes an IEEE 802.3-2022 compliant Ethernet transceiver capable of 10Mbps half-duplex point to point or multidrop operation over a single balanced pair of conductors. The transceivers support PLCA which is an optional physical layer CSMA/CD enhancement for multidrop networks that achieves bounded latencies and fair transmit opportunities, while maintaining high throughput.

PLCA

PLCA is an optional generic reconciliation sublayer (gRS) for 10BASE-T1S PHYs operating in half-duplex mode and is defined in clause 148 of the IEEE 802.3-2022 specification. PLCA is an enhancement to CSMA/CD and manipulates the carrier sense and collision detect signals to add functionality without requiring any change to the MAC layer. PLCA is not a replacement for CSMA/CD, as media access is still handled by existing CSMA/CD functions. The 10BASE-T1S network can be seamlessly switched between the two methods of medium access control when required. The PLCA layer sits between the PCS and the MAC as shown in the Architecture Overview section.

PLCA operates by granting a transmit opportunity to each node on the network in a round robin fashion based on a node ID which is unique to each node. During each transmit opportunity, only the node with the corresponding node ID is permitted to transmit. Additional references to PLCA can be found in the following sections:

- Open Alliance TC14 Supported Features Overview section
- Bootloader section
- PLCA Diagnostics section

PLCA Operation

The node with ID = 0 is known as the PLCA coordinator. A PLCA cycle begins when this node transmits a BEACON onto the network to indicate the beginning of a new cycle of transmit opportunities. All PHYs on the network use the BEACON to synchronize their transmit opportunity timers (TO_TIMER). Nodes detect their assigned transmit opportunity by comparing the number of transmit opportunities that have passed since the BEACON, with their internally assigned node ID. When a programmed number of transmit opportunities have occurred, the PLCA coordinator node issues another BEACON to start the cycle again. If the PLCA coordinator node fails, the network falls back to CSMA/CD for medium access control when no beacons are detected for 13ms. This time-out is calculated as 2 × (*max_to_timer* × *max_plca_node_count* + *beacon_timer*) bit-times which is 2 × (255 × 255 + 20) = 130,090 bit-times = 13.009ms. This is mandated by IEEE 802.3-2022 Clause 148.4.6.4. The nodes switch back to PLCA mode when the first beacon is again detected on the network.

For a network with node IDs [0, N], a PLCA cycle consists of one BEACON and N+1 transmit opportunities. When a node wishes to use its transmit opportunity to send a packet, it transmits COMMIT symbols to inform all other nodes that it is sending a packet. The PLCA cycle moves to the next transmission opportunity at the end of the packet transmission or if nothing is transmitted within the TO_TIMER period.

PLCA comes with many advantages. The round robin scheme ensures that access to the medium is fair. The PLCA cycle results in a bounded maximum link latency, which means that a 10BASE-T1S network with PLCA is deterministic. The TO_TIMER ensures that if nodes have nothing to transmit, the PLCA cycle moves to the next node ID and causes the active nodes to use the majority of the cycle time, maximizing throughput. Figure 2 shows an example of a PLCA cycle.

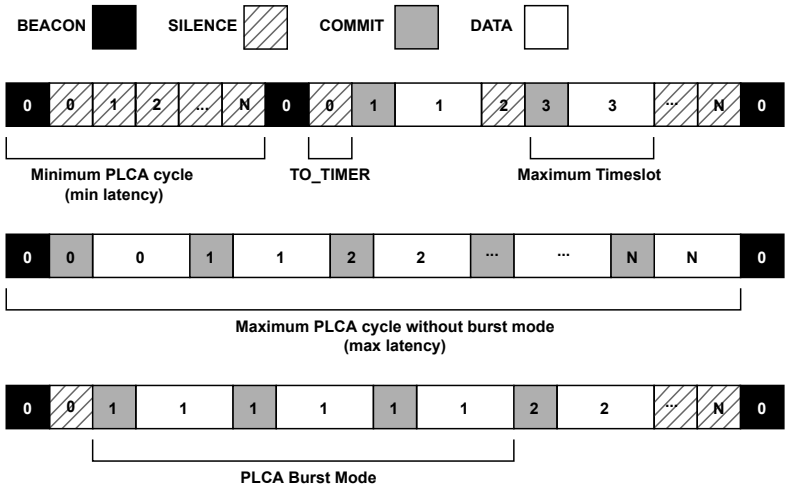

Figure 2. Overview of the PLCA Cycle

10BASE-T1S TRANSCEIVER (PHY)

Burst Mode

In PLCA burst mode, specific nodes are configured to allow the transmission of multiple frames during a single transmit opportunity up to a configured limit. During burst mode, after sending each frame, the node sends COMMIT symbols to inform other nodes that it has more frames to transmit. The number of frames that a node can transmit in burst mode is configured using the PHY_OA_PLCA_BURST.PLCAMAX-BURSTCNT bit field. When burst mode is enabled, after a successful transmission, the PHY waits for additional frames from the MAC for a duration of time configured by the PHY_OA_PLCA_BURST.PLCABURSTTIMER bit field. The minimum value that a program can set for the PHY_OA_PLCA_BURST.PLCABURSTTIMER field is the inter frame gap. Larger values increase the chance to join multiple packets from the same sender into a burst, at the expense of potentially unutilized bandwidth.

If additional frames are not sent by the MAC and the PHY_OA_PLCA_BURST.PLCABURSTTIMER expires, the PLCA cycle moves to the next node irrespective of the value in the PHY_OA_PLCA_BURST.PLCAMAXBURSTCNT field.

Precedence Mode

PLCA precedence mode is a feature that enables prioritization like a traditional CAN bus. It is enabled using the PHY_OA_PLCA_EXT register. The priority of the nodes is based on PLCA node ID in ascending order (ID = 0 is the highest priority). To use this feature, all PLCA nodes on the network must have precedence mode enabled. This feature can work alongside PLCA burst mode.

Precedence mode works by restarting the PLCA cycle after ANY packet is sent by any node. This means that the PLCA cycle only moves to the next node if all previous nodes had nothing to transmit. Therefore, as long as a node with higher priority has something to send, nodes with lower priority wait. After any node transmits a packet, the highest priority node always gets the first chance to transmit again, since the cycle restarts. An example of a PLCA cycle with precedence mode enabled is seen in Figure 3.

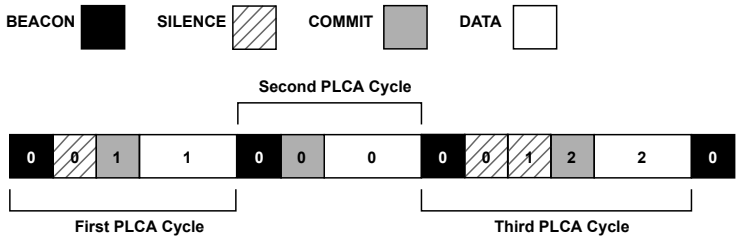

Figure 3. PLCA Cycle with Precedence Mode Enabled

Leader Mode

PLCA leader mode allows any node to be the PLCA coordinator node, regardless of PLCA ID. When enabled, any node can be configured to set itself as the PLCA coordinator node, even if it is not assigned PLCA ID = 0. This can be used to elect a back-up PLCA coordinator when the node with PLCA ID = 0 is non-functional. When leader mode is enabled, the node transmits beacons on the network. The system must ensure this is done only when the coordinator node has failed. Once the coordinator node is back functional, two nodes would be transmitting beacons on the network. This condition needs to be detected by the node that has enabled leader mode must turn off the leader mode option. Note this would likely cause a temporary disruption to traffic on the bus.

To enable any node as a PLCA Leader, set the PHY_OA_PLCA_EXT.PLCALEADEREN and PHY_OA_PLCA_EXT.PLCALEADER bits, after detecting that the PLCA coordinator node is down and not sending beacons. In addition, configure the PLCA node count value in the PHY_OA_PLCA_CTRL1.PLCANODECOUNT bit field for that particular node.

Multiple PLCA ID Support

The ADIN1140 supports the assignment of multiple PLCA IDs to a single node. This is used to adjust the frequency of transmit opportunities available, to achieve ultra-low latencies for specific nodes in a system. Figure 4 and Figure 5 show how the PLCA cycle changes when this feature is used. Assigning consecutive PLCA IDs to a single node is not supported (for example, assigning PLCA IDs 1, 2, and 3 to node B is not supported). As shown in Figure 5, there must always be a gap of at least one PLCA transmit opportunity between transmit opportunities assigned to a single node.

In Figure 4, node B is assigned a single PLCA ID. The maximum latency for each node in this cycle is 1 BEACON + 4 frame lengths. In *PLCA Cycle with Assigning Multiple PLCA IDs to Node B*, node B has been assigned three PLCA IDs. The arrangement of these node IDs is such that every second transmit opportunity in the PLCA cycle is available to node B. This reduces the maximum latency for node B at the expense

of the other nodes. Assuming that the frame size is the same for all nodes, and burst mode is not enabled for any node, node B's maximum latency is now 1 BEACON + 1 frame length, which is approximately a 66% reduction. However, the maximum latency of the other nodes is now approximately 66% larger.

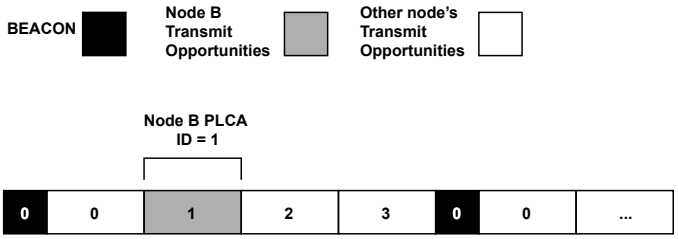

Figure 4. PLCA Cycle without Assigning Multiple PLCA IDs to Node B

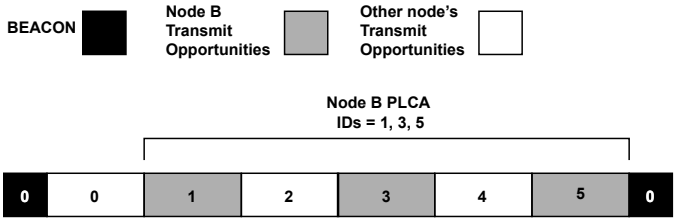

Figure 5. PLCA Cycle with Multiple PLCA IDs Assigned to Node B

PLCA Configuration

The PHY_OA_PLCA_CTRL0 register contains the controls to enable/disable the PLCA reconciliation sublayer.

The PHY_OA_PLCA_CTRL1 register is used to set the local node PLCA ID and the node count.

The controls to enable multiple PLCA IDs are found in the PHY_OA_PLCA_CTRL2 through PHY_OA_PLCA_CTRL5 registers.

The PHY_OA_PLCA_BURST register is used to enable PLCA burst mode and to configure burst mode settings. When configuring the max burst count, every integer increase allows another extra packet to be transmitted in burst mode. The burst timer parameter sets the maximum time that the PHY waits for a new packet from the MAC after a successful transmission. This must be set to greater than or equal to (≥) the IFG period.

The PHY_OA_PLCA_EXT register contains the controls to enable/disable PLCA precedence mode. It also contains controls to enable PLCA leader mode and elect the node to be the PLCA coordinator.

The PHY_OA_PLCA_TOTMR register is used to configure the TO_TIMER value.

The PHY_OA_TWEAKS_1.NO_COL_COUNT bit field can be used to disable collision counting in PLCA mode. If set, the PHY_STD_PCS_DIAGNOSTIC_2.CORRUPTEDTXCNT counter does not increment for physical collisions that are detected by the PHY.

PLCA Programming Example

Use the following procedure to configure and enable PLCA.

1. Set PLCA ID. Set the local node PLCA ID using the PHY_OA_PLCA_CTRL1.PLCALOCALID bit field.
2. Set PLCA IDs. Local node PLCA IDs are set in the following bit fields. Optionally, set multiple PLCA IDs using the following registers:
   - PHY_OA_PLCA_CTRL1.PLCALOCALID
   - PHY_OA_PLCA_CTRL2.PLCALOCALID1
   - PHY_OA_PLCA_CTRL2.PLCALOCALID2
   - PHY_OA_PLCA_CTRL3.PLCALOCALID3
   - PHY_OA_PLCA_CTRL3.PLCALOCALID4
   - PHY_OA_PLCA_CTRL4.PLCALOCALID5

- PHY_OA_PLCA_CTRL4.PLCALOCALID6
- PHY_OA_PLCA_CTRL5.PLCALOCALID7

If multiple PLCA IDs are set, then enable subsequent PLCA IDs in the PHY_OA_PLCA_CTRL5.PLCALOCALID_EN bit field.

Note that, a single node can have up to eight unique PLCA IDs.

3. Enable the PLCA by setting the PHY_OA_PLCA_CTRL0.PLCAEN bit =1 (a value of 0 disables the PLCA).

Preamble Length Handling in PLCA Mode

An Ethernet frame begins with a 7-byte preamble followed by the 1-byte start of frame delimiter (SFD). In total, the preamble and SFD must consist of 16 symbols:

- Two SYNC symbols (JJ)
- Two SSD symbols (HH)
- Ten '0x5' symbols
- The SFD (0x5, 0xD)

So, including the SFD, there should be 11 "0x5" symbols in total. However, the ADIN1140 exhibits the following preamble handling behavior in PLCA mode:

- On transmit, it may occasionally contain one fewer '0x5' symbol than specified. Including the SFD, the transmitted frame may contain ten '0x5' symbols instead of the expected 11.
- On receive, Ethernet frames containing fewer than the specified number of '0x5' preamble symbols are not dropped by the PHY.

MEDIA ACCESS CONTROLLER (MAC)

The transceiver combines an IEEE802.3-2022 Ethernet PHY and an 802.3 Clause 4 compliant MAC, which includes an OPEN alliance serial peripheral interface (OA-SPI).

This interface allows the MAC to connect to low cost microcontrollers without requiring a microcontroller with MAC interface. Ethernet packets and control/status commands are transferred over OA-SPI. OA-SPI also requires only five pins, enabling a simpler hardware interface with fewer pins than MII or RMII. The MAC has one receive first in, first out (FIFO), and two transmit FIFOs, one low priority and one high priority.

The data is transferred over the OA-SPI full duplex.

FRAME FILTERING ON RECEIVE

Received frames filtering requires configuration of the address filtering table. The ADIN1140 supports different methods for filtering the received frames.

MAC Address Filtering

The MAC can be configured to filter up to 16 different MAC addresses based on the destination MAC address (DA).

To receive frames with a particular DA, that DA must be programmed to one of the 16 MAC_ADDR_FILT_LWR[n] and MAC_ADDR_FILT_UPR[n] registers. Each register is 32 bits wide. Therefore, for example, to program a DA of 0800 005A 646B to ADDR_FILT[0], write the following:

1. 0x0800 to MAC_ADDR_FILT_UPR[n] (n = 0)
2. 0x005A646B to MAC_ADDR_FILT_LWR[n] (n = 0)

Write the addresses in order with the UPR register written first and the LWR register written last. It is important that these two writes are done one after the other with no other OA-SPI transactions (reads or writes) in between.

MAC addresses can also be masked using the MAC_ADDR_MSK_LWR[n] and MAC_ADDR_MSK_UPR[n]registers. For example, to receive all the MAC addresses in the range 0x8000 005A 64xx, use the following steps.

1. Program a DA of 0800 005A 64xx, as described above, where xx is any value.
2. Write 0xFFFF to MAC_ADDR_MSK_UPR[n] (n = 0)
3. Write 0xFFFFFF00 to MAC_ADDR_MSK_LWR[n] (n = 0)

The combination of filter table settings and forwarding unknown frames settings is described in Figure 6.

Frames received with bad CRC or with receive errors, as well as runt or jabber frames, are dropped and counted (see the MAC Layer Diagnostics section).

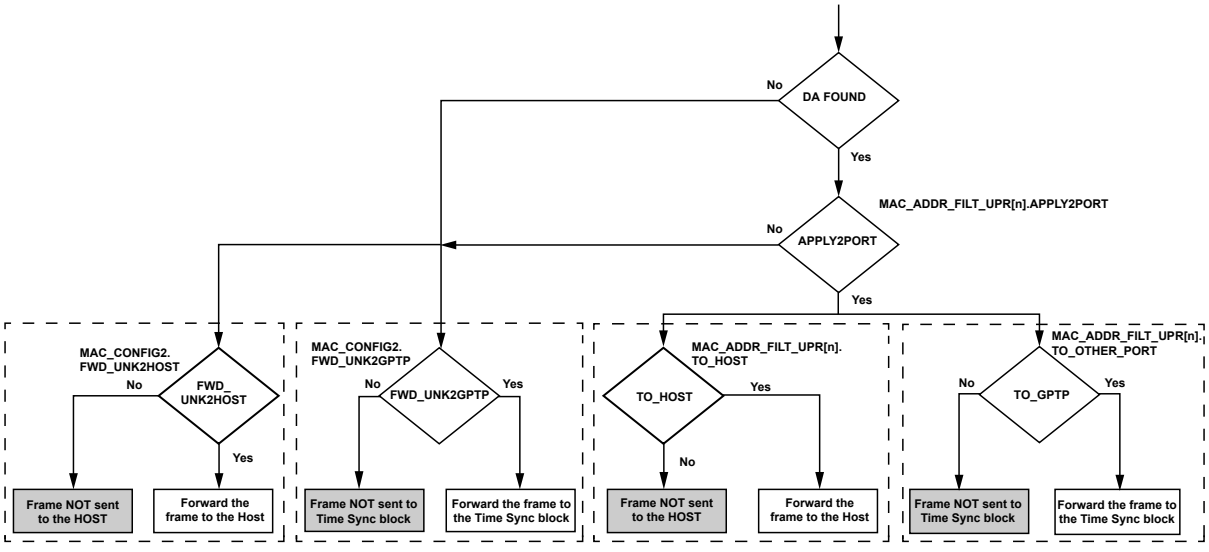

Figure 6. Filtering Algorithm

MEDIA ACCESS CONTROLLER (MAC)

VLAN Filtering

The MAC supports VLAN Identifier based filtering for IEEE 802.1Q tagged Ethernet frames to the host. VID (VLAN ID) filtering is enabled by setting the MAC_RXFILT_VID_TABLE.RXFILT_VID_EN bit. The VID table can store two VID entries. These are set by writing to the MAC_RXFILT_VID_TABLE.RXFILT_VID_ENTRY1 and MAC_RXFILT_VID_TABLE.RXFILT_VID_ENTRY2 bit fields. The MAC_RXFILT_VID_TABLE.RXFILT_VID_RULE bit field is used to set which Ethernet frames are forwarded.

- 0 = Ethernet frames are only passed if the entries match any of the two entries in the table. All other Ethernet frames are discarded, including Ethernet frames that do not have a VID.
- 1 = Ethernet frames are only discarded if the entries match any of the two entries in the table. All other Ether- net frames are forwarded to the host, including frames that do not have a VID.

The ADIN1140 support for VLAN filtering has limitations and behaviors. Refer to Untagged Frame Handling When VLAN Filtering Is Enabled section, Support for a Single VLAN Tag section, and VLAN Tag Impact on Maximum Payload Size section for more information.

Untagged Frame Handling When VLAN Filtering Is Enabled

When both MAC address filtering and VLAN filtering are enabled, and MAC_RXFILT_VID_TABLE.RXFILT_VID_RULE is set to '1', frames without a VLAN tag are forwarded to the host even if the MAC address filter would otherwise drop the frame.

Support for a Single VLAN Tag

The MAC supports decoding of one VLAN tag only, which must be a C-TAG VLAN with TPID = 0x8100. Frames containing multiple VLAN tags are not fully decoded. Any subsequent VLAN tag is treated as part of the Ethernet payload, and its TPID is interpreted as the EtherType. Frames containing an S-TAG VLAN (TPID = 0x88A8) are treated as untagged frames, and the S-TAG TPID is interpreted as the EtherType.

VLAN Tag Impact on Maximum Payload Size

The maximum transmissible Ethernet frame size is fixed at 1518 bytes. When a VLAN tag is included, this limit does not increase. As a result, the maximum supported Ethernet payload size is reduced from 1500 bytes to 1496 bytes for VLAN-tagged frames.

EtherType Filtering

The MAC also supports EtherType (Ethernet type) based filtering for all the received Ethernet frames. EtherType filtering is enabled by setting the MAC_RXFILT_ETYPE_CNRL.RXFILT_ETYPE_EN bit. The ETYPE table can store two EtherType entries. These are set by writing to the MAC_RXFILT_ETYPE_TABLE.RXFILT_ETYPE_ENTRY2 and MAC_RXFILT_ETYPE_TABLE.RXFILT_ETYPE_ENTRY1 bit fields. The MAC_RXFILT_ETYPE_CNRL.RXFILT_ETYPE_RULE field is used to set which Ethernet frames are forwarded to the host and which ones are discarded:

- 0 = Ethernet frames are only passed if the entries match any of the two entries in the ETYPE table. All other Ethernet frames are discarded.
- 1 = Ethernet frames are only discarded if the entries match any of the two entries in the table. All other Ether- net frames are forwarded to the host.

STATISTICS COUNTERS

There are 28 32-bit counters on the transmit and receive ports that increment on each frame transmit and receive. The counters are listed Table 2. These registers are described in the MAC Registers chapter.

Table 2. Statistics Counters

Name	Description
MAC_RX_FRM_CNT	Receive frame count
MAC_RX_BCAST_CNT	Receive broadcast count
MAC_RX_MCAST_CNT	Receive multicast count
MAC_RX_UCAST_CNT	Receive unicast count
MAC_RX_CRC_ERR_CNT	Receive CRC errored frame count
MAC_RX_ALGN_ERR_CNT	Receive alignment error count
MAC_RX_PREAMBLE_ERR_CNT	Receive preamble error count
MAC_RX_SHORT_ERR_CNT	Receive short frame error count

MEDIA ACCESS CONTROLLER (MAC)

Table 2. Statistics Counters (Continued)

Name	Description
MAC_RX_LONG_ERR_CNT	Receive long frame error count
MAC_RX_PHY_ERR_CNT	Receive PHY error count
MAC_RX_DROP_HOST_FULL_CNT	Receive frames dropped due to Host FIFO full
MAC_RX_DROP_FILT_CNT	Receive frames dropped due to filtering
MAC_RX_IFG_ERR_CNT	Receive frames received with interframe gap errors
MAC_TX_FRM_CNT	Transmit frame count
MAC_TX_BCAST_CNT	Transmit broadcast count
MAC_TX_MCAST_CNT	Transmit multicast count
MAC_TX_UCAST_CNT	Transmit unicast count
MAC_TX_SINGLE_COL_CNT	Transmit single collisions frame count
MAC_TX_MULTIPLE_COL_CNT	Transmit multiple collisions frame count
MAC_TX_DEFERRED_XMIT_CNT	Transmit deferred transmission frame count
MAC_TX_LATE_COL_CNT	Transmit late collision frame count
MAC_TX_XSCOLS_CNT	Transmit excess collision frame count
MAC_TX_UNR_CNT	Transmit frame dropped due to an under run count
MAC_HI_RFC	Number of frames in the receive FIFO
MAC_HI_RXSIZE	Data in the receive FIFO. Number of half words (16-bit)
MAC_TFC	Number of frames in the transmit FIFO
MAC_TXSIZE	Data in the transmit FIFO. Number of half words (16-bit)
MAC_HTX_OVF_FRM_CNT	Host transmit frames dropped due to FIFO overflow

Receive Drop FIFO Full Counter

Before the first byte of a received frame is written into the appropriate receive FIFO, the space in the FIFO is checked. If there is no space for at least 256 bytes, the frame is dropped and the MAC_RX_DROP_FILT_CNT.RX_DROP_FILT_CNT counter increments. If there is space for at least 256 bytes in the FIFO, the logic commences writing the frame to the receive FIFO. If the received frame exceeds 256 bytes and the receive FIFO fills, the frame is dropped and the MAC_RX_DROP_FILT_CNT.RX_DROP_FILT_CNT counter increments.

TRANSMIT PRIORITY QUEUES

The transmit frame priority feature is enabled using the MAC_PLCA_PRIORITY.FRAME_PRIORITY_EN bit. This enables the use of two different FIFOs on transmit: a high priority FIFO and a low priority FIFO. The MAC_TX_PRI.TX_HOST_PRI bit field is used to configure the percentage use between the two queues. The VS[0] field from the transmit data header (refer to the Transmit Data Headersection) is then used to select which queue each frame is sent to. Table 3 shows the percentage use of each queue for each transmit priority queue configuration.

Table 3. Percentage Queue Utilization per Configuration

TX_HOST_PRI	High Priority (VS = 1)	Low Priority (VS = 0)
0x0	50%	50%
0x2	75%	25%
0x4	87.5%	12.5%
0x5	100%	0%

The transmit priority queue configuration determines which FIFO transmits the next byte when both FIFOs have bytes to transmit. For example, for configuration 0x2, the high priority queue is allocated 75%. Therefore, if both queues have data to transmit, on average the high priority queue transmits 3 bytes for every 1 byte transmitted from the low priority queue.

If the high priority queue is allocated 100%, then any frame added to that queue is guaranteed to be the next frame transmitted. In this case, the low priority queue only transmits if the high priority queue is empty.

If the frame priority feature is enabled, it is important to ensure the Tx FIFOs do not overflow. This is done by ensuring there is always 256 bytes (4 transmit credits of 64-byte chunks each or 8 transmit credits of 32-byte chunks each) available in each Tx FIFO so a chunk can always be sent to retrieve the number of transmit credits.

MEDIA ACCESS CONTROLLER (MAC)

This feature is used in two ways:

- The two FIFOs are used as two different queues allowing two different parts of an application to send information using a certain split in throughput allocation.
- One queue is used as a high priority bypass queue. In this way, most of the traffic would be sent through the low priority queue, and then any traffic that must be sent immediately is sent through the high priority queue.

The priority feature works on a constantly running averaging calculation. Therefore, for example, if a lot of frames have been sent to the high priority queue and no frames have been sent to the low priority queue, low priority frames bypass high priority frames until the percentage split set by the MAC_TX_PRI.TX_HOST_PRI bit field is reached again.

Frames should be sent to one queue at a time. Sending a frame to both queues at the same time is not supported and if frames are sent to both queues at the same time, the MAC will enter an unrecoverable state and no frames will get through until the part is reset.

Note: When a transmit data chunk contains both the end of a previous frame (EV = 1) and the start of a new frame (SV = 1), the transmit priority queue must not be changed, as doing so can corrupt frame transmission and requires a MAC reset for recovery.

Note: When the transmit priority queue feature is enabled, partial frames are not supported; starting a new frame (SV = 1) before the previous frame has completed (EV = 1) can corrupt the MAC FIFOs and requires a MAC reset for recovery.

Minimum Transmit Credits for Priority Queues

When transmit priority queuing is enabled, the MAC requires a minimum amount of available transmit FIFO space before accepting a frame from the OA-SPI interface. If insufficient transmit credits are available, the received frame is dropped. Application software must ensure that frames are written to the priority queues only when the required number of transmit credits is available.

The minimum required transmit credits depend on the configured OA-SPI chunk payload size, as shown in Table 4.

Table 4. Chunk Sizes vs. Required Transmit Credits

Chunk Size (bytes)	Required Transmit Credits
8	29
16	15
32	8
64	4

The OA-SPI chunk payload size is configured using the MAC_CONFIG0.CPS register. The default chunk size is 64 bytes.

FRAME RECEIVE AND TRANSMIT ERRORS

By default, all received errored frames are dropped and counted. Received errored frames do not generate interrupts. Instead, they are dropped and counted, and the software must monitor the statistics counters.

SRAM ECC PROTECTION

When writing a frame to the FIFO, the size of the frame is inserted in a 16-bit word at the front of the frame and written to the FIFO. A 5-bit error correction code (ECC) is placed alongside the size field.

When this location is read from static random-access memory (SRAM), the ECC is checked. If a double bit error is detected, the MAC_STATUS1.TX_ECC_ERR or MAC_STATUS1.RX_ECC_ERR bits assert. If a double bit error is detected on reading a frame header from the receive FIFO, the frame is not transmitted.

In response to an ECC error, a FIFO automatically clears. All frames in the FIFO are lost, transmission stops, and a bad CRC is appended to the frame that was transmitted. The next frame received is written to a FIFO.

OPEN ALLIANCE SPI PROTOCOL

The OPEN Alliance SPI protocol Version 1.1 can transfer data over the SPI using full duplex operation, achieving bidirectional frame transfer. See the device datasheet for supported SPI clock frequencies. The transceiver supports the following OPEN Alliance SPI capabilities.

- Validation of FCS (Frame Check Sequence) appended by and received from the SPI host.

MEDIA ACCESS CONTROLLER (MAC)

- Supported chunk payload of 8, 16, 32, and 64 bytes.
- IEEE 1588 time stamp capture on transmit and receive.

The OPEN Alliance SPI protocol defines two types of transactions: data transactions for Ethernet frame transfers and control transactions for register read/write operations.

A chunk is the basic element of data transactions and is composed of 4 bytes of overhead plus the configured payload size.

Data transactions consist of an equal number of transmit and receive chunks. Chunks in both transmit and receive directions may or may not contain valid frame data independent from each other, allowing for the simultaneous transmission and reception of different length frames. The data header of the chunk in transmit frames, and the data footer in receive frames, indicate which bytes of the payload contain valid frame data. For full information on the OPEN Alliance SPI protocol used by the transceiver, refer to the *OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface v1.1*.

Note that $\overline{CS}$ can be continuously asserted for multiple transactions of the same type. When changing between control and data transactions, $\overline{CS}$ must be deasserted for the minimum high time period as shown in Figure 9. The minimum $\overline{CS}$ high time is stated in the product specific data sheet.

Data Chunks

Transmit data chunks consist of a 4-byte header followed by the transmit data chunk payload, as shown in Figure 7.

Figure 7. Transmit Data Chunk

Receive data chunks consist of the receive data chunk payload followed by a 4-byte footer, as shown in Figure 8.

Figure 8. Receive Data Chunk

The default size of the data chunk payload is 64 bytes. This size is configurable in 8, 16, 32, or 64 bytes using the chunk payload selector bits (MAC_CONFIG0.CPS). The data chunk size must be configured before enabling data transmission or reception. Therefore, when the data chunk size is configured, it must not be changed without resetting the MAC-PHY.

Data Chunk Transactions

Data transactions consist of 1 to N chunks on the SDO and SDI pins. The 4-byte data header occurs at the beginning of each transmit data chunk on SDO, and the 4-byte data footer occurs at the end of each data chunk on SDI. These headers and footers contain the information needed to determine the validity and location of the transmitted and received frames within the data chunk payload. The Ethernet frames start at any 32-bit aligned word within the payloads, as shown Figure 10 and Figure 11.

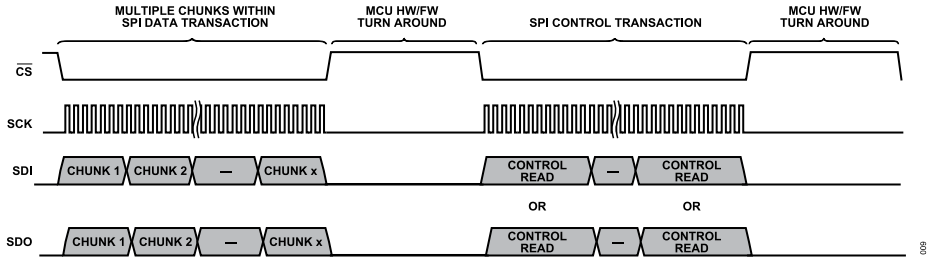

Figure 9. Ethernet Data Frame Transfer Followed by Control Transfer

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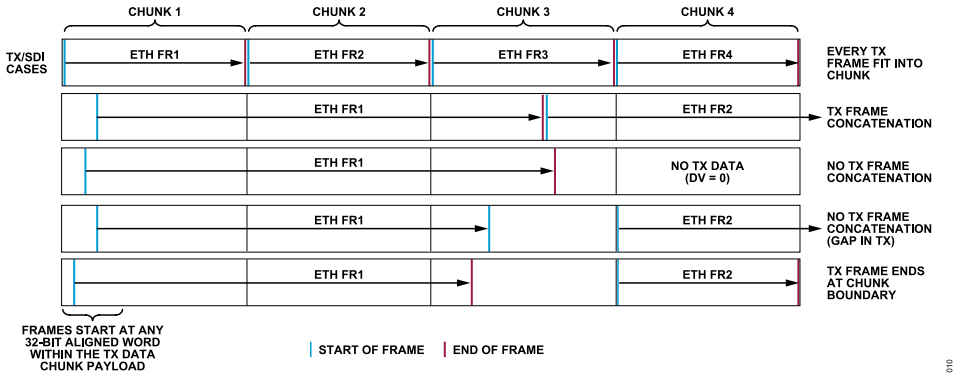

Figure 10. Transmit Data Chunk Cases

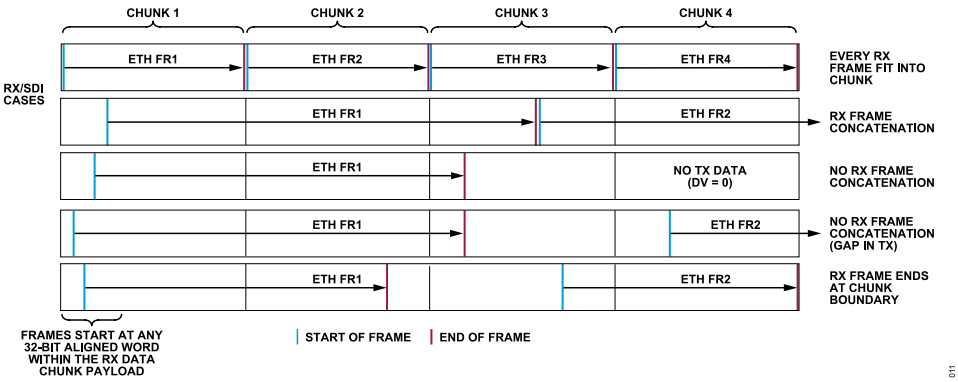

Figure 11. Receive Data Chunk Cases

Transmit Data Header

Table 5 shows the structure of a transmit data header.

Table 5. Transmit Data Header

D31	D30	D29	D28 to D24	D23 to D22	D21	D20	D19 to D16	D15	D14	D13 to D8	D7 to D6	D5 to D1	D0
1	SEQ	NORX	RSVD	VS	DV	SV	SWO	RSVD	EV	EBO	TSC	RSVD	P

The bit definitions are as follows.

- SEQ: data chunk sequence. The sequence functionality is not supported by the ADIN1140 transceiver. This bit must be set to 0.
- NORX: no receive flag. The SPI host can set this bit to indicate to the MAC-PHY that it does not process receive frame data that is in the current receive data chunk. For normal operation, set NORX to 0 to indicate that it accepts and processes any receive frame data within the current chunk.
- VS: vendor specific bits:
  - VS[0]: priority of the transmitted frame
    - 0 = Frame transmitted via the low priority queue
    - 1 = Frame transmitted via the high priority queue
  - VS[1]: set to 0
- DV: data valid flag. The SPI host uses this bit to indicate if the current chunk contains valid transmit data (DV = 1) or not. When this bit is 0, the MAC-PHY ignores the chunk payload.
- SV: start valid flag. When this bit is 1, the beginning of an Ethernet frame is present in the current transmit data chunk payload.
- SWO: start word offset. When SV is 1, this field contains the 32-bit word offset into the transmit data chunk payload that points to the start of the new Ethernet frame. If SV is 0, the host must write this field as 0.
- EV: end valid flag. When this bit is 1, the end of an Ethernet frame is present in the current transmit data chunk payload.

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- EBO: end byte offset. When EV is 1, this field contains the byte offset into the transmit data chunk payload that points to the last byte of the Ethernet frame to transmit. If EV is 0, the host must write this field as 0.
- TSC: time stamp capture. Request a time stamp capture when the frame is transmitted onto the network. See the following:
  - 00 = no action
  - 01 = capture in the pair of the MAC_TTSCAL and MAC_TTSCAH registers. The MAC_STATUS0.TTSCAA is asserted after the timestamp is captured.
  - 10 = capture in the pair of MAC_TTSCBL and MAC_TTSCBH registers. The MAC_STATUS0.TTSCAB is asserted after the timestamp is captured.
  - 11 = capture in the pair of MAC_TTSCCL and MAC_TTSCCH registers. The MAC_STATUS0.TTSCAC is asserted after the timestamp is captured.
- P : Parity bit calculated over the transmit data header. Method is odd parity.
- RSVD: reserved. Always set to 0

Note: Under specific transmit error conditions, the SV (Start Valid) field in the OA-SPI transmit data header may be decoded twice. This behavior occurs only when all of the following conditions are met:

- The MAC CRC append feature is enabled (MAC_CONFIG2.HOST_CRC_APPEND = 1)
- The OA-SPI transmit chunk payload size is 64 bytes (MAC_CONFIG0.CPS = 6)

If a transmit data chunk (chunk 1) contains the end of a frame (frame 1) and presents a parity error in the header, frame 1 is dropped as expected, and a parity error is triggered.

If the next transmit data chunk (chunk 2) contains a full frame less than 64 bytes (frame 2), the Start Valid flag (SV) is decoded twice. Frame 2 is transmitted correctly, but 3 words (2 header words and 1 data word) of the next potentially non-existent frame (frame 3) are pushed into the FIFO.

If frame 3 is not present directly after chunk 2, the FIFO will read the first 3 words and issue an underflow error. The three invalid words produce a short invalid transmission on the MII port and the next frame (frame 3) will be dropped.

If frame 3 is present directly after chunk 2, it will have an incorrect header and it will be dropped. Frame 4 will be processed correctly.

So, to be able to handle this scenario, the host can detect if the parity error is produced during chunk 1, as the EXST flag is asserted in the Rx chunk footer. The host can then check if the next frame sent to the OASPI port fits into one chunk. If these conditions are both true, the issue will occur.

To recover from the issue, the host can send a dummy frame (frame 3) which will be discarded and won't create an invalid transmission on the MII port. The dummy frame needs to use more than one chunk (for example, be greater than 64 bytes).

Receive Data Footer

Table 6 shows the structure of a receive data footer.

Table 6. Receive Data Footer

D31	D30	D29	D28 to D24	D23 to D22	D21	D20	D19 to D16	D15	D14	D13 to D8	D7	D6	D5 to D1	D0
EXST	HDRB	SYNC	RCA	VS	DV	SV	SWO	FD	EV	EBO	RTSA	RTSP	TXC	P

The bit definitions are as follows.

- EXST: extended status. This bit is set when any bit in the MAC_STATUS0 or MAC_STATUS1 registers are set and not masked.
- HDRB: received header bad. When this bit is set, the MAC-PHY has received a control or data header with a parity error.
- SYNC: configuration synchronized flag. This field reflects the state of the MAC_CONFIG0.SYNC bit. When 0, this bit indicates that the MAC-PHY configuration may not be as expected by the SPI host. Following con- figuration, the SPI host sets the corresponding bit in the configuration register, which is reflected in this field.
- RCA: receive chunks available. The RCA field indicates the minimum number of additional receive data chunks of frame data that are available for reading beyond the current one. This field is 0 when there is no more receive frame data pending in the buffer of the MAC-PHY to be read.
- VS: vendor specific bits. These two bits are set to 00.

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- DV: data valid flag. The SPI host uses this bit to know if the current chunk contains valid receive data (DV = 1) or not. When this bit is 0, the SPI host ignores the chunk payload.
- SV: start valid flag. When this bit is 1, the beginning of an Ethernet frame is present in the current receive data chunk payload. The SV bit is not to be confused with the SFD byte described in IEEE Standard 802.3.
- SWO: start word offset. When SV is 1, this field contains the 32-bit word offset into the receive data chunk payload that points to the start of the new Ethernet frame. When a receive time stamp is added to the beginning of the received frame (RTSA = 1), SWO points to the most significant byte of the time stamp. If SV is 0, this field must be 0.
- FD: frame drop. When set, this bit indicates that the MAC has detected a condition for which the SPI host must drop the received Ethernet frame. This bit is only valid at the end of a received frame (EV = 1) and must be 0 at all other times.
- EV: end valid flag. When this bit is 1, the end of an Ethernet frame is present in the current receive data chunk payload.
- EBO: end byte offset. When EV is 1, this field contains the byte offset into the receive data chunk payload that points to the last byte of the received Ethernet frame. This field is 0 when EV = 0.
- RTSA: receive time stamp added. This bit is set when a 32-bit or 64-bit time stamp is added to the beginning of the SPI frame. This bit must be 0 when SV = 0.
- TXC: transmit credits. This field contains the minimum number of transmit data chunks of frame data that the SPI host can write in a single transaction without incurring a transmit buffer overflow. (NOTE: When a frame is retransmitted due to a collision, the MAC still consumes transmit credits for the initial (unsuccessful) transmission attempt, despite that frame never actually leaving the transmitter.)
- P: parity. Parity bit calculated over the receive data header. Method is odd parity.

When the MAC Rx FIFO clear controls are used (MAC_FIFO_CLR), ongoing OASPI transactions are terminated and the frame in mid-transmission is corrupted. The end valid (EV) and frame drop (FD) flags should be asserted to indicate to the host that a transmission error occurred. However, the next OASPI chunk will contain a new frame with start valid (SV) and data valid (DV) asserted. EV and FD are never asserted for the frame which was corrupted.

So, to be able to handle this scenario, the software in the host should expect an abrupt termination of the frame when it issues a FIFO clear. It should detect that it has received two footers with SV asserted (SV = 1) without an EV assertion (EV = 1). It should issue a transmit protocol error and discard the previous frame.

OPEN Alliance SPI Cut Through Mode

If cut through from or to the host is enabled, the method to transfer frames remains the same as when using store and forward mode. However, the frame receive starts when the receive threshold is reached, and the frame transmit starts when a configured transmit threshold is reached (refer to the MAC_TX_THRESH register).

The cut through mode is enabled via the receive cut through enable bits and transmit cut through enable bits (refer to the MAC_CONFIG0 register).

On receive, the MAC returns data as it becomes available. Unlike in store and forward mode, there may be empty chunks (DV = 0) between a start of frame (SOF) chunk and an end of frame (EOF) chunk. If the host does not read frames fast enough to keep the receive FIFO empty, the frames are then buffered in the receive FIFO as if it is operating in store and forward mode. When all the frames are read, the FIFO returns to operating in cut through mode.

On transmit, the host must provide frame data at a rate fast enough (>10Mbps) to ensure that the frame does not under run on transmit. If the MAC under runs, the MAC_STATUS0.TXBUE bit asserts and the MAC stops transmitting the frame in progress and appends a bad CRC to the frame.

Cut Through Transmit Latency

The time interval between the start of an SPI data transaction with a transmit header SWO of 0 (frame starts immediately in the chunk), and the time TX_EN rises with an SPI frequency of 20MHz and MAC_TX_THRESH = 1 (one half-word) = 4µs. The PHY transmit latency is 0.44µs for a total transmit latency of 4.44µs.

Cut Through Receive Latency

The receive latency varies based on the chunk size and the SPI frequency. Table 7 indicates the latency for a SPI frequency of 20MHz and all supported chunk sizes.

MEDIA ACCESS CONTROLLER (MAC)

Table 7. Receive Latency for 20 MHz for All Supported Chunk Size (RX_THRESH = CPS)

Chunk Size (Bytes)	Time to Receive a Chunk of Data over xMII (µs)[1]	Time for chunk transfer over SPI (µs)[2]	Total Rx Latency (µs)
64	57.6	26.11	70.66
32	32	13.82	38.91
16	19.2	7.68	23.04
8	12.8	4.61	15.10

[1] Enough frame data to fill a chunk must be received before a transfer starts on the SPI. The time to receive the frame preamble is also included in this.

[2] Assuming that the µC is not waiting for an interrupt and that it is providing back-to-back OPEN Alliance data transactions on the SPI. The frame transfers start in the middle of the chunk on average.

CRC Handling After OA-SPI Parity Error

The MAC receives Ethernet frames from the OASPI interface into its transmit FIFO. When the MAC is operating in cut-through mode, an Ethernet frame may begin exiting the transmit FIFO before it has been completely received from the OASPI interface. Because of this, if a parity error is detected and the frame has already begun exiting the FIFO, the MAC cannot drop the frame and instead intentionally appends an incorrect CRC to mark the frame as invalid.

However an issue can occur as follows:

- The MAC is operating in cut-through mode.
- There is one frame stored in the FIFO (Frame 1), which is in the process of being read out of the FIFO.
- During the reception of the next frame (Frame 2), there is a parity error in the OASPI interface.
- The parity error in Frame 2 occurs at the same time that the end of Frame 1 is read out of the FIFO.
- Frame 1 is transmitted correctly.
- Because Frame 2 has not begun exiting the FIFO, it can be dropped by the MAC due to the parity error.
- The issue occurs for the next frame to be received from the OASPI interface (Frame 3). Frame 3 will be appended with incorrect CRC by the MAC.

To handle this condition, frames which are dropped due to parity error should be re-transmitted twice by the host. In this case, if the issue does not occur, both re-transmissions will be sent correctly. If the issue occurs, the first re-transmission will have incorrect CRC appended and the second re-transmission will be sent correctly.

Control Transactions

Control transactions consist of one or more control commands. These commands are used by the SPI host to read and write registers within the MAC-PHY, and each one is composed of a 32-bit control command header followed by register data. Refer to Table 8 for more information.

Note that OA-SPI control data read/write protection is always enabled.

Table 8. Control Command Header

D31	D30	D29	D28	D27 to D24	D23 to D8	D7 to D1	D0
0	HDRB	WNR	AID	MMS	ADDR[15:0]	LEN	P

- HDRB: received header bad. When set by the MAC-PHY, HDRB indicates that a header was received with a parity error. The SPI host must always clear this bit. The MAC-PHY ignores this value.
- WNR: write not read. If 1, data is to be written to registers. Otherwise, data is to be read.
- AID: address increment disable. When clear, the address is automatically post-incremented by one following each register read or write.
- MMS: memory map selector. This field selects the specific register memory map to access. See the Memory Address Space and Memory Maps section.
- ADDR: address of the first register within the selected memory map to access.
- LEN: length. Specifies the number of registers to read/write. This field is interpreted as the number of registers –1. Therefore, a length of 0 reads or writes a single register.
- P: parity. Parity bit calculated over the control command header. Method used is odd parity.

An OPEN alliance control transaction is shown in Figure 12.

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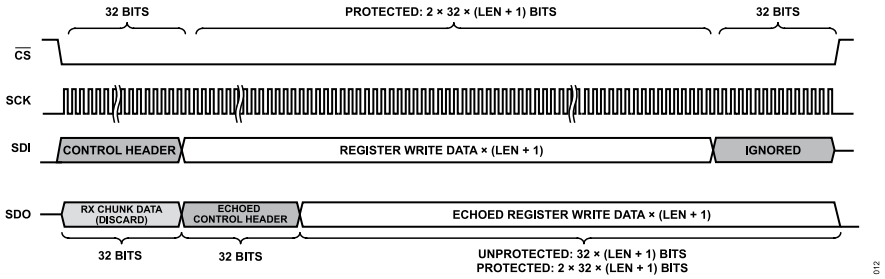

Figure 12. OPEN Alliance Control Transaction

Control Write

The MAC-PHY ignores the final 32 bits of data from the SPI host at the end of the control write command. The write header and data is also echoed from the MAC-PHY back to the SPI host so it can identify which register write failed in the case of any bus errors.

Control write commands can write either a single or multiple registers. When multiple registers are written, the address is automatically post incremented.

When a control write command is followed by another control command, the new control header must immediately follow the last word of the echoed register write data. The SPI host must deassert the CS signal following the last word of the echoed register write data when the write command is the last command of the transaction.

Control Read

The MAC-PHY ignores all data from the SPI host following the control header for the rest of the control read command. Control read commands can read either a single or multiple registers. When multiple registers are read, the address is automatically post incremented according to the address increment disable bit in the control header. Figure 13 shows a control read transaction.

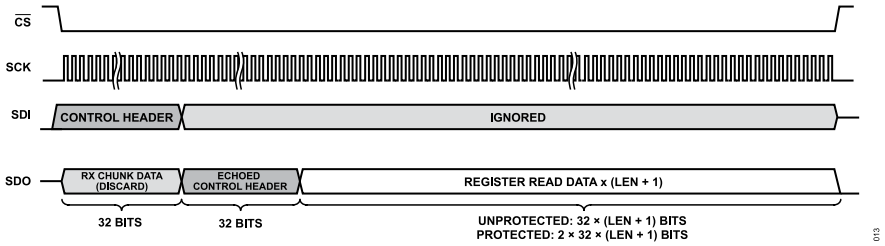

Figure 13. Control Read Transaction

OPEN Alliance SPI Errors

The following describe the OPEN Alliance SPI errors.

- SPI Header Parity Error. If a parity error is detected on a transmit header and there is a transmit frame in the process of being transferred over SPI, this frame is dropped. The MAC-PHY outputs a 32-bit constant value of 0xC0000001 until $\overline{CS}$ goes high.
  - The MAC-PHY responds with DV = 1, EV = 1, and FD = 1 in the first data footer following a new assertion of $\overline{CS}$.
  - If there is a parity error on a control transaction, the operation does not complete. Software can determine which transaction caused the error as the MAC-PHY returns a fixed 0xC0000001 on SDI for the duration of the SPI transaction. Software can then resend the corrupted control transaction after clearing the header error bit.
- Transmit Protocol Error. Occurs when the MAC-PHY detects protocol errors in the transfer of transmit data chunks. These errors are usually due to SPI host firmware issues and do not occur in normal operation. The transmit protocol error bit is set when a data header received by the MAC-PHY indicates data valid (DV = 1) without a prior start of frame indication (SV = 1), in which case the data chunk is ignored. Or, when the MAC-PHY receives two data headers indicating a start of frame (SV = 1) without an end of frame (EV = 1), the MAC-PHY drops the frame data from the previous start of frame indicator and begins accepting the frame data from the second start of frame indicator.

MEDIA ACCESS CONTROLLER (MAC)

- Transmit Buffer Overflow. Occurs when attempting to write transmit frame data to the MAC-PHY when there is no transmit buffer space available as indicated by the transmit credit field (TXC) of the previous data footer. In this condition, the MAC-PHY ignores the transmit data chunk and sets the host transmit FIFO overflow bit, and the frame data already in the buffer is dropped.
- Loss of Framing Error. This error occurs when the $\overline{CS}$ signal is de-asserted before the expected end of the data chunk or control command. The MAC-PHY and the loss of frame error is set, any transmit frame in progress is dropped, and any receive frame that is in route to the SPI host is terminated.
- Receive Buffer Overflow. This error occurs when the SPI host does not read frame data from the MAC-PHY fast enough. When this error occurs, the MAC-PHY terminates the frame being received from the PHY. In store and forward mode, no portion of the frame is transferred to the SPI host.
- Control Data Protection Error. The control data protection error (MAC_STATUS0.CDPE) and the loss of frame error (MAC_STATUS0.LOFE) bits assert when there is an error on write data received from the host. The write does not complete in this case. If possible, the software executes the write again. Protection is accomplished by duplication of each 32-bit word containing register data with its ones' complement. Errors are detected at the receiver by performing a simple exclusive-OR (XOR) of each received 32-bit word containing register data with its received complement and detecting if there are any zeros in the result.

Recommended Register Operation

Many of the MAC registers in the ADIN1140 are defined in the IEEE Standard 802.3, and the exact behavior of these registers follows the standard. This behavior may not always be obvious and is described in this section, including the recommended operation and use of the registers.

Read-Modify-Write Operation

All register write operations must be performed as read-modify-write operations. If this process is not followed, the value of the register bits can inadvertently change.

CSMA/CD

The transceiver implements PLCA in the PHY for deterministic, collision free transmission. However, if (for example) the PLCA head node fails or the PLCA is disabled, the node defaults to carrier sense multiple access with collision detection (CSMA/CD). CSMA/CD is implemented in the MAC as per the IEEE 802.3 Standard.

The CSMA/CD media access method can enable two or more stations to share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message. If, after initiating a transmission, the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (back off) before attempting to transmit again. If the maximum retry count is reached the transmit frame is dropped. The retry limit is set using the MAC_MAX_RETRY register and can be configured from 0 to 15 attempts as per the IEEE 802.3 standard.

CSMA/CD Behavior in Cut-Through Mode

When the MAC is operating in cut-through mode and using CSMA/CD to access the network (PLCA disabled), the following behavior may be observed under specific collision conditions.

This behavior occurs only when all of the following conditions are met:

- Cut-through transmit mode is enabled (TXCTE = 1)
- CSMA/CD is used for network access (PLCAEN = 0)
- The MAC CRC append feature is enabled (HOST_CRC_APPEND = 1)

Late Collision Handling at Maximum Retry Count

When transmitting long frames (greater than 80 bytes), if the maximum transmit collision retries is reached for a frame (16 collision retries), the MAC will dump that frame in normal operation. However, if the above conditions are true, and the final (16th) collision is a late collision, the MAC will dump that frame, like in normal operation, and it will also dump the next stored frame in the Tx FIFO.

So, to handle this scenario, there is an OASPI interrupt available for excessive collision retries (MAX_RR_ERR). Once the system software is notified of the frames dumped, it can decide if it needs to retransmit them or take other action.

MEDIA ACCESS CONTROLLER (MAC)

Retransmission After Collision Backoff for Short Frames

When transmitting short frames (less than 80 bytes), and a collision occurs while sending the CRC, the frame is not retransmitted when the back off timer elapses. It will be retransmitted when another frame is written into the FIFO.

This issue does not occur if the host appends the CRC. If the MAC must append the CRC, short frames can be padded up to 80 bytes to avoid this issue.

TIME SYNCHRONIZATION

The ADIN1140 transceiver integrates a full IEEE 802.1AS (gPTP) engine, which removes the need for a microcontroller for gPTP. Along with the engine, the ADIN1140 provides hardware counters and waveform generation.

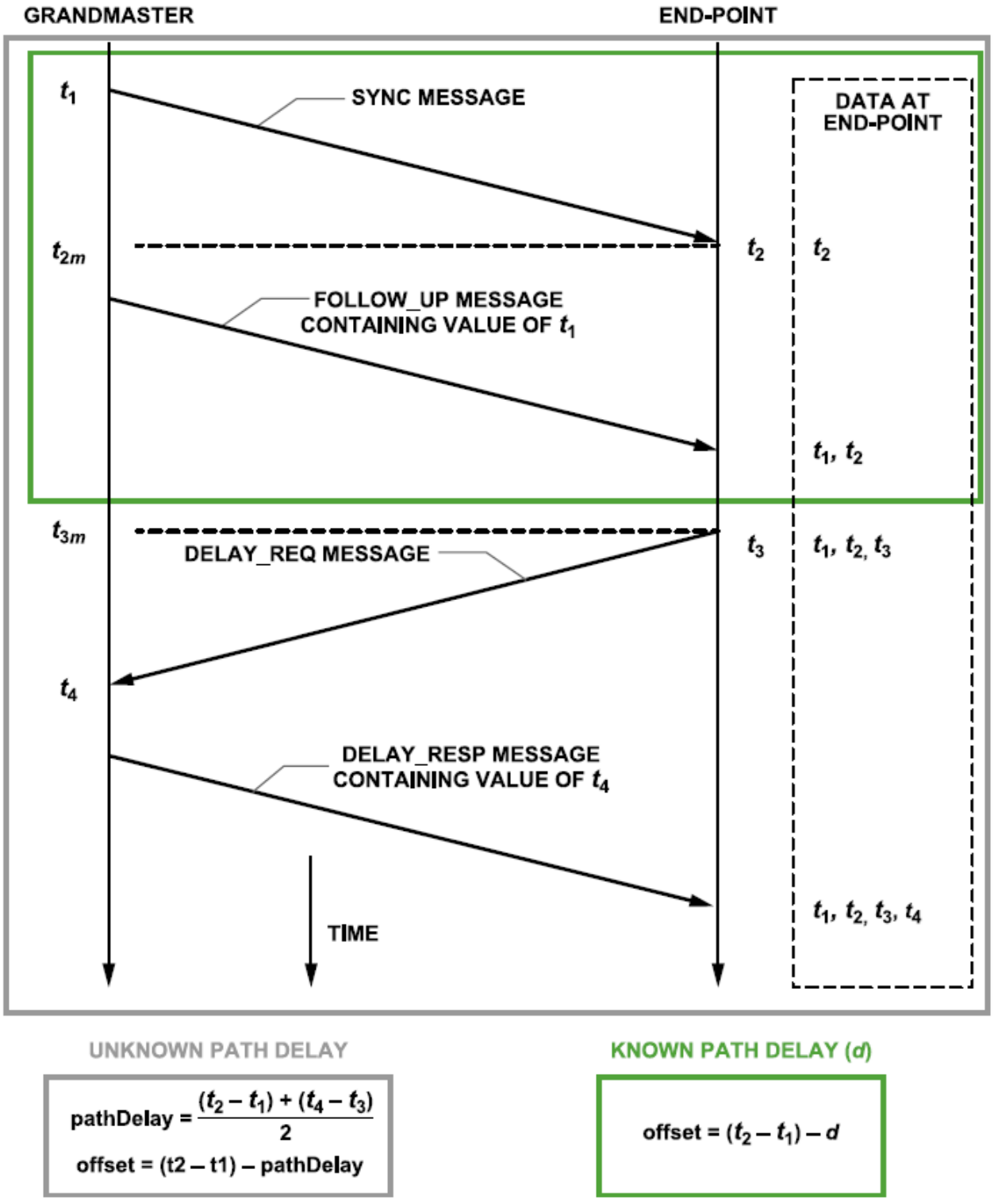

Figure 14. PTP Messages Exchange for Time Synchronization

TIME SYNCHRONIZATION

GPTP GRANDMASTER

The transceiver operating in an IEEE 802.1AS-2020 network can operate as a gPTP grandmaster and transmit sync and follow-up messages generated by the microcontroller software. The transceiver sends back the exact timestamp when the sync message was transmitted on the 10BASE-T1S bus. The hardware time-stamping is done in the PHY, therefore accounting for all variable factors, including the PLCA elastic buffer.

GPTP ENDPOINT

The transceiver operating in an 802.1AS network can operate as a gPTP endpoint and receive and process synchronization frames. The transceiver can behave as an 802.1AS target and lock to a grandmaster present on the network. Grandmaster redundancy is also supported, this enables locking to a back-up grandmaster.

The ADIN1140 continues waiting for the Follow_Up message corresponding to the earlier Sync. If a new Sync message is received while waiting for a Follow_Up message, the new Sync message is ignored until the timeout is triggered. The timeout is twice the Sync interval.

The ADIN1140 may take an extended time to lock (several seconds) if the gPTP grandmaster is reset and its gPTP time resets to a value significantly behind the gPTP time of the ADIN1140 device. To prevent this disable the initial frequency correction block after the device has initially locked to the gPTP grandmaster. To disable the initial frequency correction block, take the following steps:

1. Write value '0' to the IO_LV_GPTP_CONFIG.GPTP_RATE_RATIO_CALCULATION_ADJUST_PHASE
2. Write value '0' to the IO_LV_GPTP_CONFIG.GPTP_INITIAL_RATE_RATIO_CALCULATION

The gPTP block of the ADIN1140 does not check the values of the majorSdoID, minorSdoID, or versionPTP fields in received PTP messages. As a result, PTP messages with invalid values in these fields are not ignored.

The transceiver provides the following gPTP features.

- Internal free-running counter
- Syntonized counter

TIMESTAMP COUNTERS

The transceiver has two counters for timestamping, the internal free-running counter and the syntonized IEEE 1588 counter. The free-running counter is a 32-bit counter based on the local clock and increments in 10ns steps. The syntonized counter is the one which adjusts towards the gPTP time when gPTP messages are processed. The syntonized counter is a 64-bit counter in which the lower 32 bits represent nanoseconds with 1LSB = 1ns. When the lower 32 bits reach the value stored in MAC_TS_1SEC_CMP, these bits clear and the upper 32 bits increment, representing seconds.

The MAC_TS_CFG.TS_CAPT_FREE_CNT bit selects if the free-running counter or the syntonized counter is used for timestamping. Both counters share the same start and clear controls. The MAC_TS_CFG.TS_EN bit starts the counters, and the MAC_TS_CFG.TS_CLR bit resets the counters. The MAC_TS_NS_CNT and MAC_TS_SEC_CNT registers are used to write to the syntonized counter. These registers can be used to set an initial value. Sync and follow-up messages are used to synchronize the local syntonized counter time to gPTP time. The current time of the local counter is compared with the time received from the grandmaster, and the local counter is adjusted accordingly.

CAPTURING TIMESTAMPS OF RECEIVED FRAMES

When the counters are enabled using the MAC_TS_CFG.TS_EN bit and the MAC_CONFIG0.FTSE bit is set, the transceiver captures timestamps for all received frames. The MAC_CONFIG0.FTSS bit selects if timestamps are 32-bit or 64-bit. Only 64-bit timestamps are supported with the syntonized counter. The timestamp is appended before each data frame received as per the Open Alliance 10BASE-T1x MAC-PHY Serial Interface (TC6) standard. This time stamp can then be stored or discarded by software when reading the receive FIFO.

CAPTURING TIMESTAMPS OF TRANSMITTED FRAMES

The timestamps of transmitted frames are captured when requested. Timestamps are requested by setting the timestamp capture (TSC) field in the data header to a non-zero value. This instructs the transceiver to capture the timestamp of the transmitted frame into one of three sets of transmit timestamp capture registers. Table 9 describes the inputs to the TSC field and the associated registers the timestamp is captured in.

Table 9. Timestamp Capture (TSC) Bit Field

TSC Field	Action
00	No action

TIME SYNCHRONIZATION

Table 9. Timestamp Capture (TSC) Bit Field (Continued)

TSC Field	Action
01	Capture in the pair of MAC_TTSCAL and MAC_TTSCAH registers. The MAC_STATUS0.TTSCAA bit asserts when captured.
10	Capture in the pair of MAC_TTSCBL and MAC_TTSCBH registers. The MAC_STATUS0.TTSCAB bit asserts when captured.
11	Capture in the pair of MAC_TTSCCL and MAC_TTSCCH registers. The MAC_STATUS0.TTSCAC bit asserts when captured.

TS_CAPT

Asserting the TS_CAPT pin captures a timestamp of the syntonized counter and stores it in the MAC_TS_EXT_CAPT0 and MAC_TS_EXT_CAPT1 registers. Asserting the TS_CAPT pin also captures a timestamp of the free running counter and stores it in the MAC_TS_FREECNT_CAPT register.

TS_TIMER

The transceiver can generate an output signal (TS_TIMER) that uses two counters to generate repeating waveforms driven by the syntonized time. These two counters, MAC_TS_TIMER_HI and MAC_TS_TIMER_LO, specify the high and low period of the TS_TIMER signal and need to be programmed with multiples of 16 because the counters are effectively driven at 62.5MHz and increment in steps of 16ns.

Sometimes, the required period of TS_TIMER cannot be programmed as a multiple of 16. In such a case, the quantization error correction register (MAC_TS_TIMER_QE_CORR) is programmed with a value between 0 and 15 (0ns to 15ns) to compensate for the TS_TIMER quantization error. The quantization error correction field only reduces the low period. Therefore, if quantization error correction is enabled, the TS_TIMER high period is longer than the low period, if MAC_TS_TIMER_HI and MAC_TS_TIMER_LO are programmed with the same value. The average duty cycle in this case is greater than 50%.

For example, to achieve a TS_TIMER output period of 62 ns, MAC_TS_TIMER_HI and MAC_TS_TIMER_LO are programmed with 32 decimal. This results in a TS_TIMER period of 64ns. The MAC_TS_TIMER_QE_CORR field is then programmed with a value of 2. This reduces the low period by 2ns and results in a TS_TIMER output period of 62ns. The high period remains unchanged.

It is possible to specify a time with respect to the nanoseconds portion of the syntonized timer to start the generation of the TS_TIMER output. The MAC_TS_TIMER_START register is programmed with a value that is compared with the nanoseconds portion of the syntonized counter to generate a one-shot start. The sequence to enable the TS_TIMER output is as follows:

1. If required, change the default value of the TS_TIMER output from 0 to 1 by writing to the MAC_TS_CFG.TS_TIMER_DEF bits.
2. Write the values required for the high and low times for the TS_TIMER output to the MAC_TS_TIMER_HI and MAC_TS_TIMER_LO registers to achieve the nearest larger number than the desired period that is divisible by 16.
3. Write the value required for the quantization error correction to the MAC_TS_TIMER_QE_CORR register. MAC_TS_TIMER_QE_CORR = (MAC_TS_TIMER_HI + MAC_TS_TIMER_LO) – periodInNsec. Where periodInNsec is the desired period in nanoseconds.
4. Write a start time to the MAC_TS_TIMER_START register. When the nanoseconds part of the syntonized counter matches this value, TS_TIMER starts toggling.

The TS_TIMER output is stopped by writing 1 to the MAC_TS_CFG.TS_TIMER_STOP bits. When the TS_TIMER output is stopped, the output goes back to the default value specified in MAC_TS_CFG.TS_TIMER_DEF.

TS_TIMER GENERATION

The time synchronization block on ADIN1140 receives sync and follow-up messages from the grandmaster over the 10BASE-T1S link and processes them to achieve a lock to the grandmaster device. The offset correction between the grandmaster clock and the local device clock is applied to the nanoseconds and seconds counter. The rate correction is applied to the TS_ADDEND internal signal. The default value of the TS_ADDEND signal is 0xA0000000, which is 10ns, corresponding to the local clock period. This is the value in this register when the grandmaster device is not sending sync and follow-up messages, or when gPTP is disabled. If the grandmaster clock is running faster than the device local clock, it causes the TS_ADDEND value to be higher than 10ns. Similarly, if the grandmaster clock is running slower than the device local clock, it causes the TS_ADDEND value to be lower than 10ns.

The TS_ADDEND value is interpreted as shown Figure 15.

TIME SYNCHRONIZATION

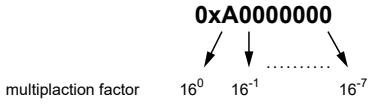

Figure 15. TS_ADDEND Value

As a first step, an enable signal is generated from the 100MHz clock, the duty cycle of which depends on the TS_ADDEND value, as shown in Figure 16. First, consider the default case of TS_ADDEND = 0xA0000000.

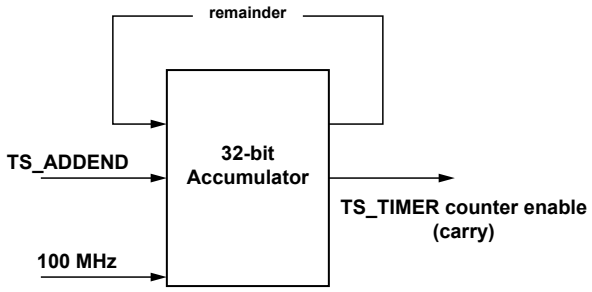

Figure 16. Enable Signal Based on TS_ADDEND

The carry signal for one cycle is as shown in Table 10.

Table 10. TS_ADDEND = 0xA000_0000

Remainder	Carry
A000_0000	0
4000_0000	1
E000_0000	0
8000_0000	1
2000_0000	1
C000_0000	0
6000_0000	1
0000_0000	1
A000_0000	(repeats)

Table 10 shows that the high period is 5/8 = 62.5%. Therefore, the TS_TIMER counter is enabled 62.5% of the time.

If the grandmaster clock is faster than the local device clock, this results in a higher value of TS_ADDEND as previously discussed, which causes the carry signal to be high for longer than shown in Table 10. Consider an example (not practical) of the grandmaster clock running at 1.125 times the local device clock. This results in TS_ADDEND = 0xA2000000.

The carry signal for a few periods for this case is shown in Table 11.

Table 11. TS_ADDEND = 0xA200_0000

Remainder	Carry
A200_0000	0
4400_0000	1
E600_0000	0
8800_0000	1
2A00_0000	1
CC00_0000	0
6E00_0000	1
1000_0000	1
B200_0000	0
5400_0000	1

TIME SYNCHRONIZATION

Table 11. TS_ADDEND = 0xA200_0000 (Continued)

Remainder	Carry
F600_0000	0
9800_0000	1
3A00_0000	1
DC00_0000	0
7E00_0000	1
2000_0000	1
C200_0000	0
6400_0000	1
0600_0000	1

The values in Table 11 show that the high period is 12/19 = 63.159%, which is 63.159/1.125 % = 56.14%. Therefore, the TS_TIMER counter is enabled 56.14% of the Grandmaster time, which averages to 62.5% (with respect to the grandmaster clock) over a longer duration.

As can be seen from the generation of this enable signal, the maximum theoretical jitter possible is 10ns in both the cases previously discussed.

The enable signal is used to generate the TS_TIMER output as shown in Figure 17.

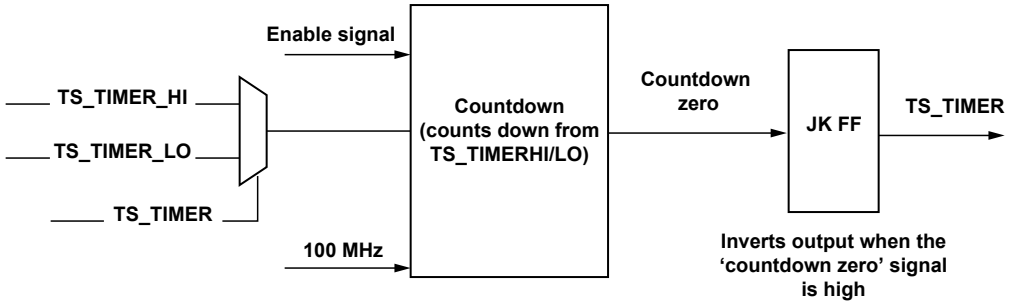

Figure 17. TS_TIMER Output

The lowest nibble for TS_TIMER_HI and TS_TIMER_LO is forced to 0 before it is fed into this block, which sets the restriction for always programming these two registers as multiples of 16, as the lower 4 bits are ignored.

The lowest common multiple between 16ns (62.5MHz) and 10ns (100MHz), which is 80ns gives the highest accuracy on the generated signal. The only contribution of jitter in this case is due to the local clock period. For all other values (multiples of 16ns, but not multiples of 80ns), an additional 10ns is introduced, as previously discussed.

The case when QE_CORR is not equal to 0 is shown in Figure 18:

TIME SYNCHRONIZATION

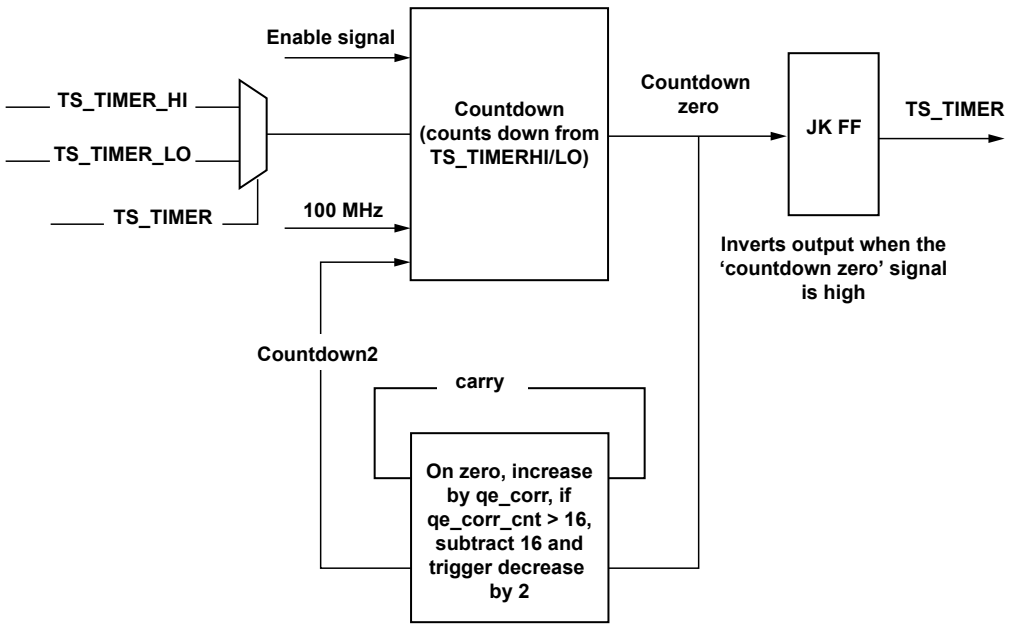

Figure 18. QE_CORR Not Equal to 0

When the countdown 2 value reaches 0, the countdown is done by 2 and an additional 10ns of jitter is introduced.

The TS_TIMER jitter specifications for the different cases discussed are located in the product specific data sheet.

ADDITIONAL TIME SYNCHRONIZATION FEATURES

The gPTP engine has the following features:

- Statistics counters for gPTP event tracking
- User settable MeanLinkDelay
- Supports grandmaster redundancy

The statistics counters provided for gPTP event tracking are listed in Table 12. The mean link delay is the measured propagation delay on the link attached to the port relative to the Local- Clock entity at the other end of the link. This delay is accounted for by writing to the IO_LV_GPTP_MEAN_LINK_DELAY register for the lower 16-bits and the IO_LV_GPTP_MEAN_LINK_DELAY_1 register for the upper 16-bits of the delay value. The mean link delay is expressed in nanoseconds. For example for a setting of 0x0000 000A, the mean link delay is 10ns.

The IO_LV_GPTP_STATUS_1.GPTP_LOCKED flag indicates whether the error of the locally synchronized timer relative to the time indicated within the sync and follow-up messages is within the lock threshold. The lock threshold has a default value of 1.1µs and is configured using the IO_LV_GPTP_LOCK_THRESHOLD.GPTP_LOCK_THRESHOLD field. Changing the lock threshold only impacts the locked status flag. It does not effect the core gPTP algorithm.

The transceiver implements grandmaster redundancy. The core always tries to lock to the main grandmaster domain, if available. After the first sync timeout, it tries to lock to a secondary backup domain and continues using the secondary domain until the main domain is available. Refer to the IO_LV_GPTP_DOMAINS register for configuring the gPTP active domain and gPTP backup domain. The bit indicates which domain the core is using for synchronization.

Table 12. gPTP Event Tracking Statistics Counters

Register	Description
gPTP Time Error and Time Error 1 Registers	802.1AS time synchronization error measured in nanoseconds. For example, a value of 0x0000 000A means a time sync error of 10ns. This indicates the time error between the local clock and the grandmaster clock for the last received sync and follow-up pair. The IO_LV_GPTP_TIME_ERROR register stores the lower 16 bits and the IO_LV_GPTP_TIME_ERROR_1 register stores the upper 16 bits.

TIME SYNCHRONIZATION

Table 12. gPTP Event Tracking Statistics Counters (Continued)

Register	Description
gPTP Sync Count and Sync Count 1 Registers	802.1AS received sync message count. The IO_LV_GPTP_SYNC_COUNT register stores the lower 16 bits and the IO_LV_GPTP_SYNC_COUNT_1 register stores the upper 16 bits.
gPTP Onestep Count and Onestep Count 1 Registers	802.1AS received one step sync message count. The IO_LV_GPTP_ONESTEP_COUNT register stores the lower 16 bits and the IO_LV_GPTP_ONESTEP_COUNT_1 register stores the upper 16 bits.
gPTP Followup Count and Followup Count 1 Registers	802.1AS received followup message count. The IO_LV_GPTP_FOLLOWUP_COUNT register stores the lower 16 bits and the IO_LV_GPTP_FOLLOWUP_COUNT_1 register stores the upper 16 bits.
gPTP Number Locks Register	Counts the number of times IO_LV_GPTP_STATUS_1.GPTP_LOCKED status changed from unlocked to locked.
gPTP Number Unlocks Register	Counts the number of times IO_LV_GPTP_STATUS_1.GPTP_LOCKED status changed from locked to unlocked.
gPTP Sequence ID Register	Stores the Sequence ID at which the IO_LV_GPTP_SEQUENCEID.GPTP_RX_STATUS_CHANGE_SEQUENCE_ID status changed last. This can either correspond to a change from locked to unlocked or from unlocked to locked.
gPTP Mean Link Delay and Mean Link De- lay 1 Registers	User settable mean link delay time in nanoseconds of the gPTP algorithm. For example set- ting 0x0000 000A the mean link delay is 10 ns. The IO_LV_GPTP_MEAN_LINK_DELAY register stores the lower 16 bits and the IO_LV_GPTP_MEAN_LINK_DELAY_1 register stores the upper 16 bits.
gPTP Status 1 Register	The IO_LV_GPTP_STATUS_1.GPTP_LOCKED bit is set if the gPTP algorithm is locked. 0 = gPTP unlocked 1 = gPTP locked
gPTP Status 1 Register	The bit indicates whether the core is using the backup domain for synchronization. 0 = Currently synchronized to the active domain. 1 = Currently synchronized to the backup domain.

EVENT MANAGEMENT

The transceiver manages various interrupt events related to the operation of the device using the transaction interrupt controller (TIC). The TIC monitors the state of various input signals from other blocks and generates interrupts based on changes to those input signals. These events are flagged through the OA-SPI interface. Additionally, the safe state controller, the PHY, and the MAC support various error management tasks and diagnostics.

For more information, see the Safe State Controller (SSC)section and the System Debug and Diagnostics section.

TRANSACTION INTERRUPT CONTROLLER (TIC)

The transaction interrupt controller supports the following features:

- Configurable number of interrupts.
- Configurable sensitivity. Interrupts can be sensitive to low level, high level, rising edge, and falling edge of the input signal.
- Two output debug ports that can mux to any input signal and any interrupt sensitivity state.
- Interrupt resend functionality.

When an enabled sensitivity on an input signal is detected, the corresponding state for that sensitivity is set to true. The state can only be switched to false by employing the clear signal associated with that sensitivity or by using the clear_all input signals. To clear all sensitivity states, consult the IO_LV_TIC_CONTROL1.TIC_CLEAR_ALL register. For clearing specific interrupts, use registers with the TIC_CLEAR prefix.

The ADIN1140 supports triggering an assertion of the IRQ OA-SPI pin if an interrupt is detected in the TIC. This is enabled by the following steps:

1. Clear (= 0) the IO_LV_TIC_CONTROL1.TIC_OASPI_INT_DISABLE bit.
2. Clear (= 0) the MAC_IMASK1.VS_INT_MASK bit.

The MAC_STATUS1.VS_INT bit indicates an interrupt flag triggered in the TIC. Refer to the OA-SPI Interrupts section for more information.

The transaction interrupt controller supports a range of input signals related to:

- Sleep/Wake
- MAC
- PHY
- gPTP
- Bootloader
- SQI
- SSC

The complete list of available interrupt inputs are described in the *IO_LV Registers* section.

To enable an interrupt input signal, write the corresponding bit position in the appropriate TIC enable register (for example IO_LV_TIC_ENABLE_8_PHY_REG0). The status of an interrupt is retained in the respective bit position of the relevant TIC status register (for example IO_LV_TIC_STATUS_FLAGS_8_AND_9).

OA-SPI INTERRUPTS

The $\overline{\text{IRQ}}$ pin of the OA-SPI interface is asserted when any of the following internal assertion conditions are met and deasserted when all the following internal deassertion conditions are met (logical OR).

- RCA – Receive Chunks Available.

  Asserted. The MAC-PHY detects $\overline{\text{CS}}$ deactivated and the previous data footer had no receive data chunks available (RCA = 0). The $\overline{\text{IRQ}}$ pin is asserted when receive data chunks become available for reading while $\overline{\text{CS}}$ is deactivated.

  Deasserted. On reception of the first data header following $\overline{\text{CS}}$ being activated.

- TXC – Transmit Chunk Credits Available.

  Asserted. The MAC-PHY detects $\overline{\text{CS}}$ deactivated and the previous data footer indicated less than MAC_CONFIG0.TXCTHRESH of transmit credits available. The $\overline{\text{IRQ}}$ pin is asserted when transmit credits become available while $\overline{\text{CS}}$ is deactivated. The minimum number of transmit

EVENT MANAGEMENT

credits that must be available before asserting $\overline{IRQ}$ is configured by the MAC_CONFIG0.TXCTHRESH bit field. The default value is TXC ≥ 1 credit (MAC_CONFIG0.TXCTHRESH set to 0x00).

Deasserted. On reception of the first data header following $\overline{CS}$ being activated.

- EXST – Extended Status Event (see Table 6).

  Asserted. The MAC-PHY detects $\overline{CS}$ deactivated and the previous data footer had no extended status assertion (EXST = 0). The $\overline{IRQ}$ pin is asserted when an event occurs that causes the extended status bit to become set while $\overline{CS}$ is deactivated. The extended status bit is set at any time a bit in the MAC_STATUS0 or MAC_STATUS1 registers, respectively, has been set that has not been masked by the MAC_IMASK0 or MAC_IMASK1 registers.

  Deasserted. On reception of the first data header following $\overline{CS}$ being activated.

In ADIN1140, the OASPI IRQn signal comes from a registered version of the logical OR combination of the three trigger signals. This means that the IRQn signal is asserted one clock cycle after any of the trigger signals are asserted. If this occurs right before CSn is asserted, the IRQn signal will be asserted when the CSn signal is active. This behavior does not affect the detection or servicing of interrupt conditions by the host.

Table 13 and Table 14 describe the interrupt conditions available in the MAC_STATUS0 and MAC_STATUS1 registers.

Detecting an assertion of $\overline{IRQ}$ from the MAC-PHY is handled by the SPI Host as per *OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface 1.1, section 7.7 IRQ Generation and Handling*.

Table 13. MAC_STATUS0 Interrupts

Bit Name	Description
CDPE	Control Data Protection Error. When control data read/write protection is enabled this bit indicates that the MAC-PHY detected an error in protected control write data received from the host. When control data read/ write protection is disabled, this bit is reserved with a read-only value of zero, as no errors are detected.
TXFCSE	Transmit Frame Check Sequence Error. This bit indicates that a frame was received over SPI from the host with an invalid FCS appended. The frame is still forwarded from the device as the FCS is checked as the frame is being transmitted.
TTSCAC	Transmit Timestamp Capture Available C.
TTSCAB	Transmit Timestamp Capture Available B.
TTSCAA	Transmit Timestamp Capture Available A.
PHYINT	PHY interrupt. This interrupt is tied to the PHY SQI block. This bit is asserted when the SQI level drops below the programmable thresholds.
RESETC	Reset Complete. This bit is set when the MAC-PHY reset is complete and ready for configuration. When it is set, it generates a nonmaskable interrupt assertion on $\overline{IRQ}$ to alert the SPI host. Additionally, the setting of the MAC_STATUS0.RESETC bit shall also set EXST = 1 in the first RX footer, or until this bit is cleared by the action of the SPI host writing a one.
HDRE	Header Error. When set, this bit indicates that the MAC-PHY has detected an invalid header received from the SPI host. The invalid header is due to a parity check error.
LOFE	Loss of Frame Error. When set, this bit indicates that the MAC-PHY has detected an early deassertion of $\overline{CS}$ prior to the expected end of a data chunk or command control transaction.
RXBOE	Receive Buffer Overflow Error. When set, this bit indicates that the receive buffer (from the network) has overflowed and receive frame data was lost.
TXBUE	Host Tx FIFO Underrun Error. This error can only assert when cut-through from the host is enabled. The host software should ensure this bit never asserts by writing frame data to the MAC at a rate greater than 10Mbps. If an underrun error occurs, transmission of the current packet is stopped. A full MAC reset is required to clear this error.
TXBOE	Host Tx FIFO Overflow. The host software should ensure this bit never asserts itself by checking the space available in the Tx FIFO before writing to the Tx FIFO. If using the Open Alliance SPI Data protocol, then the space in the Tx FIFO is indicated in the TXC field of the Rx footer. If the host Tx FIFO overflows, then the frame being written is dumped and the software may choose to re- send the entire frame. Writes to the FIFO commence at the next SOF. There is always room for more than one frame in the host Tx FIFO as it is 4k bytes (or greater) in size there- fore a frame currently being transmitted is not be interrupted by an overflow on the write side of the FIFO.
TXPE	Transmit Protocol Error. When set, this bit indicates that a Tx data chunk protocol error has occurred. Data chunk received with DV = 1 but without a prior SV = 1. Data chunk received with SV = 1 but with no EV = 1 (repeated SV = 1 received).

Table 14. MAC_STATUS1 Interrupts

Bit Name	Description
RD_ACC_ERR	Read Access Error. Memory read access error. May assert if the SPI frequency is higher than the specified value for the SPI protocol.

EVENT MANAGEMENT

Table 14. MAC_STATUS1 Interrupts (Continued)

Bit Name	Description
TX_ECC_ERR	ECC Error on Reading the Frame Size from a Tx FIFO. An uncorrectable ECC error was detected on a read of the size field from the Tx FIFO. The FIFO is automatically cleared and the frame associated with the ECC error and any other frames in the Tx FIFO are lost/dropped.
RX_ECC_ERR	ECC Error on Reading the Frame Size from an Rx FIFO. An uncorrectable ECC error was detected on a reading the frame size field from an Rx FIFO. The FIFO is automatically cleared and the frame associated with the ECC error and other frames in the Rx FIFO are lost/dropped.
MAX_RR_ERR	Transmit Max Collision Retry Reached.
RX_IFG_ERR	Rx MAC Inter Frame Gap Error. If the IFG is too short then the frame is dropped on receive. The threshold used for measuring the IFG on receive is set in the RX_IFG register.
VS_INT	Transaction Interrupt Controller Interrupt. Indicates that an interrupt flag triggered in the transaction interrupt controller
RX_RDY	Rx FIFO Contains Data. In store and forward this field indicates that there is 1 or more frames in the Rx FIFO.

If a Transaction Interrupt Controller (TIC) interrupt is detected (MAC_STATUS1.VS_INT = 1), the TIC interrupts must be cleared by setting the IO_LV_TIC_CONTROL1.TIC_CLEAR_ALL bit.

The MAC_IMASK0 and MAC_IMASK1 registers allow MACPHY interrupts that are generated in the MAC_STATUS0 and MAC_STATUS1 register to be masked.

SAFE STATE CONTROLLER (SSC)

The safe state controller (SSC) is a block that monitors fault detection mechanisms and place the device into a defined state if fault conditions are detected. This ensures that the transceiver device enters a defined state in the event of a local fault.

The SSC has two modes of operation:

1. Functional Mode – The transceiver is operating as normal with the SSC monitoring the fault detection mechanisms.
2. Safe State Mode – The transceiver halts normal operation and enters a defined state.

Note that, the SSC block was developed as a QM part, as defined in ISO 26262-1:2018, therefore no safety requirements were managed according to this standard.

SAFE STATE MODE

Safe state mode places the transceiver in a safely defined mode of operation in the event of a fault condition. Safe state mode is considered an emergency situation and the automated safety actions are applied immediately. This can disturb functional mode operations that are in progress.

The transceiver maintains the 10BASE-T1S network access in safe state mode, provided no detected safety fault would degrade the 10BASE-T1S network. This enables safety faults to be read and resolved over the 10BASE-T1S network. A 32-bit status register is available that provides the live status of all available fault detection events. This allows the system software to monitor all currently active fault conditions. The SSC also stores an index value that identifies the earliest fault detection mechanism that triggered entry to safe state mode. When in safe state mode, the transceiver can configure the SAIF interfaces into a benign state or set output pin levels to control external devices. The configurable parameters are pin direction, pin value, and pull-up/pull-down. There are six different pad configurations (outside of No change-keep functional mode configuration) that are selectable for each SAIF pin:

1. Disable input and output. Three-state.
2. Enable input and output. Drive 0 (low).
3. Enable input and output. Drive 1 (high).
4. Enable input, disable output. Regular input mode.
5. Enable input, disable output. Pull-down enabled.
6. Enable input, disable output. Pull-up enabled.

The SSC stores the SSC status flag (functional mode or safe state mode) and the fault detection status in the always- on register map. This ensures that SSC data is not lost during any sleep event. This status information is kept up to date at all times in functional mode or safe state mode, in preparation for any unexpected entry to sleep mode (for example VBAT drop).

When returning from a sleep/PoR event, the SSC retrieves the status information from the always-on register map. The transceiver correctly boots into safe state mode or functional mode depending on the SSC status flag.

Entry Into Safe State Mode

Table 15 lists the safety fault detection mechanisms available to trigger entry into safe state mode. Each fault detection mechanism is enabled or disabled individually (see the Configuring the Safe State Controller section). The SSC monitors the enabled fault detection mechanisms when in functional mode. While in safe mode the SSC continues to monitor the fault detection mechanisms. This is used for the auto_return_to_functional_mode feature and to trigger the ssc_unsuccessful_return_func interrupt.

Table 15. Fault Detection Mechanisms – Safe State Mode Entry

Fault Detection Mechanism	Description
Manual	The SSC supports manual entry into safe state mode using a register write. The IO_LV_SSC_MONITOR_TRIGGERS.SSC_MANUAL_ENTER_SAFE_MODE bit is accessed locally, or over the 10BASE-T1S network.
gPTP Unlocked	The gPTP lock status is monitored by the SSC to trigger entry to safe state mode when the gPTP target is unlocked.
Ethernet Frame Timeout	Ethernet traffic is monitored by the SSC to trigger entry to safe state mode when no Ethernet frames have been received within a user programmed time window. The timer is a 16-bit counter with a counter interval of 81.92µs. Max timeout = 5.368sec.
Device Unattended Timeout	The SSC has an Alive bit (self-clearing) that is used by the SSC to monitor if the device is left unattended. The system software must periodically set this bit before a user programmed timeout is reached to prevent the device from entering safe state mode. Setting the bit restarts the timer. The timer is a 16-bit counter with a counter interval of 81.92µs. Max timeout = 5.368sec.

SAFE STATE CONTROLLER (SSC)

Table 15. Fault Detection Mechanisms – Safe State Mode Entry (Continued)

Fault Detection Mechanism	Description
SQI Degradation	The received signal quality indicator (SQI) level is used to trigger entry to safe state mode if it transitions below a user programmed threshold.
OTP Configuration Error	The SSC can trigger entry to safe state mode if any ECC errors are detected in the OTP memory.

Exit From Safe State Mode

Safe state mode can be exited manually or automatically.

Manual exit includes:

- System software can read the SSC status flags for the fault detection mechanisms and choose to manually exit safe state mode using a register write, if all fault conditions are resolved. If all faults are not resolved, an interrupt may be triggered when attempting to exit safe mode.

Automatic exit includes:

- Automatic exit from safe sate mode is a configurable option for many fault detection mechanisms. However, not all fault detection mechanisms support automatic exit.
- If selected, the SSC can automatically exit safe state mode if all automatic exit enabled SSC fault detection mechanisms are resolved and there are no other faults detected.

Table 16 details the exit mode available for each safety fault detection mechanism. Upon exiting safe state mode, if any entry condition is active or becomes active, a new entry to safe state mode will be triggered.

Table 16. Fault Detection Mechanisms — Safe State Mode Exit

Fault Detection Mechanism	Description
Manual	Manual exit required.
gPTP Unlocked	Supports automatic exit. The SSC monitors the gPTP target lock status and exit safe state mode when the gPTP target regains lock.
Ethernet Frame Timeout	Supports automatic exit. The SSC monitors incoming Ethernet traffic and exit the safe state if valid Ethernet frames are detected.
Device Unattended Timeout	Manual exit required.
SQI Degradation	Manual exit required.
OTP Configuration Error	Manual exit required.

CONFIGURING THE SAFE STATE CONTROLLER

The IO_LV_SSC_SAFE_CHECKS_ENABLE and IO_LV_SSC_SAFE_CHECKS_ENABLE_2 registers are used to enable/disable the monitoring of each of the fault detection mechanisms and enable/disable the timeout counters for the Ethernet frame timeout and the device unattended timeout mechanisms.

The IO_LV_SSC_MONITOR_TRIGGERS register has the controls for manually entering safe state mode.

The IO_LV_SSC_CONTROLS register has controls for the following:

- Manually returning to functional mode if all fault conditions are resolved.
- Setting the SQI level which triggers safe state mode if monitoring that fault detection mechanism is enabled.
- Setting whether each SAIF pin keeps its functional mode configuration, or if it switches to a safe state configuration when in safe state mode.
- Enable/disable monitoring of PLCA BEACON as part of Ethernet timeout check.

The IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN and IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN2 registers allow programs to enable/disable the auto re- turn to functional mode feature for fault detection mechanism where this is supported.

The IO_LV_SSC_TIMEOUT_0_TIME and IO_LV_SSC_TIMEOUT_1_TIME allow the 'Ethernet frame time- out' and 'device unattended timeout' counter values to be configured respectively.

SAFE STATE CONTROLLER (SSC)

The IO_LV_SSC_MONITOR_POLARITY and IO_LV_SSC_MONITOR_POLARITY_2 registers are used to configure the polarity that triggers entry to safe state mode for each fault detection mechanism.

IO_LV_SSC_SAFE_SA_IF_CONTROLS, IO_LV_SSC_SAFE_SA_IF_CONTROLS_2, and IO_LV_SSC_SAFE_SA_IF_CONTROLS_3 registers contain the safe state configuration settings for the SAIF pins when in safe state mode.

The IO_LV_SSC_ALIVE_COUNTER_RB register is a readback for the SSC alive counter value. An alive counter is a counter that is incremented while the device is in functional mode. The counter width is 14 bits and it makes a count every 81.92us, having a roll-over time of 1.35 seconds. The purpose of this feature is to have the local microcontroller periodically read this counter value over the OA-SPI interface. This value determines whether an issue has appeared in the MAC-PHY.

The IO_LV_SSC_GENERAL_RB register provides SSC status messages such as the current device mode, if the mode is changing, and if there has been an unsuccessful return to functional mode due to unresolved fault detection mechanisms.

The IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB and IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB_2 registers provide status messages that indicate the state of the monitored fault detection mechanisms when entering safe state mode. There are also sticky versions of these registers which are only cleared when read.

The IO_LV_SSC_MUX_SEL_SAFE_ACTIVE_RB register indicates which SAIF pins have the safe state configuration enabled.

The IO_LV_SSC_MISC register provides a control for clearing all ‘sticky’ readbacks and the device unattended check bit. This bit should be periodically written to 1’b1 if that fault detection mechanism is enabled.

The IO_LV_SSC_RECOVERED_DATA_FROM_AO register contains the SSC data that is stored in the always-on memory.

BOOTING

The ADIN1140 device contains One Time Programmable (OTP) memory to store factory programmed data. The OTP memory on the ADIN1140 is locked and cannot be programmed by the user.

OTP STRUCTURE

The OTP memory is divided into blocks that are used by the bootloader during device initialization. Each OTP block is defined as a 16-byte block of data protected by one single error correction, double error detection (SECDED) code. The content of OTP is 16-bit addressable at a specified 16-bit address range. Each OTP memory block is protected with SECDED using hamming codes and with a checksum. To guard against errors in OTP data, every word (16-bits) is written into a duplicate location; complementary data for the same is written into two other locations. The bootloader uses the differential redundant (DIFF-RED) read mode to read OTP data.

The bootloader routine runs once the device comes out of reset. It goes through the contents of OTP, checks the integrity of each data block and programs the target registers where initial configuration of the device is set by the bootloader using OTP data.

BOOTLOADER

After reset, the bootloader initializes the device using ADI factory-programmed data stored in on-chip OTP memory. This data is copied into the appropriate internal registers, including ALWAYS_ON configuration and status information required for normal device operation.

Once initialization is complete, the bootloader sets an internal bootloader done flag and exits. The ADIN1140's boot time is approximately 3.286ms.

OTP BLOCK BOOTLOADER STATUS

Each OTP block is described with a 2-bit value by the bootloader, as follows:

- Not initialized = 00b
- Valid = 01b or 10b
- Corrupted = 11b

RESET

The transceiver has no input reset pin. The following chip resets are supported:

- Hardware Reset: Power-on Reset (PoR)
- Software Resets
  - LV Die Resets
  - HV Die Resets
  - Block Reset Control

All these resets put the respective blocks of the transceiver into a known state. Whenever the MAC is reset, the SDI pin is pulled down and the TS_TIMER pin is driven to a low state.

HARDWARE RESET: POWER-ON RESET

The transceiver includes HV and LV die power monitoring circuitry to monitor all of the power supplies. The HV die PoR monitors AVDD while the LV die PoR monitors DVDD and controls the reset. There is also a LVDD PoR on the LV die that is used to enable the 3.3V LV circuitry. During power-up, the transceiver is held in hardware reset until each of the supplies has crossed its minimum rising threshold value and the power is considered good.

The PoR modules include overvoltage (OV) and undervoltage (UV) protection by monitoring the supplies to detect if one or more of the supplies rises above or falls below a threshold value. If a threshold is reached, the device goes into lockout mode until the voltage returns within the threshold limits. The voltage monitoring block is designed to work with 12V battery supply only. The thresholds for OV and UV are configurable.

The undervoltage event is divided into undervoltage (UV) and deep undervoltage (DUV). When falling below UV threshold for more than 500ms, the device transitions into lockout mode. When falling below the DUV threshold, the device transitions into lockout mode immediately. Exit from lockout mode is performed when the VBAT voltage returns within the threshold limits. See the data sheet for the a description of the operating modes.

Note that, thresholds are configured using the ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_OV_THRESHOLD and ALWAYS_ON_CONFIGURATION_FIELDS_0.CFG_DUV_THRESHOLD bits.

Thresholds are enabled using the ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VBAT_OV_FLAG_EN, ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VBAT_UV_FLAG_EN and ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VBAT_DEEP_UV_FLAG_EN bits.

These settings are selected for 12V battery systems only.

Note that when the reference clock is disabled while in normal operating mode, the device must be power cycled or put in and out of sleep mode.

To avoid register map corruption when configuring the VBAT thresholds while VBAT is outside the configured DUV/OV range, disable Sleep mode before enabling or modifying the VBAT thresholds, then re-enable Sleep mode after the configuration is complete. Sleep mode is controlled by the most significant bit (MSB) of register address 0xB706 in the ALWAYS_ON register map (1 = Sleep mode disabled, 0 = Sleep mode enabled).

SOFTWARE RESET

A MAC-PHY software reset is initiated using the MAC_RESET.SWRESET bit. Writing a 1 to this bit fully resets the MAC-PHY including the integrated PHY, to an initial state including but not limited to resetting all state machines and registers to their default value. When this bit is set, the reset shall not occur until the $\overline{CS}$ signal is deasserted to allow the control command write to complete. $\overline{CS}$ must be held deasserted for at least 100ns for the reset to take effect. All blocks complete their reset cycle within 1µs of the software reset register write. This bit is self-clearing.

The transceiver can be reset via software using following sequence:

1. Issue a HV die reset followed by LV die reset on the transceiver. No delay is required between the two resets through the network to reset the complete chip (except the always-on register map) to its initial state.
2. After the LV die reset, wait for the IO_LV_BOOTLOADER_STATUS_7.BOOTLOAD_DONE bit to set (= 1) before re-configuring the node.

The reset for ADIN1140 devices can be issued over OA-SPI directly from the host. The OA-SPI core is reset before the transaction is completed, so the MAC_STATUS0.LOFE bit is set. The MAC_STATUS0.RESETC bit can also be seen set to indicate that the reset has occurred.

RESET

The reset sequence that follows resets the transceiver device except for the Always On register map:

1. Perform the HV die reset by writing 0xA55A to the IO_HV_RESET_CONTROL register (address = 0xB1FF, MMS = 0xA).
2. Perform the LV Die reset by writing 0xA55A to the IO_LV_RESET_CONTROL register (address = 0xC8FF, MMS = 0xA).
3. Read the MAC_STATUS0.RESETC bit to verify that the reset has completed (= 1).

   Note that the MAC_STATUS0.LOFE bit can also be seen as set in the MAC_STATUS0 register due to the LV die reset occurring immediately before completion of the on-going SPI transaction.
4. Clear (= 0) both MAC_STATUS0.RESETC and MAC_STATUS0.LOFE frame bits.
5. Poll for the IO_LV_BOOTLOADER_STATUS_7.BOOTLOAD_DONE bit = 1 or wait for 3.286ms)
6. Reconfigure the nodes.

   Note that the OA-SPI core is reset immediately after seeing the reset command, even before completion of the on-going SPI transaction, as shown in Figure 19. The device loses the control of the $\overline{CS}$ pin, causing a glitch on the chip-select path. This glitch can trigger the LOFE error.

When the ADI OA-SPI stack is used, this causes an ADI_OASPI_ERR_REG_WRITE_FAILED error in the software. This is because the host software is expecting the same bytes written echoed on its SDI line from the MAC- PHY. However, due to the reset, the 4th word on SDI is different.

Refer to the OA-SPI TC6 spec 1.1 for more details.

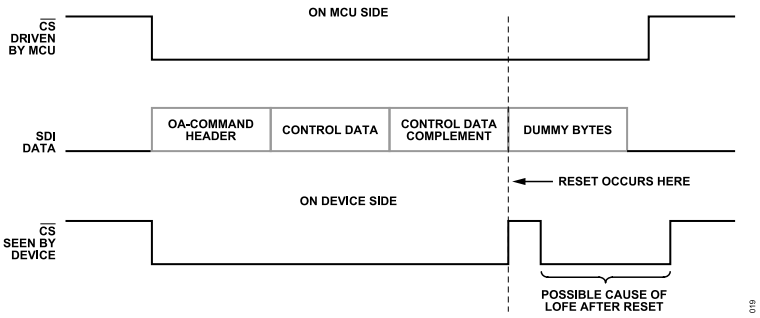

Figure 19. Reason for the LOFE (Loss of Frame Error)

LV Die Reset

A soft reset of the LV Die is initiated by writing 0xA55A to the LV Die IO_LV_RESET_CONTROL register. This resets the LV die clock domains, PHY, MAC, and LV Die register map (IO_MAP_LV).

- IO_LV_RESET_CONTROL.RESET: Main soft reset LV die
- IO_LV_BLOCK_RESET_CONTROL: Various system resets
- IO_LV_BLOCK_RESET_CONTROL.MAC_PHY_SOFT_RESET: Same function as MAC_RESET.SWRESET
- Wake/sleep controller reset
- Bootloader reset

RESET

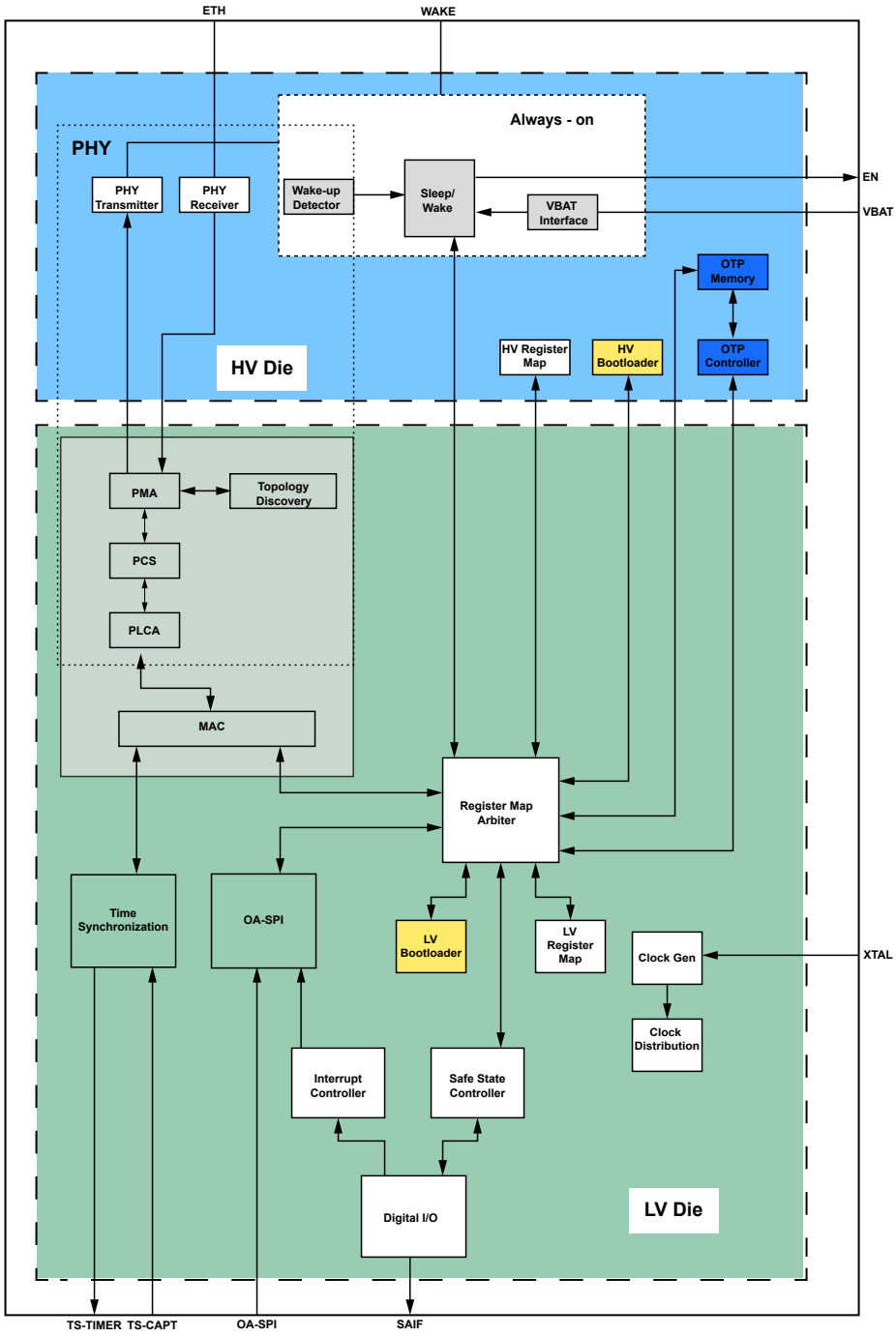

Figure 20. LV and HV Die Reset Domains

Note that, a LV die RESET resets the OA-SPI core and results in a LOFE (loss of frame error).

HV Die Reset

A soft reset of the HV die is initiated by writing 0xA55A to the HV die IO_HV_REVISION_CONTROL register. This resets the oscillator clock, communication clock and functional clock domains (IO_MAP_HV). See Figure 20.

Note that all HV die registers need to be read back twice to get the correct value.

RESET

LV Die Block Reset Control

The MAC-PHY block, wake sleep controller block, and the LV die bootloader block are independently reset using the LV Die IO_LV_BLOCK_RESET_CONTROL register.

MAC-PHY Reset

The MAC-PHY subsystem is reset by setting the IO_LV_BLOCK_RESET_CONTROL.MAC_PHY_SOFT_RESET bit to 1. This bit is self-clearing.

Wake-Sleep Controller Reset

The wake-sleep controller is reset by setting the IO_LV_BLOCK_RESET_CONTROL.WAKE_SLEEP_SOFT_RESET bit to 1. This bit is self-clearing.

Bootloader Reset

The LV die bootloader block is reset by setting the IO_LV_BLOCK_RESET_CONTROL.BOOT_LOADER_SOFT_RESET bit to 1. A reset to the LV die bootloader triggers a reboot of the LV die bootloader contents only. This is a self-clearing bit.

HV Die Block Reset Control

The HV die Bootloader block and the OTP block are reset using the HV die IO_HV_BLOCK_RESET_CONTROL register.

The IO_HV_BLOCK_RESET_CONTROL.CLR_STANDBY_STATUS bit can also be used to clear the readback of a previous detection of the WUD or Wake pin begin active (for example receive during standby). This can be done by setting this bit to 1.

Bootloader Reset

The HV die bootloader block is reset by setting the IO_HV_BLOCK_RESET_CONTROL.BOOT_LOADER_SOFT_RESET bit to 1. A reset to the HV die bootloader triggers a reboot of the HV die bootloader contents only. This is a self-clearing bit.

OTP Reset

The OTP controller is reset by setting the IO_HV_BLOCK_RESET_CONTROL.OTP_SOFT_RESET bit to 1. This is a self-clearing bit.

MAC-PHY Software Reset

The MAC_RESET.SWRESET bit completely resets the MACPHY, including the integrated PHY logic in the LV Die, to an initial state. This includes, but is not limited to, resetting all state machines and registers to their default value.

OPEN ALLIANCE TC14 SUPPORTED FEATURES OVERVIEW

The transceiver complies with OPEN Alliance TC14 specifications which define the interoperability, compliance, and EMC requirements for 10BASE-T1S PHYs. This adherence allows the transceiver to be compatible with 10BASE-T1S products developed by other semiconductor manufacturers. This user guide section covers three specific areas of the TC14 requirements: Sleep/Wake-up, topology discovery, and system implementation specifications.

SLEEP/WAKE-UP

The TC14 Sleep/Wake-up specification outlines the requirements for 10BASE-T1S PHYs to support a controlled node shutdown and fast global wake-up within the Ethernet network. It defines a Power Management (PM) client and the primitives that a PHY must provide to control the low power functionality.

In the context of this specification the term *Sleep* indicates entry to a low power state and the term *Wake-up* indicates the exit from a low power state. Sleep/Wake-up is defined at the physical layer. Higher layers can shut down nodes through the power management client to realize partial networking, where selected parts of a network are inactive. Partial networking allows the flow of normal traffic between active nodes, while sleeping nodes are connected to the same bus. The sleeping nodes are unaffected by normal traffic and are only awakened by a specific wake-up signal on the network. This wake-up signal is communicated through the network via a Wake-Up Pulse (WUP) which can be sent over the line by any node PHY or switch PHY to distribute a wake-up request over a link segment.

Wake-Up Electrical Interface

The TC14 Sleep/Wake-up specification specifies an IO interface for sleep/wake-up control. It is a requirement to have a local wake input pin on head nodes to allow an external device to trigger wake-up. Additionally, PHYs are required to have an always-on supply that is available during low-power state, and it is recommended to have an enable/inhibit pin to shut down an external regulator during sleep. The transceiver meets these requirements and the relevant device pins are listed in Table 17.

Table 17. Wake-Up Related Device Pins

Pin Name	Pin Type	Description
EN	Digital Output	Active high enable signal for external DC/DC regulator generating AVDD supply. This is set low when in sleep state.
WAKE	Digital Input	Local wake input. This is used by an external device to trigger wake-up of the local PHY and to optionally send a WUP over the network.
VBAT	Power	Always-on supply, to power the wake-up detection functionality when in sleep state.

Low Power State

When the transceiver enters low power state, the VBAT connection provides power to blocks in the always-on domain, which is seen in the block diagrams in Figure 1. This domain includes only the blocks necessary for sleep/wake functionality. These blocks handle wake-up detection and holding the EN pin low. The EN pin triggers the shutdown of the external regulator generating the AVDD supply, which ensures all blocks outside the 'always-on' domain are unpowered. Thus, minimal current is consumed in the low power state which allows these devices to surpass power consumption requirements for the power-sensitive applications. The wake-up detection block facilitates fast wake-up when the local wake pin is asserted, or a WUP is detected on the network. Please consult the relevant device datasheet for detailed information on power consumption in low power state.

Partial Networking

Partial networking is a feature of 10BASE-T1S networks where specific nodes are temporarily powered down while the rest of the network remains active. Partial networking is used in situations where nodes are not required to operate continuously. Selectively powering down these nodes helps to reduce overall power consumption. When nodes are asleep, PLCA ensures that almost all the link throughput is used by the nodes that are active, since sleeping nodes do not transmit in their transmit opportunity and the PLCA cycle moves on to the next node. For more information, see the PLCA section.

Power Management Client (Sleep/Wake Controller)

The PM client is compliant to OPEN Alliance TC10/TC14 10BASE-T1S Sleep/Wake-up version 1.0. It controls the entry of the local PHY into a low power state and the coordinated wake-up of all supporting nodes connected on the link segment. The communication between the PM client and higher layers may be through the OA-SPI interface, or through the dedicated IO pins in Table 17.

OPEN ALLIANCE TC14 SUPPORTED FEATURES OVERVIEW

Wake-Up Pulse

The WUP is a command that is sent over the line by any node PHY or switch PHY to distribute a wake-up request over a quiet or partial link segment. The WUP is transmitted directly onto the network by the 10BASE-T1S PHY. The WUP begins with a suspend symbol which informs the alert nodes that a WUP is occurring. This is followed by a Wake up Tone (WUT) which is 12 periods of a 625kHz tone. This tone is detected by the wake-up detection block in sleeping nodes, instructing them to exit the low power state.

Configuring Sleep/Wake-Up

Use the following settings for configuring Sleep/Wake-up. Local wake via the WAKE pin can be enabled by setting the ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VALID bit. This bit enables and validates all configuration controls, which include:

- ALWAYS_ON_CONFIGURATION_FIELDS_0.CFG_DUV_THRESHOLD
- ALWAYS_ON_CONFIGURATION_FIELDS_0.CFG_UV_THRESHOLD
- ALWAYS_ON_CONFIGURATION_FIELDS_0.CFG_WAKE_PIN_POL
- ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_OV_THRESHOLD
- ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VBAT_DEEP_UV_FLAG_EN
- ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VBAT_UV_FLAG_EN
- ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VBAT_OV_FLAG_EN

Note that before sending a node to standby mode, it is required to write 1 to the IO_LV_MISC_CONTROL.STANDBY_FEATURE_EN register.

The IO_LV_SLEEPWAKE_CMD register has controls for triggering a WUP and for sending the node to sleep or standby. There are duplicate controls for triggering a WUP and sending the node to sleep in the OPEN Alliance TC14 mandated PHY_OA_WS_CTRL register. The controls in this register perform the exact same function as those in the IO_LV_SLEEPWAKE_CMD register.

The IO_LV_SLEEP_HISTORY register has readbacks that show what triggered the last wake event (for example wake pin) and what triggered the last sleep event (for example under voltage).

The ALWAYS_ON_CONFIGURATION_FIELDS_0 register allows software to configure the polarity of the wake pin.

TOPOLOGY DISCOVERY

Network topology refers to the arrangement of nodes and connections within a network. In some cases, it is necessary to correlate the logical topology of a network with the physical location of nodes in the real world. A 10BASE-T1S network may contain multiple identical devices on the same bus, whose specific function depends on the physical location of the device. Topology discovery allows a 10BASE-T1S network to relate the MAC address of a node to its physical location, thereby, allowing otherwise identical modules to be differentiated from each other easily.

A 10BASE-T1S uses a multidrop topology where every node is at a different position along the cable. Topology discovery allows any node to determine the distance between itself and another node on the bus. The end node can determine the distance to each node one by one to reveal the entire topology.

The OPEN Alliance TC14 10BASE-T1S topology discovery specification outlines a mechanism to measure the distance between the nodes and the normative requirements for state machines, timing, and voltage levels associated with this measurement.

OPEN ALLIANCE TC14 SUPPORTED FEATURES OVERVIEW

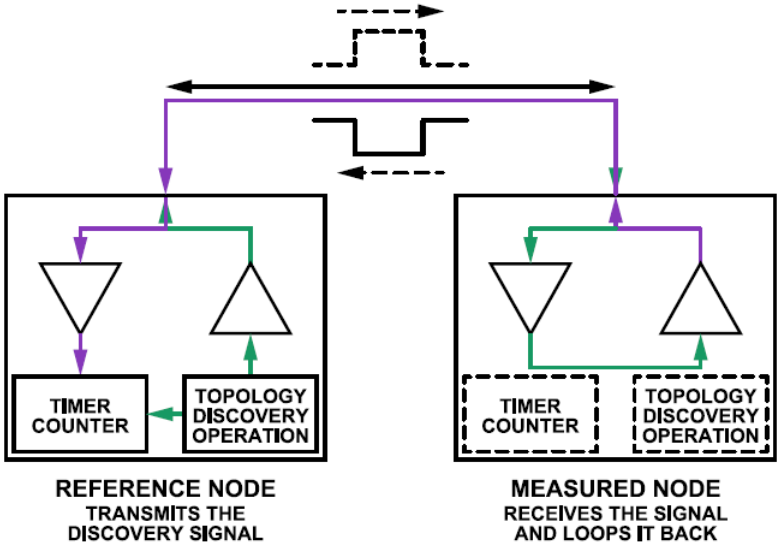

Figure 21. Topology Discovery Operation

Distance Measurement

The distance between any two nodes is determined by measuring the propagation delay of a pulse sent back and forth between the two nodes. The number of pulses received during a known time window are counted to determine the average propagation delay. Additionally, each node performs a measurement of their own internal delays, which are subtracted from the total propagation delay to determine the nominal propagation delay (NVP) of the cable. The propagation delay per meter of a pulse through single pair cable is typically (~5ns/m), so the length of single pair cable between the nodes is determined from the measured cable propagation delay. For higher accuracy, the exact nominal velocity of propagation (NVP) of used cable is considered.

Other components such as PCB traces and common mode chokes can also add signal delays. These additional delays depend on the circuit implementation and must be subtracted to obtain a more accurate distance measurement.

The measurement time window is programmable and lengthened to increase the resolution of the acquired distance measurement. But it should be noted that this does not increase the accuracy of the distance measurement.

Before the measurement procedure is started, select a reference node and a measured node. Prevent all the other nodes connected to the same line from any transmission. It is also recommended to disable the PLCA at all the nodes to avoid periodic BEACON transmissions.

The transceiver has two modes of operation for topology discovery. The manual mode allows each step of the distance measurement to be triggered individually by register map bits. The internal delay measurement on each node is triggered individually, as well as the propagation delay between the two nodes. The automatic mode completes the full distance measurement at once, triggered by a single register map bit. For information on available device registers related to topology discovery, consult the PHY_OA Registers chapter.

This distance measurement process can be used for other applications where knowing the cable length between nodes is useful. For example, it is used to determine the link latency between the nodes for time sensitive networking (TSN) with gPTP.

Configuring Topology Discovery

The PHY_OA_TD_CTRL register contains several controls for the topology discovery functionality such as the controls for running the various distance measurement steps and the setting for configuring the measurement duration.

The PHY_OA_TD_DIST_RES_UP.TD_DIST_MR register is a readback register for the number of pulses received during the latest measurement step.

The PHY_OA_TD_STAT register has status bits that indicate if measurement steps were completed or if an error was encountered.

For a full list of device registers related to topology discovery, see Table 29.

OPEN ALLIANCE TC14 SUPPORTED FEATURES OVERVIEW

10BASE-T1S PHYSICAL MEDIA ATTACHMENT TEST SUITE

The ADIN1140 transceiver device supports the functions specified in the IEEE 10BASE-T1S Physical Media Attachment (PMA) Test Suite to evaluate the functionality of the PMA sublayer of the 10BASE-T1S device, particularly focusing on the electrical specifications.

These tests verify that the product meets the specifications outlined in IEEE 802.3-2022 Clause 147, the OPEN Alliance 10BASE-T1S System Implementation Specification, and the 10BASE-T1S PMD Transceiver Interface. The product adheres to the test modes specified in these standards.

To configure the test modes, use the PHY_STD_T1S_TEST_MODE_CONTROL.PMAPATTERNSEL bits.

When selecting Test Mode 2 or Test Mode 7, ensure that Bit 12 (PHY_OA_TWEAKS_1.TXC_AUTO_RESET_CMD_ON_STUCK_RX_ED_DIS) is set before programming the test mode in PHY_STD_T1S_TEST_MODE_CONTROL register.

To enable PMA2 mode: Write 0x10C0 to the PHY_OA_TWEAKS_1 register before setting the PHY_STD_T1S_TEST_MODE_CONTROL.PMA-PATTERNSEL bit = 2. Write 0x00C0 to clear this bit.

SYSTEM IMPLEMENTATION SPECIFICATIONS

For information on the 10BASE-T1S interface circuitry, consult the product specific data sheet.

For 10BASE-T1S testing requirements and system requirements, please consult the *OPEN Alliance 10BASE-T1S System Implementation Specification* document.

SYSTEM DEBUG AND DIAGNOSTICS

The transceiver devices support diagnostics at the Physical layer and MAC layer. In addition, device diagnostics are available to read back.

PHYSICAL LAYER DIAGNOSTICS

The following diagnostics are supported in accordance with the Open Alliance TC14 Advanced Diagnostics v1.1 specification. Violations of these diagnostic conditions with respect to a configurable threshold are reported to the system locally via the OA-SPI $\overline{IRQ}$ interrupt pin and over the network.

Dynamic Channel Quality (DCQ)

Signal Quality Index (SQI) is computed and reported for received packets on the 10BASE-T1S network. The PHY_OA_DCQ_JM_CFG0.CFG_JM_PLCA_ID_SEL bit field is used to select the PLCA ID for which to analyze packets. Configuring this bit field with 0xFF analyzes all packets.

This feature is compliant with the 10BASE-T1S Advanced Diagnostics v1.1 specification, released in February 2022. The transceiver reports the SQI in one of three levels that monotonically increase with the noise level (green, yellow, red). Interrupts can be configured for red and yellow levels. These levels are triggered when the internal SQI raw data field (configured using the registers and values shown in Table 18) crosses specific programmable thresholds.

Recommended SQI Thresholds

Analog Devices recommends thresholds for the transitions, based on worst-case numbers from testing with 8-node systems using the Interoperability (IOPT) harness. The following figure shows the SQI raw values (from the PHY_OA_DCQ_JM_RB5.RB_JM_COMB_METRIC bit field) and markers indicating recommended threshold levels.

Figure 22. SQI Values and Recommended Threshold Levels

SYSTEM DEBUG AND DIAGNOSTICS

Table 18. Recommended SQI Thresholds

Threshold	Register and Bit field	Recommended Value
Good to Warning Threshold — Low to Mid	PHY_OA_DCQ_JM_CFG2.CFG_JM_TH_LOW_MID_ERR	3750
Warning to Good Threshold — Mid to Low	PHY_OA_DCQ_JM_CFG5.CFG_JM_TH_MID_LOW_ERR	3650
Warning to Bad Threshold — Mid to High	PHY_OA_DCQ_JM_CFG3.CFG_JM_TH_MID_HIGH_ERR	4950
Bad to Warning Threshold — High to Mid	PHY_OA_DCQ_JM_CFG4.CFG_JM_TH_HIGH_MID_ERR	4850

SQI Configuration

The basic flow for initializing SQI monitoring follows:

1. Clear the PHY_OA_DCQ_JM_CFG1.CFG_JM_SETTLED_RANGE_SEL bit to 0.
2. Program the thresholds in the PHY_OA_DCQ_JM_CFG2 through PHY_OA_DCQ_JM_CFG5 registers. (See Figure 22).
3. Enable interrupts if needed. (See the Event Management section).
4. Enable SQI: Set the PHY_OA_DCQ_JM_CFG0.CFG_JM_EN bit to 1.

Once SQI is enabled and enough frames are sent, the SQI level readback value (green, yellow, red) can be read from the PHY_OA_DCQ_JM_RB4.RB_JM_QUALITY_INDEX bit field.

The PHY_OA_DCQ_JM_CFG1.CFG_JM_SETTLED_RANGE_SEL bit field is used to select the number of frames after which the SQI data is settled. It is recommended that this field is set to 0, rather than using the default value of 2. A value of 0 reduces the settling time to the minimum value possible and ensures a faster response of the block.

The PHY_OA_DCQ_JM_RB0.RB_JM_OUT_VALID bit field is set only once after the initial settling time has elapsed - that is, after the first 16k carrier events (single frames or burst frames) are received. The PHY_OA_DCQ_JM_RB0.RB_JM_OUT_SETTLED bit is set when the number of frames configured by PHY_OA_DCQ_JM_CFG1.CFG_JM_SETTLED_RANGE_SEL are received.

Once this value (PHY_OA_DCQ_JM_RB4.RB_JM_QUALITY_INDEX) is reached, the SQI is updated continuously (for each frame received). The SQI metric value is only available after the settling time has elapsed. However, the jitter monitor raw value in PHY_OA_DCQ_JM_RB5.RB_JM_COMB_METRIC is available since the first frame and it is updated on a per-frame basis. The raw data value might be unstable if read before the settling time has elapsed.

With PLCA enabled, SQI can also be computed and reported over all packets received over one selected transmit opportunity. An 8-bit value in the PHY_OA_DCQ_JM_CFG0.CFG_JM_PLCA_ID_SEL bit field specifies the transmit opportunity for which SQI is computed as shown in the *Dynamic Channel Quality (DCQ)* table.

Table 19. PHY Jitter Monitor Configuration 0 Register Field Description

Field Value	Explanation
0x00	Compute SQI over packets received in PLCA transmit opportunity 0
0x01	Compute SQI over packets received in PLCA transmit opportunity 1
0x02	Compute SQI over packets received in PLCA transmit opportunity 2
...	...
0xFF	Compute SQI over all received packets. (Used for point-to-point or non-PLCA segments).

Calibrating SQI Thresholds (Optional)

Use the following procedure if there is a system requirement to calibrate SQI thresholds for the exact application harness topology:

1. Send several frames to each node on the network and read back the jitter monitor raw value from each node (PHY_OA_DCQ_JM_RB5.RB_JM_COMB_METRIC register).
2. Wait until the PHY_OA_DCQ_JM_RB0.RB_JM_OUT_SETTLED flag is set.
3. Read the PHY_OA_DCQ_JM_RB5.RB_JM_COMB_METRIC values.

   The recorded jitter monitor raw value is the good level (in the best case, no noise). This value is different for each node on the network; and needs to be recorded for all nodes.
4. Add increasing levels of noise to the harness until the bit error rate (BER) reaches 1e-10.
5. Read back the jitter monitor raw value again (PHY_OA_DCQ_JM_RB5.RB_JM_COMB_METRIC).

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ADDITIONAL INFORMATION: To accurately get the BER, a significant amount of traffic must be sent (>1e-10 bits) and the program must wait until MAC CRC errors are observed. The injection noise level to achieve the required BER is likely different for each node.

6. Based on the good jitter monitor readbacks and the bad jitter monitor readbacks, program the SQI thresholds accordingly.
   a. Set the red threshold a little lower than the exact point where BER gets to 1e-10. See the PHY_OA_DCQ_JM_CFG3 and PHY_OA_DCQ_JM_CFG4 registers for setting hysteresis on the values.
   b. Set the yellow threshold roughly halfway between the good level and the red level set above. See the PHY_OA_DCQ_JM_CFG2 and PHY_OA_DCQ_JM_CFG5 registers for setting hysteresis on the values.
   c. Repeat for each node.

PLCA DIAGNOSTICS

The PLCA diagnostics are read from the PHY_OA_PLCA_DIAG register.

PLCA Beacon Received Before Transmit Opportunity (BCNBFTO)

BCNBFTO occurs when a PLCA beacon was received before a node's transmit opportunity. It can indicate multiple PLCA coordinator nodes on the mixing segment, or one PLCA coordinator node incorrectly configured with a node count smaller than the number of nodes on the mixing segment.

PLCA Unexpected Beacon (UNEXPB)

This condition occurs on a PLCA coordinator node when it receives a beacon that it did not transmit. This indicates the presence of another PLCA coordinator node on the mixing segment.

PLCA Receive in Assigned Transmit Opportunity (RXINTO)

This condition occurs when the PHY detects the beginning of a packet in its assigned transmit opportunity. This indicates another node on the mixing segment with the same PLCA ID.

PRBS Generator

The device also has a Pseudorandom Binary Sequence generator (PRBS) to output. When PMA test mode 3 is enabled, the PHY outputs a pseudo-random binary sequence (PRBS) from the PHY.

MAC LAYER DIAGNOSTICS

MAC layer diagnostics include all the mandatory diagnostics from the IEEE 802.3 standard and also several optional ones, as listed in Table 20.

The transceivers are compliant to the Open Alliance TC6 specification and thereby support all errors which are read back from the MAC_STATUS0 register.

Table 20. MAC Layer Diagnostics from the IEEE 802.3 Standard, Clause 5.2

Diagnostic	Description
aFramesTransmittedOK	Count of frames successfully transmitted (MAC_TX_FRM_CNT register).
aSingleCollisionFrames	Count of frames involved in a single collision and subsequently transmitted successfully (MAC_TX_SINGLE_COL_CNT register). The Tx single collision count register reflects logical collisions and is not a useful metric when PLCA is enabled. Consider a case when the MAC tries to send two frames separated only by the inter-frame gap. The first frame is transmitted correctly but when the next frame starts from the MAC there is still some time before the next TO for the node appears. The PLCA data layer starts accepting the data from the MAC but the PLCA delay-line (which is 99 nibbles long, in accordance to the 802.3-2022 specification) fills before the next TO occurs. Therefore the PLCA layer sends a COL to the MAC telling it to back-off and then the PLCA data state-machine waits 512 bit-times before allowing another transmission. This means the entire PLCA cycle is missed and transmission of the frame has to wait for the next TO for the node, which occurs after the next beacon, causing the Tx single collision counter to increment.
aMultipleCollisionFrames	Count of frames involved in more than one collision and subsequently transmitted successfully (MAC_TX_MULTIPLE_COL_CNT register).
aFramesReceivedOK	Count of frames that are successfully received. This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error (MAC_RX_FRM_CNT register).

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Table 20. MAC Layer Diagnostics from the IEEE 802.3 Standard, Clause 5.2 (Continued)

Diagnostic	Description
aFrameCheckSequenceErrors	Count of frames that are an integral number of octets in length and do not pass the FCS check (MAC_RX_CRC_ERR_CNT).
aAlignmentErrors	Count of frames that are not an integral number of octets in length and do not pass the FCS check (MAC_RX_ALGN_ERR_CNT register).
aFramesWithDeferredXmissions	Count of frames whose transmission was delayed on its first attempt because the medium was busy (MAC_TX_DEFERRED_XMIT_CNT register).
aLateCollisions	Count of the times that a collision has been detected later than 512-bit times into the transmitted packet (MAC_TX_LATE_COL_CNT register). Note that a late collision is counted twice, both as a collision and as a late collision.
aFramesAbortedDueToXSColls	Count of frames that are not transmitted successfully due to excessive collisions (MAC_TX_XSCOLS_CNT register).
aFramesLostDueToIntMACXmitError	Count of frames that would otherwise be transmitted, but could not be sent due to an internal MAC sublayer transmit error. This occurs if the TX FIFO under-runs (MAC_TX_UNR_CNT register).
aFramesLostDueToIntMACRcvError	Count of frames that would otherwise be received, but could not be accepted due to an internal MAC sublayer receive error. This occurs if the RX FIFO is full and there is no space to store a new RX frame (MAC_RX_DROP_HOST_FULL_CNT register).
aMulticastFramesXmittedOK	Count of frames that are successfully transmitted to a group destination address other than broadcast (MAC_TX_MCAST_CNT register).
aBroadcastFramesXmittedOK	Count of the frames that are successfully transmitted to the broadcast address (MAC_TX_BCAST_CNT register).
aMulticastFramesReceivedOK	Count of frames that are successfully received and are directed to an active non-broadcast group address. This does not include frames received with frame-too-long, FCS, length, or alignment errors, or frames lost due to internal MAC sublayer error (MAC_RX_MCAST_CNT register).
aBroadcastFramesReceivedOK	Count of frames that are successfully received and are directed to the broadcast group address. This does not include frames received with frame-too-long, FCS, length, or alignment errors, or frames lost due to internal MAC sublayer error (MAC_RX_BCAST_CNT register).
aInRangeLengthErrors	Count of frames with a valid length field value that does not match the number of data octets received (MAC_RX_SHORT_ERR_CNT and MAC_RX_LONG_ERR_CNT registers).
aFrameTooLongErrors	Count of frames that are received and exceed the maximum permitted frame size (MAC_RX_LONG_ERR_CNT register).

DEVICE DIAGNOSTICS

The device diagnostics supported specifically by the transceiver are listed in Table 21.

Table 21. Device Diagnostics

Diagnostic	Description
MAC Loopback test	Within the MAC, MII Tx is connected to MII Rx
PHY Loopback test	PCS loopback as per IEEE 802.3-2022 clause 147.3.4
gPTP status and counters	See the Time Synchronization section for all gPTP errors supported.
Alive Counter	Free running counter used to confirm device not frozen (IO_LV_SSC_ALIVE_COUNTER_RB register).
Signal Timeout Monitor	Configurable timeout monitor reset by frame reception. Trigger may cause transition into safe state. See the Safe State Controller (SSC) section for more details.
Wake-Up Idle Monitor	Timeout on network activity after remote wake-up event. Please refer to the Sleep/wake-up section for details.
Config Validation	Software can verify Bootloader has run successfully – checks DONE and status flags.
OTP Corruption	ECC – SECDED.

REGISTERS OVERVIEW

This section describes the control registers for the 10BASE-T1S ADIN1140 transceiver.

Register address and register value information contained in the following Register chapters are written using the base 16 (hexadecimal or hex for short) number system. The prefix 0x is used to indicate that the number is being written in hexadecimal.

Exceptions to this convention can occur within register bit field descriptions and bit field enumerations. Bit fields are typically enumerated using the binary (base 2 number system) value convention.

Note that all the HV Die (IO_HV registers) must be read back twice via OA-SPI to get the correct value.

MEMORY ADDRESS SPACE AND MEMORY MAPS

Memory address space and the OA-SPI addresses are detailed in this section.

For accessing register maps via OA-SPI, the unique memory address space must be considered.

Note that the MMS and OA-SPI address appear under the register title before the register description.

MMS: Memory Map Selector.

- Refer to Section 7.4 of *OPEN_Alliance_10Base-T1x_MAC-PHY_Serial_Interface_V1.1*. The four bits within control command header of control transaction protocol selects the specific register memory map to access.
- Refer to Section 9.1 of *OPEN_Alliance_10Base-T1x_MAC-PHY_Serial_Interface_V1.1*, *Register Memory Map Selector Assignment* section.

Table 22. Memory Address Spaces for Register Access via OA-SPI

Register Map Name	OA-SPI	
	MMS (Hex)	Address (Hex)
HOST MAC Interface (MAC)	0	0000 → 002F
	1	0030 → 01FF
10BASE-T1S PHY OPEN Alliance (PHY_OA)	4	0000 → 01FF CA00 → CBFF CC00 → D1FF
10BASE-T1S PHY Standard (PHY_STD)	0	FF00 → FF0F
	3	0000 → 003F
	3	08F0 → 08FF
	2	0000 → 001F
	2	08F0 → 08FF
	4	CA00 → CA1F
Low Voltage Map (IO)	A	C800 → C9FF
One Time Programmable Memory Controller (OTP)	A	B000 → B0FF
High Voltage IO (IO_HV)[1]	A	B100 → B4FF
Always On Domain (AO)	A	B700 → B70F(8-bit data access) B710 → B71F(16-bit data access in 2x8)
Open Alliance PMD Transceiver Section (PMD)	4	D200 → D21F

[1] All HV die registers must be read back twice to get the correct value.

ABBREVIATIONS USE IN REGISTERS

The abbreviations in Table 23 are used in the register descriptions.

Table 23. Register Abbreviations

Abbreviation	Description
R/W Read/write (R/W)	Software can read and write to these bits.
Read-Only (R)	Software can only read these bits.
Write-Only (W)	Software can only write this bit. Reading the bit returns the reset value.
Write-1-to-Set (W1S)	Software write set 1 to set this bit.
Write-1-to-Clear (W1C)	Software write set 1 to clear this bit.
R0/W1S	Read always as 0. Write 1 to set. Automatic synchronous clear

REGISTERS OVERVIEW

Table 23. Register Abbreviations (Continued)

Abbreviation	Description
Read/Set (R/W1S)	Software can read as well as set this bit by writing 1. Writing 0 has no effect on the bit value.
Read/Clear (R/W1C)	Software can read as well as clear this bit by writing 1. Writing 0 has no effect on the bit value. There is an independent input to this field to make a synchronous set.
Reserved	Reserved bit. This must be kept at reset value.

ADIN1140 REGISTER LIST

This appendix lists Memory-Mapped Register address and register names. The modules are presented in alphabetical order.

Table 24. ADIN1140 ALWAYS_ON MMR Register Addresses

Memory Mapped Address	Register Name	Description	Reset Value
0xB702	ALWAYS_ON_CONFIGURATION_FIELDS_0	ALWAYS_ON Configuration Fields 0 Register	0x00000023
0xB703	ALWAYS_ON_CONFIGURATION_FIELDS_1	ALWAYS_ON Configuration Fields 1 Register	0x00000004

Table 25. ADIN1140 IO_HV MMR Register Addresses

Memory Mapped Address	Register Name	Description	Reset Value
0xB105	IO_HV_REVISION_CONTROL	IO_HV Revision Control Register	0x00000000
0xB106	IO_HV_BOOTLOADER_STATUS_0	IO_HV Bootloader Status 0 Register	0x00000000
0xB108	IO_HV_STANDBY_STATUS	IO_HV Standby Status Register	0x00000000
0xB10A	IO_HV_BOOTLOADER_STATUS_1	IO_HV Bootloader Status 1 Register	0x00000000
0xB1FE	IO_HV_BLOCK_RESET_CONTROL	IO_HV Block Reset Control Register	0x00000000
0xB1FF	IO_HV_RESET_CONTROL	IO_HV Reset Control Register	0x00000000
0xB200	IO_HV_HIGH_SPEED_SERIAL_COMM	IO_HV High Speed Serial Communications Register	0x00000000
0xB20F	IO_HV_OTP_CONFIG_0	IO_HV OTP Memory Configuration Register 0	0x00000000
0xB210	IO_HV_OTP_CONFIG_1	IO_HV OTP Memory Configuration Register 1	0x00000000
0xB21C	IO_HV_CONFIG_EN_PADS_CONFIG	IO_HV Pads Configuration Enable Register	0x000001A8

Table 26. ADIN1140 IO_LV MMR Register Addresses

Memory Mapped Address	Register Name	Description	Reset Value
0xC801	IO_LV_DEBUG_DATA_CTRL	IO_LV Debug Data Ctrl	0x00000000
0xC802	IO_LV_IO_PULL-DOWN_CTRL_1	IO_LV IO Pull-down Control 1 Register	0x00000000
0xC803	IO_LV_IO_PULL-DOWN_CTRL_2	IO_LV IO Pull-down Control 2 Register	0x00000000
0xC804	IO_LV_MAC_INTERFACE	IO_LV MAC Interface Register	0x0000000E
0xC805	IO_LV_REVISION_CONTROL	IO_LV Revision Control Register	0x00000000
0xC806	IO_LV_BOOTLOADER_STATUS_0	IO_LV Bootloader Status 0 Register	0x00000000
0xC807	IO_LV_BOOTLOADER_STATUS_1	IO_LV Bootloader Status 1 Register	0x00000000
0xC808	IO_LV_BOOTLOADER_STATUS_2	IO_LV Bootloader Status 2 Register	0x00000000
0xC809	IO_LV_BOOTLOADER_STATUS_3	IO_LV Bootloader Status 3 Register	0x00000000
0xC80A	IO_LV_BOOTLOADER_STATUS_4	IO_LV Bootloader Status 4 Register	0x00000000
0xC80B	IO_LV_BOOTLOADER_STATUS_5	IO_LV Bootloader Status 5 Register	0x00000000
0xC80C	IO_LV_BOOTLOADER_STATUS_6	IO_LV Bootloader Status 6 Register	0x00000000
0xC80D	IO_LV_BOOTLOADER_STATUS_7	IO_LV Bootloader Status 7 Register	0x00000000
0xC80F	IO_LV_SLEEP_WAKE_CFG	IO_LV Sleep Wake Configuration Register	0x00000100
0xC810	IO_LV_SLEEPWAKE_CMD	IO_LV Sleep/wake Command Register	0x00000000
0xC811	IO_LV_SLEEPWAKE_STATUS	IO_LV Sleepwake Status Register	0x00000000
0xC813	IO_LV_BOOTLOADER_RB_8	IO_LV Bootloader Readback 8 Register	0x00000000
0xC814	IO_LV_BOOTLOADER_RB_9	IO_LV Bootloader Readback 9 Register	0x00000000
0xC815	IO_LV_BOOTLOADER_RB_10	IO_LV Bootloader Readback 10 Register	0x00000000
0xC816	IO_LV_BOOTLOADER_RB_11	IO_LV Bootloader Readback 11 Register	0x00000000
0xC817	IO_LV_BOOTLOADER_RB_12	IO_LV Bootloader Readback 12 Register	0x00000000
0xC818	IO_LV_BOOTLOADER_RB_13	IO_LV Bootloader Readback 13 Register	0x00000000
0xC819	IO_LV_BOOTLOADER_RB_14	IO_LV Bootloader Readback 14 Register	0x00000000
0xC81A	IO_LV_BOOTLOADER_RB_15	IO_LV Bootloader Readback 15 Register	0x00000000

ADIN1140 REGISTER LIST

Table 26. ADIN1140 IO_LV MMR Register Addresses (Continued)

Memory Mapped Address	Register Name	Description	Reset Value
0xC81B	IO_LV_BOOTLOADER_RB_16	IO_LV Bootloader Readback 16 Register	0x00000000
0xC81C	IO_LV_BOOTLOADER_RB_17	IO_LV Bootloader Readback 17 Register	0x00000000
0xC81D	IO_LV_BOOTLOADER_RB_18	IO_LV Bootloader Readback 18 Register	0x00000000
0xC81E	IO_LV_BOOTLOADER_RB_19	IO_LV Bootloader Readback 19 Register	0x00000000
0xC81F	IO_LV_BOOTLOADER_RB_20	IO_LV Bootloader Readback 20 Register	0x00000000
0xC820	IO_LV_BOOTLOADER_RB_21	IO_LV Bootloader Readback 21 Register	0x00000000
0xC821	IO_LV_BOOTLOADER_RB_22	IO_LV Bootloader Readback 22 Register	0x00000000
0xC822	IO_LV_BOOTLOADER_RB_23	IO_LV Bootloader Readback 23 Register	0x00000000
0xC823	IO_LV_BOOTLOADER_RB_24	IO_LV Bootloader Readback 24 Register	0x00000000
0xC824	IO_LV_BOOTLOADER_RB_25	IO_LV Bootloader Readback 25 Register	0x00000000
0xC825	IO_LV_BOOTLOADER_RB_26	IO_LV Bootloader Readback 26 Register	0x00000000
0xC840	IO_LV_DEBUG_DATA_CONTROL_0	IO_LV Debug Data Control 0	0x00007F7F
0xC841	IO_LV_DEBUG_DATA_CONTROL_1	IO_LV Debug Data Control 1	0x00007F7F
0xC844	IO_LV_DEBUG_DATA_CONTROL_4	IO_LV Debug Data Control 4	0x00007F7F
0xC845	IO_LV_DEBUG_DATA_CONTROL_5	IO_LV Debug Data Control 5	0x00007F7F
0xC849	IO_LV_MISC_CONTROL	IO_LV Miscellaneous Control Register	0x00002000
0xC84F	IO_LV_IO_GLITCH_REJECT_0	IO_LV IO Glitch Reject 0 Register	0x0000FFFF
0xC850	IO_LV_IO_GLITCH_REJECT_1	IO_LV IO Glitch Reject 1 Register	0x0000033F
0xC851	IO_LV_IO_DRIVE_STRENGTH_0	IO_LV IO Drive Strength 0 Register	0x00005555
0xC852	IO_LV_IO_DRIVE_STRENGTH_1	IO_LV IO Drive Strength 1 Register	0x00000055
0xC853	IO_LV_IO_HYSTHERESIS_ENABLE	IO_LV IO Hysteresis Enable Register	0x00000000
0xC854	IO_LV_IO_SLEW_RATE	IO_LV IO Slew Rate Register	0x00000000
0xC860	IO_LV_SLEEP_HISTORY	IO_LV Sleep History Register	0x00000000
0xC882	IO_LV_MANUAL_INTERRUPT	IO_LV Manual Interrupt Register	0x00000000
0xC883	IO_LV_SSC_MUX_SEL_SAFE_ACTIVE_RB	IO_LV Pin Safe Mode Status Register	0x00000000
0xC884	IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB	IO_LV SSC Safe Checks Triggered Readback Register	0x00000000
0xC885	IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB_2	IO_LV SSC Safe Checks Triggered Readback 2 Register	0x00000000
0xC886	IO_LV_SSC_SAFE_CHECKS_TRIGGER	IO_LV SSC Safe Checks Triggered Readback (Sticky) Register	0x00000000
0xC887	IO_LV_SSC_SAFE_CHECKS_TRIGGERED_STICKY_RB_2	IO_LV SSC Safe Checks Triggered Readback 2 (Sticky) Register	0x00000000
0xC888	IO_LV_SSC_GENERAL_RB	IO_LV SSC General Readback Register	0x00000000
0xC889	IO_LV_SSC_ALIVE_COUNTER_RB	IO_LV SSC Alive Counter Read Register	0x00000000
0xC88A	IO_LV_SSC_SAFE_SA_IF_CONTROLS	IO_LV SSC Safe SAIF Control Register	0x00000000
0xC88B	IO_LV_SSC_SAFE_SA_IF_CONTROLS_2	IO_LV SSC Safe SAIF Control 2 Register	0x00000000
0xC88C	IO_LV_SSC_SAFE_SA_IF_CONTROLS_3	IO_LV SSC Safe SAIF Control 3 Register	0x00000000
0xC88D	IO_LV_SSC_MONITOR_POLARITY	IO_LV SSC Monitor Polarity Register	0x00000000
0xC88E	IO_LV_SSC_MONITOR_POLARITY_2	IO_LV SSC Monitor Polarity 2 Register	0x00000000
0xC88F	IO_LV_SSC_TIME-OUT_0_TIME	IO_LV SSC Timeout 0 Time Register	0x00000000
0xC890	IO_LV_SSC_TIME-OUT_1_TIME	IO_LV SSC Timeout 1 Time Register	0x00000000
0xC893	IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN	IO_LV SSC Auto Return To Functional Enable Register	0x00000000

ADIN1140 REGISTER LIST

Table 26. ADIN1140 IO_LV MMR Register Addresses (Continued)

Memory Mapped Address	Register Name	Description	Reset Value
0xC894	IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN2	IO_LV SSC Auto Return To Functional En2	0x00000000
0xC895	IO_LV_SSC_CONTROLS	IO_LV SSC Control Register	0x00002000
0xC896	IO_LV_SSC_SAFE_CHECK S_ENABLE	IO_LV SSC Safe Checks Enable Register	0x00000000
0xC897	IO_LV_SSC_SAFE_CHECK S_ENABLE_2	IO_LV SSC Safe Checks Enable 2 Register	0x00000000
0xC898	IO_LV_SSC_MONITOR_TRIGGERS	IO_LV SSC Monitor Triggers Register	0x00000000
0xC899	IO_LV_SSC_MISC	IO_LV SSC Miscellaneous Register	0x00000000
0xC89A	IO_LV_SSC_RECOVERED_DATA_FROM_AO	IO_LV SSC Recovered Data From Always On Register	0x00000000
0xC8FE	IO_LV_BLOCK_RESET_CONTROL	IO_LV Block Reset Control Register	0x00000000
0xC8FF	IO_LV_RESET_CONTROL	IO_LV Reset Control Register	0x00000000
0xC900	IO_LV_INTER_DIE_SERIAL_COMMUNICATION	IO_LV Inter Die Serial Communication Register	0x00000000
0xC901	IO_LV_GPTP_SYNC_COU NT	IO_LV gPTP Sync Count Register	0x00000000
0xC902	IO_LV_GPTP_SYNC_COU NT_1	IO_LV gPTP Sync Count 1 Register	0x00000000
0xC903	IO_LV_GPTP_ONESTEP_COUNT	IO_LV gPTP Onestep Count Register	0x00000000
0xC904	IO_LV_GPTP_ONESTEP_COUNT_1	IO_LV gPTP Onestep Count 1 Register	0x00000000
0xC905	IO_LV_GPTP_FOLLOWUP_COUNT	IO_LV gPTP Followup Count Register	0x00000000
0xC906	IO_LV_GPTP_FOLLOWUP_COUNT_1	IO_LV gPTP Followup Count 1 Register	0x00000000
0xC907	IO_LV_GPTP_NUM_LOCK S	IO_LV gPTP Number Locks Register	0x00000000
0xC908	IO_LV_GPTP_NUM_UNLOCKS	IO_LV gPTP Number of Unlocks Register	0x00000000
0xC909	IO_LV_GPTP_SEQUENCEID	IO_LV gPTP Sequence ID Register	0x00000000
0xC90B	IO_LV_GPTP_LOCK_THRESHOLD	IO_LV gPTP Lock Threshold Register	0x0000044C
0xC910	IO_LV_GPTP_TIME_ERROR	IO_LV gPTP Time Error Register	0x00000000
0xC911	IO_LV_GPTP_TIME_ERROR_1	IO_LV gPTP Time Error 1 Register	0x00000000
0xC912	IO_LV_GPTP_MEAN_LIN K_DELAY	IO_LV gPTP Mean Link Delay Register	0x00000000
0xC913	IO_LV_GPTP_MEAN_LIN K_DELAY_1	IO_LV gPTP Mean Link Delay 1 Register	0x00000000
0xC915	IO_LV_GPTP_STATUS_1	IO_LV gPTP Status 1 Register	0x00000000
0xC916	IO_LV_GPTP_RELOCK	IO_LV gPTP Relock Register	0x00000000
0xC917	IO_LV_GPTP_RELOCK_1	IO_LV gPTP Relock 1 Register	0x00000005
0xC92A	IO_LV_GPTP_CONFIG	IO_LV gPTP Configuration Register	0x00008928
0xC93A	IO_LV_TIC_STATUS_FLAGS_8_AND_9	IO_LV TIC Status Flags 8 and 9 Register	0x00000000
0xC93B	IO_LV_TIC_STATUS_FLAGS_10_AND_11	IO_LV TIC Status Flags 10 and 11 Register	0x00000000
0xC944	IO_LV_TIC_STATUS_FLAGS_28_AND_29	IO_LV TIC Status Flags 28 and 29 Register	0x00000000
0xC947	IO_LV_TIC_STATUS_FLAGS_34_AND_35	IO_LV TIC Status Flags 34 and 35 Register	0x00000000
0xC94D	IO_LV_TIC_CONTROL0	IO_LV TIC Control Register 0	0x00008480
0xC94E	IO_LV_TIC_CONTROL1	IO_LV TIC Control Register 1	0x0000041E
0xC961	IO_LV_TIC_ENABLE_8_PHY_REG0	IO_LV TIC Enable 8 PHY Register 0	0x00000000
0xC962	IO_LV_TIC_ENABLE_8_PHY_REG1	IO_LV TIC Enable 8 PHY Register 1	0x00000000
0xC963	IO_LV_TIC_ENABLE_9_MAC_REG0	IO_LV TIC Enable 9 MAC Register 0	0x00000000
0xC964	IO_LV_TIC_ENABLE_9_MAC_REG1	IO_LV TIC Enable 9 MAC Register 1	0x00000000
0xC965	IO_LV_TIC_ENABLE_10_REG0	IO_LV TIC Enable 10 Reg0	0x00000000
0xC989	IO_LV_TIC_ENABLE_28_MISC0_REG0	IO_LV TIC Enable 28 Miscellaneous 0 Register 0	0x00000000

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Table 26. ADIN1140 IO_LV MMR Register Addresses (Continued)

Memory Mapped Address	Register Name	Description	Reset Value
0xC98A	IO_LV_TIC_ENABLE_28_MISC0_REG1	IO_LV TIC Enable 28 Miscellaneous 0 Register 1	0x00000000
0xC98B	IO_LV_TIC_ENABLE_29_MISC1_REG0	IO_LV TIC Enable 29 Miscellaneous 1 Register 0	0x00000000
0xC98C	IO_LV_TIC_ENABLE_29_MISC1_REG1	IO_LV TIC Enable 29 Miscellaneous 1 Register 1	0x00000000
0xC9A0	IO_LV_TIC_CLEAR_8_PH Y_REG0	IO_LV TIC Clear 8 PHY Register 0	0x00000000
0xC9A1	IO_LV_TIC_CLEAR_8_PH Y_REG1	IO_LV TIC Clear 8 PHY Register 1	0x00000000
0xC9A2	IO_LV_TIC_CLEAR_9_MA C_REG0	IO_LV TIC Clear 9 MAC Register 0	0x00000000
0xC9A3	IO_LV_TIC_CLEAR_9_MA C_REG1	IO_LV TIC Clear 9 MAC Register 1	0x00000000
0xC9A4	IO_LV_TIC_CLEAR_10_REG0	IO_LV TIC Clear 10 PLCA Register 0	0x00000000
0xC9C8	IO_LV_TIC_CLEAR_28_MI SC0_REG0	IO_LV TIC Clear 28 Miscellaneous 0 Register 0	0x00000000
0xC9C9	IO_LV_TIC_CLEAR_28_MI SC0_REG1	IO_LV TIC Clear 28 Miscellaneous 0 Register 1	0x00000000
0xC9CA	IO_LV_TIC_CLEAR_29_MI SC1_REG0	IO_LV TIC Clear 29 Miscellaneous 1 Register 0	0x00000000
0xC9CB	IO_LV_TIC_CLEAR_29_MI SC1_REG1	IO_LV TIC Clear 29 Miscellaneous 1 Register 1	0x00000000
0xC9CE	IO_LV_CLOCK_GENERATION_OUTPU TS	IO_LV Clock Generation Outputs Register	0x00003C57
0xC9CF	IO_LV_CLOCK_GENERATION_OUTPU TS2	IO_LV Clock Generation Outputs2 Register	0x00000412
0xC9DF	IO_LV_TP_OUT_EN_SA_I F	IO_LV TP Output SAIF Pin Driver Enable Register	0x00000000
0xC9E0	IO_LV_TP_IP_EN_SA_IF	IO_LV TP Input Receiver SAIF Pin Enable Register	0x00000000
0xC9E2	IO_LV_EFUSE_REG	IO_LV Efuse Register	0x00000000
0xC9EF	IO_LV_GPTP_DOMAINS	IO_LV gPTP Domains Register	0x00000100
0xC9F6	IO_LV_TIC_ENABLE_34_GPIO1_REG0	IO_LV TIC Enable 34 GPIO 1 Register 0	0x00000000
0xC9F7	IO_LV_TIC_ENABLE_34_GPIO1_REG1	IO_LV TIC Enable 34 GPIO 1 Register 1	0x00000000
0xC9FA	IO_LV_TIC_CLEAR_34_GP IO1_REG0	IO_LV TIC Clear 34 GPIO0 Register 0	0x00000000
0xC9FB	IO_LV_TIC_CLEAR_34_GP IO1_REG1	IO_LV TIC Clear 34 GPIO0 Register 1	0x00000000

Table 27. ADIN1140 MAC MMR Register Addresses

Memory Mapped Address	Register Name	Description	Reset Value
0x00	MAC_IDVER	MACPHY Identification Version Register	0x00000011
0x01	MAC_PHYID	MAC PHY Identification Register	0x0283BE00
0x02	MAC_CAPABILITY	MAC Supported Capabilities Status Register	0x000006C3
0x03	MAC_RESET	MAC Reset Control and Status Register	0x00000000
0x04	MAC_CONFIG0	MAC Configuration Register 0	0x00000026
0x06	MAC_CONFIG2	MAC Configuration Register 2	0x007C2020
0x08	MAC_STATUS0	MAC Status Register 0	0x00000040
0x09	MAC_STATUS1	MAC Status Register 1	0x00000000
0x0B	MAC_BUFSTS	MAC Buffer Status Register	0x00007700
0x0C	MAC_IMASK0	MAC Interrupt Mask Register 0	0x00001FBF
0x0D	MAC_IMASK1	MAC Mask Bits for Driving the Interrupt Pin Register	0x40001F5A
0x10	MAC_TTSCAH	MAC Transmit Timestamp Capture Register A (High)	0x00000000
0x11	MAC_TTSCAL	MAC Transmit Timestamp Capture Register A (Low)	0x00000000
0x12	MAC_TTSCBH	MAC Transmit Timestamp Capture Register B (High)	0x00000000
0x13	MAC_TTSCBL	MAC Transmit Timestamp Capture Register B (Low)	0x00000000
0x14	MAC_TTSCCH	MAC Transmit Timestamp Capture Register C (High)	0x00000000
0x15	MAC_TTSCCL	MAC Transmit Timestamp Capture Register C (Low)	0x00000000
0x32	MAC_TX_SPACE	MAC Tx FIFO Space Register	0x00000FFF
0x33	MAC_RX_THRESH	MAC Receive Threshold Register	0x00000004

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Table 27. ADIN1140 MAC MMR Register Addresses (Continued)

Memory Mapped Address	Register Name	Description	Reset Value
0x34	MAC_TX_THRESH	MAC Transmit Threshold Register	0x00000001
0x35	MAC_TX_PRI	MAC Transmit Priority Register	0x00000000
0x36	MAC_FIFO_CLR	MAC FIFO Clear Register	0x00000000
0x37	MAC_SCRATCH[n]	MAC Scratch Register	0x00000000
0x38	MAC_SCRATCH[n]	MAC Scratch Register	0x00000000
0x39	MAC_SCRATCH[n]	MAC Scratch Register	0x00000000
0x3A	MAC_SCRATCH[n]	MAC Scratch Register	0x00000000
0x3D	MAC_SPI_INJ_ERR	MAC Inject Error on SDI from DUT Register	0x00000000
0x3E	MAC_FIFO_SIZE	MAC FIFO Sizes Register	0x01102022
0x3F	MAC_TFC	MAC Tx FIFO Frame Count Register	0x00000000
0x40	MAC_TXSIZE	MAC Tx FIFO Valid Half Words Register	0x00000000
0x41	MAC_HTX_OVF_FRM_CN T	MAC Host Transmit Frames Dropped Due to FIFO Overflow Register	0x00000000
0x42	MAC_MECC_ERR_ADDR	MAC ECC Error Memory Address Register	0x00000000
0x43	MAC_CECC_ERR[n]	MAC Corrected ECC Error Counters Register	0x00000000
0x44	MAC_CECC_ERR[n]	MAC Corrected ECC Error Counters Register	0x00000000
0x45	MAC_CECC_ERR[n]	MAC Corrected ECC Error Counters Register	0x00000000
0x46	MAC_CECC_ERR[n]	MAC Corrected ECC Error Counters Register	0x00000000
0x47	MAC_CECC_ERR[n]	MAC Corrected ECC Error Counters Register	0x00000000
0x48	MAC_CECC_ERR[n]	MAC Corrected ECC Error Counters Register	0x00000000
0x49	MAC_CECC_ERR[n]	MAC Corrected ECC Error Counters Register	0x00000000
0x4C	MAC_FIFO_ALMOST_EMPTY	MAC Almost Empty Assertion Threshold Value Register	0x00000004
0x50	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x51	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x52	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x53	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x54	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x55	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x56	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x57	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x58	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x59	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x5A	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x5B	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x5C	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x5D	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x5E	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x5F	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x60	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x61	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x62	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x63	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x64	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x65	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x66	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x67	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x68	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000

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Table 27. ADIN1140 MAC MMR Register Addresses (Continued)

Memory Mapped Address	Register Name	Description	Reset Value
0x69	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x6A	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x6B	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x6C	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x6D	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x6E	MAC_ADDR_FILT_UPR[n]	MAC Address Rule and DA Filter Upper 16 Bits Register	0x00000000
0x6F	MAC_ADDR_FILT_LWR[n]	MAC Address DA Filter (Lower 32 Bits) Register	0x00000000
0x70	MAC_ADDR_MSK_UPR[n]	MAC Address (Upper 32 Bits) Mask Register	0x0000FFFF
0x71	MAC_ADDR_MSK_LWR[n]	MAC Address (Lower 32 Bits) Mask Register	0xFFFFFFFF
0x72	MAC_ADDR_MSK_UPR[n]	MAC Address (Upper 32 Bits) Mask Register	0x0000FFFF
0x73	MAC_ADDR_MSK_LWR[n]	MAC Address (Lower 32 Bits) Mask Register	0xFFFFFFFF
0x80	MAC_TS_ADDEND	MAC Timestamp Accumulator Addend Register	0xA0000000
0x81	MAC_TS_1SEC_CMP	MAC Timer Update Compare Register	0x3B9ACA00
0x82	MAC_TS_SEC_CNT	MAC Seconds Counter Register	0x00000000
0x83	MAC_TS_NS_CNT	MAC Nanoseconds Counter Register	0x00000000
0x84	MAC_TS_CFG	MAC Timer Configuration Register	0x00000001
0x85	MAC_TS_TIMER_HI	MAC High Period for TS_TIMER Register	0x00000000
0x86	MAC_TS_TIMER_LO	MAC Low Period for TS_TIMER Register	0x00000000
0x87	MAC_TS_TIMER_QE_CORR	MAC Quantization Error Correction Register	0x00000000
0x88	MAC_TS_TIMER_START	MAC TS_TIMER Counter Start Time Lower Register	0x00000000
0x89	MAC_TS_EXT_CAPT0	MAC TS_CAPT Nanoseconds Timestamp Register	0x00000000
0x8A	MAC_TS_EXT_CAPT1	MAC TS_CAPT Seconds Timestamp Register	0x00000000
0x8B	MAC_TS_FREECNT_CAPT	MAC TS_CAPT Free Running Counter Register Lower Register	0x00000000
0x8D	MAC_PLCA_PRIORITY	MAC PLCA Transmit Throttle Register	0x00080000
0x90	MAC_RX_FSIZE	MAC Receive Frame Size Register	0x00000000
0xA1	MAC_RX_FRM_CNT	MAC Receive Frame Count Register	0x00000000
0xA2	MAC_RX_BCAST_CNT	MAC Receive Broadcast Frame Count Register	0x00000000
0xA3	MAC_RX_MCAST_CNT	MAC Receive Multicast Frame Count Register	0x00000000
0xA4	MAC_RX_UCAST_CNT	MAC Receive Unicast Frame Count Register	0x00000000
0xA5	MAC_RX_CRC_ERR_CNT	MAC Receive CRC Error Frame Count Register	0x00000000
0xA6	MAC_RX_ALGN_ERR_CN T	MAC Receive Align Error Count Register	0x00000000
0xA7	MAC_RX_PREAMBLE_ERR_CNT	MAC Receive Preamble Error Count Register	0x00000000
0xA8	MAC_RX_SHORT_ERR_C NT	MAC Receive Short Frame Error Count Register	0x00000000
0xA9	MAC_RX_LONG_ERR_CN T	MAC Receive Long Frame Error Count Register	0x00000000
0xAA	MAC_RX_PHY_ERR_CNT	MAC Receive PHY Error Count Register	0x00000000
0xAB	MAC_RX_DROP_HOST_FULL_CNT	MAC Receive Frames Dropped HOST FIFO Full Register	0x00000000
0xAD	MAC_RX_DROP_FILT_CN T	MAC Receive Frames Dropped Filtering Register	0x00000000
0xAE	MAC_RX_IFG_ERR_CNT	MAC Frame Received with IFG Errors Register	0x00000000
0xB1	MAC_TX_FRM_CNT	MAC Transmit Frame Count Register	0x00000000
0xB2	MAC_TX_BCAST_CNT	MAC Transmit Broadcast Frame Count Register	0x00000000
0xB3	MAC_TX_MCAST_CNT	MAC Transmit Multicast Frame Count Register	0x00000000
0xB4	MAC_TX_UCAST_CNT	MAC Transmit Unicast Frame Count Register	0x00000000
0xB5	MAC_TX_SINGLE_COL_CNT	MAC Transmit Single Collision Count Register	0x00000000
0xB6	MAC_TX_MULTIPLE_COL_CNT	MAC Transmit Multiple Collision Count Register	0x00000000
0xB7	MAC_TX_DEFERRED_XMIT_CNT	MAC Transmit Deferred Transmission Count Register	0x00000000
0xB8	MAC_TX_LATE_COL_CN T	MAC Transmit Late Collision Count Register	0x00000000

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Table 27. ADIN1140 MAC MMR Register Addresses (Continued)

Memory Mapped Address	Register Name	Description	Reset Value
0xB9	MAC_TX_XSCOLS_CNT	MAC Transmit Excess Collision Count Register	0x00000000
0xBA	MAC_TX_UNR_CNT	MAC Transmit Frames Dropped Under Run Register	0x00000000
0xBB	MAC_HI_RFC	MAC Receive FIFO Frame Count Register	0x00000000
0xBD	MAC_HI_RXSIZE	MAC Receive FIFO Valid Half Words Register	0x00000000
0xC1	MAC_TX_IFG	MAC Transmit Inter Frame Gap Register	0x0000000B
0xC2	MAC_DUPLEX	MAC Duplex Mode Register	0x00000010
0xC3	MAC_MAX_RETRY	MAC Max Retry in Half Duplex Register	0x0000000F
0xC4	MAC_LOOP	MAC Loopback Enable Register	0x00000000
0xC5	MAC_RX_CRC_EN	MAC CRC Check Enable on Receive Register	0x00000001
0xC6	MAC_RX_IFG	MAC Receive Inter Frame Gap Register	0x0000000A
0xC7	MAC_RX_MAX_LEN	MAC Max Receive Frame Length Register	0x00000618
0xC8	MAC_RX_MIN_LEN	MAC Minimum Receive Frame Length Register	0x00000040
0xC9	MAC_RXFILT_VID_TABLE	MAC VLAN Identifier Filter Table Register	0x00000000
0xCA	MAC_RXFILT_ETYPE_TABLE	MAC Ethernet Type Filter Table Register	0x00000000
0xCB	MAC_RXFILT_ETYPE_CN RL	MAC Ethernet Typer Filter Table Control Register	0x00000000

Table 28. ADIN1140 PMD MMR Register Addresses

Memory Mapped Address	Register Name	Description	Reset Value
0xD200	PMD_MIIMCTL	PMD Media-Independent Interface Control Register	0x00000000
0xD202	PMD_PHYIDH	PMD PHY Identifier Upper Bits Register	0x00000000
0xD203	PMD_PHYIDL	PMD PHY Identifier Lower Bits Register	0x00000000
0xD210	PMD_PMDCTL	PMD Physical Medium Device Control Register	0x00000000
0xD211	PMD_VS_CTRL	PMD PMD Reset Control Register	0x00000000

Table 29. ADIN1140 PHY_OA MMR Register Addresses

Memory Mapped Address	Register Name	Description	Reset Value
0x00	PHY_OA_TWEAKS_1	PHY_OA PHY Tweaks 1 Register	0x000000C0
0x03	PHY_OA_MAN- UAL_CTRL_REG_1	PHY_OA PHY Manual Control 1 Register	0x00000000
0x0F	PHY_OA_PLCA_EXT	PHY_OA PHY PLCA Ext Register	0x00000800
0x18	PHY_OA_PLCA_CTRL2	PHY_OA PHY PLCA Control 2 Register	0x0000FFFF
0x19	PHY_OA_PLCA_CTRL3	PHY_OA PHY PLCA Control 3 Register	0x0000FFFF
0x1A	PHY_OA_PLCA_CTRL4	PHY_OA PHY PLCA Control 4 Register	0x0000FFFF
0x1B	PHY_OA_PLCA_CTRL5	PHY_OA PHY PLCA Control 5 Register	0x000001FF
0x21	PHY_OA_PLCA_LUT_DBG	PHY_OA PLCA LUT Readback Register	0x00000000
0x61	PHY_OA_TD_VS_REG1	PHY_OA PHY Topology Discovery Timer Register	0x00000000
0x8A	PHY_OA_DCQ_JM_CFG0	PHY_OA PHY Jitter Monitor Configuration 0 Register	0x0000FF01
0x8B	PHY_OA_DCQ_JM_CFG1	PHY_OA PHY Jitter Monitor Configuration 1 Register	0x00000002
0x8C	PHY_OA_DCQ_JM_CFG2	PHY_OA PHY Jitter Monitor Configuration 2 Register	0x0000FFFF
0x8D	PHY_OA_DCQ_JM_CFG3	PHY_OA PHY Jitter Monitor Configuration 3 Register	0x0000FFFF
0x8E	PHY_OA_DCQ_JM_CFG4	PHY_OA PHY Jitter Monitor Configuration 4 Register	0x00000000
0x8F	PHY_OA_DCQ_JM_CFG5	PHY_OA PHY Jitter Monitor Configuration 5 Register	0x00000000
0x93	PHY_OA_DCQ_JM_RB0	PHY_OA PHY Jitter Monitor Readback 1 Register	0x00000000
0x97	PHY_OA_DCQ_JM_RB4	PHY_OA PHY Jitter Monitor Readback 4 Register	0x00000000
0x98	PHY_OA_DCQ_JM_RB5	PHY_OA PHY Jitter Monitor Readback 5 Register	0x00000000
0xCA00	PHY_OA_PLCA_IDVER	PHY_OA PHY PLCA ID Version Register	0x00000A10

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Table 29. ADIN1140 PHY_OA MMR Register Addresses (Continued)

Memory Mapped Address	Register Name	Description	Reset Value
0xCA01	PHY_OA_PLCA_CTRL0	PHY_OA PHY PLCA Control 0 Register	0x00000000
0xCA02	PHY_OA_PLCA_CTRL1	PHY_OA PHY PLCA Control 1 Register	0x000008FF
0xCA03	PHY_OA_PLCA_STATUS	PHY_OA PHY PLCA Status Register	0x00000000
0xCA04	PHY_OA_PLCA_TOTMR	PHY_OA PHY PLCA Duration of Transmit Opportunity Register	0x00000020
0xCA05	PHY_OA_PLCA_BURST	PHY_OA PHY PLCA Burst Register	0x00000080
0xCA06	PHY_OA_PLCA_DIAG	PHY_OA PHY PLCA Diagnostics Register	0x00000000
0xCE00	PHY_OA_TD_CTRL	PHY_OA PHY Topology Discovery Control Register	0x00000000
0xCE01	PHY_OA_TD_STAT	PHY_OA PHY Topology Discovery Status Register	0x00000000
0xCE02	PHY_OA_TD_DIST_RES_L OW	PHY_OA PHY Topology Discovery Destination Result Low Register	0x00000000
0xCE03	PHY_OA_TD_DIST_RES_U P	PHY_OA PHY Topology Discovery Destination Result Pulses Received Register	0x00000000
0xCE04	PHY_OA_TD_DLY_RES_L OW	PHY_OA PHY Topology Discovery Internal Delay Register	0x00000000
0xCE05	PHY_OA_TD_DLY_RES_U P	PHY_OA PHY Topology Discovery Internal Delay Receive Pulses Register	0x00000000
0xCE06	PHY_OA_TD_MNDLY_RE S_LOW	PHY_OA PHY Topology Discovery Remote Node Internal Delay Measurement Low Register	0x00000000
0xCE07	PHY_OA_TD_MNDLY_RE S_UP	PHY_OA PHY Topology Discovery Remote Node Internal Delay Measurement High Register	0x00000000
0xCE08	PHY_OA_TD_MNDLY_DU R	PHY_OA PHY Topology Discovery Internal Delay Duration Measurement Register	0x00000000
0xD000	PHY_OA_WS_STATUS	PHY_OA PHY Sleep/Wake Status Register	0x00008000
0xD001	PHY_OA_WS_CTRL	PHY_OA PHY Sleep/Wake Control Register	0x00000000

Table 30. ADIN1140 PHY_STD MMR Register Addresses

Memory Mapped Address	Register Name	Description	Reset Value
0x05	PHY_STD_DEV_IN_PACKAGE_3_1	PHY_STD Device in Package 3 Register 1	0x0000000B
0x05	PHY_STD_DEV_IN_PACKAGE_1_1	PHY_STD Device in Package 1 Register 1	0x0000000B
0x06	PHY_STD_DEV_IN_PACKAGE_1_2	PHY_STD Device in Package 1 Register 2	0x00001000
0x06	PHY_STD_DEV_IN_PACKAGE_3_2	PHY_STD Device in Package 3 Register 2	0x00001000
0x0B	PHY_STD_PMA_PMD_EXTENDED_ABILITY2	PHY_STD Physical Medium Attachment Physical Medium Dependent Extended Ability2 Register	0x00000800
0x32	PHY_STD_PMA_PMD_EXTENDED_ABILITY	PHY_STD Physical Medium Attachment, Physical Medium Dependent Extended Ability Register	0x00000008
0x8F3	PHY_STD_PCS_CONTROL	PHY_STD Physical Coding Sublayer Control Register	0x00000000
0x8F4	PHY_STD_PCS_STATUS	PHY_STD Physical Coding Sublayer Status Register	0x00000000
0x8F5	PHY_STD_PCS_DIAGNOSTIC	PHY_STD Physical Coding Sublayer Diagnostic Register	0x00000000
0x8F6	PHY_STD_PCS_DIAGNOSTIC_2	PHY_STD Physical Coding Sublayer Diagnostic 2 Register	0x00000000
0x8F9	PHY_STD_T1S_PMA_CONTROL	PHY_STD T1S Physical Medium Attachment Control Register	0x00000400
0x8FA	PHY_STD_T1S_PMA_STATUS	PHY_STD T1S Physical Medium Attachment Status Register	0x00002E00
0x8FB	PHY_STD_T1S_TEST_MODE_CONTROL	PHY_STD T1S Test Mode Control Register	0x00000000
0xFF00	PHY_STD_CONTROL_REGISTER	PHY_STD Control Register	0x00001000
0xFF01	PHY_STD_STATUS_REGISTER	PHY_STD Status Register	0x0000082D
0xFF02	PHY_STD_PHY_IDENTIFIER_1	PHY_STD Identifier 1 Register	0x00000283
0xFF03	PHY_STD_PHY_IDENTIFIER_2	PHY_STD Identifier 2 Register	0x0000BE00

REGISTER SUMMARY: ALWAYS ON DOMAIN REGISTER MAP (ALWAYS_ON)

This register map is part of the always on domain and is powered by VBAT.

Table 31. ALWAYS_ON Register Summary

Address	Name	Description	Reset	Access
0xB702	ALWAYS_ON_CONFIGURATION_FIELDS_0	Configuration Fields 0 Register.	0x23	R/W
0xB703	ALWAYS_ON_CONFIGURATION_FIELDS_1	Configuration Fields 1 Register.	0x04	R/W

REGISTER DETAILS: ALWAYS ON DOMAIN REGISTER MAP (ALWAYS_ON)

CONFIGURATION FIELDS 0 REGISTER

OA-SPI Address: 0xB702, MMS: 0xA, Reset: 0x0023

The ALWAYS_ON_CONFIGURATION_FIELDS_0 register is used to configure power settings as described in Table 32.

Table 32. Bit Descriptions for ALWAYS_ON_CONFIGURATION_FIELDS_0

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W
6	CFG_WAKE_PIN_POL	Wake pin polarity. The ALWAYS_ON_CONFIGURATION_FIELDS_0.CFG_WAKE_PIN_POL bit is used to configure the polarity of the wake pin. 0: Active high. 1: Active low.	0x0	R/W
[5:3]	CFG_UV_THRESHOLD	Undervoltage threshold. The ALWAYS_ON_CONFIGURATION_FIELDS_0.CFG_UV_THRESHOLD bits are used to configure the undervoltage threshold. 000: 5.75V. 001: 6.25V. 010: 6.75V. 011: 7.25V. 100: 7.75V. 101: 8.25V. 110: 8.75V. 111: 9.25V.	0x4	R/W
[2:0]	CFG_DUV_THRESHOLD	Deep undervoltage threshold. The ALWAYS_ON_CONFIGURATION_FIELDS_0.CFG_DUV_THRESHOLD bits are used to configure the deep undervoltage threshold. 000: 4.75V. 001: 5.25V. 010: 5.75V. 011: 6.25V. 100: 6.75V. 101: 7.25V. 110: 7.75V. 111: 8.25V.	0x3	R/W

CONFIGURATION FIELDS 1 REGISTER

OA-SPI Address: 0xB703, MMS: 0xA, Reset: 0x0004

The ALWAYS_ON_CONFIGURATION_FIELDS_1 register is used to configure power settings as described in Table 33.

Table 33. Bit Descriptions for ALWAYS_ON_CONFIGURATION_FIELDS_1

Bits	Bit Name	Description	Reset	Access
7	CFG_VALID	Enables and validates all configuration controls. The ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VALID bit is used to enable and validate all configuration controls in the ALWAYS_ON_CONFIGURATION_FIELDS_0, ALWAYS_ON_CONFIGURATION_FIELDS_1 and ALWAYS_ON_CONFIGURATION_FIELDS_2 registers. 0: Disable. 1: Enable.	0x0	R/W
6	CFG_VBAT_OV_FLAG_EN	Vbat monitor overvoltage enable. The ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VBAT_OV_FLAG_EN bit is used to enable the Vbat monitor for overvoltage. 0: Disable. 1: Enable.	0x0	R/W

REGISTER DETAILS: ALWAYS ON DOMAIN REGISTER MAP (ALWAYS_ON)

Table 33. Bit Descriptions for ALWAYS_ON_CONFIGURATION_FIELDS_1 (Continued)

Bits	Bit Name	Description	Reset	Access
5	CFG_VBAT_UV_FLAG_EN	Long term undervoltage enable. The ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VBAT_UV_FLAG_EN bit is used to enable the Vbat monitor for long term undervoltage. 0: Disable. 1: Enable.	0x0	R/W
4	CFG_VBAT_DEEP_UV_FLAG_EN	Deep undervoltage enable. The ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_VBAT_DEEP_UV_FLAG_EN bit is used to enable Vbat monitor for deep undervoltage. 0: Disable. 1: Enable.	0x0	R/W
3	RESERVED	Reserved.	0x0	R/W
[2:0]	CFG_OV_THRESHOLD	Overvoltage threshold. The ALWAYS_ON_CONFIGURATION_FIELDS_1.CFG_OV_THRESHOLD bits are used to configure the overvoltage threshold. 000: 16.5V. 001: 17V. 010: 17.5V. 011: 18V. 100: 18.5V. 101: 19V. 110: 19.5V. 111: 20V.	0x4	R/W

REGISTER SUMMARY: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 34. IO_LV Register Summary

Address	Name	Description	Reset	Access
0xC801	IO_LV_DEBUG_DATA_CTRL	Debug Data Control Register.	0x0000	R/W
0xC802	IO_LV_IO_PULLDOWN_CTRL_1	IO Pull-down Control 1 Register.	0x0000	R/W
0xC803	IO_LV_IO_PULLDOWN_CTRL_2	IO Pull-down Control 2 Register.	0x0000	R/W
0xC804	IO_LV_MAC_INTERFACE	MAC Interface Register.	0x000E	R/W
0xC805	IO_LV_REVISION_CONTROL	Revision Control Register.	0x0000	R
0xC806	IO_LV_BOOTLOADER_STATUS_0	Bootloader Status 0 Register.	0x0000	R
0xC807	IO_LV_BOOTLOADER_STATUS_1	Bootloader Status 1 Register.	0x0000	R
0xC808	IO_LV_BOOTLOADER_STATUS_2	Bootloader Status 2 Register.	0x0000	R
0xC809	IO_LV_BOOTLOADER_STATUS_3	Bootloader Status 3 Register.	0x0000	R
0xC80A	IO_LV_BOOTLOADER_STATUS_4	Bootloader Status 4 Register.	0x0000	R
0xC80B	IO_LV_BOOTLOADER_STATUS_5	Bootloader Status 5 Register.	0x0000	R
0xC80C	IO_LV_BOOTLOADER_STATUS_6	Bootloader Status 6 Register.	0x0000	R
0xC80D	IO_LV_BOOTLOADER_STATUS_7	Bootloader Status 7 Register.	0x0000	R
0xC80F	IO_LV_SLEEP_WAKE_CFG	Sleep Wake Configuration Register.	0x0100	R/W
0xC810	IO_LV_SLEEPWAKE_CMD	Sleep/wake Command Register.	0x0000	R/W
0xC811	IO_LV_SLEEPWAKE_STATUS	Sleepwake Status Register.	0x0000	R
0xC813	IO_LV_BOOTLOADER_RB_8	Bootloader Readback 8 Register.	0x0000	R/W
0xC814	IO_LV_BOOTLOADER_RB_9	Bootloader Readback 9 Register.	0x0000	R/W
0xC815	IO_LV_BOOTLOADER_RB_10	Bootloader Readback 10 Register.	0x0000	R/W
0xC816	IO_LV_BOOTLOADER_RB_11	Bootloader Readback 11 Register.	0x0000	R/W
0xC817	IO_LV_BOOTLOADER_RB_12	Bootloader Readback 12 Register.	0x0000	R/W
0xC818	IO_LV_BOOTLOADER_RB_13	Bootloader Readback 13 Register.	0x0000	R/W
0xC819	IO_LV_BOOTLOADER_RB_14	Bootloader Readback 14 Register.	0x0000	R/W
0xC81A	IO_LV_BOOTLOADER_RB_15	Bootloader Readback 15 Register.	0x0000	R/W
0xC81B	IO_LV_BOOTLOADER_RB_16	Bootloader Readback 16 Register.	0x0000	R/W
0xC81C	IO_LV_BOOTLOADER_RB_17	Bootloader Readback 17 Register.	0x0000	R/W
0xC81D	IO_LV_BOOTLOADER_RB_18	Bootloader Readback 18 Register.	0x0000	R/W
0xC81E	IO_LV_BOOTLOADER_RB_19	Bootloader Readback 19 Register.	0x0000	R/W
0xC81F	IO_LV_BOOTLOADER_RB_20	Bootloader Readback 20 Register.	0x0000	R/W
0xC820	IO_LV_BOOTLOADER_RB_21	Bootloader Readback 21 Register.	0x0000	R/W
0xC821	IO_LV_BOOTLOADER_RB_22	Bootloader Readback 22 Register.	0x0000	R/W
0xC822	IO_LV_BOOTLOADER_RB_23	Bootloader Readback 23 Register.	0x0000	R/W
0xC823	IO_LV_BOOTLOADER_RB_24	Bootloader Readback 24 Register.	0x0000	R/W
0xC824	IO_LV_BOOTLOADER_RB_25	Bootloader Readback 25 Register.	0x0000	R/W
0xC825	IO_LV_BOOTLOADER_RB_26	Bootloader Readback 26 Register.	0x0000	R/W
0xC840	IO_LV_DEBUG_DATA_CONTROL_0	Debug Data Control 0.	0x7F7F	R/W
0xC841	IO_LV_DEBUG_DATA_CONTROL_1	Debug Data Control 1.	0x7F7F	R/W
0xC844	IO_LV_DEBUG_DATA_CONTROL_4	Debug Data Control 4.	0x7F7F	R/W
0xC845	IO_LV_DEBUG_DATA_CONTROL_5	Debug Data Control 5.	0x7F7F	R/W
0xC849	IO_LV_MISC_CONTROL	Miscellaneous Control Register.	0x2000	R/W
0xC84F	IO_LV_IO_GLITCH_REJECT_0	IO Glitch Reject 0 Register.	0xFFFF	R/W
0xC850	IO_LV_IO_GLITCH_REJECT_1	IO Glitch Reject 1 Register.	0x033F	R/W
0xC851	IO_LV_IO_DRIVE_STRENGTH_0	IO Drive Strength 0 Register.	0x5555	R/W
0xC852	IO_LV_IO_DRIVE_STRENGTH_1	IO Drive Strength 1 Register.	0x0055	R/W
0xC853	IO_LV_IO_HYSTHERESIS_ENABLE	IO Hysteresis Enable Register.	0x0000	R/W
0xC854	IO_LV_IO_SLEW_RATE	IO Slew Rate Register.	0x0000	R/W
0xC860	IO_LV_SLEEP_HISTORY	Sleep History Register.	0x0000	R/W

REGISTER SUMMARY: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 34. IO_LV Register Summary (Continued)

Address	Name	Description	Reset	Access
0xC882	IO_LV_MANUAL_INTERRUPT	Manual Interrupt Register.	0x0000	R/W
0xC883	IO_LV_SSC_MUX_SEL_SAFE_ACTIVE_RB	Pin Safe Mode Status Register.	0x0000	R
0xC884	IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB	SSC Safe Checks Triggered Readback Register.	0x0000	R
0xC885	IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB_2	SSC Safe Checks Triggered Readback 2 Register.	0x0000	R
0xC886	IO_LV_SSC_SAFE_CHECKS_TRIGGER	SSC Safe Checks Triggered Readback (Sticky) Register.	0x0000	R
0xC887	IO_LV_SSC_SAFE_CHECKS_TRIGGERED_STICKY_RB_2	SSC Safe Checks Triggered Readback 2 (Sticky) Register.	0x0000	R
0xC888	IO_LV_SSC_GENERAL_RB	SSC General Readback Register.	0x0000	R
0xC889	IO_LV_SSC_ALIVE_COUNTER_RB	SSC Alive Counter Read Register.	0x0000	R
0xC88A	IO_LV_SSC_SAFE_SA_IF_CONTROLS	SSC Safe SAIF Control Register.	0x0000	R/W
0xC88B	IO_LV_SSC_SAFE_SA_IF_CONTROLS_2	SSC Safe SAIF Control 2 Register.	0x0000	R/W
0xC88C	IO_LV_SSC_SAFE_SA_IF_CONTROLS_3	SSC Safe SAIF Control 3 Register.	0x0000	R/W
0xC88D	IO_LV_SSC_MONITOR_POLARITY	SSC Monitor Polarity Register.	0x0000	R/W
0xC88E	IO_LV_SSC_MONITOR_POLARITY_2	SSC Monitor Polarity 2 Register.	0x0000	R/W
0xC88F	IO_LV_SSC_TIMEOUT_TIME_ETHERNET_TRAFFIC	SSC Ethernet Frame Timeout.	0x0000	R/W
0xC890	IO_LV_SSC_TIMEOUT_TIME_DEVICE_UNATTENDED	SSC Device Unattended Timeout.	0x0000	R/W
0xC893	IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN	SSC Auto Return To Functional Enable Register.	0x0000	R/W
0xC894	IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN2	SSC Auto Return To Functional En2.	0x0000	R/W
0xC895	IO_LV_SSC_CONTROLS	SSC Control Register.	0x2000	R/W
0xC896	IO_LV_SSC_SAFE_CHECKS_ENABLE	SSC Safe Checks Enable Register.	0x0000	R/W
0xC897	IO_LV_SSC_SAFE_CHECKS_ENABLE_2	SSC Safe Checks Enable 2 Register.	0x0000	R/W
0xC898	IO_LV_SSC_MONITOR_TRIGGERS	SSC Monitor Triggers Register.	0x0000	R/W
0xC899	IO_LV_SSC_MISC	SSC Miscellaneous Register.	0x0000	R/W
0xC89A	IO_LV_SSC_RECOVERED_DATA_FROM_AO	SSC Recovered Data From Always On Register.	0x0000	R/W
0xC8FE	IO_LV_BLOCK_RESET_CONTROL	Block Reset Control Register.	0x0000	R/W
0xC8FF	IO_LV_RESET_CONTROL	Reset Control Register.	0x0000	R/W
0xC900	IO_LV_INTER_DIE_SERIAL_COMMUNICATION	Inter Die Serial Communication Register.	0x0000	R/W
0xC901	IO_LV_GPTP_SYNC_COUNT	gPTP Sync Count Register.	0x0000	R
0xC902	IO_LV_GPTP_SYNC_COUNT_1	gPTP Sync Count 1 Register.	0x0000	R
0xC903	IO_LV_GPTP_ONESTEP_COUNT	gPTP Onestep Count Register.	0x0000	R
0xC904	IO_LV_GPTP_ONESTEP_COUNT_1	gPTP Onestep Count 1 Register.	0x0000	R
0xC905	IO_LV_GPTP_FOLLOWUP_COUNT	gPTP Followup Count Register.	0x0000	R
0xC906	IO_LV_GPTP_FOLLOWUP_COUNT_1	gPTP Followup Count 1 Register.	0x0000	R
0xC907	IO_LV_GPTP_NUM_LOCKS	gPTP Number Locks Register.	0x0000	R
0xC908	IO_LV_GPTP_NUM_UNLOCKS	gPTP Number of Unlocks Register.	0x0000	R
0xC909	IO_LV_GPTP_SEQUENCEID	gPTP Sequence ID Register.	0x0000	R
0xC90B	IO_LV_GPTP_LOCK_THRESHOLD	gPTP Lock Threshold Register.	0x044C	R/W
0xC910	IO_LV_GPTP_TIME_ERROR	gPTP Time Error Register.	0x0000	R
0xC911	IO_LV_GPTP_TIME_ERROR_1	gPTP Time Error 1 Register.	0x0000	R
0xC912	IO_LV_GPTP_MEAN_LINK_DELAY	gPTP Mean Link Delay Register.	0x0000	R/W
0xC913	IO_LV_GPTP_MEAN_LINK_DELAY_1	gPTP Mean Link Delay 1 Register.	0x0000	R/W
0xC915	IO_LV_GPTP_STATUS_1	gPTP Status 1 Register.	0x0000	R
0xC916	IO_LV_GPTP_RELOCK	gPTP Relock Register.	0x0000	R/W

REGISTER SUMMARY: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 34. IO_LV Register Summary (Continued)

Address	Name	Description	Reset	Access
0xC917	IO_LV_GPTP_RELOCK_1	gPTP Relock 1 Register.	0x0005	R/W
0xC92A	IO_LV_GPTP_CONFIG	gPTP Configuration Register.	0x8928	R/W
0xC93A	IO_LV_TIC_STATUS_FLAGS_8_AND_9	TIC Status Flags 8 and 9 Register.	0x0000	R
0xC93B	IO_LV_TIC_STATUS_FLAGS_10_AND_11	TIC Status Flags 10 and 11 Register.	0x0000	R
0xC944	IO_LV_TIC_STATUS_FLAGS_28_AND_29	TIC Status Flags 28 and 29 Register.	0x0000	R
0xC947	IO_LV_TIC_STATUS_FLAGS_34_AND_35	TIC Status Flags 34 and 35 Register.	0x0000	R
0xC94D	IO_LV_TIC_CONTROL0	TIC Control Register 0.	0x8480	R/W
0xC94E	IO_LV_TIC_CONTROL1	TIC Control Register 1.	0x041E	R/W
0xC961	IO_LV_TIC_ENABLE_8_PHY_REG0	TIC Enable 8 PHY Register 0.	0x0000	R/W
0xC962	IO_LV_TIC_ENABLE_8_PHY_REG1	TIC Enable 8 PHY Register 1.	0x0000	R/W
0xC963	IO_LV_TIC_ENABLE_9_MAC_REG0	TIC Enable 9 MAC Register 0.	0x0000	R/W
0xC964	IO_LV_TIC_ENABLE_9_MAC_REG1	TIC Enable 9 MAC Register 1.	0x0000	R/W
0xC965	IO_LV_TIC_ENABLE_10_REG0	TIC Enable 10 PLCA Register 0.	0x0000	R/W
0xC989	IO_LV_TIC_ENABLE_28_MISC0_REG0	TIC Enable 28 Miscellaneous 0 Register 0.	0x0000	R/W
0xC98A	IO_LV_TIC_ENABLE_28_MISC0_REG1	TIC Enable 28 Miscellaneous 0 Register 1.	0x0000	R/W
0xC98B	IO_LV_TIC_ENABLE_29_MISC1_REG0	TIC Enable 29 Miscellaneous 1 Register 0.	0x0000	R/W
0xC98C	IO_LV_TIC_ENABLE_29_MISC1_REG1	TIC Enable 29 Miscellaneous 1 Register 1.	0x0000	R/W
0xC9A0	IO_LV_TIC_CLEAR_8_PHY_REG0	TIC Clear 8 PHY Register 0.	0x0000	R/W
0xC9A1	IO_LV_TIC_CLEAR_8_PHY_REG1	TIC Clear 8 PHY Register 1.	0x0000	R/W
0xC9A2	IO_LV_TIC_CLEAR_9_MAC_REG0	TIC Clear 9 MAC Register 0.	0x0000	R/W
0xC9A3	IO_LV_TIC_CLEAR_9_MAC_REG1	TIC Clear 9 MAC Register 1.	0x0000	R/W
0xC9A4	IO_LV_TIC_CLEAR_10_REG0	TIC Clear 10 PLCA Register 0.	0x0000	R/W
0xC9C8	IO_LV_TIC_CLEAR_28_MISC0_REG0	TIC Clear 28 Miscellaneous 0 Register 0.	0x0000	R/W
0xC9C9	IO_LV_TIC_CLEAR_28_MISC0_REG1	TIC Clear 28 Miscellaneous 0 Register 1.	0x0000	R/W
0xC9CA	IO_LV_TIC_CLEAR_29_MISC1_REG0	TIC Clear 29 Miscellaneous 1 Register 0.	0x0000	R/W
0xC9CB	IO_LV_TIC_CLEAR_29_MISC1_REG1	TIC Clear 29 Miscellaneous 1 Register 1.	0x0000	R/W
0xC9CE	IO_LV_CLOCK_GENERATION_OUTPUTS	Clock Generation Outputs Register.	0x3C57	R/W
0xC9CF	IO_LV_CLOCK_GENERATION_OUTPUTS2	Clock Generation Outputs2 Register.	0x0412	R/W
0xC9DF	IO_LV_TP_OUT_EN_SA_IF	TP Output SAIF Pin Driver Enable Register.	0x0000	R/W
0xC9E0	IO_LV_TP_IP_EN_SA_IF	TP Input Receiver SAIF Pin Enable Register.	0x0000	R/W
0xC9E2	IO_LV_EFUSE_REG	Efuse Register.	0x0000	R
0xC9EF	IO_LV_GPTP_DOMAINS	gPTP Domains Register.	0x0100	R/W
0xC9F6	IO_LV_TIC_ENABLE_34_GPIO1_REG0	TIC Enable 34 GPIO 1 Register 0.	0x0000	R/W
0xC9F7	IO_LV_TIC_ENABLE_34_GPIO1_REG1	TIC Enable 34 GPIO 1 Register 1.	0x0000	R/W
0xC9FA	IO_LV_TIC_CLEAR_34_GPIO1_REG0	TIC Clear 34 GPIO0 Register 0.	0x0000	R/W
0xC9FB	IO_LV_TIC_CLEAR_34_GPIO1_REG1	TIC Clear 34 GPIO0 Register 1.	0x0000	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

DEBUG DATA CONTROL REGISTER

OA-SPI Address: 0xC801, MMS: 0xA, Reset: 0x0000

The IO_LV_DEBUG_DATA_CTRL register controls the internal signal muxing enable of the different pins

Table 35. Bit Descriptions for IO_LV_DEBUG_DATA_CTRL

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:0]	SA_IF_DEBUG_DATA_EN	SAIF Debug Data Enable. This bit-field enables the muxing of internal signal through the different Sensor-Actuator Interface Pins. Each bit of this 12-bit field corresponds to an individual SAIF pin, where bit 0 relates to SAIF pin 0, bit 1 relates to SAIF pin 1, etc. The signal to be brought out is selected in the registers debug_data_control_X.	0x0	R/W

IO PULL-DOWN CONTROL 1 REGISTER

OA-SPI Address: 0xC802, MMS: 0xA, Reset: 0x0000

The IO_LV_IO_PULLDOWN_CTRL_1 register is used to configure the weak pull-up/pull-down of the SAIF0 pin.

Table 36. Bit Descriptions for IO_LV_IO_PULLDOWN_CTRL_1

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R/W
[1:0]	IO_LV_PULLDOWN_SA_IF_0	SAIF0 pull-up/pull-down. The IO_LV_IO_PULLDOWN_CTRL_1.IO_PULLDOWN_SA_IF_0 bits are used to configure the weak pull-up/pull-down of the SAIF0 pin. 00: No Weak Pull-Up or Pull-Down. 01: Weak Pull-Down. 10: No Weak Pull-Up or Pull-Down. 11: Weak Pull-Up.	0x0	R/W

IO PULL-DOWN CONTROL 2 REGISTER

OA-SPI Address: 0xC803, MMS: 0xA, Reset: 0x0000

The IO_LV_IO_PULLDOWN_CTRL_2 register is used to configure the weak pull-up/pull-down of the SAIF9-11 pins.

Table 37. Bit Descriptions for IO_LV_IO_PULLDOWN_CTRL_2

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:6]	IO_LV_PULLDOWN_SA_IF_11	SAIF11 pull-up/pull-down. The IO_LV_IO_PULLDOWN_CTRL_2.IO_PULLDOWN_SA_IF_11 bits are used to configure the weak pull-up/pull-down of the SAIF11 pin. 00: No Weak Pull-Up or Pull-Down. 01: Weak Pull-Down. 10: No Weak Pull-Up or Pull-Down. 11: Weak Pull-Up.	0x0	R/W
[5:4]	IO_LV_PULLDOWN_SA_IF_10	SAIF10 pull-up/pull-down. The IO_LV_IO_PULLDOWN_CTRL_2.IO_PULLDOWN_SA_IF_10 bits are used to configure the weak pull-up/pull-down of the SAIF10 pin. 00: No Weak Pull-Up or Pull-Down. 01: Weak Pull-Down. 10: No Weak Pull-Up or Pull-Down. 11: Weak Pull-Up.	0x0	R/W
[3:2]	IO_LV_PULLDOWN_SA_IF_9	SAIF9 pull-up/pull-down. The IO_LV_IO_PULLDOWN_CTRL_2.IO_PULLDOWN_SA_IF_9 bits are used to configure the weak pull-up/pull-down of the SAIF9 pin. 00: No Weak Pull-Up or Pull-Down.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 37. Bit Descriptions for IO_LV_IO_PULLDOWN_CTRL_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		01: Weak Pull-Down. 10: No Weak Pull-Up or Pull-Down. 11: Weak Pull-Up.		
[1:0]	RESERVED	Reserved.	0x0	R/W

MAC INTERFACE REGISTER

OA-SPI Address: 0xC804, MMS: 0xA, Reset: 0x000E

The IO_LV_MAC_INTERFACE register is used to enable MAC interrupt request and MAC timer signals.

Table 38. Bit Descriptions for IO_LV_MAC_INTERFACE

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x3	R
1	MAC_INTRQ_EN	MAC INTRQ signal enable. The IO_LV_MAC_INTERFACE.MAC_INTRQ_EN bit is used to enable MAC interrupt request signals when the OA-SPI is connected. 0: Disabled. 1: Enabled.	0x1	R/W
0	MAC_TIMER_EN	MAC timer signal enable. The IO_LV_MAC_INTERFACE.MAC_TIMER_EN bit is used to enable MAC timer signals when the OA-SPI is connected. 0: Disabled. 1: Enabled.	0x0	R/W

REVISION CONTROL REGISTER

OA-SPI Address: 0xC805, MMS: 0xA, Reset: 0x0000

The IO_LV_REVISION_CONTROL register indicates chip revision information.

Table 39. Bit Descriptions for IO_LV_REVISION_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:4]	REV_CODE_DIG	Chip revision code digital. The IO_LV_REVISION_CONTROL.REV_CODE_DIG bit field indicates the chip revision digital code.	0x0	R
[3:0]	REV_CODE	Chip revision code. The IO_LV_REVISION_CONTROL.REV_CODE bit field indicates the chip revision code. 00: LV 0.1 (U1). 01: LV 0.2 (U2). 10: LV 0.5 (U5) and 1.0. 11: LV 0.3 (U3), 0.4 (U4) and 1.0.	0x0	R

BOOTLOADER STATUS 0 REGISTER

OA-SPI Address: 0xC806, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_STATUS_0 register indicates the bootloader block status as described below.

Table 40. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_0

Bits	Bit Name	Description	Reset	Access
[15:14]	BLOCK_STATUS_7	Bootloader block 7 status. The IO_LV_BOOTLOADER_STATUS_0.BLOCK_STATUS_7 bit field indicates the status of bootloader block 7. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 40. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_0 (Continued)

Bits	Bit Name	Description	Reset	Access
[13:12]	BLOCK_STATUS_6	Bootloader block 6 status. The IO_LV_BOOTLOADER_STATUS_0.BLOCK_STATUS_6 bit field indicates the status of bootloader block 6. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[11:10]	BLOCK_STATUS_5	Bootloader block 5 status. The IO_LV_BOOTLOADER_STATUS_0.BLOCK_STATUS_5 bit field indicates the status of bootloader block 5. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[9:8]	BLOCK_STATUS_4	Bootloader block 4 status. The IO_LV_BOOTLOADER_STATUS_0.BLOCK_STATUS_4 bit field indicates the status of bootloader block 4. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[7:6]	BLOCK_STATUS_3	Bootloader block 3 status. The IO_LV_BOOTLOADER_STATUS_0.BLOCK_STATUS_3 bit field indicates the status of bootloader block 3. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[5:4]	BLOCK_STATUS_2	Bootloader block 2 status. The IO_LV_BOOTLOADER_STATUS_0.BLOCK_STATUS_2 bit field indicates the status of bootloader block 2. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[3:2]	BLOCK_STATUS_1	Bootloader block 1 status. The IO_LV_BOOTLOADER_STATUS_0.BLOCK_STATUS_1 bit field indicates the status of bootloader block 1. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[1:0]	BLOCK_STATUS_0	Bootloader block 0 status. The IO_LV_BOOTLOADER_STATUS_0.BLOCK_STATUS_0 bit field indicates the status of bootloader block 0. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R

BOOTLOADER STATUS 1 REGISTER

OA-SPI Address: 0xC807, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_STATUS_1 register indicates the bootloader block status as described below.

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 41. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_1

Bits	Bit Name	Description	Reset	Access
[15:14]	BLOCK_STATUS_15	Bootloader block 15 status. The IO_LV_BOOTLOADER_STATUS_1.BLOCK_STATUS_15 bit field indicates the status of bootloader block 15. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[13:12]	BLOCK_STATUS_14	Bootloader block 14 status. The IO_LV_BOOTLOADER_STATUS_1.BLOCK_STATUS_14 bit field indicates the status of bootloader block 14. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[11:10]	BLOCK_STATUS_13	Bootloader block 13 status. The IO_LV_BOOTLOADER_STATUS_1.BLOCK_STATUS_13 bit field indicates the status of bootloader block 13. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[9:8]	BLOCK_STATUS_12	Bootloader block 12 status. The IO_LV_BOOTLOADER_STATUS_1.BLOCK_STATUS_12 bit field indicates the status of bootloader block 12. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[7:6]	BLOCK_STATUS_11	Bootloader block 11 status. The IO_LV_BOOTLOADER_STATUS_1.BLOCK_STATUS_11 bit field indicates the status of bootloader block 11. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[5:4]	BLOCK_STATUS_10	Bootloader block 10 status. The IO_LV_BOOTLOADER_STATUS_1.BLOCK_STATUS_10 bit field indicates the status of bootloader block 10. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[3:2]	BLOCK_STATUS_9	Bootloader block 9 status. The IO_LV_BOOTLOADER_STATUS_1.BLOCK_STATUS_9 bit field indicates the status of bootloader block 9. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[1:0]	BLOCK_STATUS_8	Bootloader block 8 status. The IO_LV_BOOTLOADER_STATUS_1.BLOCK_STATUS_8 bit field indicates the status of bootloader block 8. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

BOOTLOADER STATUS 2 REGISTER

OA-SPI Address: 0xC808, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_STATUS_2 register indicates the bootloader block status as described below.

Table 42. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_2

Bits	Bit Name	Description	Reset	Access
[15:14]	BLOCK_STATUS_23	Bootloader block 23 status. The IO_LV_BOOTLOADER_STATUS_2.BLOCK_STATUS_23 bit field indicates the status of bootloader block 23. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[13:12]	BLOCK_STATUS_22	Bootloader block 22 status. The IO_LV_BOOTLOADER_STATUS_2.BLOCK_STATUS_22 bit field indicates the status of bootloader block 22. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[11:10]	BLOCK_STATUS_21	Bootloader block 21 status. The IO_LV_BOOTLOADER_STATUS_2.BLOCK_STATUS_21 bit field indicates the status of bootloader block 21. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[9:8]	BLOCK_STATUS_20	Bootloader block 20 status. The IO_LV_BOOTLOADER_STATUS_2.BLOCK_STATUS_20 bit field indicates the status of bootloader block 20. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[7:6]	BLOCK_STATUS_19	Bootloader block 19 status. The IO_LV_BOOTLOADER_STATUS_2.BLOCK_STATUS_19 bit field indicates the status of bootloader block 19. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[5:4]	BLOCK_STATUS_18	Bootloader block 18 status. The IO_LV_BOOTLOADER_STATUS_2.BLOCK_STATUS_18 bit field indicates the status of bootloader block 18. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[3:2]	BLOCK_STATUS_17	Bootloader block 17 status. The IO_LV_BOOTLOADER_STATUS_2.BLOCK_STATUS_17 bit field indicates the status of bootloader block 17. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[1:0]	BLOCK_STATUS_16	Bootloader block 16 status. The IO_LV_BOOTLOADER_STATUS_2.BLOCK_STATUS_16 bit field indicates the status of bootloader block 16. 00: Not initialized.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 42. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		01: Valid. 10: Valid. 11: Corrupted.		

BOOTLOADER STATUS 3 REGISTER

OA-SPI Address: 0xC809, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_STATUS_3 register indicates the bootloader block status as described below.

Table 43. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_3

Bits	Bit Name	Description	Reset	Access
[15:14]	BLOCK_STATUS_31	Bootloader block 31 status. The IO_LV_BOOTLOADER_STATUS_3.BLOCK_STATUS_31 bit field indicates the status of bootloader block 31. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[13:12]	BLOCK_STATUS_30	Bootloader block 30 status. The IO_LV_BOOTLOADER_STATUS_3.BLOCK_STATUS_30 bit field indicates the status of bootloader block 30. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[11:10]	BLOCK_STATUS_29	Bootloader block 29 status. The IO_LV_BOOTLOADER_STATUS_3.BLOCK_STATUS_29 bit field indicates the status of bootloader block 29. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[9:8]	BLOCK_STATUS_28	Bootloader block 28 status. The IO_LV_BOOTLOADER_STATUS_3.BLOCK_STATUS_28 bit field indicates the status of bootloader block 28. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[7:6]	BLOCK_STATUS_27	Bootloader block 27 status. The IO_LV_BOOTLOADER_STATUS_3.BLOCK_STATUS_27 bit field indicates the status of bootloader block 27. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[5:4]	BLOCK_STATUS_26	Bootloader block 26 status. The IO_LV_BOOTLOADER_STATUS_3.BLOCK_STATUS_26 bit field indicates the status of bootloader block 26. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[3:2]	BLOCK_STATUS_25	Bootloader block 25 status. The IO_LV_BOOTLOADER_STATUS_3.BLOCK_STATUS_25 bit field indicates the status of bootloader block 25. 00: Not initialized.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 43. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_3 (Continued)

Bits	Bit Name	Description	Reset	Access
		01: Valid. 10: Valid. 11: Corrupted.		
[1:0]	BLOCK_STATUS_24	Bootloader block 24 status. The IO_LV_BOOTLOADER_STATUS_3.BLOCK_STATUS_24 bit field indicates the status of bootloader block 24. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R

BOOTLOADER STATUS 4 REGISTER

OA-SPI Address: 0xC80A, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_STATUS_4 register indicates the bootloader block status as described below.

Table 44. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_4

Bits	Bit Name	Description	Reset	Access
[15:14]	BLOCK_STATUS_39	Bootloader block 39 status. The IO_LV_BOOTLOADER_STATUS_4.BLOCK_STATUS_39 bit field indicates the status of bootloader block 39. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[13:12]	BLOCK_STATUS_38	Bootloader block 38 status. The IO_LV_BOOTLOADER_STATUS_4.BLOCK_STATUS_38 bit field indicates the status of bootloader block 38. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[11:10]	BLOCK_STATUS_37	Bootloader block 37 status. The IO_LV_BOOTLOADER_STATUS_4.BLOCK_STATUS_37 bit field indicates the status of bootloader block 37. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[9:8]	BLOCK_STATUS_36	Bootloader block 36 status. The IO_LV_BOOTLOADER_STATUS_4.BLOCK_STATUS_36 bit field indicates the status of bootloader block 36. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[7:6]	BLOCK_STATUS_35	Bootloader block 35 status. The IO_LV_BOOTLOADER_STATUS_4.BLOCK_STATUS_35 bit field indicates the status of bootloader block 35. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[5:4]	BLOCK_STATUS_34	Bootloader block 34 status. The IO_LV_BOOTLOADER_STATUS_4.BLOCK_STATUS_34 bit field indicates the status of bootloader block 34. 00: Not initialized.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 44. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_4 (Continued)

Bits	Bit Name	Description	Reset	Access
		01: Valid. 10: Valid. 11: Corrupted.		
[3:2]	BLOCK_STATUS_33	Bootloader block 33 status. The IO_LV_BOOTLOADER_STATUS_4.BLOCK_STATUS_33 bit field indicates the status of bootloader block 33. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[1:0]	BLOCK_STATUS_32	Bootloader block 32 status. The IO_LV_BOOTLOADER_STATUS_4.BLOCK_STATUS_32 bit field indicates the status of bootloader block 32. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R

BOOTLOADER STATUS 5 REGISTER

OA-SPI Address: 0xC80B, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_STATUS_5 register indicates the bootloader block status as described below.

Table 45. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_5

Bits	Bit Name	Description	Reset	Access
[15:14]	BLOCK_STATUS_47	Bootloader block 47 status. The IO_LV_BOOTLOADER_STATUS_5.BLOCK_STATUS_47 bit field indicates the status of bootloader block 47. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[13:12]	BLOCK_STATUS_46	Bootloader block 46 status. The IO_LV_BOOTLOADER_STATUS_5.BLOCK_STATUS_46 bit field indicates the status of bootloader block 46. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[11:10]	BLOCK_STATUS_45	Bootloader block 45 status. The IO_LV_BOOTLOADER_STATUS_5.BLOCK_STATUS_45 bit field indicates the status of bootloader block 45. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[9:8]	BLOCK_STATUS_44	Bootloader block 44 status. The IO_LV_BOOTLOADER_STATUS_5.BLOCK_STATUS_44 bit field indicates the status of bootloader block 44. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[7:6]	BLOCK_STATUS_43	Bootloader block 43 status. The IO_LV_BOOTLOADER_STATUS_5.BLOCK_STATUS_43 bit field indicates the status of bootloader block 43. 00: Not initialized.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 45. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_5 (Continued)

Bits	Bit Name	Description	Reset	Access
		01: Valid. 10: Valid. 11: Corrupted.		
[5:4]	BLOCK_STATUS_42	Bootloader block 42 status. The IO_LV_BOOTLOADER_STATUS_5.BLOCK_STATUS_42 bit field indicates the status of bootloader block 42. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[3:2]	BLOCK_STATUS_41	Bootloader block 41 status. The IO_LV_BOOTLOADER_STATUS_5.BLOCK_STATUS_41 bit field indicates the status of bootloader block 41. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[1:0]	BLOCK_STATUS_40	Bootloader block 40 status. The IO_LV_BOOTLOADER_STATUS_5.BLOCK_STATUS_40 bit field indicates the status of bootloader block 40. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R

BOOTLOADER STATUS 6 REGISTER

OA-SPI Address: 0xC80C, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_STATUS_6 register indicates the bootloader block status as described below.

Table 46. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_6

Bits	Bit Name	Description	Reset	Access
[15:14]	BLOCK_STATUS_55	Bootloader block 55 status. The IO_LV_BOOTLOADER_STATUS_6.BLOCK_STATUS_55 bit field indicates the status of bootloader block 55. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[13:12]	BLOCK_STATUS_54	Bootloader block 54 status. The IO_LV_BOOTLOADER_STATUS_6.BLOCK_STATUS_54 bit field indicates the status of bootloader block 54. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[11:10]	BLOCK_STATUS_53	Bootloader block 53 status. The IO_LV_BOOTLOADER_STATUS_6.BLOCK_STATUS_53 bit field indicates the status of bootloader block 53. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[9:8]	BLOCK_STATUS_52	Bootloader block 52 status. The IO_LV_BOOTLOADER_STATUS_6.BLOCK_STATUS_52 bit field indicates the status of bootloader block 52. 00: Not initialized.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 46. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_6 (Continued)

Bits	Bit Name	Description	Reset	Access
		01: Valid. 10: Valid. 11: Corrupted.		
[7:6]	BLOCK_STATUS_51	Bootloader block 51 status. The IO_LV_BOOTLOADER_STATUS_6.BLOCK_STATUS_51 bit field indicates the status of bootloader block 51. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[5:4]	BLOCK_STATUS_50	Bootloader block 50 status. The IO_LV_BOOTLOADER_STATUS_6.BLOCK_STATUS_50 bit field indicates the status of bootloader block 50. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[3:2]	BLOCK_STATUS_49	Bootloader block 49 status. The IO_LV_BOOTLOADER_STATUS_6.BLOCK_STATUS_49 bit field indicates the status of bootloader block 49. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[1:0]	BLOCK_STATUS_48	Bootloader block 48 status. The IO_LV_BOOTLOADER_STATUS_6.BLOCK_STATUS_48 bit field indicates the status of bootloader block 48. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R

BOOTLOADER STATUS 7 REGISTER

OA-SPI Address: 0xC80D, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_STATUS_7 register indicates the bootloader block status as described below.

Table 47. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_7

Bits	Bit Name	Description	Reset	Access
15	BOOTLOAD_DONE	Bootloader done. The IO_LV_BOOTLOADER_STATUS_7.BOOTLOAD_DONE bit indicates the status of the bootloading process. 0: Bootloader not finished. 1: Bootloader finished.	0x0	R
14	BOOTLOADER_ABORTED	Bootloader aborted. The IO_LV_BOOTLOADER_STATUS_7.BOOTLOADER_ABORTED bit indicates bootloading process status was aborted (0 = ok; 1 = aborted). See the IO_LV_BOOTLOADER_STATUS_7.BOOTLOADER_TIMEOUT flag for abort cause. 0: Not triggered. 1: Triggered.	0x0	R
13	BOOTLOADER_TIMEOUT	Bootloader timeout. The IO_LV_BOOTLOADER_STATUS_7.BOOTLOADER_TIMEOUT bit indicates that the bootloading process was not able to start within 1s (0 = able to start; 1 = timeout error). 1: Triggered. 0: Not triggered.	0x0	R
[12:10]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 47. Bit Descriptions for IO_LV_BOOTLOADER_STATUS_7 (Continued)

Bits	Bit Name	Description	Reset	Access
[9:8]	BLOCK_STATUS_60	Bootloader block 60 status. The IO_LV_BOOTLOADER_STATUS_7.BLOCK_STATUS_60 bit field indicates the status of bootloader block 60. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[7:6]	BLOCK_STATUS_59	Bootloader block 59 status. The IO_LV_BOOTLOADER_STATUS_7.BLOCK_STATUS_59 bit field indicates the status of bootloader block 59. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[5:4]	BLOCK_STATUS_58	Bootloader block 58 status. The IO_LV_BOOTLOADER_STATUS_7.BLOCK_STATUS_58 bit field indicates the status of bootloader block 58. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[3:2]	BLOCK_STATUS_57	Bootloader block 57 status. The IO_LV_BOOTLOADER_STATUS_7.BLOCK_STATUS_57 bit field indicates the status of bootloader block 57. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R
[1:0]	BLOCK_STATUS_56	Bootloader block 56 status. The IO_LV_BOOTLOADER_STATUS_7.BLOCK_STATUS_56 bit field indicates the status of bootloader block 56. 00: Not initialized. 01: Valid. 10: Valid. 11: Corrupted.	0x0	R

SLEEP WAKE CONFIGURATION REGISTER

OA-SPI Address: 0xC80F, MMS: 0xA, Reset: 0x0100

The IO_LV_SLEEP_WAKE_CFG register is used to configure the sleep wake controller.

Table 48. Bit Descriptions for IO_LV_SLEEP_WAKE_CFG

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
12	SLPWK_FAILSAFE_SLEEP_EN	Auto sleep enable. The IO_LV_SLEEP_WAKE_CFG.SLPWK_FAILSAFE_SLEEP_EN bit is used to configure the controller to automatically send the device to sleep after a selectable timeout without receiving data via the network, preventing single devices to remain powered up in a powered down network. 0: Disabled. 1: Enabled.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 48. Bit Descriptions for IO_LV_SLEEP_WAKE_CFG (Continued)

Bits	Bit Name	Description	Reset	Access
[11:10]	RESERVED	Reserved.	0x0	R
[9:8]	SLPWK_CFG_WUS_WAKEUP_IRQ_CONF_WAIT_SEL	Wait for IRQ clear. The IO_LV_SLEEP_WAKE_CFG.SLPWK_CFG_WUS_WAKEUP_IRQ_CONF_WAIT_SEL bits are used to configure the sleep wake controller's wait time selection to receive IRQ clear confirmation of the system being awake 00: SLPWK_IRQ_CONF_WAIT_SEL0. 5ms 01: SLPWK_IRQ_CONF_WAIT_SEL1. 10ms 10: SLPWK_IRQ_CONF_WAIT_SEL2. 20ms 11: SLPWK_IRQ_CONF_WAIT_SEL3. 50ms	0x1	R/W
[7:4]	SLPWK_CFG_WUS_WAKEUP_MAX_RETRY	Resend wakeup signal. The IO_LV_SLEEP_WAKE_CFG.SLPWK_CFG_WUS_WAKEUP_MAX_RETRY bits configure the sleep wake controller to re-send a Wake-Up-Signal (WUS) every 100 ms until it gets confirmation of the system being awake for a maximum of this number of times. A value of 0 does not retry, and keeps the node awake (can be used to abort the re-tries). When the max retry is reached the device goes to sleep automatically. This is only applicable when the device is waking up due to WAKE pin activation.	0x0	R/W
3	SLPWK_CFG_REQ_SYSTEM_WAKEUP_CONF	Send interrupt wake confirm. The IO_LV_SLEEP_WAKE_CFG.SLPWK_CFG_REQ_SYSTEM_WAKEUP_CONF bit is used to configure if the sleep wake controller sends an interrupt message to the network requesting that the controller node clears the interrupt to confirm that the system is awake. Otherwise the WUS is re-tried. When this bit is 0, the confirmation of system awake is obtained from any network traffic being received. 0: Disabled. 1: Enabled.	0x0	R/W
[2:0]	SLPWK_CFG_TRAFFIC_TIMER_SEL	Network traffic check delay. The IO_LV_SLEEP_WAKE_CFG.SLPWK_CFG_TRAFFIC_TIMER_SEL bits are used to select the delay for network traffic check when waking up before returning to sleep/standby. 0: SLPWK_TRAFFIC_TIMER_SEL0. 10ms 1: SLPWK_TRAFFIC_TIMER_SEL1. 100ms 2: SLPWK_TRAFFIC_TIMER_SEL2. 500ms 3: SLPWK_TRAFFIC_TIMER_SEL3. 1s 4: SLPWK_TRAFFIC_TIMER_SEL4. 2s 5: SLPWK_TRAFFIC_TIMER_SEL5. 4s 6: SLPWK_TRAFFIC_TIMER_SEL6. 8s 7: SLPWK_TRAFFIC_TIMER_SEL7. 16s	0x0	R/W

SLEEP/WAKE COMMAND REGISTER

OA-SPI Address: 0xC810, MMS: 0xA, Reset: 0x0000

The IO_LV_SLEEPWAKE_CMD register has controls for triggering a WUP and for sending the node to sleep or standby.

Table 49. Bit Descriptions for IO_LV_SLEEPWAKE_CMD

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	SLPWK_CMD_SEND_WUS	Send wake up sequence. The IO_LV_SLEEPWAKE_CMD.SLPWK_CMD_SEND_WUS bit is used to send the wake up sequence to the device. 0: Inactive. 1: Trigger.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 49. Bit Descriptions for IO_LV_SLEEPWAKE_CMD (Continued)

Bits	Bit Name	Description	Reset	Access
1	SLPWK_CMD_GOTO_STANDBY	Go to standby command. The IO_LV_SLEEPWAKE_CMD.SLPWK_CMD_GOTO_STANDBY bit is used to send the device into standby mode. 0: Inactive. 1: Trigger.	0x0	R/W
0	SLPWK_CMD_GOTO_SLEEP	Go to sleep command. The IO_LV_SLEEPWAKE_CMD.SLPWK_CMD_GOTO_SLEEP bit is used to send the device into sleep mode. 0: Inactive. 1: Trigger.	0x0	R/W

SLEEPWAKE STATUS REGISTER

OA-SPI Address: 0xC811, MMS: 0xA, Reset: 0x0000

The IO_LV_SLEEPWAKE_STATUS register is used to indicate Sleep and wake status information.

Table 50. Bit Descriptions for IO_LV_SLEEPWAKE_STATUS

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	SLPWK_SUSPEND_DETECTED	Sleep wake suspend detected. The IO_LV_SLEEPWAKE_STATUS.SLPWK_SUSPEND_DETECTED bit indicates that a sleep wake suspend has been detected. 0: Not triggered. 1: Triggered.	0x0	RC
5	SLPWK_RB_WUP_COL	Sleep Wake collision detect. The IO_LV_SLEEPWAKE_STATUS.SLPWK_RB_WUP_COL bit indicates that the sleep wake controller detected a collision during the Wake-Up Pulse (WUP) transmission. This value is kept until a new WUP is requested. 0: Not triggered. 1: Triggered.	0x0	R
4	SLPWK_STANDBY_RETURN_IS_WUD	Sleep wake exited standby WUD. The IO_LV_SLEEPWAKE_STATUS.SLPWK_STANDBY_RETURN_IS_WUD bit indicates that the sleep wake controller exited standby due to WUD. 0: Not triggered. 1: Triggered.	0x0	R
3	SLPWK_STANDBY_RETURN_IS_PIN	Sleep wake exited standby WAKE pin. The IO_LV_SLEEPWAKE_STATUS.SLPWK_STANDBY_RETURN_IS_PIN bit indicates that the sleep wake controller exited standby due to WAKE pin. 0: Not triggered. 1: Triggered.	0x0	R
2	SLPWK_RB_FAILED_STANDBY	Sleep Wake fail to enter standby. The IO_LV_SLEEPWAKE_STATUS.SLPWK_RB_FAILED_STANDBY bit indicates that the sleep wake controller failed to enter standby. 0: Not triggered. 1: Triggered.	0x0	R
1	SLPWK_RB_FAILED_SLEEP	Sleep wake fail to enter sleep. The IO_LV_SLEEPWAKE_STATUS.SLPWK_RB_FAILED_SLEEP bit indicates that the sleep wake controller failed to enter sleep mode. 0: Not triggered. 1: Triggered.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 50. Bit Descriptions for IO_LV_SLEEPWAKE_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
0	SLPWK_RB_AWAKE	Sleep wake resting in awake state. The IO_LV_SLEEPWAKE_STATUS.SLPWK_RB_AWAKE bit indicates that the sleep wake controller is resting in awake state 0: Not triggered. 1: Triggered.	0x0	R

BOOTLOADER READBACK 8 REGISTER

OA-SPI Address: 0xC813, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_8 register is used to configure the device ID.

Table 51. Bit Descriptions for IO_LV_BOOTLOADER_RB_8

Bits	Bit Name	Description	Reset	Access
[15:0]	DEVICE_ID	Programmable device ID. The IO_LV_BOOTLOADER_RB_8.DEVICE_ID bits are used to configure the device ID.	0x0	R/W

BOOTLOADER READBACK 9 REGISTER

OA-SPI Address: 0xC814, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_9 register is used to configure the device version.

Table 52. Bit Descriptions for IO_LV_BOOTLOADER_RB_9

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	DEVICE_VERSION	Programmable device version. The IO_LV_BOOTLOADER_RB_9.DEVICE_VERSION bits are used to configure the device version.	0x0	R/W

BOOTLOADER READBACK 10 REGISTER

OA-SPI Address: 0xC815, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_10 register is used to configure the PHY ID LSBs.

Table 53. Bit Descriptions for IO_LV_BOOTLOADER_RB_10

Bits	Bit Name	Description	Reset	Access
[15:0]	PHY_IDENTIFIER_0	Bootloader PHY identifier LSBs. The IO_LV_BOOTLOADER_RB_10.PHY_IDENTIFIER_0 bits indicate the bootloader PHY ID LSBs.	0x0	R/W

BOOTLOADER READBACK 11 REGISTER

OA-SPI Address: 0xC816, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_11 register indicates the bootloader PHY ID.

Table 54. Bit Descriptions for IO_LV_BOOTLOADER_RB_11

Bits	Bit Name	Description	Reset	Access
[15:0]	PHY_IDENTIFIER_1	Bootloader PHY identifier. The IO_LV_BOOTLOADER_RB_11.PHY_IDENTIFIER_1 bits indicate the bootloader PHY ID.	0x0	R/W

BOOTLOADER READBACK 12 REGISTER

OA-SPI Address: 0xC817, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_12 register indicates the bootloader PHY ID MSBs.

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Table 55. Bit Descriptions for IO_LV_BOOTLOADER_RB_12

Bits	Bit Name	Description	Reset	Access
[15:0]	PHY_IDENTIFIER_2	Bootloader PHY identifier MSBs. The IO_LV_BOOTLOADER_RB_12.PHY_IDENTIFIER_2 bits indicate the bootloader PHY ID MSBs.	0x0	R/W

BOOTLOADER READBACK 13 REGISTER

OA-SPI Address: 0xC818, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_13 register indicates the bootloader OEM data.

Table 56. Bit Descriptions for IO_LV_BOOTLOADER_RB_13

Bits	Bit Name	Description	Reset	Access
[15:0]	OEM_DATA_0	Bootloader OEM data. The IO_LV_BOOTLOADER_RB_13.OEM_DATA_0 bits indicate the bootloader OEM data.	0x0	R/W

BOOTLOADER READBACK 14 REGISTER

OA-SPI Address: 0xC819, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_14 register indicates the bootloader OEM data.

Table 57. Bit Descriptions for IO_LV_BOOTLOADER_RB_14

Bits	Bit Name	Description	Reset	Access
[15:0]	OEM_DATA_1	Bootloader OEM data. The IO_LV_BOOTLOADER_RB_14.OEM_DATA_1 bits indicate the bootloader OEM data.	0x0	R/W

BOOTLOADER READBACK 15 REGISTER

OA-SPI Address: 0xC81A, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_15 register indicates the bootloader OEM data.

Table 58. Bit Descriptions for IO_LV_BOOTLOADER_RB_15

Bits	Bit Name	Description	Reset	Access
[15:0]	OEM_DATA_2	Bootloader OEM data. The IO_LV_BOOTLOADER_RB_15.OEM_DATA_2 bits indicate the bootloader OEM data.	0x0	R/W

BOOTLOADER READBACK 16 REGISTER

OA-SPI Address: 0xC81B, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_16 register indicates the bootloader OEM data.

Table 59. Bit Descriptions for IO_LV_BOOTLOADER_RB_16

Bits	Bit Name	Description	Reset	Access
[15:0]	OEM_DATA_3	Bootloader OEM data. The IO_LV_BOOTLOADER_RB_16.OEM_DATA_3 bits indicate the bootloader OEM data.	0x0	R/W

BOOTLOADER READBACK 17 REGISTER

OA-SPI Address: 0xC81C, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_17 register indicates the bootloader OEM data.

Table 60. Bit Descriptions for IO_LV_BOOTLOADER_RB_17

Bits	Bit Name	Description	Reset	Access
[15:0]	OEM_DATA_4	Bootloader OEM data. The IO_LV_BOOTLOADER_RB_17.OEM_DATA_4 bits indicate the bootloader OEM data.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

BOOTLOADER READBACK 18 REGISTER

OA-SPI Address: 0xC81D, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_18 register indicates the bootloader OEM data.

Table 61. Bit Descriptions for IO_LV_BOOTLOADER_RB_18

Bits	Bit Name	Description	Reset	Access
[15:0]	OEM_DATA_5	Bootloader OEM data. The IO_LV_BOOTLOADER_RB_18.OEM_DATA_5 bits indicate the bootloader OEM data.	0x0	R/W

BOOTLOADER READBACK 19 REGISTER

OA-SPI Address: 0xC81E, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_19 register indicates the bootloader OEM data.

Table 62. Bit Descriptions for IO_LV_BOOTLOADER_RB_19

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R/W
[13:0]	OEM_DATA_6	Bootloader OEM data. The IO_LV_BOOTLOADER_RB_19.OEM_DATA_6 bits indicate the bootloader OEM data.	0x0	R/W

BOOTLOADER READBACK 20 REGISTER

OA-SPI Address: 0xC81F, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_20 register indicates the bootloader manufacturer data.

Table 63. Bit Descriptions for IO_LV_BOOTLOADER_RB_20

Bits	Bit Name	Description	Reset	Access
[15:0]	MANUFACTURER_DATA_0	Bootloader manufacturer data. The IO_LV_BOOTLOADER_RB_20.MANUFACTURER_DATA_0 bits indicate the bootloader manufacturer data.	0x0	R/W

BOOTLOADER READBACK 21 REGISTER

OA-SPI Address: 0xC820, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_21 register indicates the bootloader manufacturer data.

Table 64. Bit Descriptions for IO_LV_BOOTLOADER_RB_21

Bits	Bit Name	Description	Reset	Access
[15:0]	MANUFACTURER_DATA_1	Bootloader manufacturer data. The IO_LV_BOOTLOADER_RB_21.MANUFACTURER_DATA_1 bits indicate the bootloader manufacturer data.	0x0	R/W

BOOTLOADER READBACK 22 REGISTER

OA-SPI Address: 0xC821, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_22 register indicates the bootloader manufacturer data.

Table 65. Bit Descriptions for IO_LV_BOOTLOADER_RB_22

Bits	Bit Name	Description	Reset	Access
[15:0]	MANUFACTURER_DATA_2	Bootloader manufacturer data. The IO_LV_BOOTLOADER_RB_22.MANUFACTURER_DATA_2 bits indicate the bootloader manufacturer data.	0x0	R/W

BOOTLOADER READBACK 23 REGISTER

OA-SPI Address: 0xC822, MMS: 0xA, Reset: 0x0000

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

The IO_LV_BOOTLOADER_RB_23 register indicates the bootloader manufacturer data.

Table 66. Bit Descriptions for IO_LV_BOOTLOADER_RB_23

Bits	Bit Name	Description	Reset	Access
[15:0]	MANUFACTURER_DATA_3	Bootloader manufacturer data. The IO_LV_BOOTLOADER_RB_23.MANUFACTURER_DATA_3 bits indicate the bootloader manufacturer data.	0x0	R/W

BOOTLOADER READBACK 24 REGISTER

OA-SPI Address: 0xC823, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_24 register indicates the bootloader manufacturer data.

Table 67. Bit Descriptions for IO_LV_BOOTLOADER_RB_24

Bits	Bit Name	Description	Reset	Access
[15:0]	MANUFACTURER_DATA_4	Bootloader manufacturer data. The IO_LV_BOOTLOADER_RB_24.MANUFACTURER_DATA_4 bits indicate the bootloader manufacturer data.	0x0	R/W

BOOTLOADER READBACK 25 REGISTER

OA-SPI Address: 0xC824, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_25 register indicates the bootloader manufacturer data.

Table 68. Bit Descriptions for IO_LV_BOOTLOADER_RB_25

Bits	Bit Name	Description	Reset	Access
[15:0]	MANUFACTURER_DATA_5	Bootloader manufacturer data. The IO_LV_BOOTLOADER_RB_25.MANUFACTURER_DATA_5 bits indicate the bootloader manufacturer data.	0x0	R/W

BOOTLOADER READBACK 26 REGISTER

OA-SPI Address: 0xC825, MMS: 0xA, Reset: 0x0000

The IO_LV_BOOTLOADER_RB_26 register indicates the bootloader manufacturer data.

Table 69. Bit Descriptions for IO_LV_BOOTLOADER_RB_26

Bits	Bit Name	Description	Reset	Access
[15:0]	MANUFACTURER_DATA_6	Bootloader manufacturer data. The IO_LV_BOOTLOADER_RB_26.MANUFACTURER_DATA_6 bits indicate the bootloader manufacturer data.	0x0	R/W

DEBUG DATA CONTROL 0 REGISTER

OA-SPI Address: 0xC840, MMS: 0xA, Reset: 0x7F7F

The IO_LV_DEBUG_DATA_CONTROL_0 register selects the internal signal to be outputted to SAIF0 and TS_TIMER when output internal signal mode is enabled.

Table 70. Bit Descriptions for IO_LV_DEBUG_DATA_CONTROL_0

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
[14:8]	DBG_DATA_SEL_1	Debug Data Selection for TS_TIMER pin. 011110: PLCA Beacon detected signal. 110111: One pulse per second signal generated with the gPTP timestamp.	0x7F	R/W
7	RESERVED	Reserved.	0x0	R
[6:0]	DBG_DATA_SEL_0	Debug Data Selection for the Sensor-Actuator Interface Pin 0. 011110: PLCA Beacon detected signal.	0x7F	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 70. Bit Descriptions for IO_LV_DEBUG_DATA_CONTROL_0 (Continued)

Bits	Bit Name	Description	Reset	Access
		110111: One pulse per second signal generated with the gPTP timestamp.		

DEBUG DATA CONTROL 1 REGISTER

OA-SPI Address: 0xC841, MMS: 0xA, Reset: 0x7F7F

The IO_LV_DEBUG_DATA_CONTROL_1 register selects the internal signal to be outputted to TS_CAPT when output internal signal mode is enabled.

Table 71. Bit Descriptions for IO_LV_DEBUG_DATA_CONTROL_1

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0xFE	R
[6:0]	DBG_DATA_SEL_2	Debug Data Selection for the TS_CAPT pin. 011110: PLCA Beacon detected signal. 110111: One pulse per second signal generated with the gPTP timestamp.	0x7F	R/W

DEBUG DATA CONTROL 4 REGISTER

OA-SPI Address: 0xC844, MMS: 0xA, Reset: 0x7F7F

The IO_LV_DEBUG_DATA_CONTROL_4 register selects the internal signal to be outputted to SAIF9 when output internal signal mode is enabled.

Table 72. Bit Descriptions for IO_LV_DEBUG_DATA_CONTROL_4

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
[14:8]	DBG_DATA_SEL_9	Debug Data Selection for the Sensor-Actuator Interface Pin 9. 011110: PLCA Beacon detected signal. 110111: One pulse per second signal generated with the gPTP timestamp.	0x7F	R/W
[7:0]	RESERVED	Reserved.	0x7F	R

DEBUG DATA CONTROL 5 REGISTER

OA-SPI Address: 0xC845, MMS: 0xA, Reset: 0x7F7F

The IO_LV_DEBUG_DATA_CONTROL_5 register selects the internal signal to be outputted to SAIF10 and SAIF11 when output internal signal mode is enabled.

Table 73. Bit Descriptions for IO_LV_DEBUG_DATA_CONTROL_5

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
[14:8]	DBG_DATA_SEL_11	Debug Data Selection for the Sensor-Actuator Interface Pin 11. 011110: PLCA Beacon detected signal. 110111: One pulse per second signal generated with the gPTP timestamp.	0x7F	R/W
7	RESERVED	Reserved.	0x0	R
[6:0]	DBG_DATA_SEL_10	Debug Data Selection for the Sensor-Actuator Interface Pin 10. 011110: PLCA Beacon detected signal. 110111: One pulse per second signal generated with the gPTP timestamp.	0x7F	R/W

MISCELLANEOUS CONTROL REGISTER

OA-SPI Address: 0xC849, MMS: 0xA, Reset: 0x2000

The IO_LV_MISC_CONTROL register is used to configure the Standby Feature En

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 74. Bit Descriptions for IO_LV_MISC_CONTROL

Bits	Bit Name	Description	Reset	Access
15	STANDBY_FEATURE_EN	Enables standby feature.	0x0	R/W
[14:0]	RESERVED	Reserved.	0x2000	R/W

IO GLITCH REJECT 0 REGISTER

OA-SPI Address: 0xC84F, MMS: 0xA, Reset: 0xFFFF

The IO_LV_IO_GLITCH_REJECT_0 register is used to configure the glitch reject filter for SAIF0, TS_TIMER, IRQn and SDI pins.

Table 75. Bit Descriptions for IO_LV_IO_GLITCH_REJECT_0

Bits	Bit Name	Description	Reset	Access
[15:14]	IO_LV_GLITCH_REJECT_FILTER_7	SDI reject filter. The IO_LV_IO_GLITCH_REJECT_0.IO_GLITCH_REJECT_FILTER_7 bits are used to configure the reject filter of the PAD for the SDI pin. 00: Reject pulses shorter than 50ns. 01: Reject pulses shorter than 5ns. 10: Reject pulses shorter than 2.5ns. 11: Bypass glitch filter.	0x3	R/W
[13:12]	RESERVED	Reserved.	0x3	R/W
[11:10]	IO_LV_GLITCH_REJECT_FILTER_5	IRQn reject filter. The IO_LV_IO_GLITCH_REJECT_0.IO_GLITCH_REJECT_FILTER_5 bits are used to configure the reject filter of the PAD for the IRQn pin. 00: Reject pulses shorter than 50ns. 01: Reject pulses shorter than 5ns. 10: Reject pulses shorter than 2.5ns. 11: Bypass glitch filter.	0x3	R/W
[9:4]	RESERVED	Reserved.	0x3F	R/W
[3:2]	IO_LV_GLITCH_REJECT_FILTER_1	TS_TIMER reject filter. The IO_LV_IO_GLITCH_REJECT_0.IO_GLITCH_REJECT_FILTER_1 bits are used to configure the reject filter of the PAD for the TS_TIMER pin. 00: Reject pulses shorter than 50ns. 01: Reject pulses shorter than 5ns. 10: Reject pulses shorter than 2.5ns. 11: Bypass glitch filter.	0x3	R/W
[1:0]	IO_LV_GLITCH_REJECT_FILTER_0	SAIF0 reject filter. The IO_LV_IO_GLITCH_REJECT_0.IO_GLITCH_REJECT_FILTER_0 bits are used to configure the reject filter of the PAD for the SAIF0 pin. 00: Reject pulses shorter than 50ns. 01: Reject pulses shorter than 5ns. 10: Reject pulses shorter than 2.5ns. 11: Bypass glitch filter.	0x3	R/W

IO GLITCH REJECT 1 REGISTER

OA-SPI Address: 0xC850, MMS: 0xA, Reset: 0x033F

The IO_LV_IO_GLITCH_REJECT_1 register is used to configure the glitch reject filter for SAIF9-11 pins.

Table 76. Bit Descriptions for IO_LV_IO_GLITCH_REJECT_1

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved.	0x0	R
[9:8]	IO_LV_GLITCH_REJECT_FILTER_11	SAIF11 Reject Filter. The IO_LV_IO_GLITCH_REJECT_1.IO_GLITCH_REJECT_FILTER_11 bits are used to configure the reject filter of the PAD for the SAIF11 pin.	0x3	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 76. Bit Descriptions for IO_LV_IO_GLITCH_REJECT_1 (Continued)

Bits	Bit Name	Description	Reset	Access
		00: Reject pulses shorter than 50ns. 01: Reject pulses shorter than 5ns. 10: Reject pulses shorter than 2.5ns. 11: Bypass glitch filter.		
[7:6]	RESERVED	Reserved.	0x0	R
[5:4]	IO_LV_GLITCH_REJECT_FILTER_10	SAIF10 Reject Filter. The IO_LV_IO_GLITCH_REJECT_1.IO_GLITCH_REJECT_FILTER_10 bits are used to configure the reject filter of the PAD for the SAIF10 pin. 00: Reject pulses shorter than 50ns. 01: Reject pulses shorter than 5ns. 10: Reject pulses shorter than 2.5ns. 11: Bypass glitch filter.	0x3	R/W
[3:2]	IO_LV_GLITCH_REJECT_FILTER_9	SAIF9 Reject Filter. The IO_LV_IO_GLITCH_REJECT_1.IO_GLITCH_REJECT_FILTER_9 bits are used to configure the reject filter of the PAD for the SAIF9 pin. 00: Reject pulses shorter than 50ns. 01: Reject pulses shorter than 5ns. 10: Reject pulses shorter than 2.5ns. 11: Bypass glitch filter.	0x3	R/W
[1:0]	RESERVED	Reserved.	0x3	R/W

IO DRIVE STRENGTH 0 REGISTER

OA-SPI Address: 0xC851, MMS: 0xA, Reset: 0x5555

The IO_LV_IO_DRIVE_STRENGTH_0 register is used to configure the drive strength on the SAIF0 pins.

Table 77. Bit Descriptions for IO_LV_IO_DRIVE_STRENGTH_0

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x1555	R/W
[1:0]	IO_LV_DRIVE_STRENGTH_0	SAIF0 drive strength. The IO_LV_IO_DRIVE_STRENGTH_0.IO_DRIVE_STRENGTH_0 bits are used to configure the drive strength for the SAIF0 pin. 01: 4mA drive strength. 11: 12mA drive strength.	0x1	R/W

IO DRIVE STRENGTH 1 REGISTER

OA-SPI Address: 0xC852, MMS: 0xA, Reset: 0x0055

The IO_LV_IO_DRIVE_STRENGTH_1 register is used to configure the drive strength on the SAIF11 pins.

Table 78. Bit Descriptions for IO_LV_IO_DRIVE_STRENGTH_1

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:6]	IO_LV_DRIVE_STRENGTH_11	SAIF11 drive strength. The IO_LV_IO_DRIVE_STRENGTH_1.IO_DRIVE_STRENGTH_11 bits are used to configure the drive strength for the SAIF11 pin. 01: 4mA drive strength. 11: 12mA drive strength.	0x1	R/W
[5:0]	RESERVED	Reserved.	0x15	R/W

IO HYSTERESIS ENABLE REGISTER

OA-SPI Address: 0xC853, MMS: 0xA, Reset: 0x0000

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

The IO_LV_IO_HYSTHERESIS_ENABLE register is used to configure hysteresis on the SAIF pins

Table 79. Bit Descriptions for IO_LV_IO_HYSTHERESIS_ENABLE

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	IO_LV_HYSTHERESIS_ENABLE_11	SAIF11 hysteresis. The IO_LV_IO_HYSTHERESIS_ENABLE.IO_HYSTHERESIS_ENABLE_11 bit is used to configure the hysteresis of the PAD for the SAIF11 pin. 0: CMOS input receiver. 1: Schmitt input receiver.	0x0	R/W
10	IO_LV_HYSTHERESIS_ENABLE_10	SAIF10 hysteresis. The IO_LV_IO_HYSTHERESIS_ENABLE.IO_HYSTHERESIS_ENABLE_10 bit is used to configure the hysteresis of the PAD for the SAIF10 pin. 0: CMOS input receiver. 1: Schmitt input receiver.	0x0	R/W
9	IO_LV_HYSTHERESIS_ENABLE_9	SAIF9 hysteresis. The IO_LV_IO_HYSTHERESIS_ENABLE.IO_HYSTHERESIS_ENABLE_9 bit is used to configure the hysteresis of the PAD for the SAIF9 pin. 0: CMOS input receiver. 1: Schmitt input receiver.	0x0	R/W
[8:1]	RESERVED	Reserved.	0x0	R/W
0	IO_LV_HYSTHERESIS_ENABLE_0	SAIF0 hysteresis. The IO_LV_IO_HYSTHERESIS_ENABLE.IO_HYSTHERESIS_ENABLE_0 bit is used to configure the hysteresis of the PAD for the SAIF0 pin. 0: CMOS input receiver. 1: Schmitt input receiver.	0x0	R/W

IO SLEW RATE REGISTER

OA-SPI Address: 0xC854, MMS: 0xA, Reset: 0x0000

The IO_LV_IO_SLEW_RATE register is used to configure the slew rate for the SAIF0 and SAIF11 pins.

Table 80. Bit Descriptions for IO_LV_IO_SLEW_RATE

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	IO_LV_SLEW_RATE_11	SAIF11 slew rate. The IO_LV_IO_SLEW_RATE.IO_SLEW_RATE_11 bit is used to configure the slew rate for the SAIF11 pin. 1: Slow slew rate. 0: Fast slew rate.	0x0	R/W
[10:1]	RESERVED	Reserved.	0x0	R/W
0	IO_LV_SLEW_RATE_0	SAIF0 slew rate. The IO_LV_IO_SLEW_RATE.IO_SLEW_RATE_0 bit is used to configure the slew rate for the SAIF0 pin. 1: Slow slew rate. 0: Fast slew rate.	0x0	R/W

SLEEP HISTORY REGISTER

OA-SPI Address: 0xC860, MMS: 0xA, Reset: 0x0000

The IO_LV_SLEEP_HISTORY register is used to indicate sleep and wake information.

Table 81. Bit Descriptions for IO_LV_SLEEP_HISTORY

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 81. Bit Descriptions for IO_LV_SLEEP_HISTORY (Continued)

Bits	Bit Name	Description	Reset	Access
[7:4]	REASON_FOR_WAKE	Reason for wake. The IO_LV_SLEEP_HISTORY.REASON_FOR_WAKE bit field indicates the reason for wake-up mode. This information is copied from the Always On Configuration Fields 1 Register map at boot-up. 0001: Wake pin. 0010: Ethernet wake-up pulse detected. 0100: VBAT recovery. 1000: POR release.	0x0	R/W
[3:0]	REASON_FOR_SLEEP	Reason for sleep. The IO_LV_SLEEP_HISTORY.REASON_FOR_SLEEP bit field indicates the reason for going to sleep mode. This information is copied from the Always On Configuration Fields 1 Register map at boot-up. 0001: Register map. 1000: Deep undervoltage. 0100: Undervoltage. 0010: Overvoltage.	0x0	R/W

MANUAL INTERRUPT REGISTER

OA-SPI Address: 0xC882, MMS: 0xA, Reset: 0x0000

The IO_LV_MANUAL_INTERRUPT register is used to enable a user programmable interrupt.

Table 82. Bit Descriptions for IO_LV_MANUAL_INTERRUPT

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	MANUAL_INTERRUPT	Manual interrupt enable. The IO_LV_MANUAL_INTERRUPT.MANUAL_INTERRUPT bit is used to enable a user programmable interrupt. If this value is set (=1), an interrupt located at field 5 of interrupt vector 29 is triggered (if enabled in the interrupt configuration). 0: Disabled. 1: Enabled.	0x0	R/W

PIN SAFE MODE STATUS REGISTER

OA-SPI Address: 0xC883, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_MUX_SEL_SAFE_ACTIVE_RB register indicates the safe state mode of the transceiver.

Table 83. Bit Descriptions for IO_LV_SSC_MUX_SEL_SAFE_ACTIVE_RB

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:0]	SSC_MUX_SEL_SAFE_ACTIVE_RB	Pin safe mode status. The IO_LV_SSC_MUX_SEL_SAFE_ACTIVE_RB.SSC_MUX_SEL_SAFE_ACTIVE_RB bits indicate which SAIF pin has the safe configuration enabled where 1 = safe pin configuration and 0 = functional pin configuration. The bit number corresponds to the pin number (bit 0 = pin SAIF0, bit 1 = pin TS_TIMER and so on).	0x0	R

SSC SAFE CHECKS TRIGGERED READBACK REGISTER

OA-SPI Address: 0xC884, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB register provides readbacks that indicate the state of the monitored fault detection mechanisms when entering safe state mode. There are also sticky versions of these registers which are only cleared when read.

Table 84. Bit Descriptions for IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB

Bits	Bit Name	Description	Reset	Access
[15:0]	SSC_MONITOR_TRIGGERED_SIGNALS_RB[15:0]	Monitor state status. The IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB.SSC_MONITOR_TRIGGERED_SIGN	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 84. Bit Descriptions for IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB (Continued)

Bits	Bit Name	Description	Reset	Access
		ALS_RB bits indicate the state of the monitored signals when they entered safe mode. The enumeration table values indicate the bit position of each monitor triggers. The bit positions which have a one (1) indicates that its monitor signal have been triggered. 0: Indicates the value that triggers safe mode for the monitored signal SAIF0. 9: Indicates the value that triggers safe mode for the monitored signal SAIF9. 10: Indicates the value that triggers safe mode for the monitored signal SAIF10. 11: Indicates the value that triggers safe mode for the monitored signal SAIF11. 20: Indicates the value that triggers safe mode for the monitored signal gPTP lock. 21: Indicates the value that triggers safe mode for the monitored signal OTP configuration. 22: Indicates the value that triggers safe mode for the monitored signal SQI level. 23: Indicates the value that triggers safe mode for the monitored signal Global Manual Trigger.		

SSC SAFE CHECKS TRIGGERED READBACK 2 REGISTER

OA-SPI Address: 0xC885, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB_2 register provides readbacks that indicate the state of the monitored fault detection mechanisms when entering safe state mode. There are also sticky versions of these registers which are only cleared when read.

Table 85. Bit Descriptions for IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB_2

Bits	Bit Name	Description	Reset	Access
[15:14]	SSC_TIMEOUT_TRIGGERED_SIGNALS_RB	Timeout trigger status. The IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB_2.SSC_TIMEOUT_TRIGGERED_SIGNALS_RB bits indicate if each of the timeouts have been triggered. The enumeration table values indicate the bit position of each timeout trigger. The bit positions which have a one (1) indicates that its timeout signal have been triggered. 0: Ethernet Traffic Detected. 1: Device Unattended.	0x0	R
[13:8]	RESERVED	Reserved.	0x0	R
[7:0]	SSC_MONITOR_TRIGGERED_SIGNALS_RB[23:16]	Monitor state status. The IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB.SSC_MONITOR_TRIGGERED_SIGNALS_RB bits indicate the state of the monitored signals when they entered safe mode. The enumeration table values indicate the bit position of each monitor triggers. The bit positions which have a one (1) indicates that its monitor signal have been triggered. 0: Indicates the value that triggers safe mode for the monitored signal SAIF0. 9: Indicates the value that triggers safe mode for the monitored signal SAIF9. 10: Indicates the value that triggers safe mode for the monitored signal SAIF10. 11: Indicates the value that triggers safe mode for the monitored signal SAIF11. 20: Indicates the value that triggers safe mode for the monitored signal gPTP lock. 21: Indicates the value that triggers safe mode for the monitored signal OTP configuration. 22: Indicates the value that triggers safe mode for the monitored signal SQI level. 23: Indicates the value that triggers safe mode for the monitored signal Global Manual Trigger.	0x0	R

SSC SAFE CHECKS TRIGGERED READBACK (STICKY) REGISTER

OA-SPI Address: 0xC886, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_SAFE_CHECKS_TRIGGER register is the sticky version of the IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB register. This register is cleared when read.

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 86. Bit Descriptions for IO_LV_SSC_SAFE_CHECKS_TRIGGER

Bits	Bit Name	Description	Reset	Access
[15:0]	SSC_MONITOR_TRIGGERED_SIGNALS_STICKY_RB[15:0]	Monitored signals status. The IO_LV_SSC_SAFE_CHECKS_TRIGGER.SSC_MONITOR_TRIGGERED_SIGNALS_STICKY_RB bits indicate the state of the monitored signals when they entered safe mode. The enumeration table values indicate the bit position of each monitor triggers. These bits retain their value until cleared by the ssc_clear_all_triggers control. The bit positions which have a one (1) indicates that its monitor signal have been triggered. 0: Indicates the value that triggers safe mode for the monitored signal SAIF0. 9: Indicates the value that triggers safe mode for the monitored signal SAIF9. 10: Indicates the value that triggers safe mode for the monitored signal SAIF10. 11: Indicates the value that triggers safe mode for the monitored signal SAIF11. 20: Indicates the value that triggers safe mode for the monitored signal gPTP lock. 21: Indicates the value that triggers safe mode for the monitored signal OTP configuration. 22: Indicates the value that triggers safe mode for the monitored signal SQI level. 23: Indicates the value that triggers safe mode for the monitored signal Global Manual Trigger.	0x0	R

SSC SAFE CHECKS TRIGGERED READBACK 2 (STICKY) REGISTER

OA-SPI Address: 0xC887, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_SAFE_CHECKS_TRIGGERED_STICKY_RB_2 register is the sticky version of the IO_LV_SSC_SAFE_CHECKS_TRIGGERED_RB_2 register. This register is cleared when read.

Table 87. Bit Descriptions for IO_LV_SSC_SAFE_CHECKS_TRIGGERED_STICKY_RB_2

Bits	Bit Name	Description	Reset	Access
[15:14]	SSC_TIMEOUT_TRIGGERED_SIGNALS_STICKY_RB	Timeout signal trigger. The IO_LV_SSC_SAFE_CHECKS_TRIGGERED_STICKY_RB_2.SSC_TIMEOUT_TRIGGERED_SIGNALS_STICKY_RB bits indicate all the timeout signals that have been triggered. These bits retain their value until cleared by the ssc_clear_all_triggers control. The enumeration table values indicate the bit position of each timeout trigger. The bit positions which have a one (1) indicates that its timeout signal have been triggered. 1: Device Unattended. 0: Ethernet Traffic Detected.	0x0	R
[13:8]	RESERVED	Reserved.	0x0	R
[7:0]	SSC_MONITOR_TRIGGERED_SIGNALS_STICKY_RB[23:16]	Monitored signals status. The IO_LV_SSC_SAFE_CHECKS_TRIGGER.SSC_MONITOR_TRIGGERED_SIGNALS_STICKY_RB bits indicate the state of the monitored signals when they entered safe mode. The enumeration table values indicate the bit position of each monitor triggers. These bits retain their value until cleared by the ssc_clear_all_triggers control. The bit positions which have a one (1) indicates that its monitor signal have been triggered. 0: Indicates the value that triggers safe mode for the monitored signal SAIF0. 9: Indicates the value that triggers safe mode for the monitored signal SAIF9. 10: Indicates the value that triggers safe mode for the monitored signal SAIF10. 11: Indicates the value that triggers safe mode for the monitored signal SAIF11. 20: Indicates the value that triggers safe mode for the monitored signal gPTP lock. 21: Indicates the value that triggers safe mode for the monitored signal OTP configuration. 22: Indicates the value that triggers safe mode for the monitored signal SQI level. 23: Indicates the value that triggers safe mode for the monitored signal Global Manual Trigger.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

SSC GENERAL READBACK REGISTER

OA-SPI Address: 0xC888, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_GENERAL_RB register indicates SSC status as described below.

Table 88. Bit Descriptions for IO_LV_SSC_GENERAL_RB

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	SSC_MODE_CHANGE_FLAG_RB	Mode switch status. The IO_LV_SSC_GENERAL_RB.SSC_MODE_CHANGE_FLAG_RB bit is set every time the mode switches between functional mode and safe mode. 0: Inactive. 1: Triggered.	0x0	R
0	SSC_MODE_RB	SSC current mode. The IO_LV_SSC_GENERAL_RB.SSC_MODE_RB bit indicates the safe state controller current mode. 0: Functional. 1: Safe.	0x0	R

SSC ALIVE COUNTER READ REGISTER

OA-SPI Address: 0xC889, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_ALIVE_COUNTER_RB register provides the alive count value.

Table 89. Bit Descriptions for IO_LV_SSC_ALIVE_COUNTER_RB

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
[13:0]	SSC_ALIVE_COUNTER	Alive counter value. The IO_LV_SSC_ALIVE_COUNTER_RB.SSC_ALIVE_COUNTER bits display the alive counter count value. The count value increments every 81.92 us.	0x0	R

SSC SAFE SAIF CONTROL REGISTER

OA-SPI Address: 0xC88A, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_SAFE_SA_IF_CONTROLS register is used to configure the SAIF pins in safe mode.

Table 90. Bit Descriptions for IO_LV_SSC_SAFE_SA_IF_CONTROLS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
[14:12]	SSC_SAFE_SA_IF_4_CONTROLS_MUX	SCLK configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS.SSC_SAFE_SA_IF_4_CONTROLS_MUX bits are used to configure SCLK in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W
[11:9]	SSC_SAFE_SA_IF_3_CONTROLS_MUX	TEST1 configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS.SSC_SAFE_SA_IF_3_CONTROLS_MUX bits are used to configure TEST1 in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 90. Bit Descriptions for IO_LV_SSC_SAFE_SA_IF_CONTROLS (Continued)

Bits	Bit Name	Description	Reset	Access
		100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.		
[8:6]	SSC_SAFE_SA_IF_2_CONTROLS_MUX	TS_CAPT configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS.SSC_SAFE_SA_IF_2_CONTROLS_MUX bits are used to configure TS_CAPT in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W
[5:3]	SSC_SAFE_SA_IF_1_CONTROLS_MUX	TS_TIMER configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS.SSC_SAFE_SA_IF_1_CONTROLS_MUX bits are used to configure TS_TIMER in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W
[2:0]	SSC_SAFE_SA_IF_0_CONTROLS_MUX	SAIF0 configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS.SSC_SAFE_SA_IF_0_CONTROLS_MUX bits are used to configure SAIF0 in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W

SSC SAFE SAIF CONTROL 2 REGISTER

OA-SPI Address: 0xC88B, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_SAFE_SA_IF_CONTROLS_2 register is used to configure the SAIF pins in safe mode.

Table 91. Bit Descriptions for IO_LV_SSC_SAFE_SA_IF_CONTROLS_2

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
[14:12]	SSC_SAFE_SA_IF_9_CONTROLS_MUX	SAIF9 configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS_2.SSC_SAFE_SA_IF_9_CONTROLS_MUX bits are used to configure SAIF9 in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 91. Bit Descriptions for IO_LV_SSC_SAFE_SA_IF_CONTROLS_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		111: Enable input. Drive weak 1. Pull-up.		
[11:9]	SSC_SAFE_SA_IF_8_CONTROLS_MUX	SDO configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS_2.SSC_SAFE_SA_IF_8_CONTROLS_MUX bits are used to configure SDO in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W
[8:6]	SSC_SAFE_SA_IF_7_CONTROLS_MUX	SDI configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS_2.SSC_SAFE_SA_IF_7_CONTROLS_MUX bits are used to configure SDI in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W
[5:3]	SSC_SAFE_SA_IF_6_CONTROLS_MUX	CSn configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS_2.SSC_SAFE_SA_IF_6_CONTROLS_MUX bits are used to configure CSn in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W
[2:0]	SSC_SAFE_SA_IF_5_CONTROLS_MUX	IRQn configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS_2.SSC_SAFE_SA_IF_5_CONTROLS_MUX bits are used to configure IRQn in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W

SSC SAFE SAIF CONTROL 3 REGISTER

OA-SPI Address: 0xC88C, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_SAFE_SA_IF_CONTROLS_3 register is used to configure the SAIF pins in safe mode.

Table 92. Bit Descriptions for IO_LV_SSC_SAFE_SA_IF_CONTROLS_3

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 92. Bit Descriptions for IO_LV_SSC_SAFE_SA_IF_CONTROLS_3 (Continued)

Bits	Bit Name	Description	Reset	Access
[5:3]	SSC_SAFE_SA_IF_11_CONTROLS_MUX	SAIF11 configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS_3.SSC_SAFE_SA_IF_11_CONTROLS_MUX bits are used to configure SAIF11 in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W
[2:0]	SSC_SAFE_SA_IF_10_CONTROLS_MUX	SAIF10 configuration SAFE mode. The IO_LV_SSC_SAFE_SA_IF_CONTROLS_3.SSC_SAFE_SA_IF_10_CONTROLS_MUX bits are used to configure SAIF10 in safe mode. 000: No change. Keep functional configuration. 001: Disable input and output- Tri-state. Power down. 010: Enable input, enable output. Drive strong 0. 011: Enable input, enable output. Drive strong 1. 100: Enable input, disable output. Regular input mode. 110: Enable input. Drive weak 0. Pull-down. 111: Enable input. Drive weak 1. Pull-up.	0x0	R/W

SSC MONITOR POLARITY REGISTER

OA-SPI Address: 0xC88D, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_MONITOR_POLARITY register is used to configure the monitoring polarity as described below.

Table 93. Bit Descriptions for IO_LV_SSC_MONITOR_POLARITY

Bits	Bit Name	Description	Reset	Access
[15:0]	SSC_MONITOR_POLARITY[15:0]	Safe mode trigger. The IO_LV_SSC_MONITOR_POLARITY.SSC_MONITOR_POLARITY bits are used to configure the value that triggers the safe mode for each input. Each bit of this 16-bit field corresponds to an individual monitor trigger polarity, where bit 0 relates to monitoring SAIF 0, bit 1 relates to monitoring SAIF 1, etc. The value set in the bit position selects the value (0 or 1) that triggers the safe mode. 0: Selects the monitoring polarity of SAIF0. 9: Selects the monitoring polarity of SAIF9. 10: Selects the monitoring polarity of SAIF10. 11: Selects the monitoring polarity of SAIF11. 20: Selects the monitoring polarity of gPTP lock. 21: Selects the monitoring polarity of OTP configuration. 22: Selects the monitoring polarity of SQI level. 23: Selects the monitoring polarity of Global Manual Trigger.	0x0	R/W

SSC MONITOR POLARITY 2 REGISTER

OA-SPI Address: 0xC88E, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_MONITOR_POLARITY_2 register is used to configure the monitoring polarity as described below.

Table 94. Bit Descriptions for IO_LV_SSC_MONITOR_POLARITY_2

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 94. Bit Descriptions for IO_LV_SSC_MONITOR_POLARITY_2 (Continued)

Bits	Bit Name	Description	Reset	Access
[7:0]	SSC_MONITOR_POLARITY[23:16]	Safe mode trigger. The IO_LV_SSC_MONITOR_POLARITY.SSC_MONITOR_POLARITY bits are used to configure the value that triggers the safe mode for each input. Each bit of this 16-bit field corresponds to an individual monitor trigger polarity, where bit 0 relates to monitoring SAIF 0, bit 1 relates to monitoring SAIF 1, etc. The value set in the bit position selects the value (0 or 1) that triggers the safe mode. 0: Selects the monitoring polarity of SAIF0. 9: Selects the monitoring polarity of SAIF9. 10: Selects the monitoring polarity of SAIF10. 11: Selects the monitoring polarity of SAIF11. 20: Selects the monitoring polarity of gPTP lock. 21: Selects the monitoring polarity of OTP configuration. 22: Selects the monitoring polarity of SQI level. 23: Selects the monitoring polarity of Global Manual Trigger.	0x0	R/W

SSC ETHERNET FRAME TIMEOUT REGISTER

OA-SPI Address: 0xC88F, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_TIMEOUT_TIME_ETHERNET_TRAFFIC register is used to configure the valid Ethernet frame received timeout time.

Table 95. Bit Descriptions for IO_LV_SSC_TIMEOUT_TIME_ETHERNET_TRAFFIC

Bits	Bit Name	Description	Reset	Access
[15:0]	SSC_TIMEOUT_ETHERNET_ACTIVITY	Timeout 0 configure. The IO_LV_SSC_TIMEOUT_TIME_ETHERNET_TRAFFIC.SSC_TIMEOUT_ETHERNET_ACTIVITY bits are used to configure the timeout 0 value, in steps of 81.92 us.	0x0	R/W

SSC DEVICE UNATTENDED TIMEOUT REGISTER

OA-SPI Address: 0xC890, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_TIMEOUT_TIME_DEVICE_UNATTENDED register is used to configure the device unattended timeout time.

Table 96. Bit Descriptions for IO_LV_SSC_TIMEOUT_TIME_DEVICE_UNATTENDED

Bits	Bit Name	Description	Reset	Access
[15:0]	SSC_TIMEOUT_DEVICE_UNATTENDED	Timeout 1 configure. The IO_LV_SSC_TIMEOUT_TIME_DEVICE_UNATTENDED.SSC_TIMEOUT_DEVICE_UNATTENDED bits are used to configure the timeout 1 value, in steps of 81.92 us.	0x0	R/W

SSC AUTO RETURN TO FUNCTIONAL ENABLE REGISTER

OA-SPI Address: 0xC893, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN register is used to configure programs to enable/disable the auto return to functional mode feature for fault detection mechanism (where this is supported).

Table 97. Bit Descriptions for IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R/W
[11:0]	SSC_SA_IF_MON_AUTO_RETURN	Auto return for SAIF. The IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN.SSC_SA_IF_MON_AUTO_RETURN bits are used to activate the auto return to functional feature for the SAIF checks. Each bit of this 12-bit field corresponds to an individual SAIF pin, where bit 0 relates to SAIF pin 0, bit 1 relates to SAIF pin 1, etc. Setting the bit position to one (1) enables the auto return to functional feature of that SAIF monitor. 0: SAIF0. 9: SAIF9.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 97. Bit Descriptions for IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN (Continued)

Bits	Bit Name	Description	Reset	Access
		10: SAIF10. 11: SAIF11.		

SSC AUTO RETURN TO FUNCTIONAL EN2 REGISTER

OA-SPI Address: 0xC894, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN2 register is used to configure programs to enable/disable the auto return to functional mode feature for fault detection mechanism (where this is supported).

Table 98. Bit Descriptions for IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN2

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	SSC_ETH_TIMEOUT_AUTO_RETURN	Auto return for valid Ethernet frames. The IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN2.SSC_ETH_TIMEOUT_AUTO_RETURN bit activates the auto return to functional feature for the valid Ethernet frames received checks. 0: Disable. 1: Enable.	0x0	R/W
0	SSC_GPTP_LOCK_MON_AUTO_RETURN	Auto return gPTP lock. The IO_LV_SSC_AUTO_RETURN_TO_FUNCTIONAL_EN2.SSC_GPTP_LOCK_MON_AUTO_RETURN bit activates the auto return to functional feature for the gPTP lock checks. 0: Disable. 1: Enable.	0x0	R/W

SSC CONTROL REGISTER

OA-SPI Address: 0xC895, MMS: 0xA, Reset: 0x2000

The IO_LV_SSC_CONTROLS register is used to configure the SSC controller as described below.

Table 99. Bit Descriptions for IO_LV_SSC_CONTROLS

Bits	Bit Name	Description	Reset	Access
15	SSC_RETURN_TO_FUNCTIONAL_MODE	Return to functional mode. The IO_LV_SSC_CONTROLS.SSC_RETURN_TO_FUNCTIONAL_MODE bit, when triggered, returns to functional mode if safe conditions have disappeared.	0x0	R0/W1S
14	SSC_BEACON_TIMEOUT_CHECK	Beacon monitoring enable. The IO_LV_SSC_CONTROLS.SSC_BEACON_TIMEOUT_CHECK bit configures whether the beacon monitoring is added to the Ethernet traffic check. 0: Disable. 1: Enable.	0x0	R/W
13	RESERVED	Reserved.	0x1	R/W
12	SSC_SQI_MON_YELLOW_RED	SQI level safe mode. The IO_LV_SSC_CONTROLS.SSC_SQI_MON_YELLOW_RED bit selects from which SQI level the safe mode is to be triggered. 0: Red. 1: Yellow and red.	0x0	R/W
[11:0]	SSC_SAFE_MODE_ENABLE	Pin safe mode enable. The IO_LV_SSC_CONTROLS.SSC_SAFE_MODE_ENABLE bits configure whether a pin is in safe mode or functional mode. Each bit of this 12-bit field corresponds to an individual SAIF pin, where bit 0 relates to SAIF pin 0, bit 1 relates to SAIF pin 1, etc. Setting the bit position to one (1) enables the safe configuration of that SAIF pin while in SAFE mode. 0: SAIF0. 1: TS_TIMER.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 99. Bit Descriptions for IO_LV_SSC_CONTROLS (Continued)

Bits	Bit Name	Description	Reset	Access
		2: TS_CAPT. 3: TEST1. 4: SCLK. 5: IRQn. 6: CSn. 7: SDI. 8: SDO. 9: SAIF9. 10: SAIF10. 11: SAIF11.		

SSC SAFE CHECKS ENABLE REGISTER

OA-SPI Address: 0xC896, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_SAFE_CHECKS_ENABLE register is used to enable/disable the monitoring of each of the fault detection mechanisms and enable/disable the timeout counters for the Ethernet frame timeout and the device unattended timeout mechanisms.

Table 100. Bit Descriptions for IO_LV_SSC_SAFE_CHECKS_ENABLE

Bits	Bit Name	Description	Reset	Access
[15:0]	SSC_MONITOR_ENABLE[15:0]	Select input monitor enable. The IO_LV_SSC_SAFE_CHECKS_ENABLE.SSC_MONITOR_ENABLE bits enable the monitoring of each selected input. The enumeration table values indicate the bit position of each monitor trigger. Setting the bit position to one (1) enables the monitoring of the trigger. 0: Activate the safe state controller monitoring of SAIF0. 9: Activate the safe state controller monitoring of SAIF9. 10: Activate the safe state controller monitoring of SAIF10. 11: Activate the safe state controller monitoring of SAIF11. 20: Activate the safe state controller monitoring of gPTP lock. 21: Activate the safe state controller monitoring of OTP configuration. 22: Activate the safe state controller monitoring of SQI level. 23: Activate the safe state controller monitoring of Global Manual Trigger.	0x0	R/W

SSC SAFE CHECKS ENABLE 2 REGISTER

OA-SPI Address: 0xC897, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_SAFE_CHECKS_ENABLE_2 register is used to enable/disable the monitoring of each of the fault detection mechanisms and enable/disable the timeout counters for the Ethernet frame timeout and the device unattended timeout mechanisms.

Table 101. Bit Descriptions for IO_LV_SSC_SAFE_CHECKS_ENABLE_2

Bits	Bit Name	Description	Reset	Access
15	SSC_TIMEOUT_ENABLE_DEVICE_UNATTENDED	Timeout 1 enable. The IO_LV_SSC_SAFE_CHECKS_ENABLE_2.SSC_TIMEOUT_ENABLE_DEVICE_UNATTENDED bit is used to enable SSC timeout 1. 0: Timeout Disabled. 1: Timeout Enabled.	0x0	R/W
14	SSC_TIMEOUT_ENABLE_ETHERNET_TRAFFIC	Timeout 0 enable. The IO_LV_SSC_SAFE_CHECKS_ENABLE_2.SSC_TIMEOUT_ENABLE_ETHERNET_TRAFFIC bit is used to enable SSC timeout 0. 0: Timeout Disabled. 1: Timeout Enabled.	0x0	R/W
[13:8]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 101. Bit Descriptions for IO_LV_SSC_SAFE_CHECKS_ENABLE_2 (Continued)

Bits	Bit Name	Description	Reset	Access
[7:0]	SSC_MONITOR_ENABLE[23:16]	Select input monitor enable. The IO_LV_SSC_SAFE_CHECKS_ENABLE.SSC_MONITOR_ENABLE bits enable the monitoring of each selected input. The enumeration table values indicate the bit position of each monitor trigger. Setting the bit position to one (1) enables the monitoring of the trigger. 0: Activate the safe state controller monitoring of SAIF0. 9: Activate the safe state controller monitoring of SAIF9. 10: Activate the safe state controller monitoring of SAIF10. 11: Activate the safe state controller monitoring of SAIF11. 20: Activate the safe state controller monitoring of gPTP lock. 21: Activate the safe state controller monitoring of OTP configuration. 22: Activate the safe state controller monitoring of SQI level. 23: Activate the safe state controller monitoring of Global Manual Trigger.	0x0	R/W

SSC MONITOR TRIGGERS REGISTER

OA-SPI Address: 0xC898, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_MONITOR_TRIGGERS register is used to manually enter safe state mode.

Table 102. Bit Descriptions for IO_LV_SSC_MONITOR_TRIGGERS

Bits	Bit Name	Description	Reset	Access
15	SSC_MANUAL_ENTER_SAFE_MODE	Manual safe mode enable. The IO_LV_SSC_MONITOR_TRIGGERS.SSC_MANUAL_ENTER_SAFE_MODE bit is used to allow SSC software monitoring and enabling a trigger to manually enter safe mode.	0x0	R/W
[14:0]	RESERVED	Reserved.	0x0	R

SSC MISCELLANEOUS REGISTER

OA-SPI Address: 0xC899, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_MISC register is used to manage interrupts as described below.

Table 103. Bit Descriptions for IO_LV_SSC_MISC

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	SSC_CLEAR_ALL_TRIGGERS	Clear all sticky interrupts. The IO_LV_SSC_MISC.SSC_CLEAR_ALL_TRIGGERS bit is used to clear all sticky readback flags. 0: Inactive. 1: Trigger.	0x0	R0/W1S
0	SSC_DEVICE_UNNATTENDED_CHECK	Prevent timeout. The IO_LV_SSC_MISC.SSC_DEVICE_UNNATTENDED_CHECK bit is used to prevent a timeout flag that triggers the SSC and causes it to enter safe mode. This bit should be periodically written to 1'b1. 0: Inactive. 1: Trigger.	0x0	R0/W1S

SSC RECOVERED DATA FROM ALWAYS ON REGISTER

OA-SPI Address: 0xC89A, MMS: 0xA, Reset: 0x0000

The IO_LV_SSC_RECOVERED_DATA_FROM_AO register contains the trigger index value.

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 104. Bit Descriptions for IO_LV_SSC_RECOVERED_DATA_FROM_AO

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	SSC_MODE_FROM_AO	Sleep mode value. The IO_LV_SSC_RECOVERED_DATA_FROM_AO.SSC_MODE_FROM_AO bit indicates the mode value when the device went to sleep. This field is updated during the bootload. 0: Functional. 1: Safe.	0x0	R/W
[4:0]	SSC_TRIGGERED_INDEX_FROM_AO	Trigger index value. The IO_LV_SSC_RECOVERED_DATA_FROM_AO.SSC_TRIGGERED_INDEX_FROM_AO indicates the trigger index value received from the always on domain. This field is updated during bootload and represents the last cause which made the device enter safe_mode before bootloader run. 00000: SAIF0. 01001: SAIF9. 01010: SAIF10. 01011: SAIF11. 10100: gPTP Unlocked. 10101: OTP configuration error. 10110: SQI degradation. 10111: Global manual trigger. 11000: Unused. 11001: Unused. 11010: Unused. 11011: Unused. 11100: Unused. 11101: Unused. 11110: Timeout valid Ethernet frames. 11111: Device is unattended.	0x0	R/W

BLOCK RESET CONTROL REGISTER

OA-SPI Address: 0xC8FE, MMS: 0xA, Reset: 0x0000

The IO_LV_BLOCK_RESET_CONTROL register is used to configure various system resets.

Table 105. Bit Descriptions for IO_LV_BLOCK_RESET_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	MAC_PHY_SOFT_RESET	MAC PHY Soft Reset. The IO_LV_BLOCK_RESET_CONTROL.MAC_PHY_SOFT_RESET bit performs a soft reset of the MAC-PHY module. This is a self-clearing bit.	0x0	R0/W1S
4	RESERVED	Reserved.	0x0	R0/W1S
3	WAKE_SLEEP_SOFT_RESET	Wake Sleep Controller Reset. The IO_LV_BLOCK_RESET_CONTROL.WAKE_SLEEP_SOFT_RESET bit performs a wake sleep controller reset. This is a self-clearing bit. 0: Inactive. 1: Trigger.	0x0	R0/W1S
2	BOOT_LOADER_SOFT_RESET	Bootloader Reset. The IO_LV_BLOCK_RESET_CONTROL.BOOT_LOADER_SOFT_RESET bit performs a bootloader reset. A reset to the LV die bootloader triggers a re-boot of the LV die bootloader contents only. This is a self-clearing bit. 0: Inactive. 1: Trigger.	0x0	R0/W1S

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 105. Bit Descriptions for IO_LV_BLOCK_RESET_CONTROL (Continued)

Bits	Bit Name	Description	Reset	Access
[1:0]	RESERVED	Reserved.	0x0	R0/W1S

RESET CONTROL REGISTER

OA-SPI Address: 0xC8FF, MMS: 0xA, Reset: 0x0000

The IO_LV_RESET_CONTROL register is used for the main soft reset of the LV die.

Table 106. Bit Descriptions for IO_LV_RESET_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:0]	RESET	Main Soft Reset LV Die. The IO_LV_RESET_CONTROL.RESET bit field is the main soft reset signature. To execute a soft reset of the LV die, write the value of 0xA55A to this field. This resets the CLK25 domain, CLK100 domain, PHY, LV register map and the MAC.	0x0	R/W

INTER DIE SERIAL COMMUNICATION REGISTER

OA-SPI Address: 0xC900, MMS: 0xA, Reset: 0x0000

The IO_LV_INTER_DIE_SERIAL_COMMUNICATION register provides information about the status of communication over the inter die interface.

Table 107. Bit Descriptions for IO_LV_INTER_DIE_SERIAL_COMMUNICATION

Bits	Bit Name	Description	Reset	Access
15	HS_COMM_TIMEOUT_ERR_RB	No acknowledge received. The IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_TIMEOUT_ERR_RB bit indicates that no acknowledge is received from the inter-die interface. The value is kept until it is cleared with the IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_TIMEOUT_ERR_CLEAN. 0: Not triggered. 1: Triggered.	0x0	R
14	HS_COMM_PARITY_ERR_RB	Parity error. The IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_PARITY_ERR_RB bit indicates a parity error from the inter-die interface. The value is kept until it is cleaned with IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_PARITY_ERR_CLEAN. 0: Not triggered. 1: Triggered.	0x0	R
13	HS_COMM_BIT_STOP_ERR_RB	Bit stop error. The IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_BIT_STOP_ERR_RB bit indicates a bit stop error from the inter-die interface. The value is kept until it is cleaned with IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_BIT_STOP_ERR_CLEAN. 0: Not triggered. 1: Triggered.	0x0	R
[12:3]	RESERVED	Reserved.	0x0	R
2	HS_COMM_TIMEOUT_ERR_CLEAN	Timeout error clear. The IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_TIMEOUT_ERR_CLEAN bit is used to clear a timeout error clean from the inter-die interface. 1: Trigger. 0: Inactive.	0x0	R0/W1S
1	HS_COMM_PARITY_ERR_CLEAN	Parity error clear. The IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_PARITY_ERR_CLEAN bit is used to clear a parity error from the inter-die interface. 1: Trigger. 0: Inactive.	0x0	R0/W1S
0	HS_COMM_BIT_STOP_ERR_CLEAN	Bit stop error clear. The IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_BIT_STOP_ERR_CLEAN	0x0	R0/W1S

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 107. Bit Descriptions for IO_LV_INTER_DIE_SERIAL_COMMUNICATION (Continued)

Bits	Bit Name	Description	Reset	Access
		bit is used to clear the IO_LV_INTER_DIE_SERIAL_COMMUNICATION.HS_COMM_BIT_STOP_ERR_RB bit. 1: Trigger. 0: Inactive.		

GPTP SYNC COUNT REGISTER

OA-SPI Address: 0xC901, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_SYNC_COUNT register stores the lower 16 bits of the the 802.1AS received sync message count.

Table 108. Bit Descriptions for IO_LV_GPTP_SYNC_COUNT

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RX_SYNC_COUNT[15:0]	Number of sync messages received. The IO_LV_GPTP_SYNC_COUNT.GPTP_RX_SYNC_COUNT bits count the number of sync messages received by the gPTP algorithm.	0x0	R

GPTP SYNC COUNT 1 REGISTER

OA-SPI Address: 0xC902, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_SYNC_COUNT_1 register stores the upper 16 bits of the the 802.1AS received sync message count.

Table 109. Bit Descriptions for IO_LV_GPTP_SYNC_COUNT_1

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RX_SYNC_COUNT[31:16]	Number of sync messages received. The IO_LV_GPTP_SYNC_COUNT.GPTP_RX_SYNC_COUNT bits count the number of sync messages received by the gPTP algorithm.	0x0	R

GPTP ONESTEP COUNT REGISTER

OA-SPI Address: 0xC903, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_ONESTEP_COUNT register stores the lower 16 bits of the 802.1AS received one step sync message count.

Table 110. Bit Descriptions for IO_LV_GPTP_ONESTEP_COUNT

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RX_ONE_STEP_SYNC_COUNT[15:0]	One step sync messages received. The IO_LV_GPTP_ONESTEP_COUNT.GPTP_RX_ONE_STEP_SYNC_COUNT bits counts the number of one step sync messages received by the gPTP algorithm.	0x0	R

GPTP ONESTEP COUNT 1 REGISTER

OA-SPI Address: 0xC904, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_ONESTEP_COUNT_1 register stores the upper 16 bits of the 802.1AS received one step sync message count.

Table 111. Bit Descriptions for IO_LV_GPTP_ONESTEP_COUNT_1

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RX_ONE_STEP_SYNC_COUNT[31:16]	One step sync messages received. The IO_LV_GPTP_ONESTEP_COUNT.GPTP_RX_ONE_STEP_SYNC_COUNT bits counts the number of one step sync messages received by the gPTP algorithm.	0x0	R

GPTP FOLLOWUP COUNT REGISTER

OA-SPI Address: 0xC905, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_FOLLOWUP_COUNT register stores the lower 16 bits of the 802.1AS received followup message count.

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Table 112. Bit Descriptions for IO_LV_GPTP_FOLLOWUP_COUNT

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RX_FOLLOW_UP_COUNT[15:0]	Number of followup messages received. The IO_LV_GPTP_FOLLOWUP_COUNT.GPTP_RX_FOLLOW_UP_COUNT bits count the number of followup messages received by the gPTP algorithm.	0x0	R

GPTP FOLLOWUP COUNT 1 REGISTER

OA-SPI Address: 0xC906, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_FOLLOWUP_COUNT_1 register stores the upper 16 bits of the 802.1AS received followup message count.

Table 113. Bit Descriptions for IO_LV_GPTP_FOLLOWUP_COUNT_1

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RX_FOLLOW_UP_COUNT[31:16]	Number of followup messages received. The IO_LV_GPTP_FOLLOWUP_COUNT.GPTP_RX_FOLLOW_UP_COUNT bits count the number of followup messages received by the gPTP algorithm.	0x0	R

GPTP NUMBER LOCKS REGISTER

OA-SPI Address: 0xC907, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_NUM_LOCKS register counts the number of times the GPTP_LOCKED status changed from unlocked to locked.

Table 114. Bit Descriptions for IO_LV_GPTP_NUM_LOCKS

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RX_NUMBER_OF_LOCKS	Number of locks performed. The IO_LV_GPTP_NUM_LOCKS.GPTP_RX_NUMBER_OF_LOCKS bits count the number of locks performed by the gPTP algorithm.	0x0	R

GPTP NUMBER OF UNLOCKS REGISTER

OA-SPI Address: 0xC908, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_NUM_UNLOCKS register counts the number of times the GPTP_LOCKED status changed from locked to unlocked.

Table 115. Bit Descriptions for IO_LV_GPTP_NUM_UNLOCKS

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RX_NUMBER_OF_UNLOCKS	Number of unlocks. The IO_LV_GPTP_NUM_UNLOCKS.GPTP_RX_NUMBER_OF_UNLOCKS bits count the number of unlocks performed by the gPTP algorithm.	0x0	R

GPTP SEQUENCE ID REGISTER

OA-SPI Address: 0xC909, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_SEQUENCEID register stores the sequence ID at which the GPTP_LOCKED status changed last. This can either correspond to a change from locked to unlocked or from unlocked to locked.

Table 116. Bit Descriptions for IO_LV_GPTP_SEQUENCEID

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RX_STATUS_CHANGE_SEQUENCE_ID	Sequence ID locked flag. The IO_LV_GPTP_SEQUENCEID.GPTP_RX_STATUS_CHANGE_SEQUENCE_ID bits indicate the sequence ID of the packet that produced the last edge in the locked flag.	0x0	R

GPTP LOCK THRESHOLD REGISTER

OA-SPI Address: 0xC90B, MMS: 0xA, Reset: 0x044C

The IO_LV_GPTP_LOCK_THRESHOLD register configures the threshold the timer uses.

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 117. Bit Descriptions for IO_LV_GPTP_LOCK_THRESHOLD

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
[14:0]	GPTP_LOCK_THRESHOLD	Lock Threshold. The IO_LV_GPTP_LOCK_THRESHOLD.GPTP_LOCK_THRESHOLD bits configure the threshold the timer uses for the IO_LV_GPTP_STATUS_1.GPTP_LOCKED field. In nanoseconds.	0x44C	R/W

GPTP TIME ERROR REGISTER

OA-SPI Address: 0xC910, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_TIME_ERROR register indicates the lower 16 bits of the 802.1AS time synchronization error measured in nanoseconds.

Table 118. Bit Descriptions for IO_LV_GPTP_TIME_ERROR

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_TIME_ERROR[15:0]	Current time error. The IO_LV_GPTP_TIME_ERROR.GPTP_TIME_ERROR bits indicate the current time error of the gPTP algorithm measured in nanoseconds. For example the time error value 0x0000 000A = 10 ns. This indicates the time error between the local clock and the grandmaster clock for the last received sync and follow-up pair.	0x0	R

GPTP TIME ERROR 1 REGISTER

OA-SPI Address: 0xC911, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_TIME_ERROR_1 register indicates the upper 16 bits of the 802.1AS time synchronization error measured in nanoseconds.

Table 119. Bit Descriptions for IO_LV_GPTP_TIME_ERROR_1

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_TIME_ERROR[31:16]	Current time error. The IO_LV_GPTP_TIME_ERROR.GPTP_TIME_ERROR bits indicate the current time error of the gPTP algorithm measured in nanoseconds. For example the time error value 0x0000 000A = 10 ns. This indicates the time error between the local clock and the grandmaster clock for the last received sync and follow-up pair.	0x0	R

GPTP MEAN LINK DELAY REGISTER

OA-SPI Address: 0xC912, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_MEAN_LINK_DELAY register stores the lower 16 bits of the manual latency of the cable in absence of Pdelay calculations.

Table 120. Bit Descriptions for IO_LV_GPTP_MEAN_LINK_DELAY

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_MEANLINKDELAY[15:0]	Manual latency of the cable. The IO_LV_GPTP_MEAN_LINK_DELAY.GPTP_MEANLINKDELAY bits configure the mean link delay time in nanoseconds of the gPTP algorithm. For example the value 0x0000 000A is a mean link delay of 10 ns.	0x0	R/W

GPTP MEAN LINK DELAY 1 REGISTER

OA-SPI Address: 0xC913, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_MEAN_LINK_DELAY_1 register stores the upper 16 bits of the manual latency of the cable in absence of Pdelay calculations.

Table 121. Bit Descriptions for IO_LV_GPTP_MEAN_LINK_DELAY_1

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_MEANLINKDELAY[31:16]	Manual latency of the cable. The IO_LV_GPTP_MEAN_LINK_DELAY.GPTP_MEANLINKDELAY bits configure the mean link delay time in nanoseconds of the gPTP algorithm. For example the value 0x0000 000A is a mean link delay of 10 ns.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

GPTP STATUS 1 REGISTER

OA-SPI Address: 0xC915, MMS: 0xA, Reset: 0x0000

The IO_LV_GPTP_STATUS_1 register provides gPTP status as described below.

Table 122. Bit Descriptions for IO_LV_GPTP_STATUS_1

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x0	R
8	GPTP_LOCKED	gPTP algorithm is locked. The IO_LV_GPTP_STATUS_1.GPTP_LOCKED register indicates the gPTP lock status. 0: gPTP unlocked. 1: gPTP locked.	0x0	R
[7:0]	RESERVED[23:16]	Reserved.	0x0	R

GPTP RELOCK REGISTER

OA-SPI Address: 0xC916, MMS: 0xA, Reset: 0x0000

Table 123. Bit Descriptions for IO_LV_GPTP_RELOCK

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RELOCK_THRESHOLD[15:0]	Relock threshold. The IO_LV_GPTP_RELOCK.GPTP_RELOCK_THRESHOLD bits are used to relock threshold of the gPTP engine in nanoseconds.	0x0	R/W

GPTP RELOCK 1 REGISTER

OA-SPI Address: 0xC917, MMS: 0xA, Reset: 0x0005

The IO_LV_GPTP_RELOCK_1 register is used to relock the threshold of the gPTP engine.

Table 124. Bit Descriptions for IO_LV_GPTP_RELOCK_1

Bits	Bit Name	Description	Reset	Access
[15:0]	GPTP_RELOCK_THRESHOLD[31:16]	Relock threshold. The IO_LV_GPTP_RELOCK.GPTP_RELOCK_THRESHOLD bits are used to relock threshold of the gPTP engine in nanoseconds.	0x5	R/W

GPTP CONFIGURATION REGISTER

OA-SPI Address: 0xC92A, MMS: 0xA, Reset: 0x8928

The IO_LV_GPTP_CONFIG register is used to configure the gPTP module as described below.

Table 125. Bit Descriptions for IO_LV_GPTP_CONFIG

Bits	Bit Name	Description	Reset	Access
15	GPTP_RATE_RATIO_CALCULATION_ADJUST_PHASE	Initial sync. The IO_LV_GPTP_CONFIG.GPTP_RATE_RATIO_CALCULATION_ADJUST_PHASE bit is used to Uses the algorithm for the initial synchronization to the grandmaster 1: Adjust the phase error on the third sync/followup pair. 0: Do not adjust the phase error on the third sync follow up pair.	0x1	R/W
14	GPTP_REDUNDANCY_MODE	Redundancy mode. The IO_LV_GPTP_CONFIG.GPTP_REDUNDANCY_MODE bit is used to set the redundancy mode. 0: Synchronize only to the active domain. 1: Synchroniza to the active domain but if missing, synchronize to the backup domain.	0x0	R/W
[13:11]	GPTP_NUM_REQUIRED_SYNCS_TO_RELOCK	Threshold uses for the gptp_locked field. The IO_LV_GPTP_CONFIG.GPTP_NUM_REQUIRED_SYNCS_TO_RELOCK bits	0x1	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 125. Bit Descriptions for IO_LV_GPTP_CONFIG (Continued)

Bits	Bit Name	Description	Reset	Access
		are used to configure the threshold uses for the IO_LV_GPTP_STATUS_1.GPTP_LOCKED field.		
[10:8]	GPTP_NUM_MISSING_SYNCS_TO_UNLOCK	Unlock status threshold. The IO_LV_GPTP_CONFIG.GPTP_NUM_MISSING_SYNCS_TO_UNLOCK bits are used to configure the threshold uses for the IO_LV_GPTP_STATUS_1.GPTP_LOCKED field.	0x1	R/W
[7:6]	GPTP_1PPS_MODE	1pps gPTP behavior. The IO_LV_GPTP_CONFIG.GPTP_1PPS_MODE bits are used to configure the 1pps behavior. 00: Adi 1pps mode, not intended to be used. 01: Ieee 1pps mode, recommended mode. 10: Adi 8 pps mode.	0x0	R/W
5	GPTP_INITIAL_RATE_RATIO_CALCULATION	Initial sync. The IO_LV_GPTP_CONFIG.GPTP_INITIAL_RATE_RATIO_CALCULATION bit is used to instruct the grandmaster to use the algorithm for the initial synchronization. 0: Uses the default algorithm for the initial synchronization to the grandmaster. 1: Uses the fast algorithm for the initial synchronization to the grandmaster.	0x1	R/W
[4:0]	GPTP_NUM_FAST_ADJUST_FRAMES	Fast mode duration. The IO_LV_GPTP_CONFIG.GPTP_NUM_FAST_ADJUST_FRAMES bits are used to configure the number of frames where the core is in fast mode.	0x8	R/W

TIC STATUS FLAGS 8 AND 9 REGISTER

OA-SPI Address: 0xC93A, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_STATUS_FLAGS_8_AND_9 register reports the interrupt status flags for the MAC and PHY interfaces.

Table 126. Bit Descriptions for IO_LV_TIC_STATUS_FLAGS_8_AND_9

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	TIC_STATUS_FLAGS_9	PLCA interrupt status. The IO_LV_TIC_STATUS_FLAGS_8_AND_9.TIC_STATUS_FLAGS_9 bits provide the status flag of the interrupts as shown below. When the bit is set (=1) the condition exists. The table values below indicate the bit position of each interrupt status. 8: MAC Receive Frame Dropped Due To The RX FIFO Being Full. 9: PHY Error Detected in MAC Receive Frame. 12: CRC Error Detected in MAC Receive Frame.	0x0	R
7	RESERVED	Reserved.	0x0	R
[6:0]	TIC_STATUS_FLAGS_8	MAC PHY interrupt status. The IO_LV_TIC_STATUS_FLAGS_8_AND_9.TIC_STATUS_FLAGS_8 bits provide the status flag of the interrupts as shown below. When the bit is set (=1) the condition exists. The table values below indicate the bit position of each interrupt status. 2: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 3: PLCA Recovery Procedure Performed.	0x0	R

TIC STATUS FLAGS 10 AND 11 REGISTER

OA-SPI Address: 0xC93B, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_STATUS_FLAGS_10_AND_11 register reports the interrupt status flags for the PLCA interface.

Table 127. Bit Descriptions for IO_LV_TIC_STATUS_FLAGS_10_AND_11

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 127. Bit Descriptions for IO_LV_TIC_STATUS_FLAGS_10_AND_11 (Continued)

Bits	Bit Name	Description	Reset	Access
[2:0]	TIC_STATUS_FLAGS_10	PLCA interrupt status. The IO_LV_TIC_STATUS_FLAGS_10_AND_11.TIC_STATUS_FLAGS_10 bits provide the status flag of the interrupts as shown below. When the bit is set (=1) the condition exists. The table values below indicate the bit position of each interrupt status. 0: PLCA_DIAG_RISING.	0x0	R

TIC STATUS FLAGS 28 AND 29 REGISTER

OA-SPI Address: 0xC944, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_STATUS_FLAGS_28_AND_29 register provides the status of sleep/wake, UMC, HS_COMM, gPTP, BOOTLOADER and MANUAL interrupts.

Table 128. Bit Descriptions for IO_LV_TIC_STATUS_FLAGS_28_AND_29

Bits	Bit Name	Description	Reset	Access
[15:8]	TIC_STATUS_FLAGS_29	UMC, HS_COMM, GPTP, BOOTLOADER and MANUAL interrupt status. The IO_LV_TIC_STATUS_FLAGS_28_AND_29.TIC_STATUS_FLAGS_29 bits provide the status flag of UMC, HS_COMM, gPTP, BOOTLOADER and MANUAL interrupts. When the bit is set (=1) the condition exists. The table values below indicate the bit position of each interrupt status. 11: GPTP_LOCK. 12: The bootloading process is finished. 13: Manually triggered interrupt (for debug purposes). 15: Internal communications error between the two silicon cores in the package.	0x0	R
7	RESERVED	Reserved.	0x0	R
[6:0]	TIC_STATUS_FLAGS_28	SLPWK interrupt status. The IO_LV_TIC_STATUS_FLAGS_28_AND_29.TIC_STATUS_FLAGS_28 bits provide the status flag of SLPWK interrupts. When the bit is set (=1) the condition exists. The table values below indicate the bit position of each interrupt status. 1: The sleep-wake controller confirms an awaken state after booting up and successfully detecting traffic on the network. 2: The sleep-wake controller timed-out a request to sleep (or standby) while waiting to end own network transmissions. 3: The sleep-wake controller could not comply with the request to go to sleep. 4: The sleep-wake controller could not comply with the request to go to standby. 5: The sleep-wake controller confirms an awaken state after being in standby. 6: The sleep-wake controller is trying to wake up the system via WUP, and requests a confirmation from the system software to clear this interrupt, as a means to acknowledge that the system is awake. After a timeout, this flag will auto-clear and get re-triggered along with a new WUP transmission.	0x0	R

TIC STATUS FLAGS 34 AND 35 REGISTER

OA-SPI Address: 0xC947, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_STATUS_FLAGS_34_AND_35 register provides the status of GPIO and SSC interrupts.

Table 129. Bit Descriptions for IO_LV_TIC_STATUS_FLAGS_34_AND_35

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	TIC_STATUS_FLAGS_34	Status flag of SSC interrupts. The IO_LV_TIC_STATUS_FLAGS_34_AND_35.TIC_STATUS_FLAGS_34 bits provide the status flag of SSC interrupts. When the bit is set (=1) the condition exists. The table values below indicate the bit position of each interrupt status. 1: Status of the interrupt that monitors the SAIF9 value.	0x0	R

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Table 129. Bit Descriptions for IO_LV_TIC_STATUS_FLAGS_34_AND_35 (Continued)

Bits	Bit Name	Description	Reset	Access
		2: Status of the interrupt that monitors the SAIF10 value. 3: Status of the interrupt that monitors the SAIF11 value. 4: Status of the safe state controller mode interrupt. 5: Status of the safe state controller unsuccessful return to functional mode interrupt. 6: Status of the sqi reaches warning interrupt. 7: Status of the sqi reaches bad interrupt.		

TIC CONTROL REGISTER 0

OA-SPI Address: 0xC94D, MMS: 0xA, Reset: 0x8480

The IO_LV_TIC_CONTROL0 register is used to configure the TIC resend period.

Table 130. Bit Descriptions for IO_LV_TIC_CONTROL0

Bits	Bit Name	Description	Reset	Access
[15:0]	TIC_RESEND_PERIOD[15:0]	TIC resend period. The IO_LV_TIC_CONTROL0.TIC_RESEND_PERIOD bits configure the TIC resend period in nanoseconds. The bit weighting of time is 1 ns, but the value introduced in the field is rounded to the nearest 10 ns multiplier. If the value is 0000 0000 0000 0000, there are no resends. For value 0000 0000 0000 0100, 4ns is selected, but the value seen in the resend period is 10 ns.	0x8480	R/W

TIC CONTROL REGISTER 1

OA-SPI Address: 0xC94E, MMS: 0xA, Reset: 0x041E

The IO_LV_TIC_CONTROL1 register contains bits that control interrupt generation.

Table 131. Bit Descriptions for IO_LV_TIC_CONTROL1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	TIC_OASPI_INT_DISABLE	Disable OA-SPI Interrupts. If the IO_LV_TIC_CONTROL1.TIC_OASPI_INT_DISABLE bit =1, the transaction interrupt controller does not generate an OA-SPI interrupt when an interrupt is triggered. **Note:** This bit field can be written correctly, but readback will always returns 0. 0: Inactive. 1: Trigger.	0x1	R0/W
9	RESERVED	Reserved.	0x0	R0/W
8	TIC_CLEAR_ALL	Clear all interrupts. The IO_LV_TIC_CONTROL1.TIC_CLEAR_ALL bit clears all interrupts generated by the transceiver. 0: Inactive. 1: Trigger.	0x0	R0/W1S
[7:0]	TIC_RESEND_PERIOD[23:16]	TIC resend period. The IO_LV_TIC_CONTROL0.TIC_RESEND_PERIOD bits configure the TIC resend period in nanoseconds. The bit weighting of time is 1 ns, but the value introduced in the field is rounded to the nearest 10 ns multiplier. If the value is 0000 0000 0000 0000, there are no resends. For value 0000 0000 0000 0100, 4ns is selected, but the value seen in the resend period is 10 ns.	0x1E	R/W

TIC ENABLE 8 PHY REGISTER 0

OA-SPI Address: 0xC961, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_8_PHY_REG0 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 132. Bit Descriptions for IO_LV_TIC_ENABLE_8_PHY_REG0

Bits	Bit Name	Description	Reset	Access
[15:0]	TIC_ENABLE_8[15:0]	Interrupts enable PHY. The IO_LV_TIC_ENABLE_8_PHY_REG0.TIC_ENABLE_8 bits enable PHY interrupts by setting the bit (=1). 2: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 3: PLCA Recovery Procedure Performed. 10: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 11: PLCA Recovery Procedure Performed. 18: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 19: PLCA Recovery Procedure Performed. 26: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 27: PLCA Recovery Procedure Performed.	0x0	R/W

TIC ENABLE 8 PHY REGISTER 1

OA-SPI Address: 0xC962, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_8_PHY_REG1 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 133. Bit Descriptions for IO_LV_TIC_ENABLE_8_PHY_REG1

Bits	Bit Name	Description	Reset	Access
[15:0]	TIC_ENABLE_8[31:16]	Interrupts enable PHY. The IO_LV_TIC_ENABLE_8_PHY_REG0.TIC_ENABLE_8 bits enable PHY interrupts by setting the bit (=1). 2: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 3: PLCA Recovery Procedure Performed. 10: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 11: PLCA Recovery Procedure Performed. 18: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 19: PLCA Recovery Procedure Performed. 26: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 27: PLCA Recovery Procedure Performed.	0x0	R/W

TIC ENABLE 9 MAC REGISTER 0

OA-SPI Address: 0xC963, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_9_MAC_REG0 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 134. Bit Descriptions for IO_LV_TIC_ENABLE_9_MAC_REG0

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	TIC_ENABLE_9_FALLING	Interrupts enable MAC. The IO_LV_TIC_ENABLE_9_MAC_REG0.TIC_ENABLE_9_FALLING bits enable MAC interrupts by setting the bit (=1). The values in the table are the bit position of each interrupt, not the value to perform the clear/enable operation. 0: MAC Receive Frame Dropped Due To The RX FIFO Being Full. 1: PHY Error Detected in MAC Receive Frame. 4: CRC Error Detected in MAC Receive Frame.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 134. Bit Descriptions for IO_LV_TIC_ENABLE_9_MAC_REG0 (Continued)

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	TIC_ENABLE_9_RISING	Interrupts enable MAC rising. The IO_LV_TIC_ENABLE_9_MAC_REG0.TIC_ENABLE_9_RISING bits enable MAC interrupts by setting the bit (=1). 0: MAC Receive Frame Dropped Due To The RX FIFO Being Full. 1: PHY Error Detected in MAC Receive Frame. 4: CRC Error Detected in MAC Receive Frame.	0x0	R/W

TIC ENABLE 9 MAC REGISTER 1

OA-SPI Address: 0xC964, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_9_MAC_REG1 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 135. Bit Descriptions for IO_LV_TIC_ENABLE_9_MAC_REG1

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	TIC_ENABLE_9_LOW	Interrupts enable MAC. The IO_LV_TIC_ENABLE_9_MAC_REG1.TIC_ENABLE_9_LOW bits enable MAC interrupts by setting the bit (=1). The values in the table are the bit position of each interrupt, not the value to perform the clear/enable operation. 0: MAC_RX_FRAME_DROP_FULL_LOW. 1: MAC_RX_PHY_ERROR_LOW. 4: MAC_RX_ERROR_CRC_LOW.	0x0	R/W
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	TIC_ENABLE_9_HIGH	Interrupts enable MAC. The IO_LV_TIC_ENABLE_9_MAC_REG1.TIC_ENABLE_9_HIGH bits enable MAC interrupts by setting the bit (=1). The values in the table are the bit position of each interrupt, not the value to perform the clear/enable operation. 0: MAC_RX_FRAME_DROP_FULL_HIGH. 1: MAC_RX_PHY_ERROR_HIGH. 4: MAC_RX_ERROR_CRC_HIGH.	0x0	R/W

TIC ENABLE 10 PLCA REGISTER 0

OA-SPI Address: 0xC965, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_10_REG0 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 136. Bit Descriptions for IO_LV_TIC_ENABLE_10_REG0

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
[10:8]	TIC_ENABLE_10_FALLING	Interrupts enable falling. PLCA diagnostics interrupt. The enumeration table values indicates the bit position of each interrupt enable, not the value that has to be written to do the interrupt enable. Setting the bit position to one (1) enables the interrupt. 0: PLCA_DIAG_FALLING.	0x0	R/W
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	TIC_ENABLE_10_RISING	Interrupts enable rising. BB stands for Bus Busy. DNACK stands for Device Nack, that is the nack received when sending the device address. Setting the bit position to one (1) enables the interrupt. 0: PLCA_DIAG_RISING.	0x0	R/W

TIC ENABLE 28 MISCELLANEOUS 0 REGISTER 0

OA-SPI Address: 0xC989, MMS: 0xA, Reset: 0x0000

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

The IO_LV_TIC_ENABLE_28_MISC0_REG0 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 137. Bit Descriptions for IO_LV_TIC_ENABLE_28_MISC0_REG0

Bits	Bit Name	Description	Reset	Access
[15:0]	TIC_ENABLE_28[15:0]	Interrupts enable SLEEP_WAKE and SERIAL_COMM. The IO_LV_TIC_ENABLE_28_MISC0_REG1.TIC_ENABLE_28 bits enable SLEEP_WAKE and SERIAL_COMM interrupts by setting the bit (=1). Clearing the bit (=0) disables the interrupt. The values in the table are the bit position of each interrupt, not the value to perform the enable/disable operation. 0: SLPWK_FLAG_CONTROLLER_MODE_RISING. 1: SLPWK_FLAG_CONFIRM_AWAKE_RISING. 2: SLPWK_FLAG_LINE_BUSY_RISING. 3: SLPWK_FLAG_SLEEP_ERR_RISING. 4: SLPWK_FLAG_STANDBY_ERR_RISING. 5: SLPWK_FLAG_RETURNED_FROM_STANDBY_RISING. 6: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_RISING. 9: SLPWK_FLAG_CONFIRM_AWAKE_FALLING. 10: SLPWK_FLAG_LINE_BUSY_FALLING. 11: SLPWK_FLAG_SLEEP_ERR_FALLING. 12: SLPWK_FLAG_STANDBY_ERR_FALLING. 13: SLPWK_FLAG_RETURNED_FROM_STANDBY_FALLING. 14: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_FALLING. 16: SLPWK_FLAG_CONTROLLER_MODE_HIGH. 17: SLPWK_FLAG_CONFIRM_AWAKE_HIGH. 18: SLPWK_FLAG_LINE_BUSY_HIGH. 19: SLPWK_FLAG_SLEEP_ERR_HIGH. 20: SLPWK_FLAG_STANDBY_ERR_HIGH. 21: SLPWK_FLAG_RETURNED_FROM_STANDBY_HIGH. 22: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_HIGH. 24: SLPWK_FLAG_CONTROLLER_MODE_LOW. 25: SLPWK_FLAG_CONFIRM_AWAKE_LOW. 26: SLPWK_FLAG_LINE_BUSY_LOW. 27: SLPWK_FLAG_SLEEP_ERR_LOW. 28: SLPWK_FLAG_STANDBY_ERR_LOW. 29: SLPWK_FLAG_RETURNED_FROM_STANDBY_LOW. 30: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_LOW.	0x0	R/W

TIC ENABLE 28 MISCELLANEOUS 0 REGISTER 1

OA-SPI Address: 0xC98A, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_28_MISC0_REG1 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 138. Bit Descriptions for IO_LV_TIC_ENABLE_28_MISC0_REG1

Bits	Bit Name	Description	Reset	Access
[15:0]	TIC_ENABLE_28[31:16]	Interrupts enable SLEEP_WAKE and SERIAL_COMM. The IO_LV_TIC_ENABLE_28_MISC0_REG1.TIC_ENABLE_28 bits enable SLEEP_WAKE and SERIAL_COMM interrupts by setting the bit (=1). Clearing the bit (=0) disables the interrupt. The values in the table are the bit position of each interrupt, not the value to perform the enable/disable operation. 0: SLPWK_FLAG_CONTROLLER_MODE_RISING. 1: SLPWK_FLAG_CONFIRM_AWAKE_RISING.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 138. Bit Descriptions for IO_LV_TIC_ENABLE_28_MISC0_REG1 (Continued)

Bits	Bit Name	Description	Reset	Access
		2: SLPWK_FLAG_LINE_BUSY_RISING. 3: SLPWK_FLAG_SLEEP_ERR_RISING. 4: SLPWK_FLAG_STANDBY_ERR_RISING. 5: SLPWK_FLAG_RETURNED_FROM_STANDBY_RISING. 6: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_RISING. 9: SLPWK_FLAG_CONFIRM_AWAKE_FALLING. 10: SLPWK_FLAG_LINE_BUSY_FALLING. 11: SLPWK_FLAG_SLEEP_ERR_FALLING. 12: SLPWK_FLAG_STANDBY_ERR_FALLING. 13: SLPWK_FLAG_RETURNED_FROM_STANDBY_FALLING. 14: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_FALLING. 16: SLPWK_FLAG_CONTROLLER_MODE_HIGH. 17: SLPWK_FLAG_CONFIRM_AWAKE_HIGH. 18: SLPWK_FLAG_LINE_BUSY_HIGH. 19: SLPWK_FLAG_SLEEP_ERR_HIGH. 20: SLPWK_FLAG_STANDBY_ERR_HIGH. 21: SLPWK_FLAG_RETURNED_FROM_STANDBY_HIGH. 22: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_HIGH. 24: SLPWK_FLAG_CONTROLLER_MODE_LOW. 25: SLPWK_FLAG_CONFIRM_AWAKE_LOW. 26: SLPWK_FLAG_LINE_BUSY_LOW. 27: SLPWK_FLAG_SLEEP_ERR_LOW. 28: SLPWK_FLAG_STANDBY_ERR_LOW. 29: SLPWK_FLAG_RETURNED_FROM_STANDBY_LOW. 30: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_LOW.		

TIC ENABLE 29 MISCELLANEOUS 1 REGISTER 0

OA-SPI Address: 0xC98B, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_29_MISC1_REG0 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 139. Bit Descriptions for IO_LV_TIC_ENABLE_29_MISC1_REG0

Bits	Bit Name	Description	Reset	Access
[15:8]	TIC_ENABLE_29_FALLING	Interrupts enable UMC - GPTP - BOOTLOADER - MANUAL falling. The IO_LV_TIC_ENABLE_29_MISC1_REG0.TIC_ENABLE_29_FALLING bits enable UMC - GPTP - BOOTLOADER - MANUAL interrupts by setting the bit (=1). Clearing the bit (=0) disables the interrupt. 3: GPTP_LOCK_FALLING. 4: BOOTLOADER_DONE_FALLING. 5: MANUAL_INTERRUPT_FALLING. 6: EFUSE_CTRL_PRG_FALLING. 7: HS_COMM_ERROR.	0x0	R/W
[7:0]	TIC_ENABLE_29_RISING	Interrupts enable UMC - GPTP - BOOTLOADER - MANUAL. The IO_LV_TIC_ENABLE_29_MISC1_REG0.TIC_ENABLE_29_RISING bits enable UMC - GPTP - BOOTLOADER - MANUAL interrupts by setting the bit (=1). Clearing the bit (=0) disables the interrupt. The values in the table are the bit position of each interrupt, not the value to perform the enable/disable operation. 3: GPTP_LOCK_RISING. 4: BOOTLOADER_DONE_RISING. 5: MANUAL_INTERRUPT_RISING.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 139. Bit Descriptions for IO_LV_TIC_ENABLE_29_MISC1_REG0 (Continued)

Bits	Bit Name	Description	Reset	Access
		6: EFUSE_CTRL_PRG_FALLING. 7: HS_COMM_ERROR.		

TIC ENABLE 29 MISCELLANEOUS 1 REGISTER 1

OA-SPI Address: 0xC98C, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_29_MISC1_REG1 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 140. Bit Descriptions for IO_LV_TIC_ENABLE_29_MISC1_REG1

Bits	Bit Name	Description	Reset	Access
[15:8]	TIC_ENABLE_29_LOW	Interrupts enable UMC - GPTP - BOOTLOADER - MANUAL. The IO_LV_TIC_ENABLE_29_MISC1_REG1.TIC_ENABLE_29_LOW bits enable UMC - GPTP - BOOTLOADER - MANUAL interrupts by setting the bit (=1). Clearing the bit (=0) disables the interrupt. The values in the table are the bit position of each interrupt, not the value to perform the enable/disable operation. 3: GPTP_LOCK_LOW. 4: BOOTLOADER_DONE_LOW. 5: MANUAL_INTERRUPT_LOW. 6: EFUSE_CTRL_PRG_LOW. 7: HS_COMM_ERROR.	0x0	R/W
[7:0]	TIC_ENABLE_29_HIGH	Interrupts enable UMC - GPTP - BOOTLOADER - MANUAL. The IO_LV_TIC_ENABLE_29_MISC1_REG1.TIC_ENABLE_29_HIGH bits enable UMC - GPTP - BOOTLOADER - MANUAL interrupts by setting the bit (=1). Clearing the bit (=0) disables the interrupt. The values in the table are the bit position of each interrupt, not the value to perform the enable/disable operation. 3: GPTP_LOCK_HIGH. 4: BOOTLOADER_DONE_HIGH. 5: MANUAL_INTERRUPT_HIGH. 6: EFUSE_CTRL_PRG_HIGH. 7: HS_COMM_ERROR.	0x0	R/W

TIC CLEAR 8 PHY REGISTER 0

OA-SPI Address: 0xC9A0, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_8_PHY_REG0 register is used to clear the interrupts that were configured in the corresponding enable register.

Table 141. Bit Descriptions for IO_LV_TIC_CLEAR_8_PHY_REG0

Bits	Bit Name	Description	Reset	Access
[15:0]	TIC_CLEAR_8[15:0]	Clear PHY Interrupts. The IO_LV_TIC_CLEAR_8_PHY_REG0.TIC_CLEAR_8 bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 2: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 10: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 18: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 26: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 3: PLCA Recovery Procedure Performed. 11: PLCA Recovery Procedure Performed. 19: PLCA Recovery Procedure Performed.	0x0	R0/W1S

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 141. Bit Descriptions for IO_LV_TIC_CLEAR_8_PHY_REG0 (Continued)

Bits	Bit Name	Description	Reset	Access
		27: PLCA Recovery Procedure Performed.		

TIC CLEAR 8 PHY REGISTER 1

OA-SPI Address: 0xC9A1, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_8_PHY_REG1 register is used to clear the interrupts that were configured in the corresponding enable register.

Table 142. Bit Descriptions for IO_LV_TIC_CLEAR_8_PHY_REG1

Bits	Bit Name	Description	Reset	Access
[15:0]	TIC_CLEAR_8[31:16]	Clear PHY Interrupts. The IO_LV_TIC_CLEAR_8_PHY_REG0.TIC_CLEAR_8 bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 2: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 10: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 18: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 26: PLCA Status Indicator, 0 if The PLCA Control Statemachine is in The DISABLE, RESYNC or RECOVER State For More Than Plca_status_timer. 3: PLCA Recovery Procedure Performed. 11: PLCA Recovery Procedure Performed. 19: PLCA Recovery Procedure Performed. 27: PLCA Recovery Procedure Performed.	0x0	R0/W1S

TIC CLEAR 9 MAC REGISTER 0

OA-SPI Address: 0xC9A2, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_9_MAC_REG0 register is used to clear the interrupts that were configured in the corresponding enable register.

Table 143. Bit Descriptions for IO_LV_TIC_CLEAR_9_MAC_REG0

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	TIC_CLEAR_9_FALLING	Interrupts clear MAC falling. The IO_LV_TIC_CLEAR_9_MAC_REG0.TIC_CLEAR_9_FALLING bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 0: MAC Receive Frame Dropped Due To The RX FIFO Being Full. 1: PHY Error Detected in MAC Receive Frame. 4: CRC Error Detected in MAC Receive Frame.	0x0	R0/W1S
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	TIC_CLEAR_9_RISING	Interrupts clear MAC Rising. The IO_LV_TIC_CLEAR_9_MAC_REG0.TIC_CLEAR_9_RISING bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 0: MAC Receive Frame Dropped Due To The RX FIFO Being Full. 1: PHY Error Detected in MAC Receive Frame. 4: CRC Error Detected in MAC Receive Frame.	0x0	R0/W1S

TIC CLEAR 9 MAC REGISTER 1

OA-SPI Address: 0xC9A3, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_9_MAC_REG1 register is used to clear the interrupts that were configured in the corresponding enable register.

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 144. Bit Descriptions for IO_LV_TIC_CLEAR_9_MAC_REG1

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	TIC_CLEAR_9_LOW	Interrupts clear MAC. The IO_LV_TIC_CLEAR_9_MAC_REG1.TIC_CLEAR_9_LOW bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 0: MAC Receive Frame Dropped Due To The RX FIFO Being Full. 1: PHY Error Detected in MAC Receive Frame. 4: CRC Error Detected in MAC Receive Frame.	0x0	R0/W1S
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	TIC_CLEAR_9_HIGH	Interrupts clear MAC. The IO_LV_TIC_CLEAR_9_MAC_REG1.TIC_CLEAR_9_HIGH bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 0: MAC Receive Frame Dropped Due To The RX FIFO Being Full. 1: PHY Error Detected in MAC Receive Frame. 4: CRC Error Detected in MAC Receive Frame.	0x0	R0/W1S

TIC CLEAR 10 PLCA REGISTER 0

OA-SPI Address: 0xC9A4, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_10_REG0 register is used to clear the interrupts that were configured in the corresponding enable register.

Table 145. Bit Descriptions for IO_LV_TIC_CLEAR_10_REG0

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
[10:8]	TIC_CLEAR_10_FALLING	Interrupts clear. The IO_LV_TIC_CLEAR_10_REG0.TIC_CLEAR_10_FALLING bits are used to clear interrupts. BB = Bus Busy. DNACK = Device Nack, that is the nack received when sending the device address. Self clearing bits. 0: PLCA_DIAG_FALLING.	0x0	R0/W1S
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	TIC_CLEAR_10_RISING	Interrupts clear. The IO_LV_TIC_CLEAR_10_REG0.TIC_CLEAR_10_RISING bits are used to clear interrupts. BB = Bus Busy. DNACK = Device Nack, that is the nack received when sending the device address. Self clearing bits. 0: PLCA_DIAG_RISING.	0x0	R0/W1S

TIC CLEAR 28 MISCELLANEOUS 0 REGISTER 0

OA-SPI Address: 0xC9C8, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_28_MISC0_REG0 register is used to clear the interrupts that were configured in the corresponding enable register.

Table 146. Bit Descriptions for IO_LV_TIC_CLEAR_28_MISC0_REG0

Bits	Bit Name	Description	Reset	Access
[15:0]	TIC_CLEAR_28[15:0]	Interrupt Clear SLEEP_WAKE and SERIAL_COMM. The IO_LV_TIC_CLEAR_28_MISC0_REG0.TIC_CLEAR_28 bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 0: SLPWK_FLAG_CONTROLLER_MODE_RISING. 1: SLPWK_FLAG_CONFIRM_AWAKE_RISING. 2: SLPWK_FLAG_LINE_BUSY_RISING. 3: SLPWK_FLAG_SLEEP_ERR_RISING. 4: SLPWK_FLAG_STANDBY_ERR_RISING. 5: SLPWK_FLAG_RETURNED_FROM_STANDBY_RISING. 6: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_RISING. 9: SLPWK_FLAG_CONFIRM_AWAKE_FALLING. 10: SLPWK_FLAG_LINE_BUSY_FALLING. 11: SLPWK_FLAG_SLEEP_ERR_FALLING.	0x0	R0/W1S

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 146. Bit Descriptions for IO_LV_TIC_CLEAR_28_MISC0_REG0 (Continued)

Bits	Bit Name	Description	Reset	Access
		12: SLPWK_FLAG_STANDBY_ERR_FALLING. 13: SLPWK_FLAG_RETURNED_FROM_STANDBY_FALLING. 14: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_FALLING. 16: SLPWK_FLAG_CONTROLLER_MODE_HIGH. 17: SLPWK_FLAG_CONFIRM_AWAKE_HIGH. 18: SLPWK_FLAG_LINE_BUSY_HIGH. 19: SLPWK_FLAG_SLEEP_ERR_HIGH. 20: SLPWK_FLAG_STANDBY_ERR_HIGH. 21: SLPWK_FLAG_RETURNED_FROM_STANDBY_HIGH. 22: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_HIGH. 24: SLPWK_FLAG_CONTROLLER_MODE_LOW. 25: SLPWK_FLAG_CONFIRM_AWAKE_LOW. 26: SLPWK_FLAG_LINE_BUSY_LOW. 27: SLPWK_FLAG_SLEEP_ERR_LOW. 28: SLPWK_FLAG_STANDBY_ERR_LOW. 29: SLPWK_FLAG_RETURNED_FROM_STANDBY_LOW. 30: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_LOW.		

TIC CLEAR 28 MISCELLANEOUS 0 REGISTER 1

OA-SPI Address: 0xC9C9, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_28_MISC0_REG1 register is used to clear the interrupts that were configured in the corresponding enable register.

Table 147. Bit Descriptions for IO_LV_TIC_CLEAR_28_MISC0_REG1

Bits	Bit Name	Description	Reset	Access
[15:0]	TIC_CLEAR_28[31:16]	Interrupt Clear SLEEP_WAKE and SERIAL_COMM. The IO_LV_TIC_CLEAR_28_MISC0_REG0.TIC_CLEAR_28 bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 0: SLPWK_FLAG_CONTROLLER_MODE_RISING. 1: SLPWK_FLAG_CONFIRM_AWAKE_RISING. 2: SLPWK_FLAG_LINE_BUSY_RISING. 3: SLPWK_FLAG_SLEEP_ERR_RISING. 4: SLPWK_FLAG_STANDBY_ERR_RISING. 5: SLPWK_FLAG_RETURNED_FROM_STANDBY_RISING. 6: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_RISING. 9: SLPWK_FLAG_CONFIRM_AWAKE_FALLING. 10: SLPWK_FLAG_LINE_BUSY_FALLING. 11: SLPWK_FLAG_SLEEP_ERR_FALLING. 12: SLPWK_FLAG_STANDBY_ERR_FALLING. 13: SLPWK_FLAG_RETURNED_FROM_STANDBY_FALLING. 14: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_FALLING. 16: SLPWK_FLAG_CONTROLLER_MODE_HIGH. 17: SLPWK_FLAG_CONFIRM_AWAKE_HIGH. 18: SLPWK_FLAG_LINE_BUSY_HIGH. 19: SLPWK_FLAG_SLEEP_ERR_HIGH. 20: SLPWK_FLAG_STANDBY_ERR_HIGH. 21: SLPWK_FLAG_RETURNED_FROM_STANDBY_HIGH. 22: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_HIGH. 24: SLPWK_FLAG_CONTROLLER_MODE_LOW. 25: SLPWK_FLAG_CONFIRM_AWAKE_LOW.	0x0	R0/W1S

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 147. Bit Descriptions for IO_LV_TIC_CLEAR_28_MISC0_REG1 (Continued)

Bits	Bit Name	Description	Reset	Access
		26: SLPWK_FLAG_LINE_BUSY_LOW. 27: SLPWK_FLAG_SLEEP_ERR_LOW. 28: SLPWK_FLAG_STANDBY_ERR_LOW. 29: SLPWK_FLAG_RETURNED_FROM_STANDBY_LOW. 30: SLPWK_FLAG_REQ_SYSTEM_WAKEUP_CONF_LOW.		

TIC CLEAR 29 MISCELLANEOUS 1 REGISTER 0

OA-SPI Address: 0xC9CA, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_29_MISC1_REG0 register is used to clear the interrupts that were configured in the corresponding enable register.

Table 148. Bit Descriptions for IO_LV_TIC_CLEAR_29_MISC1_REG0

Bits	Bit Name	Description	Reset	Access
[15:8]	TIC_CLEAR_29_FALLING	Interrupts Clear UMC - GPTP - BOOTLOADER - MANUAL. The IO_LV_TIC_CLEAR_29_MISC1_REG0.TIC_CLEAR_29_FALLING bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 3: GPTP_LOCK_FALLING. 4: BOOTLOADER_DONE_FALLING. 5: MANUAL_INTERRUPT_FALLING. 6: EFUSE_CTRL_PROG_INT_FALLING. 7: HS_COMM_ERROR_FALLING.	0x0	R0/W1S
[7:0]	TIC_CLEAR_29_RISING	Interrupts Clear UMC - GPTP - BOOTLOADER - MANUAL. The IO_LV_TIC_CLEAR_29_MISC1_REG0.TIC_CLEAR_29_RISING bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 3: GPTP_LOCK_RISING. 4: BOOTLOADER_DONE_RISING. 5: MANUAL_INTERRUPT_RISING. 6: EFUSE_CTRL_PROG_INT_RISING. 7: HS_COMM_ERROR_RISING.	0x0	R0/W1S

TIC CLEAR 29 MISCELLANEOUS 1 REGISTER 1

OA-SPI Address: 0xC9CB, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_29_MISC1_REG1 register is used to clear the interrupts that were configured in the corresponding enable register.

Table 149. Bit Descriptions for IO_LV_TIC_CLEAR_29_MISC1_REG1

Bits	Bit Name	Description	Reset	Access
[15:8]	TIC_CLEAR_29_LOW	Interrupts Clear UMC - GPTP - BOOTLOADER - MANUAL. The IO_LV_TIC_CLEAR_29_MISC1_REG1.TIC_CLEAR_29_LOW bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 3: GPTP_LOCK_LOW. 4: BOOTLOADER_DONE_LOW. 5: MANUAL_INTERRUPT_LOW. 6: EFUSE_CTRL_PROG_INT_LOW. 7: HS_COMM_ERROR_LOW.	0x0	R0/W1S
[7:0]	TIC_CLEAR_29_HIGH	Interrupts Clear UMC - GPTP - BOOTLOADER - MANUAL. The IO_LV_TIC_CLEAR_29_MISC1_REG1.TIC_CLEAR_29_HIGH bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 3: GPTP_LOCK_HIGH. 4: BOOTLOADER_DONE_HIGH. 5: MANUAL_INTERRUPT_HIGH. 6: EFUSE_CTRL_PROG_INT_HIGH.	0x0	R0/W1S

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 149. Bit Descriptions for IO_LV_TIC_CLEAR_29_MISC1_REG1 (Continued)

Bits	Bit Name	Description	Reset	Access
		7: HS_COMM_ERROR_HIGH.		

CLOCK GENERATION OUTPUTS REGISTER

OA-SPI Address: 0xC9CE, MMS: 0xA, Reset: 0x3C57

The IO_LV_CLOCK_GENERATION_OUTPUTS register is used to configure the XTAL oscillator amplifier.

Table 150. Bit Descriptions for IO_LV_CLOCK_GENERATION_OUTPUTS

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x7	R/W
10	TA_XTAL_GM_EN_VDD	XTAL oscillator amplifier enable. The IO_LV_CLOCK_GENERATION_OUTPUTS.TA_XTAL_GM_EN_VDD bit is used to power down the XTAL oscillator amplifier if an external single-ended clock is being applied, instead of being connected to a crystal reference. 0: Disabled. 1: Enabled.	0x1	R/W
[9:0]	RESERVED	Reserved.	0x57	R/W

CLOCK GENERATION OUTPUTS2 REGISTER

OA-SPI Address: 0xC9CF, MMS: 0xA, Reset: 0x0412

The IO_LV_CLOCK_GENERATION_OUTPUTS2 register is used to enable and report the status of the XTAL oscillator.

Table 151. Bit Descriptions for IO_LV_CLOCK_GENERATION_OUTPUTS2

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	TA_XTAL_EN_VDD	XTAL oscillator enable. The IO_LV_CLOCK_GENERATION_OUTPUTS2.TA_XTAL_EN_VDD bit is used to enable the XTAL oscillator. 0: Disabled. 1: Enabled.	0x1	R/W
[9:0]	RESERVED	Reserved.	0x12	R/W

TP OUTPUT SAIF PIN DRIVER ENABLE REGISTER

OA-SPI Address: 0xC9DF, MMS: 0xA, Reset: 0x0000

The IO_LV_TP_OUT_EN_SA_IF register is used to enable the SAIF pins output drivers.

Table 152. Bit Descriptions for IO_LV_TP_OUT_EN_SA_IF

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	TP_OUT_EN_SA_IF_11	SAIF11 output driver enable. The IO_LV_TP_OUT_EN_SA_IF.TP_OUT_EN_SA_IF_11 bit is used to enable the output driver on the SAIF11 pin. 0: Disabled. 1: Enabled.	0x0	R/W
10	TP_OUT_EN_SA_IF_10	SAIF10 output driver enable. The IO_LV_TP_OUT_EN_SA_IF.TP_OUT_EN_SA_IF_10 bit is used to enable the output driver on the SAIF10 pin. 0: Disabled. 1: Enabled.	0x0	R/W
9	TP_OUT_EN_SA_IF_9	SAIF9 output driver enable. The IO_LV_TP_OUT_EN_SA_IF.TP_OUT_EN_SA_IF_9 bit is used to enable the output driver on the SAIF9 pin. 0: Disabled. 1: Enabled.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 152. Bit Descriptions for IO_LV_TP_OUT_EN_SA_IF (Continued)

Bits	Bit Name	Description	Reset	Access
[8:1]	RESERVED	Reserved.	0x0	R/W
0	TP_OUT_EN_SA_IF_0	SAIF0 output driver enable. The IO_LV_TP_OUT_EN_SA_IF.TP_OUT_EN_SA_IF_0 bit is used to enable the output driver on the SAIF0 pin. 0: Disabled. 1: Enabled.	0x0	R/W

TP INPUT RECEIVER SAIF PIN ENABLE REGISTER

OA-SPI Address: 0xC9E0, MMS: 0xA, Reset: 0x0000

The IO_LV_TP_IP_EN_SA_IF register is used to configure the SAIF pin receive inputs.

Table 153. Bit Descriptions for IO_LV_TP_IP_EN_SA_IF

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	TP_IP_EN_SA_IF_11	SAIF11 input receive enable. The IO_LV_TP_IP_EN_SA_IF.TP_IP_EN_SA_IF_11 bit is used to enable the input receiver on the SAIF11 pin. 0: Disabled. 1: Enabled.	0x0	R/W
10	TP_IP_EN_SA_IF_10	SAIF10 input receive enable. The IO_LV_TP_IP_EN_SA_IF.TP_IP_EN_SA_IF_10 bit is used to enable the input receiver on the SAIF10 pin. 0: Disabled. 1: Enabled.	0x0	R/W
9	TP_IP_EN_SA_IF_9	SAIF9 input receive enable. The IO_LV_TP_IP_EN_SA_IF.TP_IP_EN_SA_IF_9 bit is used to enable the input receiver on the SAIF9 pin. 0: Disabled. 1: Enabled.	0x0	R/W
[8:1]	RESERVED	Reserved.	0x0	R/W
0	TP_IP_EN_SA_IF_0	SAIF0 input receive enable. The IO_LV_TP_IP_EN_SA_IF.TP_IP_EN_SA_IF_0 bit is used to enable the input receiver on the SAIF0 pin. 0: Disabled. 1: Enabled.	0x0	R/W

EFUSE REGISTER

OA-SPI Address: 0xC9E2, MMS: 0xA, Reset: 0x0000

Provides majority voting logic pass readback.

Table 154. Bit Descriptions for IO_LV_EFUSE_REG

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	EFUSE_MVL_PASS	Efuse majority voting logic pass readback. 0: Fail. 1: Pass.	0x0	R

GPTP DOMAINS REGISTER

OA-SPI Address: 0xC9EF, MMS: 0xA, Reset: 0x0100

The IO_LV_GPTP_DOMAINS register is used to configure the gPTP active domain which is used to implement grandmaster redundancy. The core always tries to lock to the main grandmaster domain, if available. After the first sync timeout, it tries to lock to a secondary backup domain and continues using the secondary domain until the main domain is available.

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 155. Bit Descriptions for IO_LV_GPTP_DOMAINS

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x1	R/W
[7:0]	GPTP_ACTIVE_DOMAIN	gPTP Active Domain. The IO_LV_GPTP_DOMAINS.GPTP_ACTIVE_DOMAIN bits set the active domain of the gPTP algorithm.	0x0	R/W

TIC ENABLE 34 GPIO 1 REGISTER 0

OA-SPI Address: 0xC9F6, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_34_GPIO1_REG0 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 156. Bit Descriptions for IO_LV_TIC_ENABLE_34_GPIO1_REG0

Bits	Bit Name	Description	Reset	Access
[15:8]	TIC_ENABLE_34_FALLING	Interrupts Enable SSC falling. The IO_LV_TIC_ENABLE_34_GPIO1_REG0.TIC_ENABLE_34_FALLING bits enable SSC interrupts by setting the bit (=1). 1: SAIF9_FALLING. 2: SAIF10_FALLING. 3: SAIF11_FALLING. 4: Safe State Controller has Changed its Mode. From Functional to Safe or from safe to Functional. 5: Tried to get out of safe mode, but there were safe triggers activated. 6: SQI_REACHES_WARNING_FALLING. 7: SQI_REACHES_BAD_FALLING.	0x0	R/W
[7:0]	TIC_ENABLE_34_RISING	Interrupts Enable SSC rising. The IO_LV_TIC_ENABLE_34_GPIO1_REG0.TIC_ENABLE_34_RISING bits enable SSC interrupts by setting the bit (=1). 1: SAIF9_RISING. 2: SAIF10_RISING. 3: SAIF11_RISING. 4: Safe State Controller has Changed its Mode. From Functional to Safe or from safe to Functional. 5: Tried to get out of safe mode, but there were safe triggers activated. 6: SQI_REACHES_WARNING_RISING. 7: SQI_REACHES_BAD_RISING.	0x0	R/W

TIC ENABLE 34 GPIO 1 REGISTER 1

OA-SPI Address: 0xC9F7, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_ENABLE_34_GPIO1_REG1 register is used to enable interrupts. These interrupts are cleared in the corresponding clear register.

Table 157. Bit Descriptions for IO_LV_TIC_ENABLE_34_GPIO1_REG1

Bits	Bit Name	Description	Reset	Access
[15:8]	TIC_ENABLE_34_LOW	Interrupts Enable SSC. The IO_LV_TIC_ENABLE_34_GPIO1_REG1.TIC_ENABLE_34_LOW bits enable SSC interrupts by setting the bit (=1). The values in the table are the bit position of each interrupt, not the value to perform the clear/enable operation. 1: SAIF9_LOW. 2: SAIF10_LOW. 3: SAIF11_LOW. 4: Safe State Controller has Changed its Mode. From Functional to Safe or from safe to Functional. 5: Tried to get out of safe mode, but there were safe triggers activated.	0x0	R/W

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 157. Bit Descriptions for IO_LV_TIC_ENABLE_34_GPIO1_REG1 (Continued)

Bits	Bit Name	Description	Reset	Access
		6: SQI_REACHES_WARNING_LOW. 7: SQI_REACHES_BAD_LOW.		
[7:0]	TIC_ENABLE_34_HIGH	Interrupts Enable SSC. The IO_LV_TIC_ENABLE_34_GPIO1_REG1.TIC_ENABLE_34_HIGH bits enable SSC interrupts by setting the bit (=1). The values in the table are the bit position of each interrupt, not the value to perform the clear/enable operation. 1: SAIF9_HIGH. 2: SAIF10_HIGH. 3: SAIF11_HIGH. 4: Safe State Controller has Changed its Mode. From Functional to Safe or from safe to Functional. 5: Tried to get out of safe mode, but there were safe triggers activated. 6: SQI_REACHES_WARNING_HIGH. 7: SQI_REACHES_BAD_HIGH.	0x0	R/W

TIC CLEAR 34 GPIO0 REGISTER 0

OA-SPI Address: 0xC9FA, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_34_GPIO1_REG0 register is used to clear the interrupts that were configured in the corresponding enable register.

Table 158. Bit Descriptions for IO_LV_TIC_CLEAR_34_GPIO1_REG0

Bits	Bit Name	Description	Reset	Access
[15:8]	TIC_CLEAR_34_FALLING	Interrupts Clear SSC. The IO_LV_TIC_CLEAR_34_GPIO1_REG0.TIC_CLEAR_34_FALLING bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 1: SAIF9_FALLING. 2: SAIF10_FALLING. 3: SAIF11_FALLING. 4: Safe State Controller has Changed its Mode. From Functional to Safe or from safe to Functional. 5: Tried to get out of safe mode, but there were safe triggers activated. 6: SQI_REACHES_WARNING_FALLING. 7: SQI_REACHES_BAD_FALLING.	0x0	R0/W1S
[7:0]	TIC_CLEAR_34_RISING	Interrupts Clear SSC. The IO_LV_TIC_CLEAR_34_GPIO1_REG0.TIC_CLEAR_34_RISING bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 1: SAIF9_RISING. 2: SAIF10_RISING. 3: SAIF11_RISING. 4: Safe State Controller has Changed its Mode. From Functional to Safe or from safe to Functional. 5: Tried to get out of safe mode, but there were safe triggers activated. 6: SQI_REACHES_WARNING_RISING. 7: SQI_REACHES_BAD_RISING.	0x0	R0/W1S

TIC CLEAR 34 GPIO0 REGISTER 1

OA-SPI Address: 0xC9FB, MMS: 0xA, Reset: 0x0000

The IO_LV_TIC_CLEAR_34_GPIO1_REG1 register is used to clear the interrupts that were configured in the corresponding enable register.

REGISTER DETAILS: LOW VOLTAGE IO REGISTER MAP (IO_LV)

Table 159. Bit Descriptions for IO_LV_TIC_CLEAR_34_GPIO1_REG1

Bits	Bit Name	Description	Reset	Access
[15:8]	TIC_CLEAR_34_LOW	Interrupts Clear SSC. The IO_LV_TIC_CLEAR_34_GPIO1_REG1.TIC_CLEAR_34_LOW bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 1: SAIF9_LOW. 2: SAIF10_LOW. 3: SAIF11_LOW. 4: Safe State Controller has Changed its Mode. From Functional to Safe or from safe to Functional. 5: Tried to get out of safe mode, but there were safe triggers activated. 6: SQI_REACHES_WARNING_LOW. 7: SQI_REACHES_BAD_LOW.	0x0	R0/W1S
[7:0]	TIC_CLEAR_34_HIGH	Interrupts Clear SSC. The IO_LV_TIC_CLEAR_34_GPIO1_REG1.TIC_CLEAR_34_HIGH bits clear the interrupts by setting (=1) the bit. These bits are self clearing. 1: SAIF9_HIGH. 2: SAIF10_HIGH. 3: SAIF11_HIGH. 4: Safe State Controller has Changed its Mode. From Functional to Safe or from safe to Functional. 5: Tried to get out of safe mode, but there were safe triggers activated. 6: SQI_REACHES_WARNING_HIGH. 7: SQI_REACHES_BAD_HIGH.	0x0	R0/W1S

REGISTER SUMMARY: HIGH VOLTAGE IO REGISTER MAP (IO_HV)

Note that all the HV Die Registers (IO_HV) need to be read back twice to get the correct value.

Table 160. IO_HV Register Summary

Address	Name	Description	Reset	Access
0xB105	IO_HV_REVISION_CONTROL	Revision Control Register.	0x0000	R
0xB106	IO_HV_BOOTLOADER_STATUS_0	Bootloader Status 0 Register.	0x0000	R
0xB108	IO_HV_STANDBY_STATUS	Standby Status Register.	0x0000	R
0xB10A	IO_HV_BOOTLOADER_STATUS_1	Bootloader Status 1 Register.	0x0000	R
0xB1FE	IO_HV_BLOCK_RESET_CONTROL	Block Reset Control Register.	0x0000	R/W
0xB1FF	IO_HV_RESET_CONTROL	Reset Control Register.	0x0000	R/W
0xB200	IO_HV_HIGH_SPEED_SERIAL_COMM	High Speed Serial Communications Register.	0x0000	R/W
0xB20F	IO_HV_OTP_CONFIG_0	OTP Memory Configuration Register 0.	0x0000	R/W
0xB210	IO_HV_OTP_CONFIG_1	OTP Memory Configuration Register 1.	0x0000	R/W
0xB21C	IO_HV_CONFIG_EN_PADS_CONFIG	Pads Configuration Enable Register.	0x01A8	R/W

REGISTER DETAILS: HIGH VOLTAGE IO REGISTER MAP (IO_HV)

Note that all the HV Die Registers (IO_HV) need to be read back twice to get the correct value.

REVISION CONTROL REGISTER

OA-SPI Address: 0xB105, MMS: 0xA, Reset: 0x0000

The IO_HV_REVISION_CONTROL register provides die revision information.

Table 161. Bit Descriptions for IO_HV_REVISION_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:4]	REV_CODE_DIG	Digital revision code. The IO_HV_REVISION_CONTROL.REV_CODE_DIG bits provide the chip digital revision code.	0x0	R
[3:0]	REV_CODE	Chip revision code. The IO_HV_REVISION_CONTROL.REV_CODE bits provide the chip revision code. 000: HV 0.1 (U1) and 0.2 (U2). 011: HV 0.3 (U3). 100: HV 0.4 (U4), 0.5 (U5) and 1.0.	0x0	R

BOOTLOADER STATUS 0 REGISTER

OA-SPI Address: 0xB106, MMS: 0xA, Reset: 0x0000

The IO_HV_BOOTLOADER_STATUS_0 register provides bootloader block status information.

Table 162. Bit Descriptions for IO_HV_BOOTLOADER_STATUS_0

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	BLOCK_STATUS_0	Bootloader block0 and 1 status. The IO_HV_BOOTLOADER_STATUS_0.BLOCK_STATUS_0 bit field provides the block 0 and block 1 bootloader status of the bootloader starting from the LSBs. 00: Not initialized. 01: Correct. 10: ECC fixed. 11: Error.	0x0	R

STANDBY STATUS REGISTER

OA-SPI Address: 0xB108, MMS: 0xA, Reset: 0x0000

The IO_HV_STANDBY_STATUS register is used to report wake status for the die.

Table 163. Bit Descriptions for IO_HV_STANDBY_STATUS

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	WUD	Wake-up detect. The IO_HV_STANDBY_STATUS.WUD bit indicates the current live output of the Wake-up Detect block.	0x0	R
2	WAKE_PIN	Wake pin value. The IO_HV_STANDBY_STATUS.WAKE_PIN bit indicates the current (live) value of the WAKE pin (polarity corrected to active high).	0x0	R
1	DETECTED_WUD	The IO_HV_STANDBY_STATUS.DETECTED_WUD bit indicates a previous detection of the WUD begin active (for example received during standby). 0: Not triggered. 1: Triggered.	0x0	R
0	DETECTED_WAKE_PIN	Wake detected. The IO_HV_STANDBY_STATUS.DETECTED_WAKE_PIN bit indicates a previous detection of the WAKE pin begin active (for example received during standby). 0: Not triggered. 1: Triggered.	0x0	R

BOOTLOADER STATUS 1 REGISTER

OA-SPI Address: 0xB10A, MMS: 0xA, Reset: 0x0000

REGISTER DETAILS: HIGH VOLTAGE IO REGISTER MAP (IO_HV)

The IO_HV_BOOTLOADER_STATUS_1 register provides bootloader status information.

Table 164. Bit Descriptions for IO_HV_BOOTLOADER_STATUS_1

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	BOOTLOAD_TIMEOUT	Bootloader timeout. The IO_HV_BOOTLOADER_STATUS_1.BOOTLOAD_TIMEOUT bit indicates that the bootloader did not finish in 500ms. In this case the Bootloader operation is aborted. 0: Not triggered. 1: Triggered.	0x0	R
0	BOOTLOAD_DONE	Bootloader done. The IO_HV_BOOTLOADER_STATUS_1.BOOTLOAD_DONE bit indicates if the bootloader is done. 0: Bootload not finished. 1: Bootload finished.	0x0	R

BLOCK RESET CONTROL REGISTER

OA-SPI Address: 0xB1FE, MMS: 0xA, Reset: 0x0000

The IO_HV_BLOCK_RESET_CONTROL register is used to configure block reset as described below.

Table 165. Bit Descriptions for IO_HV_BLOCK_RESET_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	CLR_STANDBY_STATUS	Clear standby status. The IO_HV_BLOCK_RESET_CONTROL.CLR_STANDBY_STATUS bit clears the readback of a previous detection of active WUD or WAKE pins (for example received during standby). 0: Inactive. 1: Trigger.	0x0	R/W
1	BOOT_LOADER_SOFT_RESET	Bootloader reset. The IO_HV_BLOCK_RESET_CONTROL.BOOT_LOADER_SOFT_RESET bit resets the bootloader. This is a self-clearing bit. 0: Inactive. 1: Trigger.	0x0	R0/W1S
0	OTP_SOFT_RESET	OTP reset. The IO_HV_BLOCK_RESET_CONTROL.OTP_SOFT_RESET bit resets the OTP controller. This is a self-clearing bit. 0: Inactive. 1: Trigger.	0x0	R0/W1S

RESET CONTROL REGISTER

OA-SPI Address: 0xB1FF, MMS: 0xA, Reset: 0x0000

The IO_HV_RESET_CONTROL register is the primary soft reset register.

Table 166. Bit Descriptions for IO_HV_RESET_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:0]	RESET	HV die reset. The IO_HV_RESET_CONTROL.RESET bits provide the primary soft reset signature. Software must write a value of 0xA55A to this field to cause a soft reset on the HV die. The oscillator clock, communication clock and functional clock domains are reset.	0x0	R/W

HIGH SPEED SERIAL COMMUNICATIONS REGISTER

OA-SPI Address: 0xB200, MMS: 0xA, Reset: 0x0000

The IO_HV_HIGH_SPEED_SERIAL_COMM register is used to clear error bits.

REGISTER DETAILS: HIGH VOLTAGE IO REGISTER MAP (IO_HV)

Table 167. Bit Descriptions for IO_HV_HIGH_SPEED_SERIAL_COMM

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	HS_COMM_BIT_STOP_ERR_CLEAN	Clear bit stop error. The IO_HV_HIGH_SPEED_SERIAL_COMM.HS_COMM_BIT_STOP_ERR_CLEAN bit, when set, clears the bit stop error from the inter-die interface.	0x0	R0/W1S
0	HS_COMM_PARITY_ERR_CLEAN	Clear parity error. The IO_HV_HIGH_SPEED_SERIAL_COMM.HS_COMM_PARITY_ERR_CLEAN bit, when set, clears the parity error from the inter-die interface.	0x0	R0/W1S

OTP MEMORY CONFIGURATION REGISTER 0

OA-SPI Address: 0xB20F, MMS: 0xA, Reset: 0x0000

The IO_HV_OTP_CONFIG_0 register is used to configure the OTP read type.

Table 168. Bit Descriptions for IO_HV_OTP_CONFIG_0

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	OTP_READ_TYPE_DIFF_RED	OTP read type. The IO_HV_OTP_CONFIG_0.OTP_READ_TYPE_DIFF_RED bit is used to configure the OTP read type. 0: Single ended. 1: Differential redundant.	0x0	R/W

OTP MEMORY CONFIGURATION REGISTER 1

OA-SPI Address: 0xB210, MMS: 0xA, Reset: 0x0000

The IO_HV_OTP_CONFIG_1 register is used to configure the OTP mux type.

Table 169. Bit Descriptions for IO_HV_OTP_CONFIG_1

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	OTP_ACCESS_MUX_CTRL	OTP access mux control. The IO_HV_OTP_CONFIG_1.OTP_ACCESS_MUX_CTRL bit is used to enable the type of access to the OTP. 0: Bootloader access. 1: OTP controller/programmer.	0x0	R/W

PADS CONFIGURATION ENABLE REGISTER

OA-SPI Address: 0xB21C, MMS: 0xA, Reset: 0x01A8

The IO_HV_CONFIG_EN_PADS_CONFIG register is used to enable the EN pads.

Table 170. Bit Descriptions for IO_HV_CONFIG_EN_PADS_CONFIG

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x35	R
2	TP_OUT_ENB_EN	Output driver disable. The IO_HV_CONFIG_EN_PADS_CONFIG.TP_OUT_ENB_EN bit is used to disable the output driver on the EN pad. 0: Enabled. 1: Disabled.	0x0	R/W
1	TP_IP_EN_EN	Input receive enable. The IO_HV_CONFIG_EN_PADS_CONFIG.TP_IP_EN_EN bit is used to enable the input receiver on the EN pad. 0: Disabled. 1: Enabled.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 171. MAC Register Summary

Address	Name	Description	Reset	Access
0x0000	MAC_IDVER	MACPHY Identification Version Register.	0x00000011	R
0x0001	MAC_PHYID	PHY Identification Register.	0x0283BE00	R
0x0002	MAC_CAPABILITY	Supported Capabilities Status Register.	0x000006C3	R
0x0003	MAC_RESET	MAC Reset Control and Status Register.	0x00000000	W
0x0004	MAC_CONFIG0	MAC Configuration Register 0.	0x00000026	R/W
0x0006	MAC_CONFIG2	MAC Configuration Register 2.	0x007C2020	R/W
0x0008	MAC_STATUS0	MAC Status Register 0.	0x00000040	R/W
0x0009	MAC_STATUS1	MAC Status Register 1.	0x00000000	R/W
0x000B	MAC_BUFSTS	Buffer Status Register.	0x00007700	R
0x000C	MAC_IMASK0	Interrupt Mask Register 0.	0x00001FBF	R/W
0x000D	MAC_IMASK1	Mask Bits for Driving the Interrupt Pin Register.	0x40001F5A	R/W
0x0010	MAC_TTSCAH	Transmit Timestamp Capture Register A (High).	0x00000000	R
0x0011	MAC_TTSCAL	Transmit Timestamp Capture Register A (Low).	0x00000000	R
0x0012	MAC_TTSCBH	Transmit Timestamp Capture Register B (High).	0x00000000	R
0x0013	MAC_TTSCBL	Transmit Timestamp Capture Register B (Low).	0x00000000	R
0x0014	MAC_TTSCCH	Transmit Timestamp Capture Register C (High).	0x00000000	R
0x0015	MAC_TTSCCL	Transmit Timestamp Capture Register C (Low).	0x00000000	R
0x0032	MAC_TX_SPACE	Tx FIFO Space Register.	0x00000FFF	R
0x0033	MAC_RX_THRESH	MAC Receive Threshold Register.	0x00000004	R/W
0x0034	MAC_TX_THRESH	Transmit Threshold Register.	0x00000001	R/W
0x0035	MAC_TX_PRI	Transmit Priority Register.	0x00000000	R/W
0x0036	MAC_FIFO_CLR	MAC FIFO Clear Register.	0x00000000	W
0x0037 to 0x003A by 1	MAC_SCRATCHn	MAC Scratch Register.	0x00000000	R/W
0x003D	MAC_SPI_INJ_ERR	MAC Inject Error on SDI from DUT Register.	0x00000000	R/W
0x003E	MAC_FIFO_SIZE	FIFO Sizes Register.	0x01102022	R/W
0x003F	MAC_TFC	Tx FIFO Frame Count Register.	0x00000000	R
0x0040	MAC_TXSIZE	Tx FIFO Valid Half Words Register.	0x00000000	R
0x0041	MAC_HTX_OVF_FRM_CNT	Host Transmit Frames Dropped Due to FIFO Overflow Register.	0x00000000	R
0x0042	MAC_MECC_ERR_ADDR	ECC Error Memory Address Register.	0x00000000	R
0x0043 to 0x0049 by 1	MAC_CECC_ERRn	Corrected ECC Error Counters Register.	0x00000000	R
0x004C	MAC_FIFO_ALMOST_EMPTY	Almost Empty Assertion Threshold Value Register.	0x00000004	R/W
0x0050 to 0x006E by 2	MAC_ADDR_FILT_UPRn	MAC Address Rule and DA Filter Upper 16 Bits Register.	0x00000000	R/W
0x0051 to 0x006F by 2	MAC_ADDR_FILT_LWRn	MAC Address DA Filter (Lower 32 Bits) Register.	0x00000000	R/W
0x0070 to 0x0072 by 2	MAC_ADDR_MSK_UPRn	MAC Address (Upper 32 Bits) Mask Register.	0x0000FFFF	R/W
0x0071 to 0x0073 by 2	MAC_ADDR_MSK_LWRn	MAC Address (Lower 32 Bits) Mask Register.	0xFFFFFFFF	R/W
0x0080	MAC_TS_ADDEND	Timestamp Accumulator Addend Register.	0xA0000000	R/W
0x0081	MAC_TS_1SEC_CMP	Timer Update Compare Register.	0x3B9ACA00	R/W
0x0082	MAC_TS_SEC_CNT	Seconds Counter Register.	0x00000000	R/W
0x0083	MAC_TS_NS_CNT	Nanoseconds Counter Register.	0x00000000	R/W
0x0084	MAC_TS_CFG	Timer Configuration Register.	0x00000001	R/W
0x0085	MAC_TS_TIMER_HI	High Period for TS_TIMER Register.	0x00000000	R/W
0x0086	MAC_TS_TIMER_LO	Low Period for TS_TIMER Register.	0x00000000	R/W
0x0087	MAC_TS_TIMER_QE_CORR	Quantization Error Correction Register.	0x00000000	R/W
0x0088	MAC_TS_TIMER_START	TS_TIMER Counter Start Time Lower Register.	0x00000000	R/W
0x0089	MAC_TS_EXT_CAPT0	TS_CAPT Nanoseconds Timestamp Register.	0x00000000	R

REGISTER SUMMARY: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 171. MAC Register Summary (Continued)

Address	Name	Description	Reset	Access
0x008A	MAC_TS_EXT_CAPT1	TS_CAPT Seconds Timestamp Register.	0x00000000	R
0x008B	MAC_TS_FREECNT_CAPT	TS_CAPT Free Running Counter Register Lower Register.	0x00000000	R
0x008D	MAC_PLCA_PRIORITY	PLCA Transmit Throttle Register.	0x00080000	R/W
0x0090	MAC_RX_FSIZE	MAC Receive Frame Size Register.	0x00000000	R
0x00A1	MAC_RX_FRM_CNT	MAC Receive Frame Count Register.	0x00000000	R
0x00A2	MAC_RX_BCAST_CNT	MAC Receive Broadcast Frame Count Register.	0x00000000	R
0x00A3	MAC_RX_MCAST_CNT	MAC Receive Multicast Frame Count Register.	0x00000000	R
0x00A4	MAC_RX_UCAST_CNT	MAC Receive Unicast Frame Count Register.	0x00000000	R
0x00A5	MAC_RX_CRC_ERR_CNT	MAC Receive CRC Error Frame Count Register.	0x00000000	R
0x00A6	MAC_RX_ALGN_ERR_CNT	MAC Receive Align Error Count Register.	0x00000000	R
0x00A7	MAC_RX_PREAMBLE_ERR_CNT	MAC Receive Preamble Error Count Register.	0x00000000	R
0x00A8	MAC_RX_SHORT_ERR_CNT	MAC Receive Short Frame Error Count Register.	0x00000000	R
0x00A9	MAC_RX_LONG_ERR_CNT	MAC Receive Long Frame Error Count Register.	0x00000000	R
0x00AA	MAC_RX_PHY_ERR_CNT	MAC Receive PHY Error Count Register.	0x00000000	R
0x00AB	MAC_RX_DROP_HOST_FULL_CNT	MAC Receive Frames Dropped HOST FIFO Full Register.	0x00000000	R
0x00AD	MAC_RX_DROP_FILT_CNT	MAC Receive Frames Dropped Filtering Register.	0x00000000	R
0x00AE	MAC_RX_IFG_ERR_CNT	MAC Frame Received with IFG Errors Register.	0x00000000	R
0x00B1	MAC_TX_FRM_CNT	MAC Transmit Frame Count Register.	0x00000000	R
0x00B2	MAC_TX_BCAST_CNT	MAC Transmit Broadcast Frame Count Register.	0x00000000	R
0x00B3	MAC_TX_MCAST_CNT	MAC Transmit Multicast Frame Count Register.	0x00000000	R
0x00B4	MAC_TX_UCAST_CNT	MAC Transmit Unicast Frame Count Register.	0x00000000	R
0x00B5	MAC_TX_SINGLE_COL_CNT	MAC Transmit Single Collision Count Register.	0x00000000	R
0x00B6	MAC_TX_MULTIPLE_COL_CNT	MAC Transmit Multiple Collision Count Register.	0x00000000	R
0x00B7	MAC_TX_DEFERRED_XMIT_CNT	MAC Transmit Deferred Transmission Count Register.	0x00000000	R
0x00B8	MAC_TX_LATE_COL_CNT	MAC Transmit Late Collision Count Register.	0x00000000	R
0x00B9	MAC_TX_XSCOLS_CNT	MAC Transmit Excess Collision Count Register.	0x00000000	R
0x00BA	MAC_TX_UNR_CNT	MAC Transmit Frames Dropped Under Run Register.	0x00000000	R
0x00BB	MAC_HI_RFC	MAC Receive FIFO Frame Count Register.	0x00000000	R
0x00BD	MAC_HI_RXSIZE	MAC Receive FIFO Valid Half Words Register.	0x00000000	R
0x00C1	MAC_TX_IFG	MAC Transmit Inter Frame Gap Register.	0x0000000B	R/W
0x00C2	MAC_DUPLEX	MAC Duplex Mode Register.	0x00000010	R/W
0x00C3	MAC_MAX_RETRY	Max Retry in Half Duplex Register.	0x0000000F	R/W
0x00C4	MAC_LOOP	MAC Loopback Enable Register.	0x00000000	R/W
0x00C5	MAC_RX_CRC_EN	MAC CRC Check Enable on Receive Register.	0x00000001	R/W
0x00C6	MAC_RX_IFG	MAC Receive Inter Frame Gap Register.	0x0000000A	R/W
0x00C7	MAC_RX_MAX_LEN	MAC Max Receive Frame Length Register.	0x00000618	R/W
0x00C8	MAC_RX_MIN_LEN	MAC Minimum Receive Frame Length Register.	0x00000040	R/W
0x00C9	MAC_RXFILT_VID_TABLE	MAC VLAN Identifier Filter Table Register.	0x00000000	R/W
0x00CA	MAC_RXFILT_ETYPE_TABLE	MAC Ethernet Type Filter Table Register.	0x00000000	R/W
0x00CB	MAC_RXFILT_ETYPE_CNRL	MAC Ethernet Typer Filter Table Control Register.	0x00000000	R/W

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

MACPHY IDENTIFICATION VERSION REGISTER

OA-SPI Address: 0x0000, MMS: 0x0, Reset: 0x00000010 (see note)

The MAC_IDVER register indicates the MACPHY version information.

Note: ADIN1140 supports OASPI version 1.**1**, however the MINVER will return 0 instead.

Table 172. Bit Descriptions for MAC_IDVER

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R
[7:4]	MAJVER	OA major version. The MAC_IDVER.MAJVER bits are the major version identifier of the OPEN Alliance Serial 10BASE-T1x MACPHY Interface Specification supported by this device.	0x1	R
[3:0]	MINVER	OA minor version. The MAC_IDVER.MINVER bits are the minor version identifier of the OPEN Alliance Serial 10BASE-T1x MACPHY Interface Specification supported by this device. **Note:** Although this bit field is returning 0, but ADIN1140 is supporting minor version 1 (OASPI version 1.1).	0x0 (see note)	R

PHY IDENTIFICATION REGISTER

OA-SPI Address: 0x0001, MMS: 0x0, Reset: 0x0283BE00

The MAC_PHYID register provides information on the PHY interface as described below.

Table 173. Bit Descriptions for MAC_PHYID

Bits	Bit Name	Description	Reset	Access
[31:10]	OUI	Organizationally unique identifier (bits 2:23). The 22 MAC_PHYID.OUI bits correspond to the 22 most significant bits of the manufacturers assigned 24-bit Organizationally Unique Identifier (OUI). The OUI is arranged into the PHYID register such that OUI bit 2 is located at PHYID bit 31 and OUI bit 23 is located at PHYID bit 10.	0xA0EF	R
[9:4]	MODEL	Manufacturers model number. The MAC_PHYID.MODEL bits are used to identify the device model.	0x20	R
[3:0]	REVISION	Manufacturers revision number. The MAC_PHYID.REVISION bits provide the manufacturers product revision number which is used to indicate a revision level of the device.	0x0	R

SUPPORTED CAPABILITIES STATUS REGISTER

OA-SPI Address: 0x0002, MMS: 0x0, Reset: 0x000006C3 (see note)

The MAC_CAPABILITY register indicates MAC capabilities as described below.

Note: ADIN1140 supports Direct PHY Register Access Capability and does not support Indirect PHY Register Access Capability, but the **IPRAC** bit is set instead of the **DPRAC** bit. So, the device supports only Direct PHY Register Access and does not support Indirect PHY Register Access, despite the register field values. Host software should not rely on the IPRAC/DPRAC bits to determine the supported PHY register access method.

Table 174. Bit Descriptions for MAC_CAPABILITY

Bits	Bit Name	Description	Reset	Access
[31:11]	RESERVED	Reserved.	0x0	R
10	TXFCSVC	Transmit check sequence validation. The MAC_CAPABILITY.TXFCSVC bit indicates the ability to validate the FCS appended by and received from the SPI host. When this bit is set (=1) it also indicates the ability of the MAC to: accept egress frames with padding have the FCS appended by the SPI host and send ingress frames to the SPI host with the received FCS 0: Transmit FCS Validation is Not Supported. 1: Transmit FCS Validation is Supported.	0x1	R
9	IPRAC	Indirect PHY register access. The MAC_CAPABILITY.IPRAC bit indicates if the PHY registers are indirectly accessible through the MDIO/MDC register MDIOACCn. 0: PHY Registers are Not Indirectly Accessible. 1: PHY Registers are Indirectly Accessible.	0x1 (see note)	R

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 174. Bit Descriptions for MAC_CAPABILITY (Continued)

Bits	Bit Name	Description	Reset	Access
		Note: The device supports only Direct PHY Register Access and does not support Indirect PHY Register Access, despite the register field values.		
8	DPRAC	Direct PHY register access. The MAC_CAPABILITY.DPRAC bit indicates if the PHY registers are directly accessible within the SPI register memory space. 0: PHY Registers are Not Directly Accessible. 1: PHY Registers are Directly Accessible. **Note:** The device supports only Direct PHY Register Access and does not support Indirect PHY Register Access, despite the register field values.	0x0 (see note)	R
7	CTC	Cut through. The MAC_CAPABILITY.CTC bit indicates if the MACPHY device supports cut-through transfer of frames through the MACPHY to/from the network. 0: Cut-Through Not Supported. 1: Cut-Through Supported.	0x1	R
6	FTSC	Frame Timestamp. The MAC_CAPABILITY.FTSC bit indicates if the MACPHY device supports the capturing of IEEE 1588 timestamps on frame receive from or transmit to the network. 1: IEEE 1588 Timestamp Capture on Frame Tx/Rx is Supported. 0: IEEE 1588 Timestamp Capture on Frame Tx/Rx is Not Supported.	0x1	R
5	AIDC	Address increment disable. The MAC_CAPABILITY.AIDC bit indicates if the MACPHY device supports disabling the automatic post-incrementing of the register address in control command reads and writes through the AID bit in the control command header. Address increment disable is not supported. 0: Address Increment Disable Not Supported. 1: Address Increment Disable Supported.	0x0	R
4	SEQC	Transmit data chunk sequence and retry. The MAC_CAPABILITY.SEQC bit indicates if the MACPHY supports monitoring the SEQ bit sent by the SPI host in the transmit data chunk header and the retry of transmit data chunks. 1: TX Data Chunk Sequence and Retry is Supported. 0: TX Data Chunk Sequence and Retry is Not Supported.	0x0	R
3	RESERVED	Reserved.	0x0	R
[2:0]	MINCPS	Minimum supported chunk payload. The MAC_CAPABILITY.MINCPS bit indicates the minimum size chunk payload that may be configured using the MAC_CONFIG0.CPS bits. The minimum supported chunk payload size is 2^N, where N is the value of this bit field. 110: Minimum Supported Chunk Payload Size is 64 Bytes. 101: Minimum Supported Chunk Payload Size is 32 Bytes. 100: Minimum Supported Chunk Payload Size is 16 Bytes. 011: Minimum Supported Chunk Payload Size is 8 Bytes.	0x3	R

MAC RESET CONTROL AND STATUS REGISTER

OA-SPI Address: 0x0003, MMS: 0x0, Reset: 0x00000000

The MAC_RESET register is used the perform a software reset on the MAC/PHY interface.

Table 175. Bit Descriptions for MAC_RESET

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	SWRESET	Software reset. The MAC_RESET.SWRESET bit is used to perform a software reset. The action of writing a 1 to this bit fully resets the MACPHY, including the integrated PHY, to an initial state including but not limited to resetting all state machines and registers to their default value. When this bit is set, the reset does not occur until the CSn signal is de-asserted to allow for the control command write to complete. CSn must be held asserted for at least 100 ns for the reset to take effect. This bit is self-clearing.	0x0	W

MAC CONFIGURATION REGISTER 0

OA-SPI Address: 0x0004, MMS: 0x0, Reset: 0x000000E6

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

The MAC_CONFIG0 register is used to configure the interface as described below.

Table 176. Bit Descriptions for MAC_CONFIG0

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
15	SYNC	Configuration synchronization. The state of the MAC_CONFIG0.SYNC bit is reflected in the Rx Footer SYNC bit. This bit defaults to 0 upon reset. Once written to a 1 by the SPI host, writing 0 does not clear this bit. Immediately after any reset this bit is cleared (=0) and the MAC_STATUS0.RESETC bit is set (=1) and the interrupt pin asserts. 0: The MACPHY Has Been Reset and is Not Configured. 1: The MACPHY is Configured.	0x0	R/W1S
14	TXFCSVE	Transmit frame check sequence validation enable. When the MAC_CONFIG0.TXFCSVE bit =1, the final 4 octets of all Ethernet frames received are treated as the CRC and validated. The MAC_CONFIG2.HOST_CRC_APPEND must =0 if this bit is set. In other words the MAC must not be configured to append a CRC to each transmitted frame. The CRC must be appended by the SPI main. 0: Transmit Frame Check Sequence Validation is Disabled. 1: Transmit Frame Check Sequence Validation is Enabled.	0x0	R/W
13	CSARFE	Chip select align receive frame enable. When the MAC_CONFIG0.CSARFE bit =1, all receive Ethernet frames data only start at the beginning of the first receive chunk payload following CSn assertion. The start word offset (SWO) always =0. Receive frames may begin within any receive chunk when this bit is clear. 0: CSn Align Receive Frame is Disabled. 1: CSn Align Receive Frame is Enabled.	0x0	R/W
12	ZARFE	Zero-align receive frame enable. When the MAC_CONFIG0.ZARFE bit =1, all receive Ethernet frames data are aligned to start at the beginning of the receive chunk payload with a start word offset (SWO) of zero. Receive frames may begin anywhere within the receive chunk payload when this bit is clear. 0: Zero-Align Receive Frame is Disabled. 1: Zero-Align Receive Frame is Enabled.	0x0	R/W
[11:10]	TXCTHRESH	Transmit credit threshold. The MAC_CONFIG0.TXCTHRESH bits configure the number of transmit credits (TXC) of free buffer that must be available for writing before IRQn is asserted. 00: 1 credit (deafult). 01: 4 Credits. 10: 8 Credits. 11: 16 Credits.	0x0	R/W
9	TXCTE	Transmit cut-through enable. The MAC_CONFIG0.TXCTE bit enables the cut-through mode of frame transfer through the MACPHY device from the SPI Host to the network.When cut-through on transmit is enabled, the host must ensure that data is provided to the device at a rate of > 10Mbps to ensure frame transmission does not under-run. 0: Transmit Cut-Through is Disabled. 1: Transmit Cut-Through is Enabled.	0x0	R/W
8	RXCTE	Receive cut-through enable. The MAC_CONFIG0.RXCTE bit enables the cut-through mode of frame transfer through the MACPHY device from the network to the SPI host. Cut-through must be enabled on the device configuration before receiving frames is enabled. Enable cut-through before setting or writing to the address filter registers. 0: Receive Cut-Through is Disabled. 1: Receive Cut-Through is Enabled.	0x0	R/W
7	FTSE	Frame timestamp enable. The MAC_CONFIG0.FTSE bit enables IEEE 1588 receive and transmit frame timestamps. 0: Frame Receive/Transmit Timestamps are Disabled. 1: Frame Receive/Transmit Timestamps are Enabled.	0x0	R/W
6	FTSS	Receive frame timestamp select. The MAC_CONFIG0.FTSS bit, (when supported by this MACPHY device and enabled by FTSE=1), configures the size and format of the timestamps appended to received frames and capture on request of transmit frames. 0: 32-bit Timestamps. 1: 64-bit Timestamps.	0x0	R/W

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 176. Bit Descriptions for MAC_CONFIG0 (Continued)

Bits	Bit Name	Description	Reset	Access
5	PROTE	Control data read write protection enable. When the MAC_CONFIG0.PROTE bit is set and using the Open Alliance SPI protocol, all control data written to and read from the MACPHY is transferred with its complement for detecting bit errors. **Note:** The the MAC_CONFIG0.PROTE bit cannot be written, so protection cannot be disabled. 0: Control Data Read Write Protection is Disabled. 1: Control Data Read Write Protection is Enabled.	0x1	R
4	SEQE	Transmit data chunk sequence retry enable. The MAC_CONFIG0.SEQE bit (when supported by this MACPHY device), enables MACPHY monitoring of the SEQ bit transmitted in the TX data chunk header by the SPI host and TX data chunk retries. 0 = Support for TX data chunk sequence and retry is disabled. The MACPHY ignores the TX Header SEQ bit. 1 = Support for TX data chunk sequence and retry is enabled. The MACPHY monitors the SEQ bit in the TX header and allows for the rewriting of TX data chunks when the SEQ bit does not change. 0: Receive Cut-Through is Disabled. 1: Receive Cut-Through is Enabled.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
[2:0]	CPS	Chunk payload select. The MAC_CONFIG0.CPS bits are used to configure the chunk size. This bit field should be configured on device configuration before frame transmission from the host starts and before enabling receiving frames into the receive FIFOs. This field cannot be modified while transmitting a frame from the host or while sending a received frame to the host. Once the configuration synchronization (MAC_CONFIG0.SYNC) bit has been set, the chunk payload size must not be changed without a reset of the MACPHY. The minimum supported chunk payload size for this MACPHY device is indicated in the MAC_CAPABILITY.MINCPS bit field. The chunk payload size is 2^N. N = 3 minimum and 6 maximum. The default is 64 bytes. 011: Chunk size is 8 byte. 100: Chunk size is 16 byte. 101: Chunk size is 32 byte. 110: Chunk size is 64 byte. Note: When transmit priority queuing is enabled, a minimum number of transmit credits is required before frames are accepted from OA-SPI. Refer to the Transmit Priority Queues section for details.	0x6	R/W

MAC CONFIGURATION REGISTER 2

OA-SPI Address: 0x0006, MMS: 0x0, Reset: 0x007C0020

Vendor specific.

Table 177. Bit Descriptions for MAC_CONFIG2

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
23	TX_BACK_OFF_DIS	Transmit back off. The MAC_CONFIG2.TX_BACK_OFF_DIS bit is used to disable transmit backoff. If enabled the MAC does not back off after a collision and retries again if the line is free. 0: Transmit Back off Enabled. 1: Transmit Back off Disabled.	0x0	R/W
22	TX_IFG_PART2_EN	Part1/Part2 enable. The MAC_CONFIG2.TX_IFG_PART2_EN bit enables the MAC support for IFG part1/part2. 0: Part1/Part2 IFG Mode is Disabled. 1: Part1/Part2 IFG Mode is Enabled.	0x1	R/W
21	RX_LENGTH_FIELD_CHK_EN	Checks the Length Field and Dumps the Frame If Incorrect. The MAC_CONFIG2.RX_LENGTH_FIELD_CHK_EN bit enables MAC dump of any frame where the length does not match with the value received in the length field. 0: Frames with Incorrect Length Field are Dumped. 1: Frames with Incorrect Length Field are Admitted.	0x1	R/W

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 177. Bit Descriptions for MAC_CONFIG2 (Continued)

Bits	Bit Name	Description	Reset	Access
20	RX_IGNORE_PREAMBLE_ERR	Admit frames with preamble errors. The MAC_CONFIG2.RX_IGNORE_PREAMBLE_ERR bit enables the MAC to admit frames with preamble errors. 0: Frames with Preamble Errors are Not Admitted. 1: Frames with Preamble Errors are Admitted.	0x1	R/W
19	RX_IGNORE_PREAMBLE	Admit Frames Without Preamble. The MAC_CONFIG2.RX_IGNORE_PREAMBLE bit enables the MAC to admit frames without preamble. Only the SDF is used to admit a frame. 0: Frames Without a Preamble are Not Admitted. 1: Frames Without a Preamble are Admitted.	0x1	R/W
18	RESERVED	Reserved.	0x1	R/W
17	LO_PRIO_FIFO_CRC_APPEND	CRC append for frames from the other queue. When the MAC_PLCA_PRIORITY.FRAME_PRIORITY_EN bit is set, the MAC_CONFIG2.LO_PRIO_FIFO_CRC_APPEND bit enables CRC append for the low priority FIFO. If this bit =0, the MAC assumes that the host is providing a frame with a valid CRC header at the end. Programs should ensure that the host always appends a CRC32 with the frame as this provides error detection over the SPI interface for transmitted frames. The CRC32 is checked as the frame is transmitted. If an error is detected then the MAC_STATUS0.TXFCSE interrupt is generated. Similarly, on receive the CRC32 is forwarded with the frame to the host where the host should verify that it is correct. 0: CRC is Appended by the Other Port. 1: CRC is Appended by the MAC.	0x0	R/W
[16:14]	RESERVED	Reserved.	0x0	R
13	FWD_UNK2GPTP	Forward Frames Not Matching a MAC Addr to gPTP. Determines the default rule for forwarding unknown frames.If a frame has a destination address that does not match a MAC address then the frame is dropped if this field is 0 and UNK_TO_HOST is 0. 0: Frames Not Matching Any MAC Address are Dumped. 1: Frames Not Matching Any MAC Address are Forwarded to Port2.	0x1	R/W
[12:9]	RESERVED	Reserved.	0x0	R
8	TX_RDY_ON_EMPTY	Assert TX_RDY transmit FIFO empty. The MAC_CONFIG2.TX_RDY_ON_EMPTY bit (by default) asserts when a frame has been transmitted. If this bit is set then TX_RDY asserts when the transmit FIFO is empty. 0: TX_RDY is Asserted When Frame Transmitted. 1: TX_RDY is Asserted When Tx FIFO is Empty.	0x0	R/W
7	SFD_DETECT_SRC	SFD detect. The MAC_CONFIG2.SFD_DETECT_SRC bit configures if the start frame delimiter (SFD) is detected in the PHY or MAC. 0: Select the SFD from the PHY. This option provides the least jitter as the SFD is detected in the same 120MHz clock domain as is used in 1588 timer logic. 1: Select the SFD from the MAC. The SFD from the MAC is from the 25MHz clock domain and will result in additional jitter on the SFD detection.	0x0	R/W
6	STATS_CLR_ON_RD	Clear statistics on read. The MAC_CONFIG2.STATS_CLR_ON_RD bits determines if the following registers/counters are cleared on reading. 0: Statistic Counter is Not Cleared on Reading. When the max value is reached the counters roll over to 0x0. 1: Clear Statistics Counters on Reading. If a counter reaches its max value then the counter will hold at its max until read. **Note:** When STATS_CLR_ON_READ is enabled, only the first register in a burst read returns valid data; subsequent reads in the same burst may return zero because the counters are cleared before the read completes.	0x0	R/W

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 177. Bit Descriptions for MAC_CONFIG2 (Continued)

Bits	Bit Name	Description	Reset	Access
		This is affecting the following registers reads: MAC_RX_PHY_ERR_CNT, MAC_RX_DROP_HOST_FULL_CNT, and MAC_RX_DROP_FILT_CNT.		
5	HOST_CRC_APPEND	CRC append frames from host. The MAC_CONFIG2.HOST_CRC_APPEND bit enables CRC appendage by the MAC. If this bit is cleared (=0), the MAC assumes that the host is providing a frame with a valid CRC header at the end. The host should always append a CRC32 with the frame to provide error detection over the SPI interface for transmitted frames. The CRC32 is checked as the frame is transmitted. If an error is detected then the MAC_STATUS0.TXFCSE interrupt is generated. Similarly, on receive the CRC32 is forwarded with the frame to the host where the host verifies that it is valid. 0: CRC is Appended by the HOST. 1: CRC is Appended by the MAC.	0x1	R/W
4	RCV_IFG_ERR_FRM	Admit frames with IFG errors. The MAC_CONFIG2.RCV_IFG_ERR_FRM bit enables the MAC to admit frames with IFG errors that violate the minimum IFG requirement. 0: Frames with IFG Errors are Dumped. 1: Frames with IFG Errors are Admitted.	0x0	R/W
3	RESERVED	Reserved.	0x0	R/W
2	FWD_UNK2HOST	Forward frames rule. The MAC_CONFIG2.FWD_UNK2HOST bit configures the default rule for forwarding unknown frames. Frames with an unknown destination address are forwarding to HOST. 0x0: Frames Not Matching Any MAC Address are Dumped. 0x1: Frames Not Matching Any MAC Address are Forwarded to Host.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R/W

MAC STATUS REGISTER 0

OA-SPI Address: 0x0008, MMS: 0x0, Reset: 0x00000040

The MAC_STATUS0 register provides status information on the MAC interface as described below.

Table 178. Bit Descriptions for MAC_STATUS0

Bits	Bit Name	Description	Reset	Access
[31:13]	RESERVED	Reserved.	0x0	R
12	CDPE	Control data protection error. The MAC_STATUS0.CDPE bit (=1) indicates that the MACPHY detected an error in protected control write data received from the host when control data read/write protection is enabled. When not implemented, this bit is reserved with a read-only value of zero.	0x0	R/W1C
11	TXFCSE	Transmit frame check sequence error. The MAC_STATUS0.TXFCSE bit (=1) indicates that a frame was received over SPI from the host with an invalid FCS appended. The frame is still forwarded from the device as the FCS is checked as the frame is being transmitted.	0x0	R/W1C
10	TTSCAC	Transmit timestamp capture available C.	0x0	R/W1C
9	TTSCAB	Transmit timestamp capture available B.	0x0	R/W1C
8	TTSCAA	Transmit timestamp capture available A.	0x0	R/W1C
7	PHYINT	PHY Interrupt. This interrupt is tied to the PHY SQI block. This bit will be asserted when the SQI level drops below the programmable thresholds. Note: on exiting power on reset or pin reset this bit is asserted but this field is masked from asserting an interrupt by default.	0x0	R
6	RESETC	Reset complete. The MAC_STATUS0.RESETC bit (=1) when the MACPHY reset is complete and ready for configuration. When it is set, it generates a non-maskable interrupt assertion on IRQn to alert the SPI host. Additionally, setting this bit also sets EXST =1 in the first receive footer, or until this bit is cleared by action of the SPI host writing a 1.	0x1	R/W1C
5	HDRE	Header error. The MAC_STATUS0.HDRE bit (=1) indicates that the MACPHY has detected an invalid header received from the SPI host. The invalid header is due to a parity check error.	0x0	R/W1C

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 178. Bit Descriptions for MAC_STATUS0 (Continued)

Bits	Bit Name	Description	Reset	Access
4	LOFE	Loss of frame error. The MAC_STATUS0.LOFE bit (=1) indicates that the MACPHY has detected an early de-assertion of CSn prior to the expected end of a data chunk or command control transaction.	0x0	R/W1C
3	RXBOE	Receive buffer overflow error. The MAC_STATUS0.RXBOE bit (=1) indicates that the receive buffer (from the network) has overflowed and receive frame data was lost.	0x0	R/W1C
2	TXBUE	Host transmit FIFO Underrun error. The MAC_STATUS0.TXBUE bit indicates an error which is generated when cut-through from the host is enabled. The host software should ensure this bit never is never set by writing frame data to the MAC at a rate greater than 10 Mbps. If an underrun error occurs, transmission of the current packet stops. A full MAC reset is required to clear this error.	0x0	R/W1C
1	TXBOE	Host transmit FIFO overflow. Host software should ensure the MAC_STATUS0.TXBOE bit never asserts by checking the space available in the Tx FIFO before writing to the Tx FIFO. If using the Open Alliance SPI Data protocol then the space in the Tx FIFO is indicated in the TXC field of the Rx footer. If the host Tx FIFO overflows then the frame being written is dumped and software may choose to resend the entire frame. Writes to the FIFO commence at the next SOF. There is always room for more than one frame in the host transmit FIFO as it is 4k bytes (or greater) in size. Therefore a frame currently being transmitted is not interrupted by an overflow on the write side of the FIFO.	0x0	R/W1C
0	TXPE	Transmit protocol error. The MAC_STATUS0.TXPE bit (=1) indicates that a transmit data chunk protocol error has occurred. Data chunk received with DV=1 but without a prior SV=1. Data chunk received with SV=1 but with no EV=1 (repeated SV=1 received). A write of the TX_FSIZE register was detected but the MAC still expects further writes to the TX register related to the previous frame size written to the TX_FSIZE register.	0x0	R/W1C

MAC STATUS REGISTER 1

OA-SPI Address: 0x0009, MMS: 0x0, Reset: 0x00000000

The MAC_STATUS1 register provides status information on the MAC interface as described below.

Table 179. Bit Descriptions for MAC_STATUS1

Bits	Bit Name	Description	Reset	Access
31	RESERVED	Reserved.	0x0	R/W1C
30	RD_ACC_ERR	Memory read access error. The MAC_STATUS1.RD_ACC_ERR bit may assert if the SPI frequency is higher than the specified value for the SPI protocol.	0x0	R/W1C
[29:13]	RESERVED	Reserved.	0x0	R
12	TX_ECC_ERR	ECC transmit error on frame size. The MAC_STATUS1.TX_ECC_ERR bit indicates that an uncorrectable ECC error was detected on reading the frame size field from a Tx FIFO. The FIFO is automatically cleared and the frame associated with the ECC error and other frames in the Tx FIFO are not lost/dropped.	0x0	R/W1C
11	RX_ECC_ERR	ECC receive error on frame size. The MAC_STATUS1.RX_ECC_ERR bit indicates that an uncorrectable ECC error was detected on reading the frame size field from a Rx FIFO. The FIFO is automatically cleared and the frame associated with the ECC error and other frames in the Rx FIFO are not lost/ dropped.	0x0	R/W1C
10	RESERVED	Reserved.	0x0	R/W1C
9	MAX_RR_ERR	Transmit max collision retry reached. The MAC_STATUS1.MAX_RR_ERR bit indicates that the transmit max collision retry has been reached when in half-duplex mode.	0x0	R/W1C
8	RX_IFG_ERR	MAC receive IFG error. The MAC_STATUS1.RX_IFG_ERR bit (=1) if the IFG is too short then the frame is dropped on receive. The threshold used for measuring the IFG on receive can be set in the MAC_RX_IFG register.	0x0	R/W1C
7	RESERVED	Reserved.	0x0	R
6	VS_INT	Transaction interrupt controller interrupt. The MAC_STATUS1.VS_INT bit (=1) indicates that an interrupt flag triggered in the Transaction Interrupt Controller (TIC).	0x0	R
5	RESERVED	Reserved.	0x0	R
4	RX_RDY	Receive FIFO contains data. The MAC_STATUS1.RX_RDY bit indicates that there is 1 or more frames in the Rx FIFO in store and forward mode.In cut-through mode this bit indicates that the receive threshold (MAC_RX_THRESH) has been reached or the EOF byte of a frame has been received.	0x0	R
[3:0]	RESERVED	Reserved.	0x0	R/W1C

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

BUFFER STATUS REGISTER

OA-SPI Address: 0x000B, MMS: 0x0, Reset: 0x00007700

The MAC_BUFSTS register indicates the status of the chunk buffers as described below.

Table 180. Bit Descriptions for MAC_BUFSTS

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:8]	TXC	Transmit credits available. The MAC_BUFSTS.TXC bits indicate the number of chunk buffers of transmit data currently available for the SPI host to write. Reading this field allows the SPI host to queue up the number of transmit chunks available into a single DMA, if desired. The value in this field is saturated to 31 and sent in the 5-bit MAC_BUFSTS.TXC field of every receive data footer. The default (maximum) number of transmit buffer credits available is implementation specific.	0x77	R
[7:0]	RCA	Receive chunks available. The MAC_BUFSTS.RCA bits indicate the number of chunks of receive data currently available for the SPI host to read. Reading this field allows the SPI host to queue up the number of receive chunks available into a single DMA, if desired.	0x0	R

INTERRUPT MASK REGISTER 0

OA-SPI Address: 0x000C, MMS: 0x0, Reset: 0x00001FBF

The MAC_IMASK0 register allows MACPHY interrupts that are generated in the MAC_STATUS0 register to be masked as described below.

Table 181. Bit Descriptions for MAC_IMASK0

Bits	Bit Name	Description	Reset	Access
[31:13]	RESERVED	Reserved.	0x0	R
12	CDPEM	Control data protection error mask. The MAC_IMASK0.CDPEM bit, when set (=1), masks the corresponding control data protection error interrupt (MAC_STATUS0.CDPE) from asserting the footer EXST bit.	0x1	R/W
11	TXFCSEM	Transmit frame check sequence error mask. The MAC_IMASK0.TXFCSEM bit, when set (=1), masks the corresponding transmit frame check sequence interrupt (MAC_STATUS0.TXFCSE) from asserting.	0x1	R/W
10	TTSCACM	Transmit timestamp capture available C mask. The MAC_IMASK0.TTSCACM bit, when set (=1), masks the corresponding transmit timestamp capture available C interrupt (MAC_STATUS0.TTSCAC) from asserting the footer EXST bit.	0x1	R/W
9	TTSCABM	Transmit timestamp capture available B mask. The MAC_IMASK0.TTSCABM bit, when set (=1), masks the corresponding transmit timestamp capture available B interrupt (MAC_STATUS0.TTSCAB) from asserting the footer EXST bit.	0x1	R/W
8	TTSCAAM	Transmit timestamp capture available A mask. The MAC_IMASK0.TTSCAAM bit, when set (=1), masks the corresponding transmit timestamp capture available A interrupt (MAC_STATUS0.TTSCAA) from asserting the footer EXST bit.	0x1	R/W
7	PHYINTM	Physical layer interrupt mask. The MAC_IMASK0.PHYINTM bit, when set (=1), masks the corresponding physical layer interrupt (MAC_STATUS0.PHYINT) from asserting the footer EXST bit.	0x1	R/W
6	RESETCM	RESET complete mask. The MAC_IMASK0.RESETCM bit is reserved as a mask for the reset complete (MAC_STATUS0.RESETC) status bit. This bit is read only and always reads zero as the MAC_STATUS0.RESETC status bit is a non-maskable interrupt that causes IRQn to always assert when MAC_STATUS0.RESETC is set.	0x0	R
5	HDREM	Header error mask. The MAC_IMASK0.HDREM bit, when set (=1), masks the corresponding header error interrupt (MAC_STATUS0.HDRE) from asserting the footer EXST bit.	0x1	R/W
4	LOFEM	Loss of frame error mask. The MAC_IMASK0.LOFEM bit, when set (=1), masks the corresponding loss of frame error error interrupt (MAC_STATUS0.LOFE) from asserting the footer EXST bit.	0x1	R/W
3	RXBOEM	Receive buffer overflow error mask. The MAC_IMASK0.RXBOEM bit, when set (=1), masks the corresponding receive buffer overflow error interrupt (MAC_STATUS0.RXBOE) from asserting the footer EXST bit.	0x1	R/W
2	TXBUEM	Transmit buffer underflow error mask. The MAC_IMASK0.TXBUEM bit, when set (=1), masks the corresponding transmit buffer underflow error interrupt (MAC_STATUS0.TXBUE) from asserting the footer EXST bit.	0x1	R/W
1	TXBOEM	Transmit buffer overflow error mask. The MAC_IMASK0.TXBOEM bit, when set (=1), masks the corresponding transmit buffer overflow error interrupt (MAC_STATUS0.TXBOE) from asserting the footer EXST bit.	0x1	R/W

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 181. Bit Descriptions for MAC_IMASK0 (Continued)

Bits	Bit Name	Description	Reset	Access
0	TXPEM	Transmit protocol error mask. The MAC_IMASK0.TXPEM bit, when set (=1), masks the corresponding transmit protocol error status interrupt (MAC_STATUS0.TXPE).	0x1	R/W

MASK BITS FOR DRIVING THE INTERRUPT PIN REGISTER

OA-SPI Address: 0x000D, MMS: 0x0, Reset: 0x40001F5A

The MAC_IMASK1 register allows MACPHY interrupts that are generated in the MAC_STATUS1 register to be masked as described below.

Table 182. Bit Descriptions for MAC_IMASK1

Bits	Bit Name	Description	Reset	Access
31	RESERVED	Reserved.	0x0	R
30	RD_ACC_ERR_MASK	RD_ACC_ERR mask. The MAC_IMASK1.RD_ACC_ERR_MASK bit is used to mask the corresponding status interrupt bit (MAC_STATUS1.RD_ACC_ERR).	0x1	R/W
[29:13]	RESERVED	Reserved.	0x0	R
12	TX_ECC_ERR_MASK	TXF_ECC_ERR mask. The MAC_IMASK1.TX_ECC_ERR_MASK bit is used to mask the corresponding status interrupt bit (MAC_STATUS1.TX_ECC_ERR).	0x1	R/W
11	RX_ECC_ERR_MASK	RXF_ECC_ERR mask. The MAC_IMASK1.RX_ECC_ERR_MASK bit is used to mask the corresponding status interrupt bit (MAC_STATUS1.RX_ECC_ERR).	0x1	R/W
10	RESERVED	Reserved.	0x1	R/W
9	MAX_RR_ERR_MASK	MAX_RR_ERR mask. The MAC_IMASK1.MAX_RR_ERR_MASK bit is used to mask the corresponding status interrupt bit (MAC_STATUS1.MAX_RR_ERR).	0x1	R/W
8	RX_IFG_ERR_MASK	RX_IFG_ERR mask. The MAC_IMASK1.RX_IFG_ERR_MASK bit is used to mask the corresponding status interrupt bit (MAC_STATUS1.RX_IFG_ERR).	0x1	R/W
7	RESERVED	Reserved.	0x0	R
6	VS_INT_MASK	VS_INT mask. The MAC_IMASK1.VS_INT_MASK bit is used to mask the corresponding status interrupt bit (MAC_STATUS1.VS_INT).	0x1	R/W
5	RESERVED	Reserved.	0x0	R
4	P1_RX_RDY_MASK	P1_RX_RDY mask. The MAC_IMASK1.P1_RX_RDY_MASK bit is used to mask the corresponding status interrupt bit (MAC_STATUS1.RX_RDY).	0x1	R/W
[3:0]	RESERVED	Reserved.	0xA	R/W

TRANSMIT TIMESTAMP CAPTURE REGISTER A (HIGH)

OA-SPI Address: 0x0010, MMS: 0x0, Reset: 0x00000000

The MAC_TTSCAH register contains the upper 32-bits of the captured timestamp for when the requested frame was transmitted.

Table 183. Bit Descriptions for MAC_TTSCAH

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCH_A	Transmit timestamp A bits 63-32 (seconds). The MAC_TTSCAH.TTSCH_A bits indicate the transmit timestamp for bits 63-32 in seconds.	0x0	R

TRANSMIT TIMESTAMP CAPTURE REGISTER A (LOW)

OA-SPI Address: 0x0011, MMS: 0x0, Reset: 0x00000000

The MAC_TTSCAL register contains the lower 32-bits of the captured timestamp for when the requested frame was transmitted.

Table 184. Bit Descriptions for MAC_TTSCAL

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCL_A	Transmit timestamp A bits 31-0 (nanoseconds). The MAC_TTSCAL.TTSCL_A bits indicate the transmit timestamp for bits 31-0 in nanoseconds.	0x0	R

TRANSMIT TIMESTAMP CAPTURE REGISTER B (HIGH)

OA-SPI Address: 0x0012, MMS: 0x0, Reset: 0x00000000

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

The MAC_TTSCBH register contains the upper 32-bits of the captured timestamp for when the requested frame was transmitted.

Table 185. Bit Descriptions for MAC_TTSCBH

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCH_B	Transmit timestamp B bits 63-32 (seconds). The MAC_TTSCBH.TTSCH_B bits indicate the transmit timestamp for bits 63-32 in seconds.	0x0	R

TRANSMIT TIMESTAMP CAPTURE REGISTER B (LOW)

OA-SPI Address: 0x0013, MMS: 0x0, Reset: 0x00000000

The MAC_TTSCBL register contains the lower 32-bits of the captured timestamp for when the requested frame was transmitted.

Table 186. Bit Descriptions for MAC_TTSCBL

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCL_B	Transmit timestamp B bits 31-0 (nanoseconds). The MAC_TTSCBL.TTSCL_B bits indicate the transmit timestamp for bits 31-0 in nanoseconds.	0x0	R

TRANSMIT TIMESTAMP CAPTURE REGISTER C (HIGH)

OA-SPI Address: 0x0014, MMS: 0x0, Reset: 0x00000000

The MAC_TTSCCH register contains the upper 32-bits of the captured timestamp for when the requested frame was transmitted.

Table 187. Bit Descriptions for MAC_TTSCCH

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCH_C	Transmit timestamp C bits 63-32 (seconds). The MAC_TTSCCH.TTSCH_C bits indicate the transmit timestamp for bits 63-32 in seconds.	0x0	R

TRANSMIT TIMESTAMP CAPTURE REGISTER C (LOW)

OA-SPI Address: 0x0015, MMS: 0x0, Reset: 0x00000000

The MAC_TTSCCL register contains the lower 32-bits of the captured timestamp for when the requested frame was transmitted.

Table 188. Bit Descriptions for MAC_TTSCCL

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCL_C	Transmit timestamp C bits 31-0 (nanoseconds). The MAC_TTSCCL.TTSCL_C bits indicate the transmit timestamp for bits 31-0 in nanoseconds.	0x0	R

TX FIFO SPACE REGISTER

OA-SPI Address: 0x0032, MMS: 0x1, Reset: 0x00000FFF

The MAC_TX_SPACE register is used by the host software to determine if there is space in the Tx FIFO for a frame.

Table 189. Bit Descriptions for MAC_TX_SPACE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	TX_SPACE	Transmit FIFO space available. The MAC_TX_SPACE.TX_SPACE bits are used by the host software to determine if there is space in the Tx FIFO for a frame.The software can queue two frames for transmission and wait for a TX_RDY interrupt or it can fill the Tx FIFO with multiple frames and use these bits to determine if there is space for the next frame. An extra two words of space is needed per frame in the host Tx FIFO to store the frame size and header. For example, if the these bits are 64 then the max size frame that can be written is (64 - 2) x 2 bytes = 124 bytes.	0xFFF	R

MAC RECEIVE THRESHOLD REGISTER

OA-SPI Address: 0x0033, MMS: 0x1, Reset: 0x00000004

The MAC_RX_THRESH register is used to configure the receive threshold value.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 190. Bit Descriptions for MAC_RX_THRESH

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
[5:0]	RX_THRESH	Receive threshold in cut through. The MAC_RX_THRESH.RX_THRESH bits are used to configure the receive threshold in half words (16 bit) when cut through on receive is enabled (MAC_CONFIG0.RXCTE=1). This field is not used when store and forward is enabled. This bit field should be configured to greater than or equal to the chunk size (this bit value >= (2^MAC_CONFIG0.CPS)/2). If configured to less than the chunk size then internally the device uses (2^CPS)/2 as the receive threshold. The minimum value for this field is 4 half words which corresponds to a chunk size of 8 bytes.The maximum value for this field is 32 half words.	0x4	R/W

TRANSMIT THRESHOLD REGISTER

OA-SPI Address: 0x0034, MMS: 0x1, Reset: 0x00000001

The MAC_TX_THRESH register is used to configure the host transmit start threshold in cut through.

Table 191. Bit Descriptions for MAC_TX_THRESH

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
[5:0]	HOST_TX_THRESH	Host transmit start threshold in cut through. When cut through on Tx is enabled (MAC_CONFIG0.TXCTE=1), the MAC_TX_THRESH.HOST_TX_THRESH bits are used to set the threshold in half words (16 bits) at which frame transmission starts for frames coming from the host. The range of valid values for this field is 1 to 26 half words. **Note:** When operating in cut-through mode, the frame may be sent before the host transmit start threshold is reached. The data will start exiting the FIFO at most 4 words before the threshold is reached.	0x1	R/W

TRANSMIT PRIORITY REGISTER

OA-SPI Address: 0x0035, MMS: 0x1, Reset: 0x00000000

The MAC_TX_PRI register is used to configure the host transmit priority.

Table 192. Bit Descriptions for MAC_TX_PRI

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
[2:0]	TX_HOST_PRI	Host transmit priority. The MAC_TX_PRI.TX_HOST_PRI bits configure the host transmit priority. When frames are queued to egress from both High queue and Low queue at the same time, this field determines the ratio of access to the port. For example if the field is set to 75/25 High/Low, then 75% of the frames transmitted is from the high queue and 25% from low queue. The ratio is based on comparing the recent number of bytes transmitted from the high queue and low queue. 000: 50/50 High/Low. 001: Reserved. 010: 75/25 High/Low. 011: Reserved. 100: 85.5/12.5 High/Low. 101: 100/0 High/Low. High is always guaranteed access to wire. 110: Reserved. Port to port traffic always gets priority.	0x0	R/W

MAC FIFO CLEAR REGISTER

OA-SPI Address: 0x0036, MMS: 0x1, Reset: 0x00000000

The MAC_FIFO_CLR register is used to clear MAC FIFOs.

Note: The MAC FIFO clear signals in the MAC_FIFO_CLR register do not clear the full data path. There are some internal FIFOs which are not cleared by these commands. Similarly, when an uncorrectable error in a frame header occurs, the FIFOs should be automatically cleared. This automatic clear has the same limitation. If needed a full MAC reset is required to ensure that all internal MAC FIFOs are fully cleared.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 193. Bit Descriptions for MAC_FIFO_CLR

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
2	ALL_FIFOS_CLR	Clear all FIFOs. The MAC_FIFO_CLR.ALL_FIFOS_CLR bit is used to clear all FIFOs. Use this setting when an uncorrectable ECC error is detected. If a frame is currently being transmitted from a Tx FIFO then transmission stops and a bad CRC is appended to the frame.Writes to Rx FIFO's resume at the start of the next received frame.	0x0	W
1	RESERVED	Reserved.	0x0	W
0	MAC_RXF_CLR	Clear receive FIFO(s). The MAC_FIFO_CLR.MAC_RXF_CLR bit is used to clear receive FIFOs. Use this setting when an uncorrectable ECC error is detected on a read from a Rx FIFO. Writes to the Rx FIFO resume at the start of the next frame.	0x0	W

MAC SCRATCH REGISTER

OA-SPI Address: 0x0037 to 0x003A (increments of 1), MMS: 0x1, Reset: 0x00000000

The MAC_SCRATCHN registers ([n] = 0-3) are used for debug operations.

Table 194. Bit Descriptions for MAC_SCRATCHn

Bits	Bit Name	Description	Reset	Access
[31:0]	SCRATCH_DATA	Scratch data. The MAC_SCRATCHN.SCRATCH_DATA bits are used for debug control to check that the write and read access to the MAC register map is working correctly without changing the configuration of any functional control.	0x0	R/W

MAC INJECT ERROR ON SDI FROM DUT REGISTER

OA-SPI Address: 0x003D, MMS: 0x1, Reset: 0x00000000

The MAC_SPI_INJ_ERR register is used to configure the ability to test that errors received on SDI are correctly detected in software.

Table 195. Bit Descriptions for MAC_SPI_INJ_ERR

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	TEST_SPI_INJ_ERR	Inject error on SPI SDI path enable. The MAC_SPI_INJ_ERR.TEST_SPI_INJ_ERR bit enables software to test that errors received on SDI are correctly detected in software. If this bit =1 and the program is using the following protocols:-Open Alliance SPI protocol for data transaction. The parity bit in the Rx Footer is inverted.-Open Alliance SPI protocol for protected control burst write transactions. Starting from the 2nd word in a burst, the most significant bit of each echoed 32-bit complement word is inverted.-Open Alliance SPI protocol for protected control read transactions. The most significant bit of each 32-bit complement word is inverted.	0x0	R/W

FIFO SIZES REGISTER

OA-SPI Address: 0x003E, MMS: 0x1, Reset: 0x00000022

Before modifying the FIFO sizes, frame reception and transmission must be stopped and the FIFOs must be empty.

Configure ADDR_RULE to drop all frames and set MAC_CONFIG2.FWD_UNK2HOST to 0 to ensure all received frames are dropped.

Use MAC_FIFO_CLR.ALL_FIFOS_CLR to reset the FIFOs. Then the FIFO sizes can be modified.

The total FIFO size must less than or equal to {+}16k bytes.

Note: The MAC FIFO size configuration does not include underflow protection. Setting any FIFO size field in the MAC_FIFO_SIZE register to zero will result in an underflow and the FIFO will be assigned the maximum size, using the same memory space as other FIFOs. FIFO size fields must be configured to nonzero values for all FIFOs that may be written by the system.

Table 196. Bit Descriptions for MAC_FIFO_SIZE

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 196. Bit Descriptions for MAC_FIFO_SIZE (Continued)

Bits	Bit Name	Description	Reset	Access
[27:24]	T1S_2_PTP_SIZE	T1S to LCE FIFO Size. The MAC_FIFO_SIZE.T1S_2_PTP_SIZE bits are used to configure the T1S to GPTP FIFO size 0000: 0 Bytes. 0001: 2k Bytes.	0x1	R/W
[23:20]	LOW_TX_FIFO_SIZE	HOST to T1S Low Priority FIFO Size. 0000: 0 Bytes. 0001: 2k Bytes. 0010: 4k Bytes. 0011: 6k Bytes. 0100: 8k Bytes. 0101: 10k Bytes. 0110: 12k Bytes. 0111: 14k Bytes. 1000: 16k Byte.	0x1	R/W
[19:8]	RESERVED	Reserved.	0x20	R
[7:4]	T1S_2_HOST_SIZE	T1S to HOST FIFO size. The MAC_FIFO_SIZE.T1S_2_HOST_SIZE bits are used to configure the T1S to HOST FIFO size. 0000: 0K Bytes. 0001: 2k Bytes. 0010: 4k Bytes. 0011: 6k Bytes. 0100: 8k Bytes. 0101: 10k Bytes. 0110: 12k Bytes. 0111: 14k Bytes. 1000: 16k Bytes.	0x2	R/W
[3:0]	HIGH_TX_FIFO_SIZE	HOST to T1S high priority FIFO size. The MAC_FIFO_SIZE.HIGH_TX_FIFO_SIZE bits are used to configure the HOST to T1S high priority FIFO size. 0000: 0k Bytes. 0001: 2k Bytes. 0010: 4k Bytes. 0011: 6k Bytes. 0100: 8k Bytes. 0101: 10k Bytes. 0110: 12k Bytes. 0111: 14k Bytes. 1000: 16k Byte.	0x2	R/W

TX FIFO FRAME COUNT REGISTER

OA-SPI Address: 0x003F, MMS: 0x1, Reset: 0x00000000

The MAC_TFC register is used for debug only. It indicates the number of frames in the transmit FIFO.

Table 197. Bit Descriptions for MAC_TFC

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved.	0x0	R
[8:0]	TFC	Number of frames in Tx FIFO. The MAC_TFC.TFC bits indicate the number of frames in the Tx FIFO.	0x0	R

TX FIFO VALID HALF WORDS REGISTER

OA-SPI Address: 0x0040, MMS: 0x1, Reset: 0x00000000

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

The MAC_TXSIZE register is used to indicate the number of valid half words (16-bit) in the host Tx FIFO.

Table 198. Bit Descriptions for MAC_TXSIZE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	TX_SIZE	Tx FIFO size. The MAC_TXSIZE.TX_SIZE its indicate data in the Tx FIFO in the number of half words (16-bit).	0x0	R

HOST TRANSMIT FRAMES DROPPED DUE TO FIFO OVERFLOW REGISTER

OA-SPI Address: 0x0041, MMS: 0x1, Reset: 0x00000000

The MAC_HTX_OVF_FRM_CNT register indicates the number of HOST transmit frames dropped due to FIFO overflow.

Table 199. Bit Descriptions for MAC_HTX_OVF_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	HTX_OVF_FRM_CNT	Host Tx Frames Dropped FIFO Overflow. The MAC_HTX_OVF_FRM_CNT.HTX_OVF_FRM_CNT register indicates the number of HOST transmit frames dropped due to FIFO overflow.	0x0	R

ECC ERROR MEMORY ADDRESS REGISTER

OA-SPI Address: 0x0042, MMS: 0x1, Reset: 0x00000000

The MAC_MECC_ERR_ADDR register indicates the the address of the first uncorrectable ECC error detected.

Table 200. Bit Descriptions for MAC_MECC_ERR_ADDR

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	MECC_ERR_ADDR	Address of uncorrectable ECC error. The MAC_MECC_ERR_ADDR.MECC_ERR_ADDR bits provide the address of the first uncorrectable ECC error detected. This error is indicated when either the MAC_STATUS1.RX_ECC_ERR or MAC_STATUS1.TX_ECC_ERR bits assert. When MAC_STATUS1.RX_ECC_ERR or MAC_STATUS1.TX_ECC_ERR are cleared, the register is opened to capture the address of the next ECC error. SRAM is 16 bits wide and this address points to the location in SRAM.	0x0	R

CORRECTED ECC ERROR COUNTERS REGISTER

OA-SPI Address: 0x0043, MMS: 0x1, Reset: 0x00000000

The MAC_CECC_ERRN register contains a counter for the number of bit errors corrected by ECC.

Table 201. Bit Descriptions for MAC_CECC_ERRn

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved.	0x0	R
[9:0]	CECC_ERR_CNT	Corrected ECC error count. The MAC_CECC_ERRN.CECC_ERR_CNT counters map to FIFO's as follows: CECC_ERR[0] - T1S to HOST FIFO CECC_ERR[4] - HOST to T1S High Priority FIFO CECC_ERR[5] - HOST to T1S Low Priority FIFO CECC_ERR[6] - T1S to GPTP FIFO (LES only) **Note:** The MAC_CECC_ERR_CNT[4] corrected ECC error counter is not reliable, and may increase in large increments due to a single corrected ECC error.	0x0	R

ALMOST EMPTY ASSERTION THRESHOLD VALUE REGISTER

OA-SPI Address: 0x004C, MMS: 0x1, Reset: 0x00000004

The MAC_FIFO_ALMOST_EMPTY register is used to configure the almost empty threshold value.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 202. Bit Descriptions for MAC_FIFO_ALMOST_EMPTY

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R
[7:0]	AE_THRESH	Almost empty threshold. The MAC_FIFO_ALMOST_EMPTY.AE_THRESH bits are used to configure the almost empty threshold value. This affects all FIFOs. An almost full signal is asserted when the FIFO fill level reaches this value.	0x4	R/W

MAC ADDRESS RULE AND DA FILTER UPPER 16 BITS REGISTER

OA-SPI Address: 0x0050 to 0x006E (increments of 2), MMS: 0x1, Reset: 0x00000000

Contains the Upper 16 Bits of a MAC Address and the filtering rule associated with the MAC address.

When writing the ADDR_FILT registers two register locations must be written in order for a given table entry.

For example to write table entry 0 the registers should be written in this order:

1: ADDR_FILT_UPR[0]

2: ADDR_FILT_LWR[0]

Table 203. Bit Descriptions for MAC_ADDR_FILT_UPRn

Bits	Bit Name	Description	Reset	Access
31	RESERVED	Reserved.	0x0	R/W
30	APPLY2PORT	Apply rule. The MAC_ADDR_FILT_UPRN.APPLY2PORT bit is used to apply (=1) the rule configured in the MAC_ADDR_FILT_UPRN.TO_HOST bit. 0: Do Not Apply. Do not apply this table entry/rule to frames received. 1: Apply. Apply this table entry/rule to frames received.	0x0	R/W
[29:18]	RESERVED	Reserved.	0x0	R
17	TO_GPTP	Controls Forwarding of Frames Matching This MAC Address to the Other Port. The MAC_ADDR_FILT_UPRN.TO_GPTP bit is used to configure how the MAC forwards frames that match this MAC address to the other port. 0: Drop frames matching DA. If APPLY is set to 1, then frames matching the DA for this entry will be dropped. 1: Forward frames matching DA. If APPLY is set to 1, then frames matching this DA will be forwarded to the other port.	0x0	R/W
16	TO_HOST	Forward frames match MAC address to host. If MAC_ADDR_FILT_UPRN.APPLY2PORT is set (=1) and MAC_ADDR_FILT_UPRN.TO_HOST = 1, then frames matching this DA are forwarded to the host. If MAC_ADDR_FILT_UPRN.TO_HOST = 0, frames matching the DA for this entry are dropped. 0: Drop frames matching DA. If APPLY is set to 1, then frames matching the DA for this entry will be dropped. 1: Forward frames matching DA. If APPLY is set to 1, then frames matching this DA will be forwarded to the host.	0x0	R/W
[15:0]	MAC_ADDR[47:32]	MAC address.	0x0	R/W

MAC ADDRESS DA FILTER (LOWER 32 BITS) REGISTER

OA-SPI Address: 0x0051 to 0x006F (increments of 2), MMS: 0x1, Reset: 0x00000000

The MAC_ADDR_FILT_LWRN registers ([n] = 0-15) contain the lower 32 bits of a MAC address in the DA filter table. A write to one of lower registers must be preceded by a write to the corresponding MAC_ADDR_FILT_UPRN register.

Table 204. Bit Descriptions for MAC_ADDR_FILT_LWRn

Bits	Bit Name	Description	Reset	Access
[31:0]	MAC_ADDR[31:0]	MAC address.	0x0	R/W

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

MAC ADDRESS (UPPER 32 BITS) MASK REGISTER

OA-SPI Address: 0x0070 to 0x0072 (increments of 2), MMS: 0x1, Reset: 0x0000FFFF

The MAC_ADDR_MSK_UPRN registers ([n] = 0-15) configure the upper 32 bits of a MAC address mask in the DA mask table. When writing the address mask registers, both lower and upper registers must be written with the upper register written first followed by the lower register (for a given table entry).

The mask entry field is used to indicate how many bits, from left to right, the filter checks against the MAC address. For example, to require an exact match with the MAC address (to check all 48 bits) enter 0xFFFF_FFFF_FFFF in the mask filter. To check only the first 32 bits, enter 0xFFFF_FFFF_0000.

Table 205. Bit Descriptions for MAC_ADDR_MSK_UPRn

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	MAC_ADDR_MASK[47:32]	MAC mask address.	0xFFFF	R/W

MAC ADDRESS (LOWER 32 BITS) MASK REGISTER

OA-SPI Address: 0x0071 to 0x0073 (increments of 2), MMS: 0x1, Reset: 0xFFFFFFFF

The MAC_ADDR_MSK_LWRN registers ([n] = 0-15) configure the lower 32 bits of a MAC address mask in the DA mask table. When writing the address mask registers, both lower and upper registers must be written with the upper register written first followed by the lower register (for a given table entry).

Table 206. Bit Descriptions for MAC_ADDR_MSK_LWRn

Bits	Bit Name	Description	Reset	Access
[31:0]	MAC_ADDR_MASK[31:0]	MAC mask address.	0xFFFFFFFF	R/W

TIMESTAMP ACCUMULATOR ADDEND REGISTER

OA-SPI Address: 0x0080, MMS: 0x1, Reset: 0xA0000000

The MAC_TS_ADDEND register is used to configure the nanoseconds counter.

Table 207. Bit Descriptions for MAC_TS_ADDEND

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_ADDEND	Timestamp accumulator addend. The MAC_TS_ADDEND.TS_ADDEND bits are used to configure the nanoseconds counter. The counter increments by 80 decimal every time the carry output from the accumulator is high. The accumulator defaults to 0x8000_0000 so the nanoseconds counter effectively increments at rate of 12.5 MHz by default.	0xA0000000	R/W

TIMER UPDATE COMPARE REGISTER

OA-SPI Address: 0x0081, MMS: 0x1, Reset: 0x3B9ACA00

The MAC_TS_1SEC_CMP register contains the timestamp 1 second compare value, which is the value in ns where the 'nanoseconds' counter resets and the 'seconds' counter increments by 1.

Table 208. Bit Descriptions for MAC_TS_1SEC_CMP

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_1SEC_CMP	Timestamp 1 second compare. The MAC_TS_1SEC_CMP.TS_1SEC_CMP bits are used to configure the timestamp 1 second compare value.	0x3B9ACA00	R/W

SECONDS COUNTER REGISTER

OA-SPI Address: 0x0082, MMS: 0x1, Reset: 0x00000000

The MAC_TS_SEC_CNT register is used to write to the seconds counter.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 209. Bit Descriptions for MAC_TS_SEC_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_SEC_CNT	Write to seconds counter. To speed up synchronization to a system time it is possible to write to the MAC_TS_SEC_CNT.TS_SEC_CNT bits via the MAC_TS_SEC_CNT registers and the nanoseconds counter can be written via the MAC_TS_NS_CNT register.	0x0	R/W

NANOSECONDS COUNTER REGISTER

OA-SPI Address: 0x0083, MMS: 0x1, Reset: 0x00000000

The MAC_TS_NS_CNT register is used to write to the nanoseconds counter.

Table 210. Bit Descriptions for MAC_TS_NS_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_NS_CNT	Write to nanoseconds counter. To speed up synchronization to a system time it is possible to write to the MAC_TS_NS_CNT.TS_NS_CNT bits via the MAC_TS_NS_CNT registers and the seconds counter can be written via the MAC_TS_SEC_CNT register. Note that this register must be programmed with a value that is divisible by 16 decimal. This is because the counters are driven by a 120 MHz clock and increments in steps of 16.	0x0	R/W

TIMER CONFIGURATION REGISTER

OA-SPI Address: 0x0084, MMS: 0x1, Reset: 0x00000001

The MAC_TS_CFG register is used to configure the MAC timer as described below.

Table 211. Bit Descriptions for MAC_TS_CFG

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved.	0x0	R
4	TS_CAPT_FREE_CNT	Capture the Free Running Counter. When the MAC_TS_CFG.TS_CAPT_FREE_CNT bit is set (=1) and MAC_CONFIG0.FTSS =0 then timestamps are captured from the 32-bit free running counter.If this bit =0 and MAC_CONFIG0.FTSS =0 then 32-bit timestamps as defined in the Open Alliance MAC-PHY spec are captured.If MAC_CONFIG0.FTSS =1 then 64 bit timestamps as defined in the Open Alliance MAC-PHY spec are captured.	0x0	R/W
3	TS_TIMER_STOP	Stop toggling TS_TIMER output. Write 1 to the MAC_TS_CFG.TS_TIMER_STOP bit to stop the TS_TIMER output toggling and return it to its default value. Write to the MAC_TS_TIMER_START register to start the TS_TIMER output signal again.This bit automatically clears to 0.	0x0	W
2	TS_TIMER_DEF	Default value for TS_TIMER output. The MAC_TS_CFG.TS_TIMER_DEF bit is used to change the default value of the TS_TIMER from 0. Write 1 to this field before enabling the TS_TIMER (its enabled when MAC_TS_TIMER_START.TS_TSTART is written). Note that on writing 1 to this register the TS_TIMER output immediately toggles from 0 to 1.Writing to this field has no effect if the TS_TIMER has already been enabled.	0x0	R/W
1	TS_CLR	Clear 1588 timestamp counters. The MAC_TS_CFG.TS_CLR bit clears the timestamp counter by setting the bit (=1). Four counters are cleared, the accumulator, the nanoseconds counter, the seconds counter and the "free running" counter. This bit automatically clears to 0 after it is written =1.	0x0	W
0	TS_EN	Enable 1588 timestamp counter. The MAC_TS_CFG.TS_EN bit enables the 1588 timestamp counter. When this bit is set, (=1) the timestamp counter is enabled and timestamps are captured for all received frames.The counters are not cleared when this bit =0, they simply freeze. It is recommended to write to MAC_TS_CFG.TS_CLR after disabling the counters so they are in a known state before starting again.	0x1	R/W

HIGH PERIOD FOR TS_TIMER REGISTER

OA-SPI Address: 0x0085, MMS: 0x1, Reset: 0x00000000

The MAC_TS_TIMER_HI register is used to configure the high period for the TS_TIMER.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 212. Bit Descriptions for MAC_TS_TIMER_HI

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_TIMER_HI	TS_TIMER high period. The MAC_TS_TIMER_HI.TS_TIMER_HI bits are used to configure the high period for the TS_TIMER. Note that this register must be programmed with a value that is divisible by 16 decimal. This is because the counters are driven by a 62.5 MHz nominal clock and therefore increment in steps of 16 ns. The minimum value that can be written to this field is 16 decimal.	0x0	R/W

LOW PERIOD FOR TS_TIMER REGISTER

OA-SPI Address: 0x0086, MMS: 0x1, Reset: 0x00000000

Table 213. Bit Descriptions for MAC_TS_TIMER_LO

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_TIMER_LO	TS_TIMER low period. The MAC_TS_TIMER_LO.TS_TIMER_LO bits are used to configure the low period for the TS_TIMER. Note that this register must be programmed with a value that is divisible by 16 decimal. This is because the counters are driven by a 62.5 MHz nominal clock and therefore increment in steps of 16 ns. The minimum value that can be written to this field is 16 decimal.	0x0	R/W

QUANTIZATION ERROR CORRECTION REGISTER

OA-SPI Address: 0x0087, MMS: 0x1, Reset: 0x00000000

The MAC_TS_TIMER_QE_CORR register is used to configure a compensation value for quantization error.

If the required TS_TIMER low and high periods are not directly divisible by 16 then program this field with a value between 0 and 15 to compensate for the TS_TIMER quantization error.

Table 214. Bit Descriptions for MAC_TS_TIMER_QE_CORR

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R
[7:0]	TS_TIMER_QE_CORR	TS_TIMER quantization error correction value. The MAC_TS_TIMER_QE_CORR.TS_TIMER_QE_CORR bits are used to configure a compensation value for quantization error.If the required TS_TIMER low and high periods are not directly divisible by 16 then program this field with a value between 0 and 15 to compensate for the TS_TIMER quantization error. 0: No Quantization Error Correction. 1: 1ns Quantization Error Correction. 2: 2ns Quantization Error Correction. 3: 3ns Quantization Error Correction. 4: 4ns Quantization Error Correction. 5: 5ns Quantization Error Correction. 6: 6ns Quantization Error Correction. 7: 7ns Quantization Error Correction. 8: 8ns Quantization Error Correction. 9: 9ns Quantization Error Correction. 10: 10ns Quantization Error Correction. 11: 11ns Quantization Error Correction. 12: 12ns Quantization Error Correction. 13: 13ns Quantization Error Correction. 14: 14ns Quantization Error Correction. 15: 15ns Quantization Error Correction.	0x0	R/W

TS_TIMER COUNTER START TIME LOWER REGISTER

OA-SPI Address: 0x0088, MMS: 0x1, Reset: 0x00000000

The MAC_TS_TIMER_START register is used to configure the point in time at which to start the TS_TIMER counter.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 215. Bit Descriptions for MAC_TS_TIMER_START

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_TSTART	Point in Time at Which to Start the TS_TIMER Counter (NS). Writing to the MAC_TS_TIMER_START.TS_TSTART bits start the TS_TIMER output.After the TS_TIMER has started, writing to MAC_TS_CFG.TS_TIMER_STOP stops the timer and returns the TS_TIMER output to its default value.	0x0	R/W

TS_CAPT NANOSECONDS TIMESTAMP REGISTER

OA-SPI Address: 0x0089, MMS: 0x1, Reset: 0x00000000

The MAC_TS_EXT_CAPT0 register indicates if the timestamp was captured on the assertion of the TS_CAPT pin.

Table 216. Bit Descriptions for MAC_TS_EXT_CAPT0

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_EXT_CAPTD[31:0]	Timestamp captured on assertion of TS_CAPT pin. The MAC_TS_EXT_CAPT1.TS_EXT_CAPTD bits indicate if the timestamp was captured on the assertion of the TS_CAPT pin.	0x0	R

TS_CAPT SECONDS TIMESTAMP REGISTER

OA-SPI Address: 0x008A, MMS: 0x1, Reset: 0x00000000

The MAC_TS_EXT_CAPT1 register indicates if the timestamp was captured on the assertion of the TS_CAPT pin.

Table 217. Bit Descriptions for MAC_TS_EXT_CAPT1

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_EXT_CAPTD[63:32]	Timestamp captured on assertion of TS_CAPT pin. The MAC_TS_EXT_CAPT1.TS_EXT_CAPTD bits indicate if the timestamp was captured on the assertion of the TS_CAPT pin.	0x0	R

TS_CAPT FREE RUNNING COUNTER REGISTER LOWER REGISTER

OA-SPI Address: 0x008B, MMS: 0x1, Reset: 0x00000000

The MAC_TS_FREECNT_CAPT register indicates the capture of the free running counter when the TS_CAPT pin asserts.

Table 218. Bit Descriptions for MAC_TS_FREECNT_CAPT

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_CNT_CAPTD	Captured free running counter. The MAC_TS_FREECNT_CAPT.TS_CNT_CAPTD 32 bit counter is captured on the assertion of TS_CAPT pin as is TS_EXT_CAPT.	0x0	R

PLCA TRANSMIT THROTTLE REGISTER

OA-SPI Address: 0x008D, MMS: 0x1, Reset: 0x00080000

The MAC_PLCA_PRIORITY register is used to control aspects of PLCA operation as described below.

Table 219. Bit Descriptions for MAC_PLCA_PRIORITY

Bits	Bit Name	Description	Reset	Access
[31:20]	RESERVED	Reserved.	0x0	R
19	PLCA_PENDING_PKT_FORCE	Force PCLA pending packing enable. PLCA normal operation is the following in this scenario: 1) Node 1 is receiving a frame 2) MAC in Node 1 gets a frame to transmit, as CRS is high, it holds off 3) Node 1 finishes receiving frame, CRS goes low, IFG counter starts 4) Node 1 gets its transmit opportunity straight away as it is the next node 5) Node 1 transmit opportunity times out before the IFG in the MAC, Node 1 misses its transmit opportunity If this bit is high, the MAC will force the PLCA pending_packet in that scenario and it won't miss its transmit opportunity. WARNING - This functionality only works with the PLCA. It is not part of the IEEE spec, but it does not violate it.	0x1	R/W
[18:17]	RESERVED	Reserved.	0x0	R/W

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 219. Bit Descriptions for MAC_PLCA_PRIORITY (Continued)

Bits	Bit Name	Description	Reset	Access
16	FRAME_PRIORITY_EN	Frame priority enable. The MAC_PLCA_PRIORITY.FRAME_PRIORITY_EN bit is used to enable frame priority.	0x0	R/W
[15:8]	NET_PRIORITY_ID	Network priority list. The MAC_PLCA_PRIORITY.NET_PRIORITY_ID bits are used to configure the network priority list where each bit represents a single frame priority.	0x0	R/W
[7:0]	NODE_PRIORITY_ID	Current active priority. Current active priority	0x0	R/W

MAC RECEIVE FRAME SIZE REGISTER

OA-SPI Address: 0x0090, MMS: 0x1, Reset: 0x00000000

The MAC_RX_FSIZE register indicates the size of the frame at the head of the Rx FIFO in bytes.

Table 220. Bit Descriptions for MAC_RX_FSIZE

Bits	Bit Name	Description	Reset	Access
[31:11]	RESERVED	Reserved.	0x0	R
[10:0]	RX_FRM_SIZE	Receive frame size. The MAC_RX_FSIZE.RX_FRM_SIZE bits indicate the size of the frame at the head of the receive FIFO in bytes. The size includes the appended header.	0x0	R

MAC RECEIVE FRAME COUNT REGISTER

OA-SPI Address: 0x00A1, MMS: 0x1, Reset: 0x00000000

The MAC_RX_FRM_CNT register indicates the number of frames that are successfully received.

Table 221. Bit Descriptions for MAC_RX_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_FRM_CNT	Receive frame count. The MAC_RX_FRM_CNT.RX_FRM_CNT bits indicate the number of frames that are successfully received (receiveOK). This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the ReceiveStatus is reported as receiveOK.	0x0	R

MAC RECEIVE BROADCAST FRAME COUNT REGISTER

OA-SPI Address: 0x00A2, MMS: 0x1, Reset: 0x00000000

The MAC_RX_BCAST_CNT register indicates the count of frames that are successfully received and are directed to the broadcast group address.

Table 222. Bit Descriptions for MAC_RX_BCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_BCAST_CNT	Receive broadcast frame count. The MAC_RX_BCAST_CNT.RX_BCAST_CNT bits indicate the number of frames that are successfully received and are directed to the broadcast group address. This does not include frames received with frame-too-long, FCS, length, or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField.	0x0	R

MAC RECEIVE MULTICAST FRAME COUNT REGISTER

OA-SPI Address: 0x00A3, MMS: 0x1, Reset: 0x00000000

The MAC_RX_MCAST_CNT register indicates the number of frames that are successfully received and are directed to an active nonbroadcast group address.

Table 223. Bit Descriptions for MAC_RX_MCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 223. Bit Descriptions for MAC_RX_MCAST_CNT (Continued)

Bits	Bit Name	Description	Reset	Access
[23:0]	RX_MCAST_CNT	Receive multicast frame count. The MAC_RX_MCAST_CNT.RX_MCAST_CNT bits indicate the number of frames that are successfully received and are directed to an active non broadcast group address. This does not include frames received with frame-too-long, FCS, length, or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField.	0x0	R

MAC RECEIVE UNICAST FRAME COUNT REGISTER

OA-SPI Address: 0x00A4, MMS: 0x1, Reset: 0x00000000

The MAC_RX_UCAST_CNT register indicates the number of frames that are successfully received and are directed to an active unicast address.

Table 224. Bit Descriptions for MAC_RX_UCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_UCAST_CNT	Receive unicast frame count. The MAC_RX_UCAST_CNT.RX_UCAST_CNT bits indicate the number of frames that are successfully received and are directed to an active unicast address. This does not include frames received with frame-too-long, FCS, length, or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField.	0x0	R

MAC RECEIVE CRC ERROR FRAME COUNT REGISTER

OA-SPI Address: 0x00A5, MMS: 0x1, Reset: 0x00000000

The MAC_RX_CRC_ERR_CNT register indicates the count of frames that are an integral number of octets in length and do not pass the FCS check.

Table 225. Bit Descriptions for MAC_RX_CRC_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_CRC_ERR_CNT	Receive CRC error frame count. The MAC_RX_CRC_ERR_CNT.RX_CRC_ERR_CNT bits indicate the count of frames that are an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as frameCheckError.	0x0	R

MAC RECEIVE ALIGN ERROR COUNT REGISTER

OA-SPI Address: 0x00A6, MMS: 0x1, Reset: 0x00000000

The MAC_RX_ALGN_ERR_CNT register indicates the number of frames that are not an integral number of octets in length and do not pass the FCS check.

Table 226. Bit Descriptions for MAC_RX_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_ALGN_ERR_CNT	Receive align error count. The MAC_RX_ALGN_ERR_CNT.RX_ALGN_ERR_CNT bits indicate the number of frames that are not an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as alignmentError.	0x0	R

MAC RECEIVE PREAMBLE ERROR COUNT REGISTER

OA-SPI Address: 0x00A7, MMS: 0x1, Reset: 0x00000000

The MAC_RX_PREAMBLE_ERR_CNT register indicates the number of frames that are received with preamble errors.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 227. Bit Descriptions for MAC_RX_PREAMBLE_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_PREAMBLE_ERR_CNT	Receive preamble error count. The MAC_RX_PREAMBLE_ERR_CNT.RX_PREAMBLE_ERR_CNT bits indicate the number of frames that are received with preamble errors. The counter is only incremented if the MAC_CONFIG2.RX_IGNORE_PREAMBLE or the MAC_CONFIG2.RX_IGNORE_PREAMBLE_ERR bits are not enabled.	0x0	R

MAC RECEIVE SHORT FRAME ERROR COUNT REGISTER

OA-SPI Address: 0x00A8, MMS: 0x1, Reset: 0x00000000

The MAC_RX_SHORT_ERR_CNT register indicates the number of frames that are received and it is shorter the minimum permitted frame size.

Table 228. Bit Descriptions for MAC_RX_SHORT_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_SHORT_ERR_CNT	Receive short frame error count. The MAC_RX_SHORT_ERR_CNT.RX_SHORT_ERR_CNT bits indicate the number of frames that are received and are shorter the minimum permitted frame size. This counter is incremented when the status of a frame reception is frameTooShort.	0x0	R

MAC RECEIVE LONG FRAME ERROR COUNT REGISTER

OA-SPI Address: 0x00A9, MMS: 0x1, Reset: 0x00000000

The MAC_RX_LONG_ERR_CNT register indicates the number of received frames that exceed the maximum permitted frame size.

Table 229. Bit Descriptions for MAC_RX_LONG_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_LONG_ERR_CNT	Receive long frame error count. The MAC_RX_LONG_ERR_CNT.RX_LONG_ERR_CNT bits indicate the number of frames that are received and exceed the maximum permitted frame size. This counter is incremented when the status of a frame reception is frameTooLong.	0x0	R

MAC RECEIVE PHY ERROR COUNT REGISTER

OA-SPI Address: 0x00AA, MMS: 0x1, Reset: 0x00000000

The MAC_RX_PHY_ERR_CNT register indicates the number of PHY errors detected somewhere in the frame presently being transferred from the PHY to the reconciliation sublayer.

Table 230. Bit Descriptions for MAC_RX_PHY_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_PHY_ERR_CNT	MAC receive PHY error count. The MAC_RX_PHY_ERR_CNT.RX_PHY_ERR_CNT bits indicate the number of PHY errors detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer. These errors include coding errors, or any errors that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer. Note that the receive path is unaware of collisions because they belong to the transmit path. Therefore, during a collision, receive PHY errors may occur because the receiving signal is being corrupted.	0x0	R

MAC RECEIVE FRAMES DROPPED HOST FIFO FULL REGISTER

OA-SPI Address: 0x00AB, MMS: 0x1, Reset: 0x00000000

The MAC_RX_DROP_HOST_FULL_CNT register indicates the number of receive frames dropped.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 231. Bit Descriptions for MAC_RX_DROP_HOST_FULL_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_DROP_HOST_FULL_CNT	Receive Frames Dropped Host FIFO Full. The MAC_RX_DROP_HOST_FULL_CNT.RX_DROP_HOST_FULL_CNT bits indicate the number of frames dropped due to a full receive FIFO.	0x0	R

MAC RECEIVE FRAMES DROPPED FILTERING REGISTER

OA-SPI Address: 0x00AD, MMS: 0x1, Reset: 0x00000000

The MAC_RX_DROP_FILT_CNT register indicates the number of frames dropped.

Table 232. Bit Descriptions for MAC_RX_DROP_FILT_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_DROP_FILT_CNT	Receive frames dropped due to filtering. The MAC_RX_DROP_FILT_CNT.RX_DROP_FILT_CNT register indicates the number of frames that are dropped due to the address not meeting the filter table configuration. This does not include frames received with frame-too-long, FCS, length or alignment errors. Note that there is a limitation with VLAN/Ethertype filtering, where the counter only increases if there is a hit in the MAC address table. **Note:** If an Ethernet frame is dropped due to VLAN or Ethertype filtering, the RX_DROP_FILT_CNT counter will only increment if there was a hit in the MAC address filter table. If VLAN/Ethertype filtering is implemented and counting the dropped frames is a requirement, a dummy entry can be added to the MAC address filter table which allows all frames through. This will trigger a hit for every frame. Therefore the frames dropped due to VLAN/Ethertype filtering will be counted since there was a hit in the MAC address filter table.	0x0	R

MAC FRAME RECEIVED WITH IFG ERRORS REGISTER

OA-SPI Address: 0x00AE, MMS: 0x1, Reset: 0x00000000

The MAC_RX_IFG_ERR_CNT register indicates the number of received frames with IFG errors.

Table 233. Bit Descriptions for MAC_RX_IFG_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	RX_IFG_ERR_CNT	IFG error counter for received frames. The MAC_RX_IFG_ERR_CNT.RX_IFG_ERR_CNT bits indicate the number of frames that are received with IFG errors.	0x0	R

MAC TRANSMIT FRAME COUNT REGISTER

OA-SPI Address: 0x00B1, MMS: 0x1, Reset: 0x00000000

The MAC_TX_FRM_CNT register indicates the number of frames that are successfully transmitted.

Table 234. Bit Descriptions for MAC_TX_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_FRM_CNT	Transmit frame count. The MAC_TX_FRM_CNT.TX_FRM_CNT bits indicate the number of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmit OK.	0x0	R

MAC TRANSMIT BROADCAST FRAME COUNT REGISTER

OA-SPI Address: 0x00B2, MMS: 0x1, Reset: 0x00000000

The MAC_TX_BCAST_CNT register indicates the number of the frames that were successfully transmitted.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 235. Bit Descriptions for MAC_TX_BCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_BCAST_CNT	Transmit broadcast frame count. The MAC_TX_BCAST_CNT.TX_BCAST_CNT bits indicate the number of the frames that were successfully transmitted, as indicated by the TransmitStatus transmit OK, to the broadcast address. Frames transmitted to multicast addresses are not broadcast frames and are excluded.	0x0	R

MAC TRANSMIT MULTICAST FRAME COUNT REGISTER

OA-SPI Address: 0x00B3, MMS: 0x1, Reset: 0x00000000

The MAC_TX_MCAST_CNT register indicates the number of frames that are successfully transmitted.

Table 236. Bit Descriptions for MAC_TX_MCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_MCAST_CNT	Transmit multicast frame count. The MAC_TX_MCAST_CNT.TX_MCAST_CNT bits indicate the number of frames that are successfully transmitted, as indicated by the status value transmit OK, to a group destination address other than broadcast.	0x0	R

MAC TRANSMIT UNICAST FRAME COUNT REGISTER

OA-SPI Address: 0x00B4, MMS: 0x1, Reset: 0x00000000

The MAC_TX_UCAST_CNT register indicates the number of unicast frames that are successfully transmitted.

Table 237. Bit Descriptions for MAC_TX_UCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_UCAST_CNT	Transmit unicast frame count. The MAC_TX_UCAST_CNT.TX_UCAST_CNT bits indicate the number of frames that are successfully transmitted, as indicated by the status value transmit OK, to a unicast address.	0x0	R

MAC TRANSMIT SINGLE COLLISION COUNT REGISTER

OA-SPI Address: 0x00B5, MMS: 0x1, Reset: 0x00000000

The MAC_TX_SINGLE_COL_CNT register indicates the number of frames that are involved in a single collision and are subsequently transmitted successfully.

Note: ADIN1140 also increases this counter when the max collision retries for a frame has been reached.

Table 238. Bit Descriptions for MAC_TX_SINGLE_COL_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_SINGLE_COL_CNT	Transmit single collision frame count. The MAC_TX_SINGLE_COL_CNT.TX_SINGLE_COL_CNT bits indicate the number of frames that are involved in a single collision and are subsequently transmitted successfully. This counter is incremented when the result of a transmission is reported as transmit OK and the attempt is 2.	0x0	R

MAC TRANSMIT MULTIPLE COLLISION COUNT REGISTER

OA-SPI Address: 0x00B6, MMS: 0x1, Reset: 0x00000000

The MAC_TX_MULTIPLE_COL_CNT register indicates the number of frames that are involved in more than one collision and are subsequently transmitted successfully.

Note: ADIN1140 also increases this counter when the max collision retries for a frame has been reached.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 239. Bit Descriptions for MAC_TX_MULTIPLE_COL_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_MULTIPLE_COL_CNT	Transmit multiple collision frame count. The MAC_TX_MULTIPLE_COL_CNT.TX_MULTIPLE_COL_CNT bits indicate the number of frames that are involved in more than one collision and are subsequently transmitted successfully. This counter is incremented when the TransmitStatus is reported as transmit OK and the value of the attempts variable is greater than 2 and less or equal to attemptLimit.	0x0	R

MAC TRANSMIT DEFERRED TRANSMISSION COUNT REGISTER

OA-SPI Address: 0x00B7, MMS: 0x1, Reset: 0x00000000

The MAC_TX_DEFERRED_XMIT_CNT register indicates the number of frames whose transmission was delayed on its first attempt because the medium was busy.

Table 240. Bit Descriptions for MAC_TX_DEFERRED_XMIT_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_DEFERRED_XMIT_CNT	Transmit deferred transmission frame count. As per the standard definition of this recommended counter, the MAC_TX_DEFERRED_XMIT_CNT.TX_DEFERRED_XMIT_CNT bits indicate the number of frames whose transmission was delayed on its first attempt because the medium was busy. This counter is incremented when the boolean variable deferred has been asserted by the TransmitLinkMgmt function (4.2.8). Frames involved in any collisions are not counted. **Note:** Although this counter should only increase if the medium was busy and the frame had no collisions, but ADIN1140 does not increase the counter for the above conditions and instead increases this counter when the max collision retries for a frame has been reached or when the frame transmission encounters a collision.	0x0	R

MAC TRANSMIT LATE COLLISION COUNT REGISTER

OA-SPI Address: 0x00B8, MMS: 0x1, Reset: 0x00000000

The MAC_TX_LATE_COL_CNT register indicates the number of the times that a collision has been detected later than 512 bit times into the transmitted packet.

Table 241. Bit Descriptions for MAC_TX_LATE_COL_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_LATE_COL_CNT	Transmit late collision frame count. The MAC_TX_LATE_COL_CNT.TX_LATE_COL_CNT bits indicate the number of the times that a collision has been detected later than 512 bit times into the transmitted packet. A late collision is counted twice, both as a collision and as a lateCollision. This counter is incremented when the lateCollisionCount variable is nonzero.	0x0	R

MAC TRANSMIT EXCESS COLLISION COUNT REGISTER

OA-SPI Address: 0x00B9, MMS: 0x1, Reset: 0x00000000

The MAC_TX_XSCOLS_CNT register indicates the number of the frames that, due to excessive collisions, are not transmitted successfully.

Table 242. Bit Descriptions for MAC_TX_XSCOLS_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_XSCOLS_CNT	Transmit excess collision frame count. The MAC_TX_XSCOLS_CNT.TX_XSCOLS_CNT bits indicate the number of frames that are not transmitted successfully due to excessive collisions. This counter is incremented when the value of the attempts variable equals attemptLimit during a transmission.	0x0	R

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

MAC TRANSMIT FRAMES DROPPED UNDER RUN REGISTER

OA-SPI Address: 0x00BA, MMS: 0x1, Reset: 0x00000000

The MAC_TX_UNR_CNT register indicates the number of frames that were dropped due to an under run.

Table 243. Bit Descriptions for MAC_TX_UNR_CNT

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:0]	TX_UNR_CNT	Transmit frame dropped under run. The MAC_TX_UNR_CNT.TX_UNR_CNT bits indicate the number of frames dropped due to a full receive FIFO.	0x0	R

MAC RECEIVE FIFO FRAME COUNT REGISTER

OA-SPI Address: 0x00BB, MMS: 0x1, Reset: 0x00000000

The MAC_HI_RFC register indicates the number of frames in the receive FIFO.

Table 244. Bit Descriptions for MAC_HI_RFC

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved.	0x0	R
[8:0]	RFC	Receive frame count. The MAC_HI_RFC.RFC bits indicate the number of frames in the receive FIFO and is provided for debug purposes. In store and forward the host software only needs to know that there is at least one frame available - RX_RDY.	0x0	R

MAC RECEIVE FIFO VALID HALF WORDS REGISTER

OA-SPI Address: 0x00BD, MMS: 0x1, Reset: 0x00000000

The MAC_HI_RXSIZE register indicates the number of valid half words (16 bit) in the high priority receive FIFO.

Table 245. Bit Descriptions for MAC_HI_RXSIZE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	RXSIZE	Data in receive FIFO. The MAC_HI_RXSIZE.RXSIZE bits indicate the data in the Rx FIFO. The value is reported in the number of 16-bit half words.	0x0	R

MAC TRANSMIT INTER FRAME GAP REGISTER

OA-SPI Address: 0x00C1, MMS: 0x1, Reset: 0x0000000B

The MAC_TX_IFG register is used to configure inter frame gaps.

Table 246. Bit Descriptions for MAC_TX_IFG

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:8]	TX_IFG_PART2	Inter frame gap part2. During the inter frame gap, this bitfield defines when the device stops checking for frames transmitted by other nodes. Is it calculated as (P1_TX_IFG_PART2 + 1) * 8 bit times, and it applied backwards from the end of the IFG. For example, if the IFG is 9.6us, and the above calculation results in a value of 3.2us, then the device will monitor the bus during the first 6.4us of the IFG (9.6 - 3.2 = 6.4). **Note:** This bit field can be written correctly, but readback will always returns 0.	0x0	R/W
[7:0]	TX_IFG	Inter frame gap transmit. This bitfield defines the inter frame gap (IFG) which is the minimum distance between frames. It is calculated as (P1_TX_IFG + 1) * 8 bit times.	0xB	R/W

MAC DUPLEX MODE REGISTER

OA-SPI Address: 0x00C2, MMS: 0x1, Reset: 0x00000010

The MAC_DUPLEX register is used to configure the duplex mode of the MAC interface.

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 247. Bit Descriptions for MAC_DUPLEX

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved.	0x0	R
[6:1]	TX_JAM_SIZE	Jam size. The MAC_DUPLEX.TX_JAM_SIZE bits are used to configure the size of the jam added after a collision. **Note:** This bit field can be written correctly, but readback will always returns 0.	0x8	R/W
0	RESERVED	Reserved.	0x0	R/W

MAX RETRY IN HALF DUPLEX REGISTER

OA-SPI Address: 0x00C3, MMS: 0x1, Reset: 0x0000000F

The MAC_MAX_RETRY register configures the number of retries the MAC performs after a collision.

Table 248. Bit Descriptions for MAC_MAX_RETRY

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
[3:0]	MAX_RETRY	Max retry after collision. The MAC_MAX_RETRY.MAX_RETRY bits configure the number of retries the MAC performs after a collision.	0xF	R/W

MAC LOOPBACK ENABLE REGISTER

OA-SPI Address: 0x00C4, MMS: 0x1, Reset: 0x00000000

The MAC_LOOP register is used to enable loopback in the interface.

Table 249. Bit Descriptions for MAC_LOOP

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	LOOPBACK_EN	MAC loopback enable. The MAC_LOOP.LOOPBACK_EN bit is used to enable loopback on the MII interface to the PHY. 0: Normal Operation - Loopback Disabled. 1: Loopback Enabled.	0x0	R/W

MAC CRC CHECK ENABLE ON RECEIVE REGISTER

OA-SPI Address: 0x00C5, MMS: 0x1, Reset: 0x00000001

The MAC_RX_CRC_EN register is used to enable CRC checking.

Table 250. Bit Descriptions for MAC_RX_CRC_EN

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	CRC_CHK_EN	CRC check on receive enable. The MAC_RX_CRC_EN.CRC_CHK_EN bits is used to enable CRC check on receive. 0: CRC is Not Checked on Receive. 1: CRC is Checked on Receive.	0x1	R/W

MAC RECEIVE INTER FRAME GAP REGISTER

OA-SPI Address: 0x00C6, MMS: 0x1, Reset: 0x0000000A

The MAC_RX_IFG register configures the minimum IFG for frames to be considered valid.

Table 251. Bit Descriptions for MAC_RX_IFG

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

Table 251. Bit Descriptions for MAC_RX_IFG (Continued)

Bits	Bit Name	Description	Reset	Access
[7:0]	RX_IFG	Inter frame gap. The MAC_RX_IFG.RX_IFG bits are used to configure the receive IFG. The receive MAC checks that the IFG is greater than this value x 8 bit times. If the received IFG is too small the MAC drops the received frame, asserts MAC_STATUS1.RX_IFG_ERR, and increases the MAC_RX_IFG_ERR_CNT counter.	0xA	R/W

MAC MAX RECEIVE FRAME LENGTH REGISTER

OA-SPI Address: 0x00C7, MMS: 0x1, Reset: 0x00000618

The MAC_RX_MAX_LEN register is used to configure the maximum receive frame length in bytes.

Table 252. Bit Descriptions for MAC_RX_MAX_LEN

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	MAX_FRM_LEN	Max frame length on receive. The MAC_RX_MAX_LEN.MAX_FRM_LEN bits are used to configure the maximum receive frame length in bytes.	0x618	R/W

MAC MINIMUM RECEIVE FRAME LENGTH REGISTER

OA-SPI Address: 0x00C8, MMS: 0x1, Reset: 0x00000040

The MAC_RX_MIN_LEN register is used to configure the minimum receive frame length in bytes.

Table 253. Bit Descriptions for MAC_RX_MIN_LEN

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	MIN_FRM_LEN	Min frame length on receive. The MAC_RX_MIN_LEN.MIN_FRM_LEN bits are used to configure the minimum receive frame length in bytes.	0x40	R/W

MAC VLAN IDENTIFIER FILTER TABLE REGISTER

OA-SPI Address: 0x00C9, MMS: 0x1, Reset: 0x00000000

The MAC_RXFILT_VID_TABLE register is used to configure and enable VLAN operation as described below.

Table 254. Bit Descriptions for MAC_RXFILT_VID_TABLE

Bits	Bit Name	Description	Reset	Access
31	RXFILT_VID_EN	VLAN identifier filtering enable. The MAC_RXFILT_VID_TABLE.RXFILT_VID_EN bit is used to enable the VLAN identifier based filtering for the IEEE 802.1Q tagged ENET frame to the host.	0x0	R/W
30	RXFILT_VID_RULE	VLAN identifier filter rule to entry table. The MAC_RXFILT_VID_TABLE.RXFILT_VID_RULE bits are used to configure the rule for the entries in the VID table to match and decide to forward or discard the ENET frame to the host or other port. 0 - ENET frames are only passed if the entries match any of the 2 entries in the table. All other ENET frames are discarded.ENET frames are discarded when the ENET frames does not have VID. 1 - ENET frames are only discarded if the entries match any of the 2 entries in the table. All other ENET frames are forwarded.ENET frames are forwarded when the ENET frames does not have VID.	0x0	R/W
[29:28]	RESERVED	Reserved.	0x0	R
[27:16]	RXFILT_VID_ENTRY2	VLAN filter identifier table entry 2. The MAC_RXFILT_VID_TABLE.RXFILT_VID_ENTRY2 bits are used to configure the second entry in the VLAN identifier table entries (two in total) to match and forward/discard the the IEEE 802.1Q tagged ENET frame to host.	0x0	R/W
[15:12]	RESERVED	Reserved.	0x0	R
[11:0]	RXFILT_VID_ENTRY1	VLAN filter identifier table entry 1. The MAC_RXFILT_VID_TABLE.RXFILT_VID_ENTRY1 bits are used to configure the first entry in the VLAN identifier table entries (two in total) to match and forward/discard the the IEEE 802.1Q tagged ENET frame to host.	0x0	R/W

MAC ETHERNET TYPE FILTER TABLE REGISTER

OA-SPI Address: 0x00CA, MMS: 0x1, Reset: 0x00000000

REGISTER DETAILS: HOST MAC INTERFACE REGISTER MAP (MAC)

The MAC_RXFILT_ETYPE_TABLE register is used to configure the filter types used to forward or discard Ethernet frames.

Table 255. Bit Descriptions for MAC_RXFILT_ETYPE_TABLE

Bits	Bit Name	Description	Reset	Access
[31:16]	RXFILT_ETYPE_ENTRY2	Ethernet type filter identifier table entry 2. The MAC_RXFILT_ETYPE_TABLE.RXFILT_ETYPE_ENTRY2 bits are used to configure the second entry of the two ENET type identifier table entries to match and to forward or discard the ENET frame to host.	0x0	R/W
[15:0]	RXFILT_ETYPE_ENTRY1	Ethernet type filter identifier table entry 1. The MAC_RXFILT_ETYPE_TABLE.RXFILT_ETYPE_ENTRY1 bits are used to configure the first entry of the two ENET type identifier table entries to match and to forward or discard the ENET frame to host.	0x0	R/W

MAC ETHERNET TYPER FILTER TABLE CONTROL REGISTER

OA-SPI Address: 0x00CB, MMS: 0x1, Reset: 0x00000000

The MAC_RXFILT_ETYPE_CNRL register is used to define the rule for two entries and enable the Ethernet type filter.

Table 256. Bit Descriptions for MAC_RXFILT_ETYPE_CNRL

Bits	Bit Name	Description	Reset	Access
31	RXFILT_ETYPE_EN	Ethernet type based filtering enable. The MAC_RXFILT_ETYPE_CNRL.RXFILT_ETYPE_EN bit is used to enable the ENET type based filtering for all the received ENET frames.	0x0	R/W
30	RXFILT_ETYPE_RULE	Ethernet type filter rule to entry table. The MAC_RXFILT_ETYPE_CNRL.RXFILT_ETYPE_RULE bit is used to configure the rule for the entries in the ETYPE table to match and decide to forward or discard the ENET frame to the host or other port. 0 - ENET frames are only passed if the entries match any of the 2 entries in the table. All other ENET frames are discarded. 1 - ENET frames are only discarded if the entries match any of the 2 entries in the table. All other ENET frames are forwarded. 0: Pass on match. ENET frames are only passed if the entries match any of the 2 entries in the table. All other ENET frames are discarded. 1: Discard on match. ENET frames are only discarded if the entries match any of the 2 entries in the table. All other ENET frames are forwarded.	0x0	R/W
[29:0]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY: PMD TRANSCEIVER REGISTER MAP (PMD)

Table 257. PMD Register Summary

Address	Name	Description	Reset	Access
0xD200	PMD_MIIMCTL	Media-Independent Interface Control Register.	0x0000	R/W
0xD202	PMD_PHYIDH	PHY Identifier Upper Bits Register.	0x0000	R
0xD203	PMD_PHYIDL	PHY Identifier Lower Bits Register.	0x0000	R
0xD210	PMD_PMDCTL	Physical Medium Device Control Register.	0x0000	R/W
0xD211	PMD_VS_CTRL	PMD Reset Control Register.	0x0000	R/W

REGISTER DETAILS: PMD TRANSCEIVER REGISTER MAP (PMD)

MEDIA-INDEPENDENT INTERFACE CONTROL REGISTER

OA-SPI Address: 0xD200, MMS: 0xA, Reset: 0x0000

The PMD_MIIMCTL register is used to enable loopback and to reset the interface.

Table 258. Bit Descriptions for PMD_MIIMCTL

Bits	Bit Name	Description	Reset	Access
15	RESET	Reset MII. The PMD_MIIMCTL.RESET bit is used to reset the block and its associated register map controls. The bit is only effective when Physical Medium Device (PMD) is not (or is no longer) in CONFIGURATION mode. This bit clears automatically when the reset is applied internally. 0: Inactive. 1: Trigger.	0x0	R/W
14	LOOPBACK	Loopback enable. The PMD_MIIMCTL.LOOPBACK bit is used to to enable a digital loopback while not transmitting on the cable. 0: Disabled. 1: Enabled.	0x0	R/W
[13:0]	RESERVED	Reserved.	0x0	R

PHY IDENTIFIER UPPER BITS REGISTER

OA-SPI Address: 0xD202, MMS: 0xA, Reset: 0x0000

The PMD_PHYIDH register provides upper bits of the ID of the PHY.

Table 259. Bit Descriptions for PMD_PHYIDH

Bits	Bit Name	Description	Reset	Access
[15:0]	PHYID[31:16]	PHY identifier. The PMD_PHYIDH.PHYID bits provide the ID of the PHY interface.	0x0	R

PHY IDENTIFIER LOWER BITS REGISTER

OA-SPI Address: 0xD203, MMS: 0xA, Reset: 0x0000

The PMD_PHYIDL register provides lower bits of the ID of the PHY.

Table 260. Bit Descriptions for PMD_PHYIDL

Bits	Bit Name	Description	Reset	Access
[15:0]	PHYID[15:0]	PHY identifier. The PMD_PHYIDH.PHYID bits provide the ID of the PHY interface.	0x0	R

PHYSICAL MEDIUM DEVICE CONTROL REGISTER

OA-SPI Address: 0xD210, MMS: 0xA, Reset: 0x0000

The PMD_PMDCTL register provides control and status for the PMD.

Table 261. Bit Descriptions for PMD_PMDCTL

Bits	Bit Name	Description	Reset	Access
15	FDCAP	Full-duplex capability. The PMD_PMDCTL.FDCAP bit indicates the full-duplex status of the PMD.	0x0	R
14	HDCAP	Half-duplex capability. The PMD_PMDCTL.HDCAP bit indicates the half-duplex status of the PMD.	0x0	R
[13:2]	RESERVED	Reserved.	0x0	R
1	TPREFN	Topology discovery mode. The PMD_PMDCTL.TPREFN bit is used to configure topology discovery mode as a reference node or a measured node. 0: Measure node. 1: Reference node.	0x0	R/W
0	TPEN	Topology discovery enable. The PMD_PMDCTL.TPEN bit is used to enable topology discovery. 0: Disabled. 1: Enabled.	0x0	R/W

REGISTER DETAILS: PMD TRANSCEIVER REGISTER MAP (PMD)

PMD RESET CONTROL REGISTER

OA-SPI Address: 0xD211, MMS: 0xA, Reset: 0x0000

The PMD_VS_CTRL register is used to reset all RW bits in the PMD register map (for initialization purposes).

Table 262. Bit Descriptions for PMD_VS_CTRL

Bits	Bit Name	Description	Reset	Access
15	REGMAP_CLEAR	Reset all RW bits. The PMD_VS_CTRL.REGMAP_CLEAR bit is used to reset all RW bits in the PMD register map (for initialization purposes) without affecting the PMD state machine. The effect of the reset is immediate. This is a self-clearing bit. 0: Inactive. 1: Trigger.	0x0	R/W
[14:0]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

Table 263. PHY_OA Register Summary

Address	Name	Description	Reset	Access
0x0000	PHY_OA_TWEAKS_1	PHY Tweaks 1 Register.	0x00C0	R/W
0x0003	PHY_OA_MANUAL_CTRL_REG_1	PHY Manual Control 1 Register.	0x0000	R/W
0x000F	PHY_OA_PLCA_EXT	PHY PLCA Ext Register.	0x0800	R/W
0x0018	PHY_OA_PLCA_CTRL2	PHY PLCA Control 2 Register.	0xFFFF	R/W
0x0019	PHY_OA_PLCA_CTRL3	PHY PLCA Control 3 Register.	0xFFFF	R/W
0x001A	PHY_OA_PLCA_CTRL4	PHY PLCA Control 4 Register.	0xFFFF	R/W
0x001B	PHY_OA_PLCA_CTRL5	PHY PLCA Control 5 Register.	0x01FF	R/W
0x0021	PHY_OA_PLCA_LUT_DBG	PHY_OA PLCA LUT Readback Register	0x0000	R
0x0061	PHY_OA_TD_VS_REG1	PHY Topology Discovery Timer Register.	0x0000	R/W
0x008A	PHY_OA_DCQ_JM_CFG0	PHY Jitter Monitor Configuration 0 Register.	0xFF01	R/W
0x008B	PHY_OA_DCQ_JM_CFG1	PHY Jitter Monitor Configuration 1 Register.	0x0002	R/W
0x008C	PHY_OA_DCQ_JM_CFG2	PHY Jitter Monitor Configuration 2 Register.	0xFFFF	R/W
0x008D	PHY_OA_DCQ_JM_CFG3	PHY Jitter Monitor Configuration 3 Register.	0xFFFF	R/W
0x008E	PHY_OA_DCQ_JM_CFG4	PHY Jitter Monitor Configuration 4 Register.	0x0000	R/W
0x008F	PHY_OA_DCQ_JM_CFG5	PHY Jitter Monitor Configuration 5 Register.	0x0000	R/W
0x0093	PHY_OA_DCQ_JM_RB0	PHY Jitter Monitor Readback 1 Register.	0x0000	R
0x0097	PHY_OA_DCQ_JM_RB4	PHY Jitter Monitor Readback 4 Register.	0x0000	R
0x0098	PHY_OA_DCQ_JM_RB5	PHY Jitter Monitor Readback 5 Register.	0x0000	R
0xCA00	PHY_OA_PLCA_IDVER	PHY PLCA ID Version Register.	0x0A10	R
0xCA01	PHY_OA_PLCA_CTRL0	PHY PLCA Control 0 Register.	0x0000	R/W
0xCA02	PHY_OA_PLCA_CTRL1	PHY PLCA Control 1 Register.	0x08FF	R/W
0xCA03	PHY_OA_PLCA_STATUS	PHY PLCA Status Register.	0x0000	R
0xCA04	PHY_OA_PLCA_TOTMR	PHY PLCA Duration of Transmit Opportunity Register.	0x0020	R/W
0xCA05	PHY_OA_PLCA_BURST	PHY PLCA Burst Register.	0x0080	R/W
0xCA06	PHY_OA_PLCA_DIAG	PHY PLCA Diagnostics Register.	0x0000	R/W
0xCE00	PHY_OA_TD_CTRL	PHY Topology Discovery Control Register.	0x0000	R/W
0xCE01	PHY_OA_TD_STAT	PHY Topology Discovery Status Register.	0x0000	R
0xCE02	PHY_OA_TD_DIST_RES_LOW	PHY Topology Discovery Destination Result Low Register.	0x0000	R
0xCE03	PHY_OA_TD_DIST_RES_UP	PHY Topology Discovery Destination Result Pulses Received Register.	0x0000	R
0xCE04	PHY_OA_TD_DLY_RES_LOW	PHY Topology Discovery Internal Delay Register.	0x0000	R
0xCE05	PHY_OA_TD_DLY_RES_UP	PHY Topology Discovery Internal Delay Receive Pulses Register.	0x0000	R
0xCE06	PHY_OA_TD_MNDLY_RES_LOW	PHY Topology Discovery Remote Node Internal Delay Measurement Low Register.	0x0000	R
0xCE07	PHY_OA_TD_MNDLY_RES_UP	PHY Topology Discovery Remote Node Internal Delay Measurement High Register.	0x0000	R
0xCE08	PHY_OA_TD_MNDLY_DUR	PHY Topology Discovery Internal Delay Duration Measurement Register.	0x0000	R
0xD000	PHY_OA_WS_STATUS	PHY Sleep/Wake Status Register.	0x8000	R
0xD001	PHY_OA_WS_CTRL	PHY Sleep/Wake Control Register.	0x0000	R/W

REGISTER DETAILS: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

PHY TWEAKS 1 REGISTER

OA-SPI Address: 0x0000, MMS: 0x4, Reset: 0x00C0

The PHY_OA_TWEAKS_1 register is used to configure the PHY interface as described below.

Table 264. Bit Descriptions for PHY_OA_TWEAKS_1

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R/W
12	TXC_AUTO_RESET_CMD_ON_STUCK_RX_ED_DIS	Automatic reset. The PHY_OA_TWEAKS_1.TXC_AUTO_RESET_CMD_ON_STUCK_RX_ED_DIS bit is used to automatically send reset commands to the 3-pin interface on the other die, if the Rx/ED pins are detected as static (with ED=1) for 1 us. 0: Send Resets When Required. 1: Never Send Resets.	0x0	R/W
11	RESERVED	Reserved.	0x0	R/W
10	NO_COL_COUNT	Disable collision detection. The PHY_OA_TWEAKS_1.NO_COL_COUNT bit is used to disable collision detection counting in PLCA mode. 0: Collision detection counting enabled. 1: Collision detection counting disabled.	0x0	R/W
[9:0]	RESERVED	Reserved.	0xC0	R/W

PHY MANUAL CONTROL 1 REGISTER

OA-SPI Address: 0x0003, MMS: 0x4, Reset: 0x0000

The PHY_OA_MANUAL_CTRL_REG_1 register is used to power down interface components.

Table 265. Bit Descriptions for PHY_OA_MANUAL_CTRL_REG_1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	PD_XTAL_BUFFER	XTAL buffer power down. The PHY_OA_MANUAL_CTRL_REG_1.PD_XTAL_BUFFER bit is used to power down the XTAL buffer. 0: Power down disabled. 1: Power down enabled.	0x0	R/W
9	PD_DLL	DLL power down. The PHY_OA_MANUAL_CTRL_REG_1.PD_DLL bit is used to power down the DLL. 0: Power down disabled. 1: Power down enabled.	0x0	R/W
[8:0]	RESERVED	Reserved.	0x0	R

PHY PLCA EXT REGISTER

OA-SPI Address: 0x000F, MMS: 0x4, Reset: 0x0800

The PHY_OA_PLCA_EXT register is used to configure the PLCA interface as described below.

Table 266. Bit Descriptions for PHY_OA_PLCA_EXT

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
12	PLCAPRECEN	Precedence mode enable. The PHY_OA_PLCA_EXT.PLCAPRECEN bit is used to enable the PLCA precedence mode feature. 0: Disable. 1: Enable.	0x0	R/W
[11:2]	RESERVED	Reserved.	0x200	R/W
1	PLCALEADEREN	Leader node alternate. The PHY_OA_PLCA_EXT.PLCALEADEREN bit is used to select a node with an ID other than 0 as the PLCA leader.	0x0	R/W

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Table 266. Bit Descriptions for PHY_OA_PLCA_EXT (Continued)

Bits	Bit Name	Description	Reset	Access
		0: Disable. 1: Enable.		
0	PLCALEADER	PLCA leader select. The PHY_OA_PLCA_EXT.PLCALEADER bit is used to select the node as PLCA leader despite the value of its assigned node ID. 0: Not PLCA leader. 1: PLCA leader.	0x0	R/W

PHY PLCA CONTROL 2 REGISTER

OA-SPI Address: 0x0018, MMS: 0x4, Reset: 0xFFFF

The PHY_OA_PLCA_CTRL2 register register holds the multiple PLCA IDs.

Table 267. Bit Descriptions for PHY_OA_PLCA_CTRL2

Bits	Bit Name	Description	Reset	Access
[15:8]	PLCALOCALID2	PLCA Local ID2. If PHY_OA_PLCA_CTRL5.PLCALOCALID_EN is configured for this ID, the PHY_OA_PLCA_CTRL2.PLCALOCALID2 bits are used to provide the node with a 2nd unique PLCA ID.	0xFF	R/W
[7:0]	PLCALOCALID1	PLCA Local ID1. If PHY_OA_PLCA_CTRL5.PLCALOCALID_EN is configured for this ID, the PHY_OA_PLCA_CTRL2.PLCALOCALID1 bits are used to provide the node with a unique PLCA ID.	0xFF	R/W

PHY PLCA CONTROL 3 REGISTER

OA-SPI Address: 0x0019, MMS: 0x4, Reset: 0xFFFF

The PHY_OA_PLCA_CTRL3 register holds the multiple PLCA IDs.

Table 268. Bit Descriptions for PHY_OA_PLCA_CTRL3

Bits	Bit Name	Description	Reset	Access
[15:8]	PLCALOCALID4	PLCA Local ID4. If PHY_OA_PLCA_CTRL5.PLCALOCALID_EN is configured for this ID, the PHY_OA_PLCA_CTRL3.PLCALOCALID4 bits are used to provide the node with a 4th unique PLCA ID.	0xFF	R/W
[7:0]	PLCALOCALID3	PLCA Local ID3. If PHY_OA_PLCA_CTRL5.PLCALOCALID_EN is configured for this ID, the PHY_OA_PLCA_CTRL3.PLCALOCALID3 bits are used to provide the node with a 3rd unique PLCA ID.	0xFF	R/W

PHY PLCA CONTROL 4 REGISTER

OA-SPI Address: 0x001A, MMS: 0x4, Reset: 0xFFFF

The PHY_OA_PLCA_CTRL4 register register holds the multiple PLCA IDs.

Table 269. Bit Descriptions for PHY_OA_PLCA_CTRL4

Bits	Bit Name	Description	Reset	Access
[15:8]	PLCALOCALID6	PLCA Local ID6. If PHY_OA_PLCA_CTRL5.PLCALOCALID_EN is configured for this ID, the PHY_OA_PLCA_CTRL4.PLCALOCALID6 bits are used to provide the node with a 6th unique PLCA ID.	0xFF	R/W
[7:0]	PLCALOCALID5	PLCA Local ID5. If PHY_OA_PLCA_CTRL5.PLCALOCALID_EN is configured for this ID, the PHY_OA_PLCA_CTRL4.PLCALOCALID5 bits are used to provide the node with a 5th unique PLCA ID.	0xFF	R/W

PHY PLCA CONTROL 5 REGISTER

OA-SPI Address: 0x001B, MMS: 0x4, Reset: 0x01FF

The PHY_OA_PLCA_CTRL5 register is used to enable multiple PLCA IDs.

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Table 270. Bit Descriptions for PHY_OA_PLCA_CTRL5

Bits	Bit Name	Description	Reset	Access
[15:8]	PLCALOCALID_EN	PLCA multiple node enable. The PHY_OA_PLCA_CTRL5.PLCALOCALID_EN bits are used to enable the additional nodes that are configured in the control registers. 8: Enable The PLCA ID Specified by plcaLocalID. 9: Enable The PLCA ID Specified by plcaLocalID1. 10: Enable The PLCA ID Specified by plcaLocalID2. 11: Enable The PLCA ID Specified by plcaLocalID3. 12: Enable The PLCA ID Specified by plcaLocalID4. 13: Enable The PLCA ID Specified by plcaLocalID5. 14: Enable The PLCA ID Specified by plcaLocalID6. 15: Enable The PLCA ID Specified by plcaLocalID7.	0x1	R/W
[7:0]	PLCALOCALID7	PLCA Local ID7. If PHY_OA_PLCA_CTRL5.PLCALOCALID_EN is configured for this ID, the PHY_OA_PLCA_CTRL5.PLCALOCALID7 bits are used to provide the node with a 7th unique PLCA ID.	0xFF	R/W

PLCA LUT READBACK REGISTER

OA-SPI Address: 0x0021, MMS: 0x4, Reset: 0x0000

Table 271. Bit Descriptions for PHY_OA_PLCA_LUT_DBG

Bits	Bit Name	Description	Reset	Access
15	RB_EFFECTIVE_PLCA_EN	Effective PLCA En value. The PHY_OA_PLCA_LUT_DBG.RB_EFFECTIVE_PLCA_EN bit is used to indicate the effective PLCA En value, considering that PLCA cannot be started while in the middle of receiving a frame.	0x1	R
[7:0]	RB_EFFECTIVE_PLCA_ID0	Effective PLCA ID. The PHY_OA_PLCA_LUT_DBG.RB_EFFECTIVE_PLCA_ID0 bits are used to indicate the effective PLCA ID0 value, considering whether the PLCA LUT was enabled and which code was selected based on the interface pins.	0xFF	R

PHY TOPOLOGY DISCOVERY TIMER REGISTER

OA-SPI Address: 0x0061, MMS: 0x4, Reset: 0x0000

The PHY_OA_TD_VS_REG1 register is used to disable the TD_DM_TO hardware timer, and instead rely on SW control of a (longer) timer.

Table 272. Bit Descriptions for PHY_OA_TD_VS_REG1

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	TD_DM_TO_DIS	Disable the TD_DM_TO timer. The PHY_OA_TD_VS_REG1.TD_DM_TO_DIS bit is used to disable the TD_DM_TO hardware timer, and instead rely on SW control of a (longer) timer. In this case the timeout abort is executed by SW bringing the TX_EN signal low. 0: Internal time out to complete measurement in 1s is enabled. 1: No internal timeout, the TD_EN bit needs to be written to exit Topology Discovery mode.	0x0	R/W

PHY JITTER MONITOR CONFIGURATION 0 REGISTER

OA-SPI Address: 0x008A, MMS: 0x4, Reset: 0xFF01

The PHY_OA_DCQ_JM_CFG0 register is used to configure and enable jitter monitoring.

Table 273. Bit Descriptions for PHY_OA_DCQ_JM_CFG0

Bits	Bit Name	Description	Reset	Access
[15:8]	CFG_JM_PLCA_ID_SEL	Jitter monitor ID. The PHY_OA_DCQ_JM_CFG0.CFG_JM_PLCA_ID_SEL bits is used to configure which PLCA transmit opportunity ID to monitor. The value 0xFF monitors all IDs.	0xFF	R/W
[7:2]	RESERVED	Reserved.	0x0	R/W

REGISTER DETAILS: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

Table 273. Bit Descriptions for PHY_OA_DCQ_JM_CFG0 (Continued)

Bits	Bit Name	Description	Reset	Access
1	CFG_JM_PAUSE	Pauses updates of readback. The PHY_OA_DCQ_JM_CFG0.CFG_JM_PAUSE bit is used to pause updates of readback data while active. 0: Disable. 1: Enable.	0x0	R/W
0	CFG_JM_EN	Jitter monitor enable. The PHY_OA_DCQ_JM_CFG0.CFG_JM_EN bit is used to enable the jitter monitor feature. 0: Disable. 1: Enable.	0x1	R/W

PHY JITTER MONITOR CONFIGURATION 1 REGISTER

OA-SPI Address: 0x008B, MMS: 0x4, Reset: 0x0002

The PHY_OA_DCQ_JM_CFG1 register is used to configure the number of packets that need to be received from enable to flag out_settled.

Table 274. Bit Descriptions for PHY_OA_DCQ_JM_CFG1

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
[1:0]	CFG_JM_SETTLED_RANGE_SEL	Jitter monitor - Selects the number of packets that need to be received from enable to flag out_settled. The PHY_OA_DCQ_JM_CFG1.CFG_JM_SETTLED_RANGE_SEL bits are used to configure the number of packets that need to be received from enable to flag out_settled. 00: Integrator will be settled once it has reached the maximum shift, after 16K frames. 01: Integrator will be settled once it has reached the maximum shift (16K frames) plus additional frames until reaching a total of 60K frames. 10: Integrator will be settled once it has reached the maximum shift (16K frames) plus additional frames until reaching a total of 80K frames. 11: Integrator will be settled once it has reached the maximum shift (16K frames) plus additional frames until reaching a total of 100K frames.	0x2	R/W

PHY JITTER MONITOR CONFIGURATION 2 REGISTER

OA-SPI Address: 0x008C, MMS: 0x4, Reset: 0xFFFF

The PHY_OA_DCQ_JM_CFG2 register is used to configure the threshold for low-to-mid level on combined metric.

Table 275. Bit Descriptions for PHY_OA_DCQ_JM_CFG2

Bits	Bit Name	Description	Reset	Access
[15:0]	CFG_JM_TH_LOW_MID_ERR	Jitter low-to-mid level. The PHY_OA_DCQ_JM_CFG2.CFG_JM_TH_LOW_MID_ERR bits are used to configure the threshold for low-to-mid level on combined metric.	0xFFFF	R/W

PHY JITTER MONITOR CONFIGURATION 3 REGISTER

OA-SPI Address: 0x008D, MMS: 0x4, Reset: 0xFFFF

The PHY_OA_DCQ_JM_CFG3 register is used to configure the threshold for mid-to-high level on combined metric.

Table 276. Bit Descriptions for PHY_OA_DCQ_JM_CFG3

Bits	Bit Name	Description	Reset	Access
[15:0]	CFG_JM_TH_MID_HIGH_ERR	Jitter monitor - Threshold for mid-to-high level on combined metric. The PHY_OA_DCQ_JM_CFG3.CFG_JM_TH_MID_HIGH_ERR bits are used to configure the threshold for mid-to-high level on combined metric.	0xFFFF	R/W

REGISTER DETAILS: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

PHY JITTER MONITOR CONFIGURATION 4 REGISTER

OA-SPI Address: 0x008E, MMS: 0x4, Reset: 0x0000

The PHY_OA_DCQ_JM_CFG4 register is used to configure the threshold for high-to-mid level on combined metric.

Table 277. Bit Descriptions for PHY_OA_DCQ_JM_CFG4

Bits	Bit Name	Description	Reset	Access
[15:0]	CFG_JM_TH_HIGH_MID_ERR	Jitter monitor - Threshold for high-to-mid level on combined metric. The PHY_OA_DCQ_JM_CFG4.CFG_JM_TH_HIGH_MID_ERR bits are used to configure the threshold for high-to-mid level on combined metric.	0x0	R/W

PHY JITTER MONITOR CONFIGURATION 5 REGISTER

OA-SPI Address: 0x008F, MMS: 0x4, Reset: 0x0000

The PHY_OA_DCQ_JM_CFG5 register is used to configure the threshold for mid-to-low level on combined metric.

Table 278. Bit Descriptions for PHY_OA_DCQ_JM_CFG5

Bits	Bit Name	Description	Reset	Access
[15:0]	CFG_JM_TH_MID_LOW_ERR	Jitter monitor - Threshold for mid-to-low level on combined metric. The PHY_OA_DCQ_JM_CFG5.CFG_JM_TH_MID_LOW_ERR bits are used to configure the threshold for mid-to-low level on combined metric.	0x0	R/W

PHY JITTER MONITOR READBACK 1 REGISTER

OA-SPI Address: 0x0093, MMS: 0x4, Reset: 0x0000

The PHY_OA_DCQ_JM_RB0 register provides information on jitter monitor status.

Table 279. Bit Descriptions for PHY_OA_DCQ_JM_RB0

Bits	Bit Name	Description	Reset	Access
15	RB_JM_OUT_SETTLED	Readback stable. The PHY_OA_DCQ_JM_RB0.RB_JM_OUT_SETTLED bit indicates when the metric read-backs are considered stable (and valid). 0: Metric readback not yet settled (integrator might have reached maximum shift but additional settling time not elapsed). 1: Metric readback considered settled (integrator has reached maximum shift and additional settling time has elapsed).	0x0	R
14	RB_JM_OUT_VALID	Readback valid. The PHY_OA_DCQ_JM_RB0.RB_JM_OUT_VALID bit indicates when the metric read-backs are valid (but could be unstable). 0: Metric read-backs not considered valid yet (integrator has not reached maximum shift). 1: Metric read-backs considered valid (integrator has reached maximum shift).	0x0	R
[13:0]	RESERVED	Reserved.	0x0	R

PHY JITTER MONITOR READBACK 4 REGISTER

OA-SPI Address: 0x0097, MMS: 0x4, Reset: 0x0000

The PHY_OA_DCQ_JM_RB4 register provides information on jitter monitor quality.

Table 280. Bit Descriptions for PHY_OA_DCQ_JM_RB4

Bits	Bit Name	Description	Reset	Access
[15:13]	RB_JM_QUALITY_INDEX	Jitter monitor Quality index. The PHY_OA_DCQ_JM_RB4.RB_JM_QUALITY_INDEX bits indicate Jitter monitor quality. 100: Lowest amount of error. Good. Green. 010: Medium amount of error. Warning. Yellow. 000: High amount of error. Bad. Red.	0x0	R
[12:0]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

PHY JITTER MONITOR READBACK 5 REGISTER

OA-SPI Address: 0x0098, MMS: 0x4, Reset: 0x0000

The PHY_OA_DCQ_JM_RB5 register indicates Jitter on a combined metric, normalized per frame length.

Table 281. Bit Descriptions for PHY_OA_DCQ_JM_RB5

Bits	Bit Name	Description	Reset	Access
[15:0]	RB_JM_COMB_METRIC	Jitter monitor combined metric. The PHY_OA_DCQ_JM_RB5.RB_JM_COMB_METRIC bits indicate the jitter metric on combined metric, normalized per frame length. Notation is fixed point 0.14 (divide this integer by 16384.0).	0x0	R

PHY PLCA ID VERSION REGISTER

OA-SPI Address: 0xCA00, MMS: 0x4, Reset: 0x0A11

The PHY_OA_PLCA_IDVER register provides information on the memory maps used with the interface.

Table 282. Bit Descriptions for PHY_OA_PLCA_IDVER

Bits	Bit Name	Description	Reset	Access
[15:8]	PLCAIDM	OA memory map compatibility version. The PHY_OA_PLCA_IDVER.PLCAIDM bits indicates the compatibility with the version of the OA memory map definition this layout adheres to.	0xA	R
[7:0]	PLCAVER	OA memory map version. The PHY_OA_PLCA_IDVER.PLCAVER bits indicates the version of the OA memory map definition this layout adheres to. **Note:** The PLCAVER reported value is incorrect, The ADIN1140 device supports **v1.3** specification.	0x11	R

PHY PLCA CONTROL 0 REGISTER

OA-SPI Address: 0xCA01, MMS: 0x4, Reset: 0x0000

The PHY_OA_PLCA_CTRL0 register is used to enable and reset the interface.

Table 283. Bit Descriptions for PHY_OA_PLCA_CTRL0

Bits	Bit Name	Description	Reset	Access
15	PLCAEN	PLCA enable. The PHY_OA_PLCA_CTRL0.PLCAEN is used to enable the PLCA interface. 0: Disabled. 1: Enabled.	0x0	R/W
14	PLCARST	PLCA reset. The PHY_OA_PLCA_CTRL0.PLCARST bit is used to reset PLCA interface. This is a self-clearing bit. 0: Inactive. 1: Trigger.	0x0	R/W
[13:0]	RESERVED	Reserved.	0x0	R

PHY PLCA CONTROL 1 REGISTER

OA-SPI Address: 0xCA02, MMS: 0x4, Reset: 0x08FF

The PHY_OA_PLCA_CTRL1 register is used to configure the number of nodes in the system and their IDs.

Table 284. Bit Descriptions for PHY_OA_PLCA_CTRL1

Bits	Bit Name	Description	Reset	Access
[15:8]	PLCANODECOUNT	PLCA node count. The PHY_OA_PLCA_CTRL1.PLCANODECOUNT bits are used to configure the number of nodes in the system.	0x8	R/W
[7:0]	PLCALOCALID	PLCA local ID. The PHY_OA_PLCA_CTRL1.PLCALOCALID bits are used to provide the local node with a unique ID. The node with ID = 0 is the PLCA coordinator.	0xFF	R/W

PHY PLCA STATUS REGISTER

OA-SPI Address: 0xCA03, MMS: 0x4, Reset: 0x0000

The PHY_OA_PLCA_STATUS register is used to indicate the status of the interface.

REGISTER DETAILS: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

Table 285. Bit Descriptions for PHY_OA_PLCA_STATUS

Bits	Bit Name	Description	Reset	Access
15	PLCASTATUS	PLCA status. The PHY_OA_PLCA_STATUS.PLCASTATUS bit is used to indicate line activity on the interface. 0: No PLCA activity on the line detected. 1: PLCA activity on the line detected.	0x0	R
[14:0]	RESERVED	Reserved.	0x0	R

PHY PLCA DURATION OF TRANSMIT OPPORTUNITY REGISTER

OA-SPI Address: 0xCA04, MMS: 0x4, Reset: 0x0020

The PHY_OA_PLCA_TOTMR register is used to configure the duration of the PLCA transmit opportunity.

Table 286. Bit Descriptions for PHY_OA_PLCA_TOTMR

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	PLCATOTIMER	Minimum duration of PLCA transmit. The PHY_OA_PLCA_TOTMR.PLCATOTIMER bit are used to configure the minimum duration of the PLCA transmit opportunity in units of Tbits. **Note:** The 2 LSBs of this field must remain at zero. If the 2 LSBs are set to any other value, the timer configurations will not be accurate due to quantization error.	0x20	R/W

PHY PLCA BURST REGISTER

OA-SPI Address: 0xCA05, MMS: 0x4, Reset: 0x0080

The PHY_OA_PLCA_BURST register is used to configure PLCA burst operations as described below.

Table 287. Bit Descriptions for PHY_OA_PLCA_BURST

Bits	Bit Name	Description	Reset	Access
[15:8]	PLCAMAXBURSTCNT	PLCA maximum burst count. The PHY_OA_PLCA_BURST.PLCAMAXBURSTCNT bits are used to configure the number of frames that a node can transmit in burst mode.	0x0	R/W
[7:0]	PLCABURSTTIMER	PLCA burst time. The PHY_OA_PLCA_BURST.PLCABURSTTIMER bits are used to configure the maximum time to wait for a new packet from the MAC after a successful transmission (100 ns units of time). **Note:** The 2 LSBs of this field must remain at zero. If the 2 LSBs are set to any other value, the timer configurations will not be accurate due to quantization error.	0x80	R/W

PHY PLCA DIAGNOSTICS REGISTER

OA-SPI Address: 0xCA06, MMS: 0x4, Reset: 0x0000

The PHY_OA_PLCA_DIAG register is used to report PLCA diagnostics.

Table 288. Bit Descriptions for PHY_OA_PLCA_DIAG

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	PLCADIAGRXINTO	Receive In transmit opportunity. The PHY_OA_PLCA_DIAG.PLCADIAGRXINTO bit is the PLCA diagnostic receive in transmit opportunity. 0: Not triggered. 1: Triggered.	0x0	R/W1C
1	PLCADIAGUNEXPB	Unexpected beacon. The PHY_OA_PLCA_DIAG.PLCADIAGUNEXPB bit is the PLCA diagnostic unexpected beacon. 0: Not triggered. 1: Triggered.	0x0	R/W1C
0	PLCADIAGBCNBFTO	Beacon before transmit. The PHY_OA_PLCA_DIAG.PLCADIAGBCNBFTO bit is the PLCA diagnostic beacon before transmit opportunity. 0: Not triggered.	0x0	R/W1C

REGISTER DETAILS: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

Table 288. Bit Descriptions for PHY_OA_PLCA_DIAG (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Triggered.		

PHY TOPOLOGY DISCOVERY CONTROL REGISTER

OA-SPI Address: 0xCE00, MMS: 0x4, Reset: 0x0000

The PHY_OA_TD_CTRL register is used to configure topology discovery in the PHY interface.

Table 289. Bit Descriptions for PHY_OA_TD_CTRL

Bits	Bit Name	Description	Reset	Access
15	TD_EN	Main topology discovery enable. The PHY_OA_TD_CTRL.TD_EN bit is used to enable the main topology discovery. The topology discovery takes over the transmit path while disabling it for data frames. 0: Disabled. 1: Enabled.	0x0	R/W
14	TD_REFN	Node type. The PHY_OA_TD_CTRL.TD_REFN bit is used with topology discovery to define which type of node this is. 0: Measured node. 1: Reference node.	0x0	R/W
13	TD_DLYM_START	Delay measurement. The PHY_OA_TD_CTRL.TD_DLYM_START bit is used to run the internal delay measurement step. 0: Inactive. 1: Trigger.	0x0	R/W
[12:9]	TD_DM_DUR	Duration of measurement. The PHY_OA_TD_CTRL.TD_DM_DUR bits are used to set the duration of measurement in ms (0 = 1ms).	0x0	R/W
8	TD_DM_START	Run distance measurement. The PHY_OA_TD_CTRL.TD_DM_START bit is used to run the distance measurement step. 0: Inactive. 1: Trigger.	0x0	R/W
7	TD_AUTO_START	Run automatic flow. The PHY_OA_TD_CTRL.TD_AUTO_START bit is used to start the automatic TD flow. 0: Inactive. 1: Trigger.	0x0	R/W
[6:0]	RESERVED	Reserved.	0x0	R

PHY TOPOLOGY DISCOVERY STATUS REGISTER

OA-SPI Address: 0xCE01, MMS: 0x4, Reset: 0x0000

The PHY_OA_TD_STAT register is used to report topology discovery status in the PHY interface.

Table 290. Bit Descriptions for PHY_OA_TD_STAT

Bits	Bit Name	Description	Reset	Access
15	TD_DLYM_DONE	Internal delay measurement done. The PHY_OA_TD_STAT.TD_DLYM_DONE bit indicates the internal delay measurement is complete. 0: Not done or there were errors. 1: Done without errors.	0x0	R
14	TD_DLYM_ERR	Error in internal delay measurement. The PHY_OA_TD_STAT.TD_DLYM_ERR bit indicates an error in the internal delay measurement. 0: No errors. 1: Error detected.	0x0	R
13	TD_DM_DONE	Distance measurement done. The PHY_OA_TD_STAT.TD_DM_DONE bit indicates the distance measurement is complete. 0: Not done or there were errors.	0x0	R

REGISTER DETAILS: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

Table 290. Bit Descriptions for PHY_OA_TD_STAT (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Done without errors.		
12	TD_DM_ERR	Error in distance measurement. The PHY_OA_TD_STAT.TD_DM_ERR bit indicates an error in the distance measurement. 0: No errors. 1: Error detected.	0x0	R
11	TD_AUTO_ERR	Error in automatic flow. The PHY_OA_TD_STAT.TD_AUTO_ERR bit indicates an error in the automatic flow. 0: No errors. 1: Error detected.	0x0	R
[10:0]	RESERVED	Reserved.	0x0	R

PHY TOPOLOGY DISCOVERY DESTINATION RESULT LOW REGISTER

OA-SPI Address: 0xCE02, MMS: 0x4, Reset: 0x0000

The PHY_OA_TD_DIST_RES_LOW register reports the result of the distance measurement.

Table 291. Bit Descriptions for PHY_OA_TD_DIST_RES_LOW

Bits	Bit Name	Description	Reset	Access
[15:0]	TD_DIST_MR[15:0]	Result of distance measurement, pulses. The PHY_OA_TD_DIST_RES_LOW.TD_DIST_MR bits report the result of the distance measurement in number of pulses received.	0x0	R

PHY TOPOLOGY DISCOVERY DESTINATION RESULT PULSES RECEIVED REGISTER

OA-SPI Address: 0xCE03, MMS: 0x4, Reset: 0x0000

The PHY_OA_TD_DIST_RES_UP register reports the result of the distance measurement.

Table 292. Bit Descriptions for PHY_OA_TD_DIST_RES_UP

Bits	Bit Name	Description	Reset	Access
[15:0]	TD_DIST_MR[31:16]	Result of distance measurement, pulses. The PHY_OA_TD_DIST_RES_LOW.TD_DIST_MR bits report the result of the distance measurement in number of pulses received.	0x0	R

PHY TOPOLOGY DISCOVERY INTERNAL DELAY REGISTER

OA-SPI Address: 0xCE04, MMS: 0x4, Reset: 0x0000

The PHY_OA_TD_DLY_RES_LOW register reports the result of the internal delay measurement.

Table 293. Bit Descriptions for PHY_OA_TD_DLY_RES_LOW

Bits	Bit Name	Description	Reset	Access
[15:0]	TD_DLYM_MR[15:0]	Result of internal delay. The PHY_OA_TD_DLY_RES_LOW.TD_DLYM_MR bits report the result of the internal delay measurement in number of pulses received.	0x0	R

PHY TOPOLOGY DISCOVERY INTERNAL DELAY RECEIVE PULSES REGISTER

OA-SPI Address: 0xCE05, MMS: 0x4, Reset: 0x0000

The PHY_OA_TD_DLY_RES_UP register reports the result of the internal delay measurement.

Table 294. Bit Descriptions for PHY_OA_TD_DLY_RES_UP

Bits	Bit Name	Description	Reset	Access
[15:0]	TD_DLYM_MR[31:16]	Result of internal delay. The PHY_OA_TD_DLY_RES_LOW.TD_DLYM_MR bits report the result of the internal delay measurement in number of pulses received.	0x0	R

PHY TOPOLOGY DISCOVERY REMOTE NODE INTERNAL DELAY MEASUREMENT LOW REGISTER

OA-SPI Address: 0xCE06, MMS: 0x4, Reset: 0x0000

REGISTER DETAILS: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

The PHY_OA_TD_MNDLY_RES_LOW register reports the lower bits of the remote node's internal delay measurement in number of pulses.

Table 295. Bit Descriptions for PHY_OA_TD_MNDLY_RES_LOW

Bits	Bit Name	Description	Reset	Access
[15:0]	TD_REMOTE_DLYM_MR[15:0]	Result of remote node internal delay bits. The PHY_OA_TD_MNDLY_RES_LOW.TD_REMOTE_DLYM_MR bits report the result of the remote node's internal delay measurement in number of pulses received (auto mode).	0x0	R

PHY TOPOLOGY DISCOVERY REMOTE NODE INTERNAL DELAY MEASUREMENT HIGH REGISTER

OA-SPI Address: 0xCE07, MMS: 0x4, Reset: 0x0000

The PHY_OA_TD_MNDLY_RES_UP register reports the upper bits of the remote node's internal delay measurement in number of pulses.

Table 296. Bit Descriptions for PHY_OA_TD_MNDLY_RES_UP

Bits	Bit Name	Description	Reset	Access
[15:0]	TD_REMOTE_DLYM_MR[31:16]	Result of remote node internal delay bits. The PHY_OA_TD_MNDLY_RES_LOW.TD_REMOTE_DLYM_MR bits report the result of the remote node's internal delay measurement in number of pulses received (auto mode).	0x0	R

PHY TOPOLOGY DISCOVERY INTERNAL DELAY DURATION MEASUREMENT REGISTER

OA-SPI Address: 0xCE08, MMS: 0x4, Reset: 0x0000

The PHY_OA_TD_MNDLY_DUR register reports the estimated duration of the remote node's internal delay measurement.

Table 297. Bit Descriptions for PHY_OA_TD_MNDLY_DUR

Bits	Bit Name	Description	Reset	Access
[15:12]	TD_REMOTE_DLYM_DUR	Remote node internal delay measurement. The PHY_OA_TD_MNDLY_DUR.TD_REMOTE_DLYM_DUR bits report the estimated duration of the remote node's Internal delay measurement in ms (0 = 1ms) (auto mode).	0x0	R
[11:0]	RESERVED	Reserved.	0x0	R

PHY SLEEP/WAKE STATUS REGISTER

OA-SPI Address: 0xD000, MMS: 0x4, Reset: 0x8000

The PHY_OA_WS_STATUS register is used to report the sleep/wake status of the PHY interface.

Table 298. Bit Descriptions for PHY_OA_WS_STATUS

Bits	Bit Name	Description	Reset	Access
15	WS_LPCAP	PM client capability. The PHY_OA_WS_STATUS.WS_LPCAP bit indicates the status of the power management client. 0: No Power Manager Client supported. 1: The Power Manager Client is supported by the local PHY.	0x1	R
14	WS_LPFAIL	Sleep/wake low power entry request. The PHY_OA_WS_STATUS.WS_LPFAIL bit indicates the sleep/wake low power entry request status. This bit is cleared when a request to transition to LOW POWER is received. 0: No failure detected. 1: Error.	0x0	R
[13:0]	RESERVED	Reserved.	0x0	R

PHY SLEEP/WAKE CONTROL REGISTER

OA-SPI Address: 0xD001, MMS: 0x4, Reset: 0x0000

The PHY_OA_WS_CTRL register is used to configure PHY power as described below.

REGISTER DETAILS: 10BASE-T1S PHY OPEN ALLIANCE REGISTER MAP (PHY_OA)

Table 299. Bit Descriptions for PHY_OA_WS_CTRL

Bits	Bit Name	Description	Reset	Access
15	WS_LPREQ	Request sleep. The PHY_OA_WS_CTRL.WS_LPREQ bit is used to request a transition to low power on local node (go to sleep). This is a self-clearing bit. 0: Inactive. 1: Trigger.	0x0	R/W
14	WS_LPEXIT	Send wake-up. The PHY_OA_WS_CTRL.WS_LPEXIT bit is used to request a transition from low power on a network segment (send wake-up signal (WUS)). This is a self-clearing bit. 0: Inactive. 1: Trigger.	0x0	R/W
[13:0]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

Table 300. PHY_STD Register Summary

Address	Name	Description	Reset	Access
0x0005	PHY_STD_DEV_IN_PACKAGE_1_1	Device in Package 1 Register 1.	0x000B	R
0x0005	PHY_STD_DEV_IN_PACKAGE_3_1	Device in Package 3 Register 1.	0x000B	R
0x0006	PHY_STD_DEV_IN_PACKAGE_1_2	Device in Package 1 Register 2.	0x1000	R
0x0006	PHY_STD_DEV_IN_PACKAGE_3_2	Device in Package 3 Register 2.	0x1000	R
0x000B	PHY_STD_PMA_PMD_EXTENDED_ABILITY2	PHY Physical Medium Attachment Physical Medium Dependent Extended Ability2 Register.	0x0800	R
0x0032	PHY_STD_PMA_PMD_EXTENDED_ABILITY	PHY Physical Medium Attachment, Physical Medium Dependent Extended Ability Register.	0x0008	R
0x08F3	PHY_STD_PCS_CONTROL	PHY Physical Coding Sublayer Control Register.	0x0000	R/W
0x08F4	PHY_STD_PCS_STATUS	PHY Physical Coding Sublayer Status Register.	0x0000	R
0x08F5	PHY_STD_PCS_DIAGNOSTIC	PHY Physical Coding Sublayer Diagnostic Register.	0x0000	R
0x08F6	PHY_STD_PCS_DIAGNOSTIC_2	PHY Physical Coding Sublayer Diagnostic 2 Register.	0x0000	R
0x08F9	PHY_STD_T1S_PMA_CONTROL	PHY T1S Physical Medium Attachment Control Register.	0x0400	R/W
0x08FA	PHY_STD_T1S_PMA_STATUS	PHY T1S Physical Medium Attachment Status Register.	0x2E00	R
0x08FB	PHY_STD_T1S_TEST_MODE_CONTROL	PHY T1S Test Mode Control Register.	0x0000	R/W
0xFF00	PHY_STD_CONTROL_REGISTER	PHY Control Register.	0x1000	R/W
0xFF01	PHY_STD_STATUS_REGISTER	PHY Status Register.	0x082D	R
0xFF02	PHY_STD_PHY_IDENTIFIER_1	PHY Identifier 1 Register.	0x0283	R
0xFF03	PHY_STD_PHY_IDENTIFIER_2	PHY Identifier 2 Register.	0xBE00	R

REGISTER DETAILS: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

DEVICE IN PACKAGE 1 REGISTER 1

OA-SPI Address: 0x0005, MMS: 0x3, Reset: 0x000B

The PHY_STD_DEV_IN_PACKAGE_1_1 register provides information about the PHY in the transceiver.

Table 301. Bit Descriptions for PHY_STD_DEV_IN_PACKAGE_1_1

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	POWER_UNIT_PRESENT	Power unit in package. The PHY_STD_DEV_IN_PACKAGE_1_1.POWER_UNIT_PRESENT bit indicates that power unit is present in the package. 0: Not present. 1: Present.	0x0	R
12	OFDM_PRESENT	OFDM in package. The PHY_STD_DEV_IN_PACKAGE_1_1.OFDM_PRESENT bit indicates that OFDM is present in the package. 0: Not present. 1: Present.	0x0	R
[11:8]	SPMA_PRESENT	Separated PMA in package. The PHY_STD_DEV_IN_PACKAGE_1_1.SPMA_PRESENT bit indicates that separated PMA is present in the package.	0x0	R
7	AN_PRESENT	Auto negotiation in package. The PHY_STD_DEV_IN_PACKAGE_1_1.AN_PRESENT bit indicates that auto negotiation is present in the package. 0: Not present. 1: Present.	0x0	R
6	TC_PRESENT	TC in package. The PHY_STD_DEV_IN_PACKAGE_1_1.TC_PRESENT bit indicates that TC is present in the package. 0: Not supported. 1: Supported.	0x0	R
5	DTEXS_PRESENT	DTE XS in package. The PHY_STD_DEV_IN_PACKAGE_1_1.DTEXS_PRESENT bit indicates that DTE XS is present in the package. 0: Not present. 1: Present.	0x0	R
4	PHYXS_PRESENT	PHY XS in Package. The PHY_STD_DEV_IN_PACKAGE_1_1.PHYXS_PRESENT bit indicates that PHY XS is present in the package. 1: Not present. 0: Present.	0x0	R
3	PCSDEVINPKG	PCS in package. The PHY_STD_DEV_IN_PACKAGE_1_1.PCSDEVINPKG bit indicates that PCS is present in the package. 0: Not present. 1: Present.	0x1	R
2	WIS_PRESENT	WIS in package. The PHY_STD_DEV_IN_PACKAGE_1_1.WIS_PRESENT bit indicates that WIS is present in the package. 0: Not present. 1: Present.	0x0	R
1	PMADEVINPKG	PMA in package. The PHY_STD_DEV_IN_PACKAGE_1_1.PMADEVINPKG bit indicates that PMA is present in the package. 0: Not present. 1: Present.	0x1	R
0	C22DEVINPKG	Clause 22 registers in package. The PHY_STD_DEV_IN_PACKAGE_1_1.C22DEVINPKG bit indicates that clause 22 registers are present in the package. 0: Not present. 1: Present.	0x1	R

REGISTER DETAILS: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

DEVICE IN PACKAGE 3 REGISTER 1

OA-SPI Address: 0x0005, MMS: 0x2, Reset: 0x000B

The PHY_STD_DEV_IN_PACKAGE_3_1 register provides information about the PHY in the transceiver.

Table 302. Bit Descriptions for PHY_STD_DEV_IN_PACKAGE_3_1

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	POWER_UNIT_PRESENT_1	Power Unit in Package. The PHY_STD_DEV_IN_PACKAGE_3_1.POWER_UNIT_PRESENT_1 bit indicates that power unit is present in the package. 0: Not present. 1: Present.	0x0	R
12	OFDM_PRESENT_1	OFDM in Package. The PHY_STD_DEV_IN_PACKAGE_3_1.OFDM_PRESENT_1 bit indicates that OFDM is present in the package. 0: Not present. 1: Present.	0x0	R
[11:8]	SPMA_PRESENT_1	Separated PMA in Package. The PHY_STD_DEV_IN_PACKAGE_3_1.SPMA_PRESENT_1 bit indicates that separated PMA is present in the package.	0x0	R
7	AN_PRESENT_1	Auto Negotiation in Package. The PHY_STD_DEV_IN_PACKAGE_3_1.AN_PRESENT_1 bit indicates that auto negotiation is present in the package. 0: Not present. 1: Present.	0x0	R
6	TC_PRESENT_1	TC in Package. The PHY_STD_DEV_IN_PACKAGE_3_1.TC_PRESENT_1 bit indicates that TC is present in the package. 0: Not present. 1: Present.	0x0	R
5	DTEXS_PRESENT_1	DTE XS in Package. The PHY_STD_DEV_IN_PACKAGE_3_1.DTEXS_PRESENT_1 bit indicates that DTE XS is present in the package. 0: Not present. 1: Present.	0x0	R
4	PHYXS_PRESENT_1	PHY XS in Package. The PHY_STD_DEV_IN_PACKAGE_3_1.PHYXS_PRESENT_1 bit indicates that PHY XS is present in the package. 0: Not present. 1: Present.	0x0	R
3	PCSDEVINPKG_1	PCS in package. The PHY_STD_DEV_IN_PACKAGE_3_1.PCSDEVINPKG_1 bit indicates that PCS is present in the package. 0: Not present. 1: Present.	0x1	R
2	WIS_PRESENT_1	WIS in Package. The PHY_STD_DEV_IN_PACKAGE_3_1.WIS_PRESENT_1 bit indicates that WIS is present in the package. 0: Not present. 1: Present.	0x0	R
1	PMADEVINPKG_1	PMA in package. The PHY_STD_DEV_IN_PACKAGE_3_1.PMADEVINPKG_1 bit indicates that PMA is present in the package. 0: Not present. 1: Present.	0x1	R
0	C22DEVINPKG_1	Clause 22 registers in package. The PHY_STD_DEV_IN_PACKAGE_3_1.C22DEVINPKG_1 bit indicates that clause 22 registers are present in the package. 0: Not present.	0x1	R

REGISTER DETAILS: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

Table 302. Bit Descriptions for PHY_STD_DEV_IN_PACKAGE_3_1 (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Present.		

DEVICE IN PACKAGE 1 REGISTER 2

OA-SPI Address: 0x0006, MMS: 0x3, Reset: 0x1000

The PHY_STD_DEV_IN_PACKAGE_1_2 register provides information about the PHY in the transceiver.

Table 303. Bit Descriptions for PHY_STD_DEV_IN_PACKAGE_1_2

Bits	Bit Name	Description	Reset	Access
15	VSD2_PRESENT	Vendor specific device 2 in package. The PHY_STD_DEV_IN_PACKAGE_1_2.VSD2_PRESENT bit indicates that vendor specific device 2 is present in the package. 0: Not present. 1: Present.	0x0	R
14	VSD1_PRESENT	Vendor specific device 1 in package. The PHY_STD_DEV_IN_PACKAGE_1_2.VSD1_PRESENT bit indicates that vendor specific device 1 is present in the package. 0: Not present. 1: Present.	0x0	R
13	CL22E_NOT_PRESENT	Clause 22 Extension not in package. The PHY_STD_DEV_IN_PACKAGE_1_2.CL22E_NOT_PRESENT bit indicates that clause 22 extension is not present in the package. 0: Not present. 1: Present.	0x0	R
12	PLCADEVINPKG	PLCA in package. The PHY_STD_DEV_IN_PACKAGE_1_2.PLCADEVINPKG bit indicates that PLCA is present in the package. 0: Not present. 1: Present.	0x1	R
[11:0]	RESERVED	Reserved.	0x0	R

DEVICE IN PACKAGE 3 REGISTER 2

OA-SPI Address: 0x0006, MMS: 0x2, Reset: 0x1000

The PHY_STD_DEV_IN_PACKAGE_3_2 register provides information about the PHY in the transceiver.

Table 304. Bit Descriptions for PHY_STD_DEV_IN_PACKAGE_3_2

Bits	Bit Name	Description	Reset	Access
15	VSD2_PRESENT_1	Vendor specific device 2 in package. The PHY_STD_DEV_IN_PACKAGE_3_2.VSD2_PRESENT_1 bit indicates that vendor specific device 2 is present in the package. 0: Not present. 1: Present.	0x0	R
14	VSD1_PRESENT_1	Vendor specific device 1 in package. The PHY_STD_DEV_IN_PACKAGE_3_2.VSD1_PRESENT_1 bit indicates that vendor specific device 1 is present in the package. 0: Not present. 1: Present.	0x0	R
13	CL22E_NOT_PRESENT_1	Clause 22 extension not in package. The PHY_STD_DEV_IN_PACKAGE_3_2.CL22E_NOT_PRESENT_1 bit indicates that clause 22 extension is not present in the package. 0: Not present. 1: Present.	0x0	R

REGISTER DETAILS: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

Table 304. Bit Descriptions for PHY_STD_DEV_IN_PACKAGE_3_2 (Continued)

Bits	Bit Name	Description	Reset	Access
12	PLCADEVINPKG_1	PLCA in package. The PHY_STD_DEV_IN_PACKAGE_3_2.PLCADEVINPKG_1 bit indicates that PLCA is present in the package. 0: Not present. 1: Present.	0x1	R
[11:0]	RESERVED	Reserved.	0x0	R

PHY PHYSICAL MEDIUM ATTACHMENT PHYSICAL MEDIUM DEPENDENT EXTENDED ABILITY2 REGISTER

OA-SPI Address: 0x000B, MMS: 0x3, Reset: 0x0800

The PHY_STD_PMA_PMD_EXTENDED_ABILITY2 register indicates the extended abilities of BASE T1S.

Table 305. Bit Descriptions for PHY_STD_PMA_PMD_EXTENDED_ABILITY2

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	PMAEXTAB10T1	Base-T1 Extended Abilities. The PHY_STD_PMA_PMD_EXTENDED_ABILITY2.PMAEXTAB10T1 bit indicates that the PHY supports BASE-T1 extended abilities. 0: Not supported. 1: Supported.	0x1	R
[10:0]	RESERVED	Reserved.	0x0	R

PHY PHYSICAL MEDIUM ATTACHMENT, PHYSICAL MEDIUM DEPENDENT EXTENDED ABILITY REGISTER

OA-SPI Address: 0x0032, MMS: 0x3, Reset: 0x0008

The PHY_STD_PMA_PMD_EXTENDED_ABILITY register provides information about the PHY in the transceiver.

Table 306. Bit Descriptions for PHY_STD_PMA_PMD_EXTENDED_ABILITY

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	PMAEXTAB10T1S	PHY Supports 10Base-T1S Capability. The PHY_STD_PMA_PMD_EXTENDED_ABILITY.PMAEXTAB10T1S bit indicates that the PHY supports 10BASE-T1S capability. 0: Not supported. 1: Supported.	0x1	R
2	PMAEXTAB10T1L	PHY Supports 10BASE-T1L Capability. The PHY_STD_PMA_PMD_EXTENDED_ABILITY.PMAEXTAB10T1L bit indicates that the PHY supports 10BASE-T1L capability. 0: Not supported. 1: Supported.	0x0	R
[1:0]	RESERVED	Reserved.	0x0	R

PHY PHYSICAL CODING SUBLAYER CONTROL REGISTER

OA-SPI Address: 0x08F3, MMS: 0x2, Reset: 0x0000

The PHY_STD_PCS_CONTROL register is used to configure the PHY PCS as described below.

Table 307. Bit Descriptions for PHY_STD_PCS_CONTROL

Bits	Bit Name	Description	Reset	Access
15	PCSRST	PCS and PMA layer reset. The PHY_STD_PCS_CONTROL.PCSRST bit resets the PCS and PMA layers. 0: Inactive.	0x0	W1

REGISTER DETAILS: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

Table 307. Bit Descriptions for PHY_STD_PCS_CONTROL (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Trigger.		
14	PCSLOOPBACK	PCS loop back mode enable. The PHY_STD_PCS_CONTROL.PCSLOOPBACK bit enables PCS loop back mode. 0: Disable. 1: Enable.	0x0	R/W
[13:0]	RESERVED	Reserved.	0x0	R

PHY PHYSICAL CODING SUBLAYER STATUS REGISTER

OA-SPI Address: 0x08F4, MMS: 0x2, Reset: 0x0000

The PHY_STD_PCS_STATUS register is used to indicate the PHY PCS status as described below.

Table 308. Bit Descriptions for PHY_STD_PCS_STATUS

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	JABDETECTED	Remote or local jabber detected. The PHY_STD_PCS_STATUS.JABDETECTED bit indicates that a remote or local jabber has been detected. 1: Detected. 0: Not detected.	0x0	R
[6:0]	RESERVED	Reserved.	0x0	R

PHY PHYSICAL CODING SUBLAYER DIAGNOSTIC REGISTER

OA-SPI Address: 0x08F5, MMS: 0x2, Reset: 0x0000

The PHY_STD_PCS_DIAGNOSTIC register is used to report diagnostics for the PHY PCS.

Table 309. Bit Descriptions for PHY_STD_PCS_DIAGNOSTIC

Bits	Bit Name	Description	Reset	Access
[15:0]	REMOTEJABCNT	Remote jabber error counter. The PHY_STD_PCS_DIAGNOSTIC.REMOTEJABCNT bits display the remote jabber error counter.	0x0	R

PHY PHYSICAL CODING SUBLAYER DIAGNOSTIC 2 REGISTER

OA-SPI Address: 0x08F6, MMS: 0x2, Reset: 0x0000

The PHY_STD_PCS_DIAGNOSTIC_2 register is used to report diagnostics for the PHY PCS.

Table 310. Bit Descriptions for PHY_STD_PCS_DIAGNOSTIC_2

Bits	Bit Name	Description	Reset	Access
[15:0]	CORRUPTEDTXCNT	Physical collision detected counter. The PHY_STD_PCS_DIAGNOSTIC_2.CORRUPTEDTXCNT bits display the physical collision detected counter.	0x0	R

PHY T1S PHYSICAL MEDIUM ATTACHMENT CONTROL REGISTER

OA-SPI Address: 0x08F9, MMS: 0x3, Reset: 0x0400

The PHY_STD_T1S_PMA_CONTROL register is used to configure the PHY interface PMA as described below.

Table 311. Bit Descriptions for PHY_STD_T1S_PMA_CONTROL

Bits	Bit Name	Description	Reset	Access
15	SRESET_1	PCS and PMA PHY Layer Reset. The PHY_STD_T1S_PMA_CONTROL.SRESET_1 bit is used to reset the PCS and PMA PHY layers. 0: Inactive. 1: Trigger.	0x0	R/W

REGISTER DETAILS: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

Table 311. Bit Descriptions for PHY_STD_T1S_PMA_CONTROL (Continued)

Bits	Bit Name	Description	Reset	Access
14	PMATXDISABLE	PMA transmission disable. The PHY_STD_T1S_PMA_CONTROL.PMATXDISABLE bit disables PMA transmission. 0: Disable. 1: Enable.	0x0	R/W
[13:12]	RESERVED	Reserved.	0x0	R
11	LOWPWRMODE_1	Low power mode enable. The PHY_STD_T1S_PMA_CONTROL.LOWPWRMODE_1 bit enables low power mode. 0: Disable. 1: Enable.	0x0	R
10	PMAMULTIDROP	Multi-drop mode enabled. The PHY_STD_T1S_PMA_CONTROL.PMAMULTIDROP bit enables multi-drop mode. 0: Disable. 1: Enable.	0x1	R
[9:1]	RESERVED	Reserved.	0x0	R
0	PMALOOPBACK_1	PMA loop back mode enable. The PHY_STD_T1S_PMA_CONTROL.PMALOOPBACK_1 bit enables loop back mode. 0: Disable. 1: Enable.	0x0	R/W

PHY T1S PHYSICAL MEDIUM ATTACHMENT STATUS REGISTER

OA-SPI Address: 0x08FA, MMS: 0x3, Reset: 0x2E00

The PHY_STD_T1S_PMA_STATUS register provides PHY PMA status information as described below.

Table 312. Bit Descriptions for PHY_STD_T1S_PMA_STATUS

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	PMALOOPBACKABIL	PMA loop back mode. The PHY_STD_T1S_PMA_STATUS.PMALOOPBACKABIL bit indicates that PMA loop back mode is supported. 0: Not supported. 1: Supported.	0x1	R
12	RESERVED	Reserved.	0x0	R
11	LOWPWRABILITY	Low power mode interface. The PHY_STD_T1S_PMA_STATUS.LOWPWRABILITY bit indicates that the low power mode interface is supported. 0: Not supported. 1: Supported.	0x1	R
10	PMAMULTIDROPABI	Half-duplex multi-drop mode. The PHY_STD_T1S_PMA_STATUS.PMAMULTIDROPABI bit indicates that Half-duplex multi-drop mode is supported. 0: Not supported. 1: Supported.	0x1	R
9	PMARXFAULTABILI	Detection of receive faults. The PHY_STD_T1S_PMA_STATUS.PMARXFAULTABILI bit indicates that detection of receive faults is supported. 0: Not supported. 1: Supported.	0x1	R
[8:2]	RESERVED	Reserved.	0x0	R
1	REMOTEJABBER_1	Remote jabber event detected. The PHY_STD_T1S_PMA_STATUS.REMOTEJABBER_1 bit indicates a remote jabber event has been detected. 0: Not detected. 1: Detected.	0x0	R
0	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

PHY T1S TEST MODE CONTROL REGISTER

OA-SPI Address: 0x08FB, MMS: 0x3, Reset: 0x0000

The PHY_STD_T1S_TEST_MODE_CONTROL register is used to configure the PMA transmit pattern.

Table 313. Bit Descriptions for PHY_STD_T1S_TEST_MODE_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:13]	PMAPATTERNSEL	PMA transmit pattern select. The PHY_STD_T1S_TEST_MODE_CONTROL.PMAPATTERNSEL bits select the PMA transmit pattern. 000: Normal operation (default). 001: Test Mode 1 (Transmitter Output Voltage). 010: Test Mode 2 (Transmitter Output Droop). 011: Test Mode 3 (Transmitter PSD mask). 100: Test Mode 4 (Transmitter High Impedance). 101: Reserved. 110: Reserved. 111: Exercise WUT.	0x0	R/W
[12:0]	RESERVED	Reserved.	0x0	R

PHY CONTROL REGISTER

OA-SPI Address: 0xFF00, MMS: 0x0, Reset: 0x1000

The PHY_STD_CONTROL_REGISTER register is used to program the PHY interface as described below.

Table 314. Bit Descriptions for PHY_STD_CONTROL_REGISTER

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W
14	LOOPBACK	Loop back enable. The PHY_STD_CONTROL_REGISTER.LOOPBACK bit is used to enable loop back mode. 0: Disable. 1: Enable.	0x0	R/W
13	SPEEDSEL0	Speed indication LSB. The PHY_STD_CONTROL_REGISTER.SPEEDSEL0 bit, in conjunction with the PHY_STD_CONTROL_REGISTER.SPEEDSEL1 bit indicate the speed value of the PHY.	0x0	R
12	LINKCTL	Link control. The PHY_STD_CONTROL_REGISTER.LINKCTL bit is used to configure link control. 0: PLCA, PCS and the PMA subsystems are held in reset state. 1: PHY can transmit and receive.	0x1	R/W
11	LOWPWRMODE	Low power mode enable. This bit is redundant, field has no effect. 0: Disable. 1: Enable.	0x0	R/W
10	RESERVED	Reserved.	0x0	R/W
9	LINKRST	Reset link status. The PHY_STD_CONTROL_REGISTER.LINKRST bit causes the transceiver to reset its link status, then resume normal operation. 0: Disable. 1: Enable.	0x0	W1
8	DUPLEXMODE	PHY duplex mode. The PHY_STD_CONTROL_REGISTER.DUPLEXMODE bit indicates which duplex mode the PHY is using. Note that T1S operation is always half-duplex. 0: Half-duplex. 1: Full-duplex.	0x0	R
7	COLLISIONTEST	Collision test enable. The PHY_STD_CONTROL_REGISTER.COLLISIONTEST bit is used to enable collision test mode. When this bit is set the PHY reports a collision within 512 BT for any frame transmitted. 0: Disable. 1: Enable.	0x0	R/W

REGISTER DETAILS: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

Table 314. Bit Descriptions for PHY_STD_CONTROL_REGISTER (Continued)

Bits	Bit Name	Description	Reset	Access
6	SPEEDSEL1	Speed indication MSB. The PHY_STD_CONTROL_REGISTER.SPEEDSEL1 bit, in conjunction with the PHY_STD_CONTROL_REGISTER.SPEEDSEL0 bit indicate the speed value of the PHY. 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	0x0	R
[5:0]	RESERVED	Reserved.	0x0	R

PHY STATUS REGISTER

OA-SPI Address: 0xFF01, MMS: 0x0, Reset: 0x082D

The PHY_STD_STATUS_REGISTER register is used to report interface status as described below.

Table 315. Bit Descriptions for PHY_STD_STATUS_REGISTER

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	SPEED10M	Half-duplex speed. he PHY_STD_STATUS_REGISTER.SPEED10M bit indicates that the PHY operates at 10 Mb/s in half-duplex mode. 0: Not supported. 1: Supported.	0x1	R
[10:8]	RESERVED	Reserved.	0x0	R
7	UNIDIRABILITY	MII transmit status. The PHY_STD_STATUS_REGISTER.UNIDIRABILITY bit indicates that the PHY can transmit from media independent interface (MII) only when the PHY has determined that a valid link has been established. 1: Supported. 0: Not supported.	0x0	R
6	PREAMBSUPPR	Suppressed MDIO support. The PHY_STD_STATUS_REGISTER.PREAMBSUPPR bit indicates that the PHY does not accept MDIO frames with a suppressed preamble. 0: Not active. 1: Active.	0x0	R
5	LINKNEGCOMPLETE	Link negotiation complete. The PHY_STD_STATUS_REGISTER.LINKNEGCOMPLETE bit indicates that link negotiation is complete. 0: Not triggered. 1: Triggered.	0x1	R
4	REMOTEJABBER	Remote jabber event detected. The PHY_STD_STATUS_REGISTER.REMOTEJABBER bit indicates that a Remote jabber event has been detected. 0: Not detected. 1: Detected.	0x0	R
3	AUTONEGABILITY	Auto-Negotiation interface. The PHY_STD_STATUS_REGISTER.AUTONEGABILITY bit indicates that the PHY supports the Auto-Negotiation interface. 0: Not supported. 1: Supported.	0x1	R
2	RESERVED	Reserved.	0x1	R
1	LOCALJABBER	Local jabber event detected. The PHY_STD_STATUS_REGISTER.LOCALJABBER bit indicates that a local jabber event has been detected. 1: Detected. 0: Not detected.	0x0	R
0	EXTENDEDCAPAB	Clause 22 to clause 45 status. The PHY_STD_STATUS_REGISTER.EXTENDEDCAPAB bit indicates that the PHY supports Clause 22 to Clause 45 bridge access method. 0: Not supported. 1: Supported.	0x1	R

REGISTER DETAILS: 10BASE-T1S PHY STANDARD REGISTER MAP (PHY_STD)

PHY IDENTIFIER 1 REGISTER

OA-SPI Address: 0xFF02, MMS: 0x0, Reset: 0x0283

The PHY_STD_PHY_IDENTIFIER_1 register indicates the IEEE Organizationally Unique Identifier LSBs.

Table 316. Bit Descriptions for PHY_STD_PHY_IDENTIFIER_1

Bits	Bit Name	Description	Reset	Access
[15:0]	PHYIDOUT_3_18	IEEE Identifier LSBs. The PHY_STD_PHY_IDENTIFIER_1.PHYIDOUT_3_18 bits display the IEEE Organizationally Unique Identifier LSBs.	0x283	R

PHY IDENTIFIER 2 REGISTER

OA-SPI Address: 0xFF03, MMS: 0x0, Reset: 0xBE00

The PHY_STD_PHY_IDENTIFIER_2 register indicates PHY manufacturer information as described below.

Table 317. Bit Descriptions for PHY_STD_PHY_IDENTIFIER_2

Bits	Bit Name	Description	Reset	Access
[15:10]	PHYIDOUT_19_24	IEEE Organizationally Unique identifier MSBs. The PHY_STD_PHY_IDENTIFIER_2.PHYIDOUT_19_24 bits indicate the IEEE organizationally unique identifier MSBs.	0x2F	R
[9:4]	PHYIDICMODEL	Manufacturers model number. The PHY_STD_PHY_IDENTIFIER_2.PHYIDICMODEL bits indicate the manufacturers model number.	0x20	R
[3:0]	PHYIDCHIPREV	Manufacturers revision number. The PHY_STD_PHY_IDENTIFIER_2.PHYIDCHIPREV bits indicate the manufacturers revision number.	0x0	R

NOTES