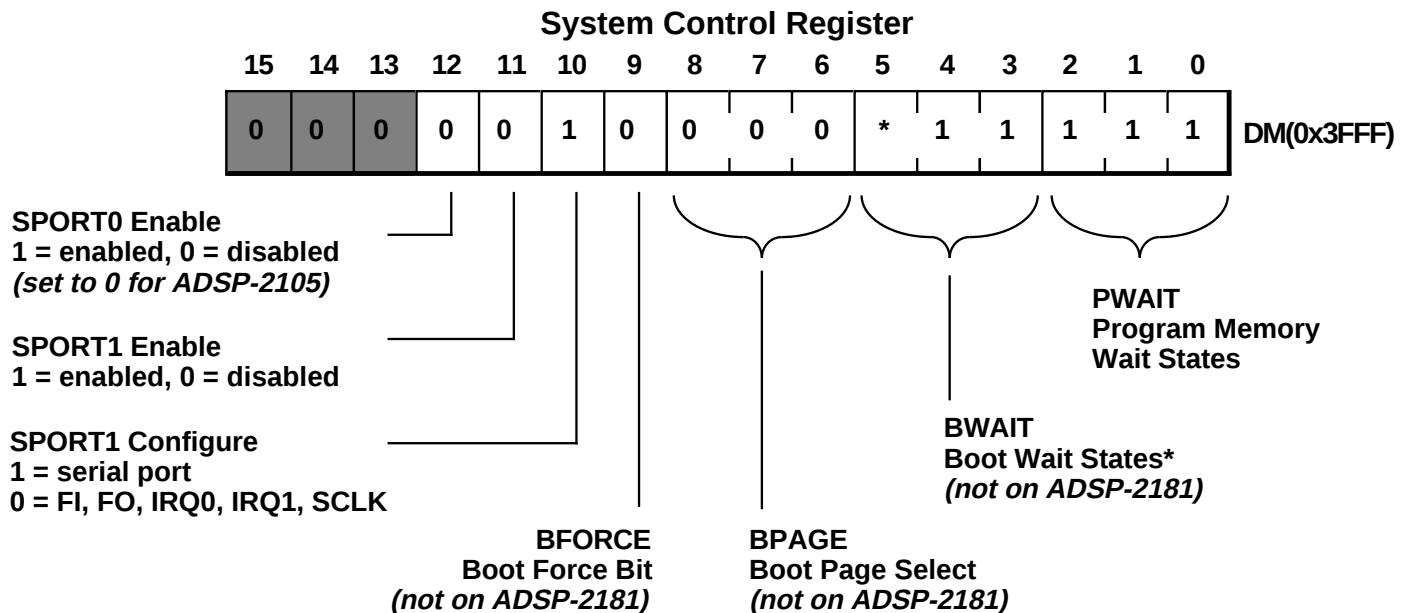


Control/Status Registers E

E.1 OVERVIEW

This appendix shows bit definitions for 1) the memory-mapped control registers and 2) other (non-memory-mapped) control and status registers of all ADSP-21xx processors. The memory-mapped registers are listed in descending address order. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a gray field. These bits should always be written with zeros.

Memory-Mapped Registers



* Bit 5 initialized to 1 on ADSP-2171, ADSP-21msp58/59
Bit 5 initialized to 0 on ADSP-2101, ADSP-2105, ADSP-2115, ADSP-2111

E Control/Status Registers

Processor Core

DATA ADDRESS GENERATORS

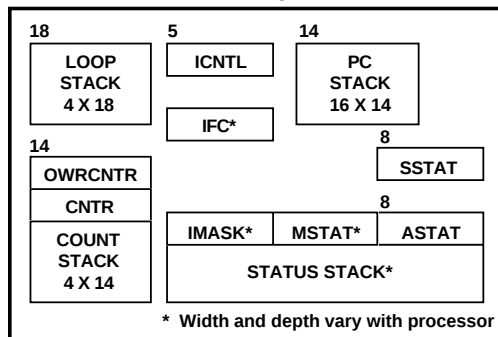
DAG1
(DM addressing only)
Bit-reverse capability

I0	L0	M0
I1	L1	M1
I2	L2	M2
I3	L3	M3
14	14	14

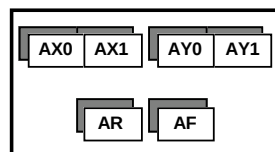
DAG2
(DM and PM addressing)
Indirect branch capability

I4	L4	M4
I5	L5	M5
I6	L6	M6
I7	L7	M7
14	14	14

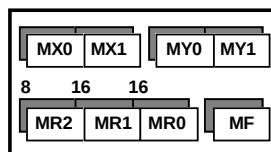
PROGRAM SEQUENCER



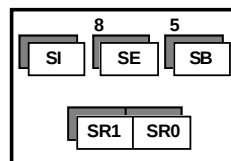
ALU



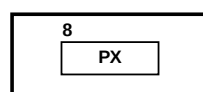
MAC



SHIFTER



BUS EXCHANGE



TIMER

0x3FFD	TPERIOD
0x3FFC	TCOUNT
0x3FFB	TSCALE

MEMORY INTERFACE

0x3FFF	System Control Register
0x3FFE	Wait States
(ADSP-2181)	
3	DMOVLAY
3	PMOVLAY

SPORT 0

RX0	TX0
Multichannel enables	
0x3FFA	RX 31-16
0x3FF9	RX 15-0
0x3FF8	TX 31-16
0x3FF7	TX 15-0
SPORT0 Control	
0x3FF6	Control
0x3FF5	SCLKDIV
0x3FF4	RFSDIV
0x3FF3	Autobuffer

ANALOG INTERFACE (ADSP-21msp5x)

0x3FEF	Autobuffer
0x3FEE	Control
0x3FED	ADC Receive
0x3FEC	DAC Transmit

SPORT 1

RX1	TX1
SPORT1 Control	
0x3FF2	Control
0x3FF1	SCLKDIV
0x3FF0	RFSDIV
0x3FEF	Autobuffer

HOST INTERFACE PORT (ADSP-2171, ADSP-2111, ADSP-21msp5x)

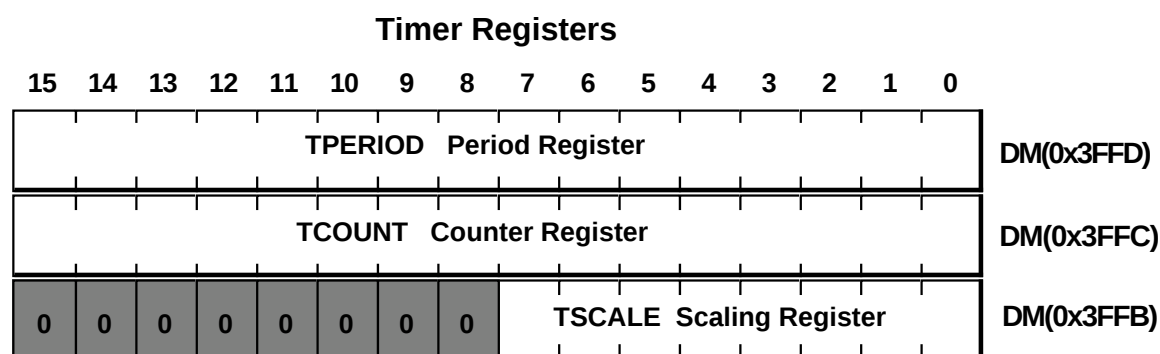
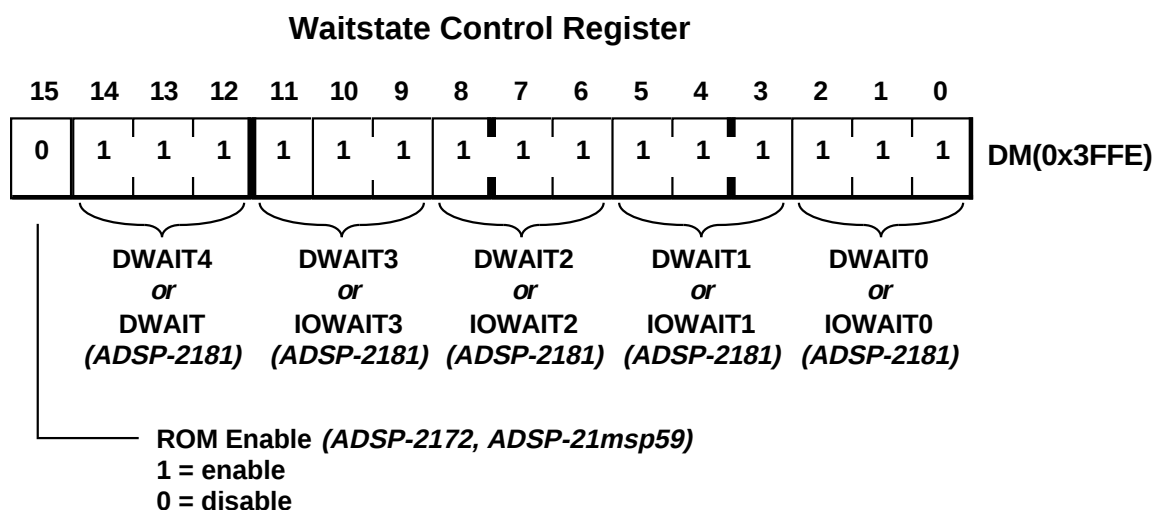
0x3FE8	HMASK	Data Registers	
		0x3FE5	HDR5
Status Registers		0x3FE4	HDR4
0x3FE7	HSR7	0x3FE3	HDR3
0x3FE6	HSR6	0x3FE2	HDR2
		0x3FE1	HDR1
		0x3FE0	HDR0

IDMA PORT BDMA PORT PROGRAMMABLE FLAGS (ADSP-2181)

IDMA Registers		BDMA Registers	
0x3FE0	IDMA Control Register	0x3FE4	BWCOUNT
Programmable Flag Registers		0x3FE3	BDMA Control
0x3FE6	PFTYPE	0x3FE2	BEAD
0x3FE5	PFDATA	0x3FE1	BIAD

Control/Status Registers E

Memory-Mapped Registers



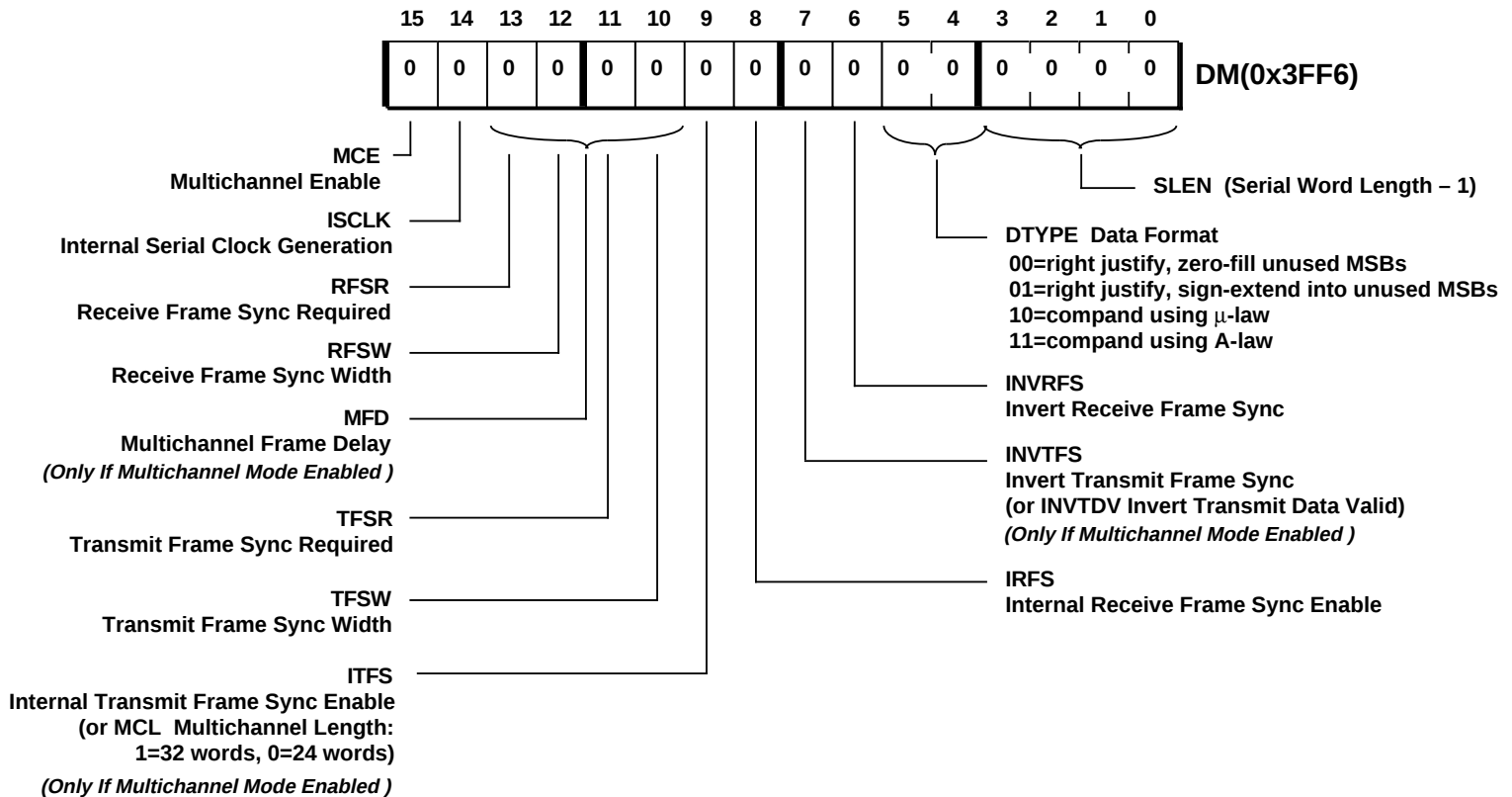
Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
 Reserved bits are shown on a gray field—these bits should always be written with zeros.

E Control/Status Registers

Memory-Mapped Registers

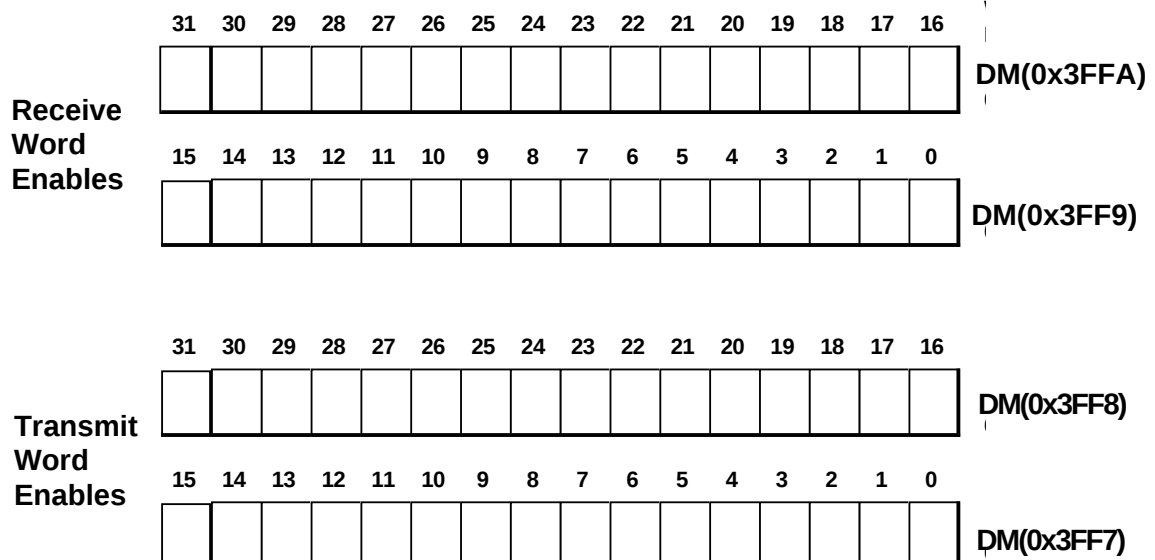
SPORT0 Control Register

(Not on ADSP-2105)



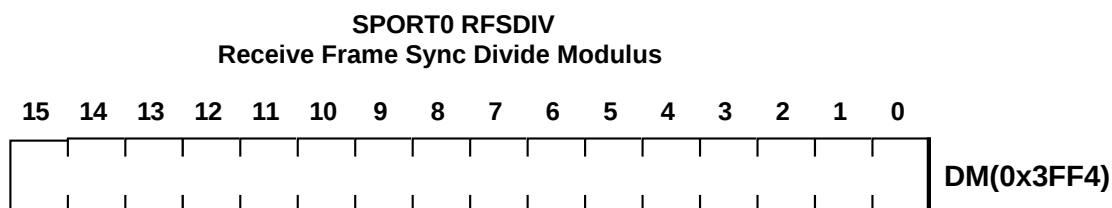
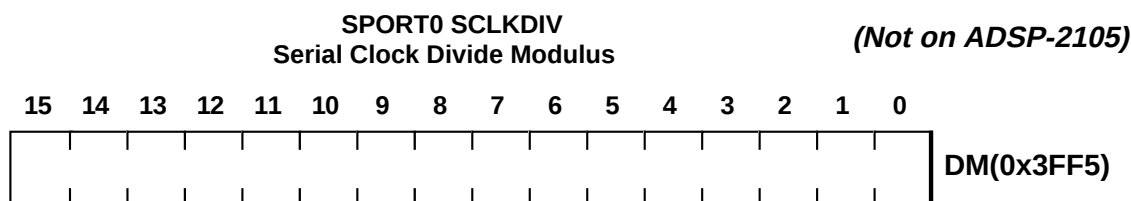
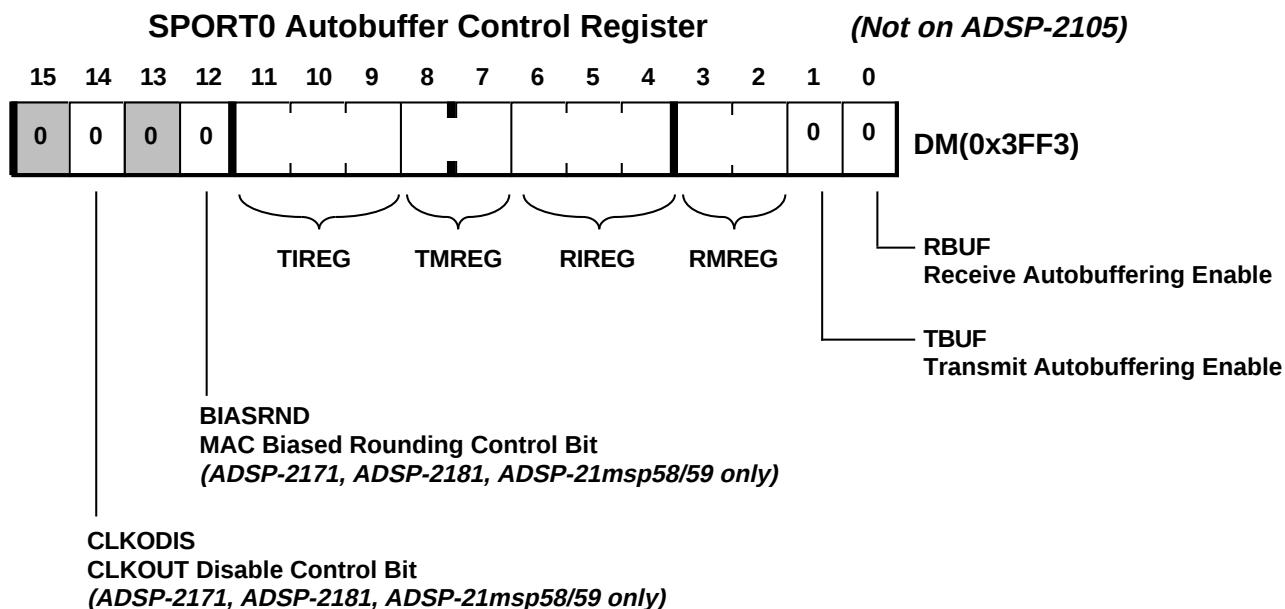
SPORT0 Multichannel Word Enables

(Not on ADSP-2105)



Control/Status Registers E

Memory-Mapped Registers



$$\text{SCLKDIV} = \frac{\text{CLKOUT frequency}}{2 * (\text{SCLK frequency})} - 1$$

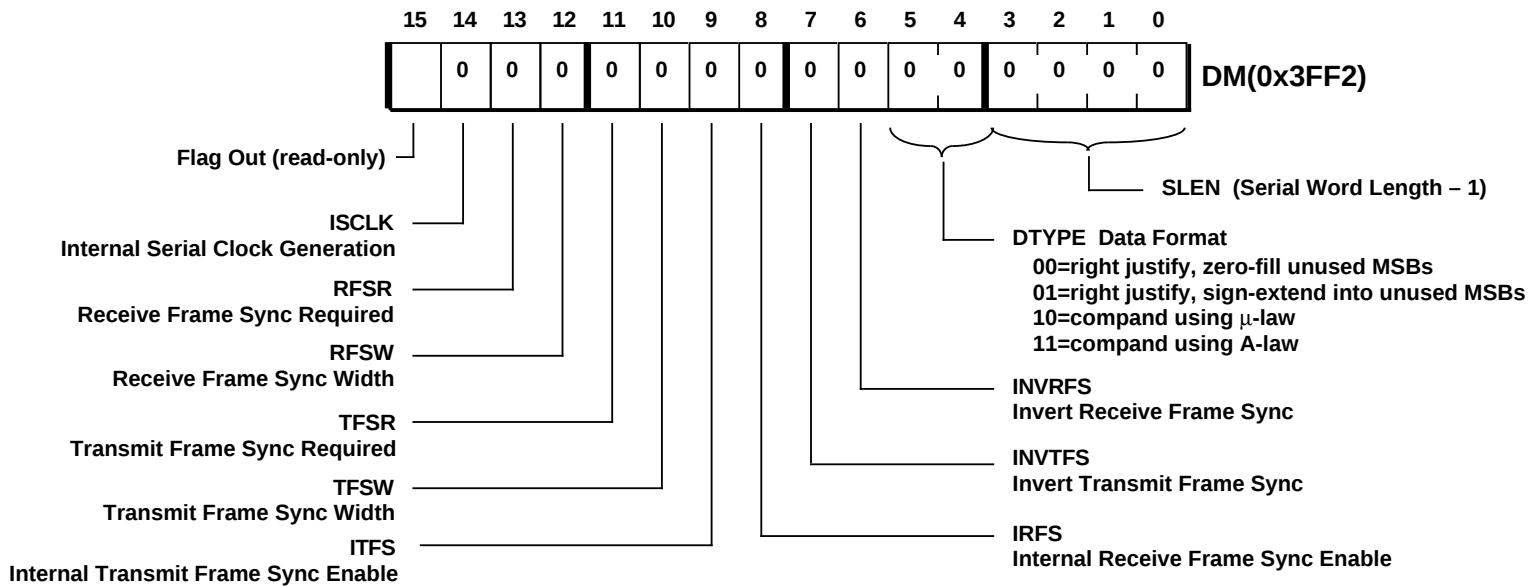
$$\text{RFSDIV} = \frac{\text{SCLK frequency}}{\text{RFS frequency}} - 1$$

Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

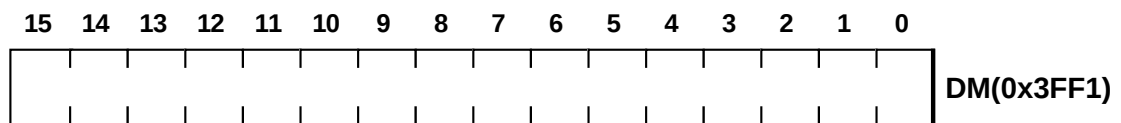
E Control/Status Registers

Memory-Mapped Registers

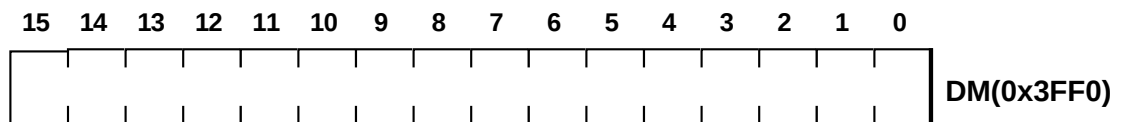
SPORT1 Control Register



SPORT1 SCLKDIV
Serial Clock Divide Modulus



SPORT1 RFSDIV
Receive Frame Sync Divide Modulus



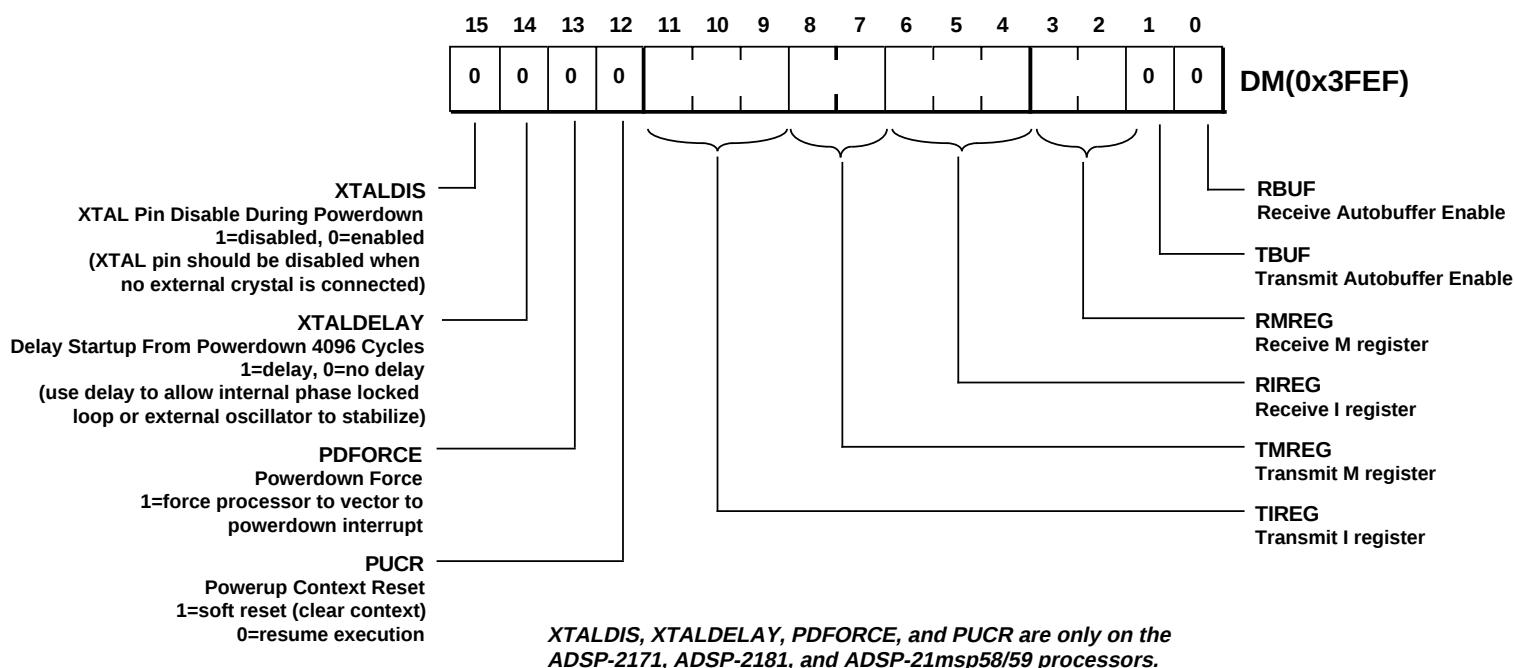
$$\text{SCLKDIV} = \frac{\text{CLKOUT frequency}}{2 * (\text{SCLK frequency})} - 1$$

$$\text{RFSDIV} = \frac{\text{SCLK frequency}}{\text{RFS frequency}} - 1$$

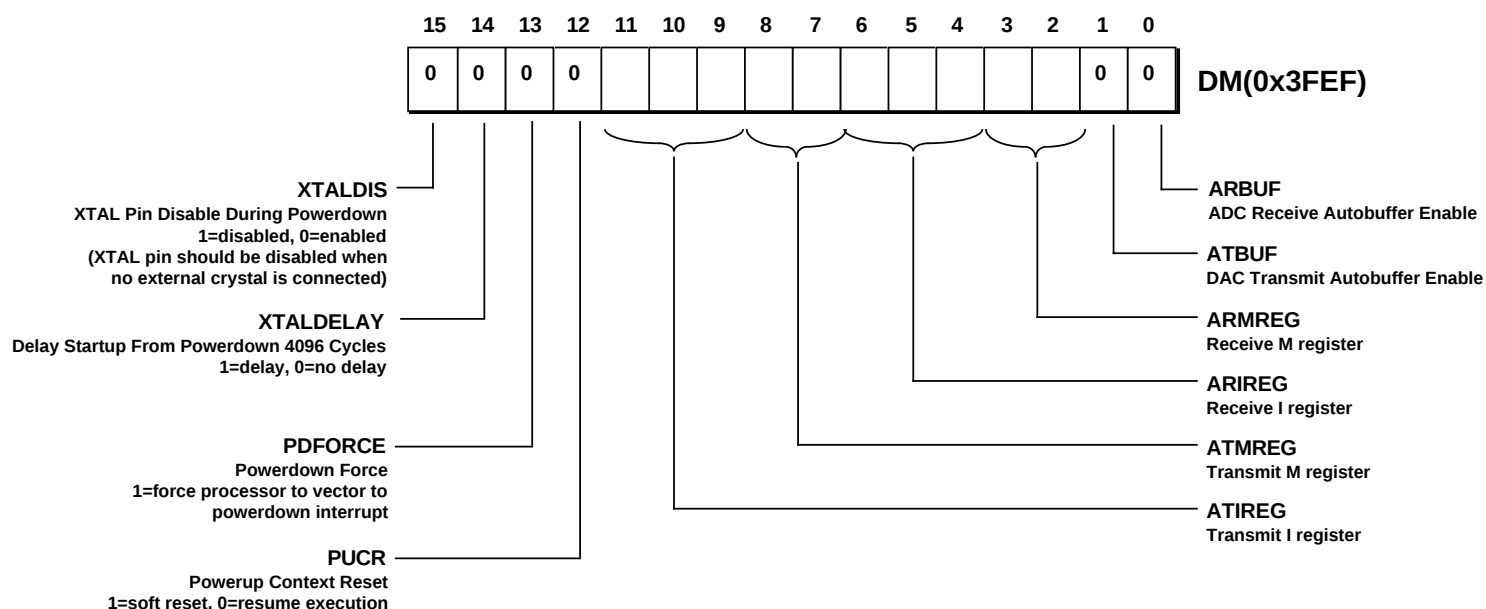
Control/Status Registers E

Memory-Mapped Registers

SPORT1 Autobuffer Control Register (Not on ADSP-21msp5x)



Analog Autobuffer Control Register (ADSP-21msp5x only)



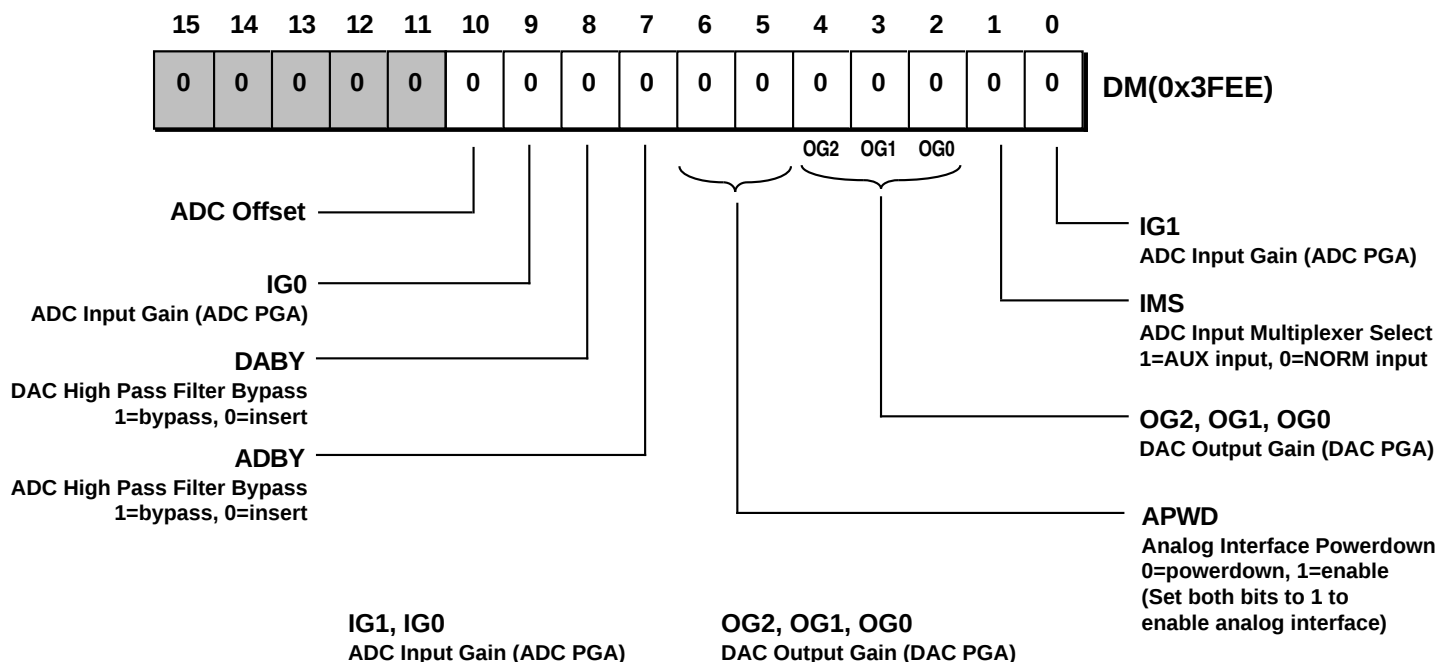
Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

E Control/Status Registers

Memory-Mapped Registers

Analog Control Register

(ADSP-21msp5x only)



Analog Data Registers

(ADSP-21msp5x only)

ADC Receive Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

DM(0x3FED)

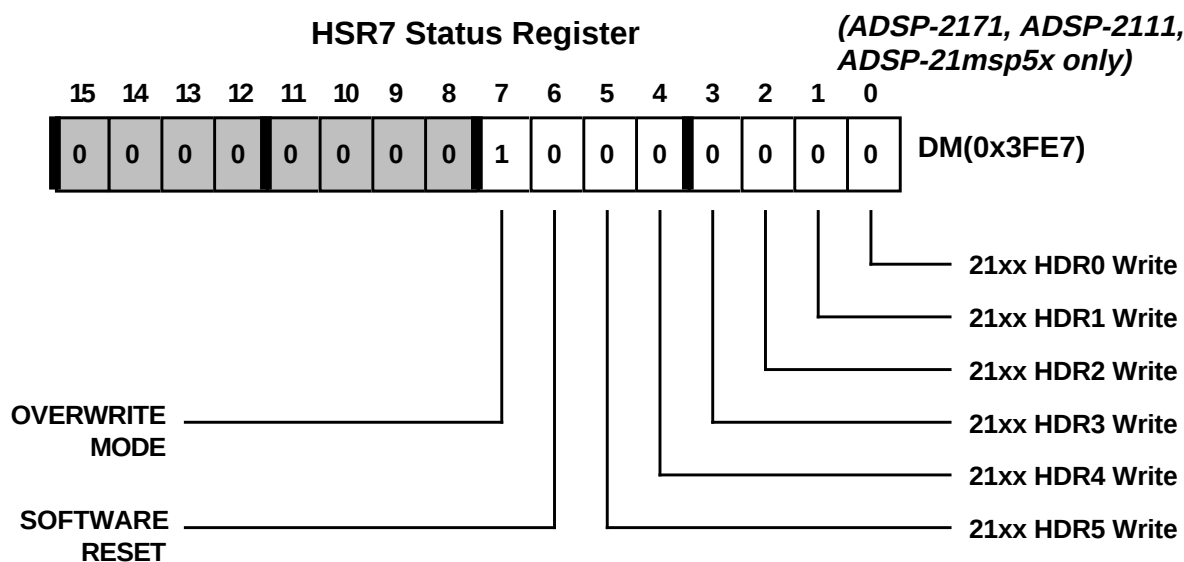
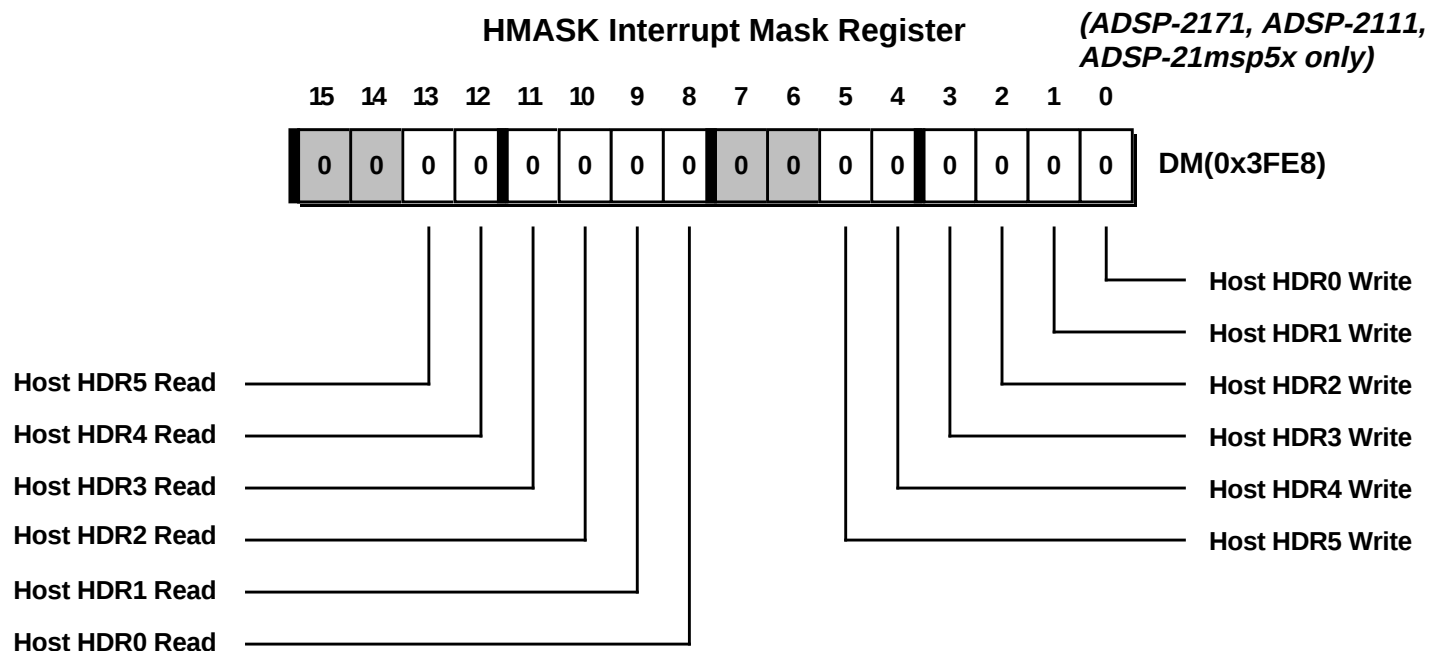
DAC Transmit Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

DM(0x3FEC)

Control/Status Registers E

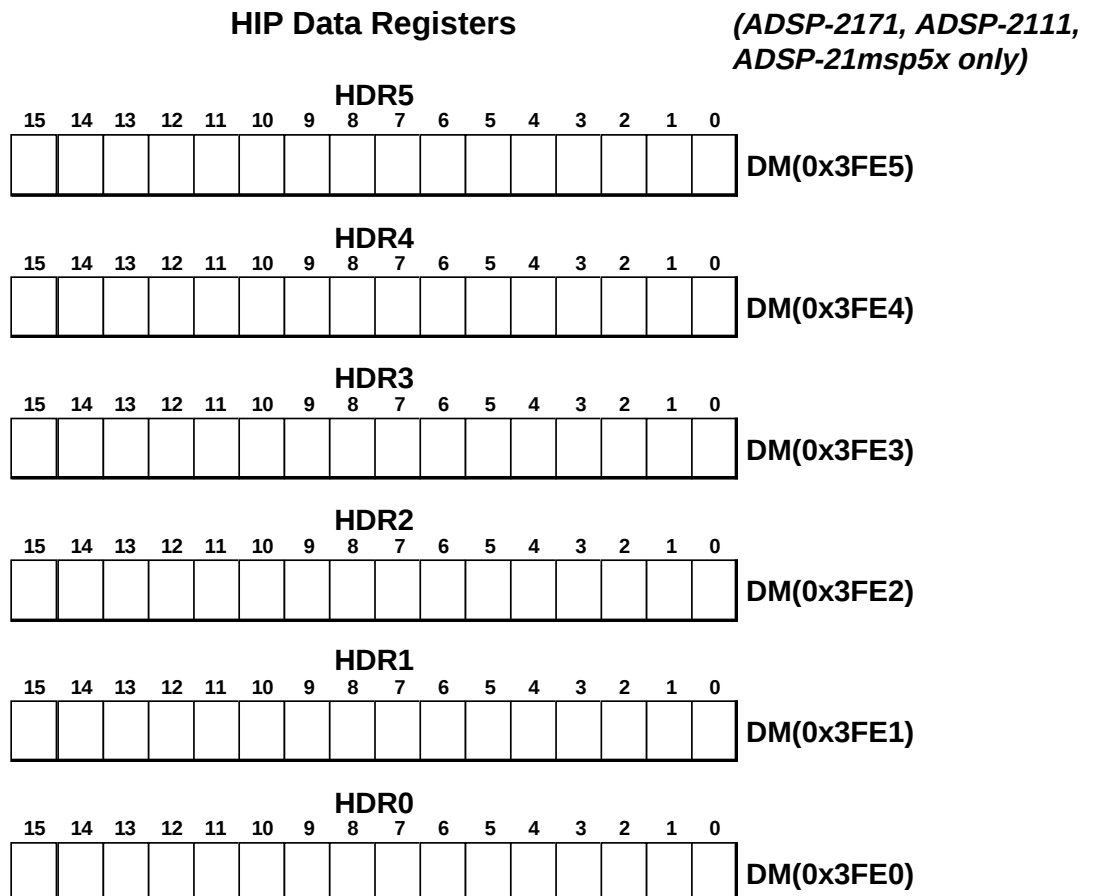
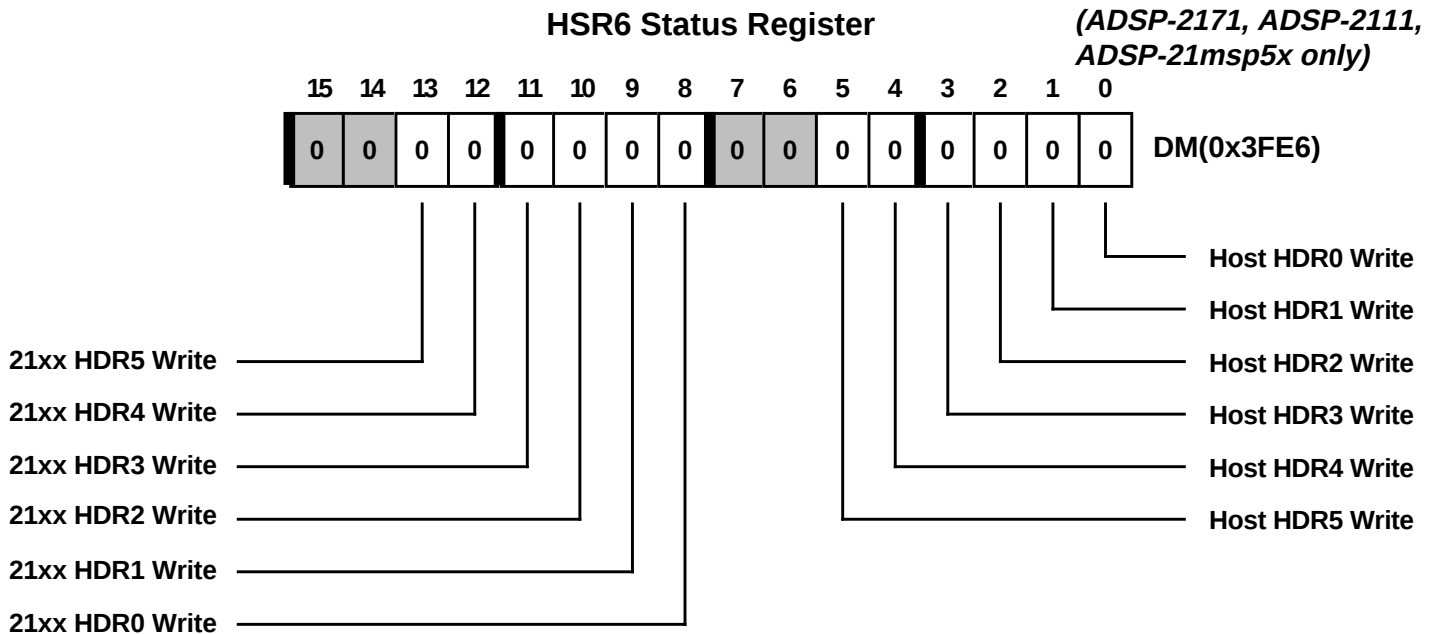
Memory-Mapped Registers



Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

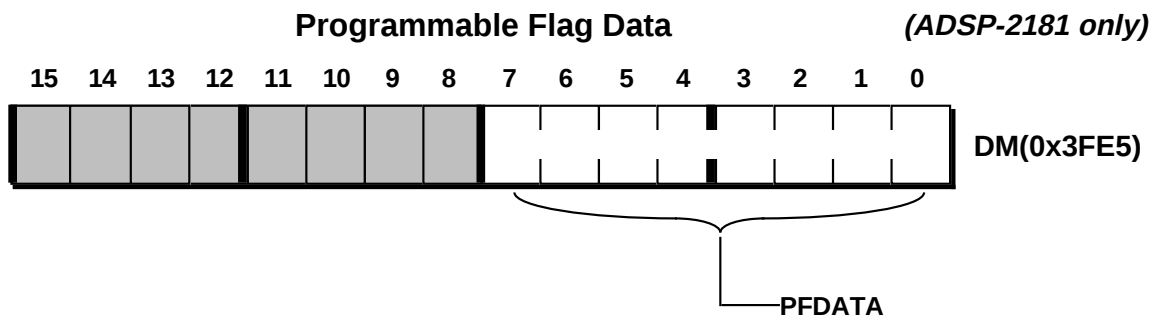
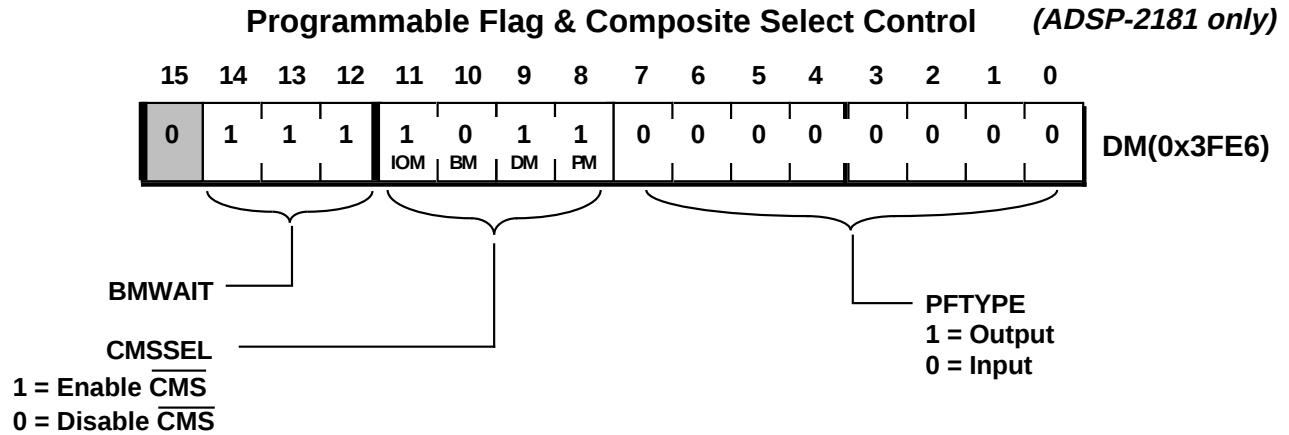
E Control/Status Registers

Memory-Mapped Registers



Control/Status Registers E

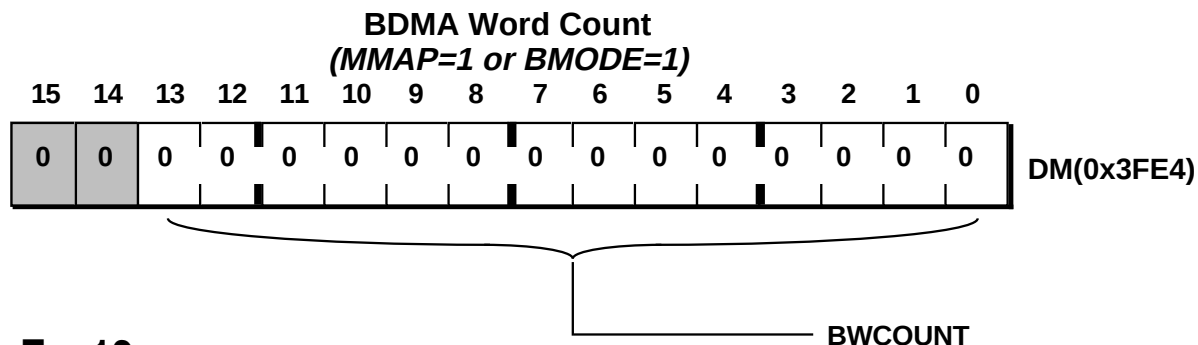
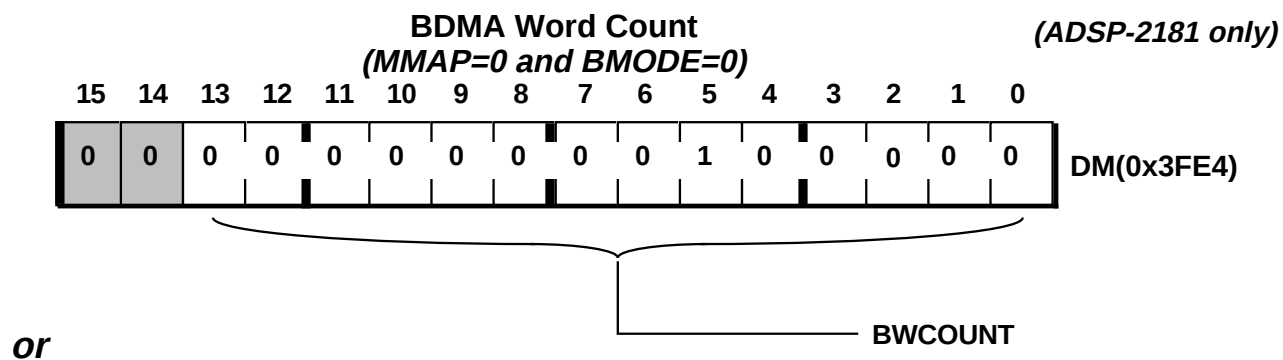
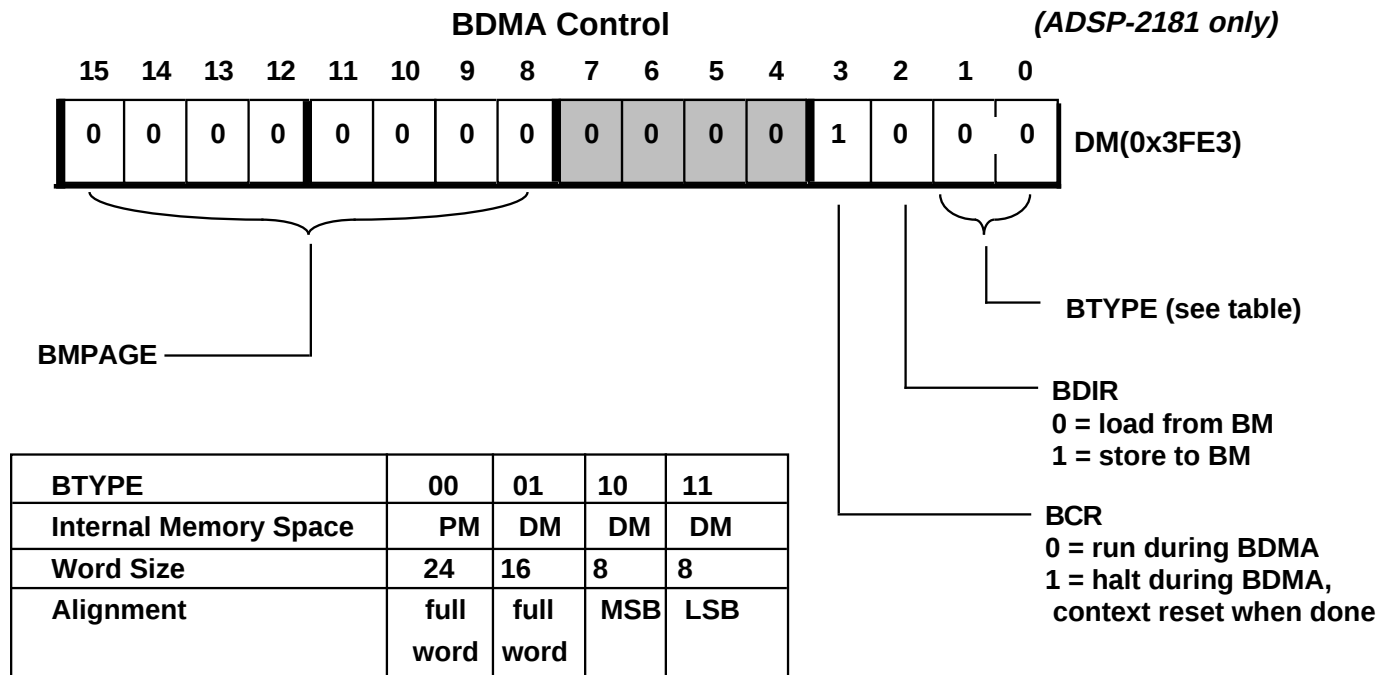
Memory-Mapped Registers



Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

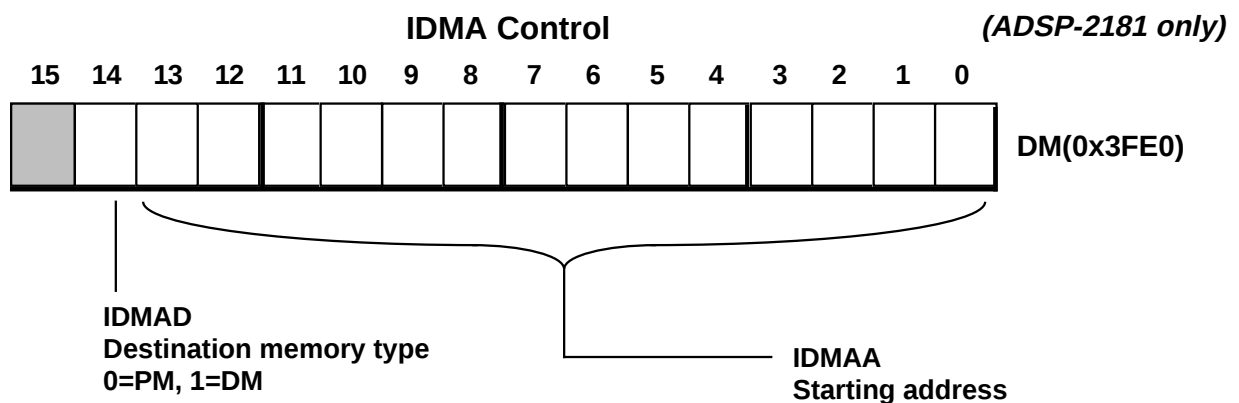
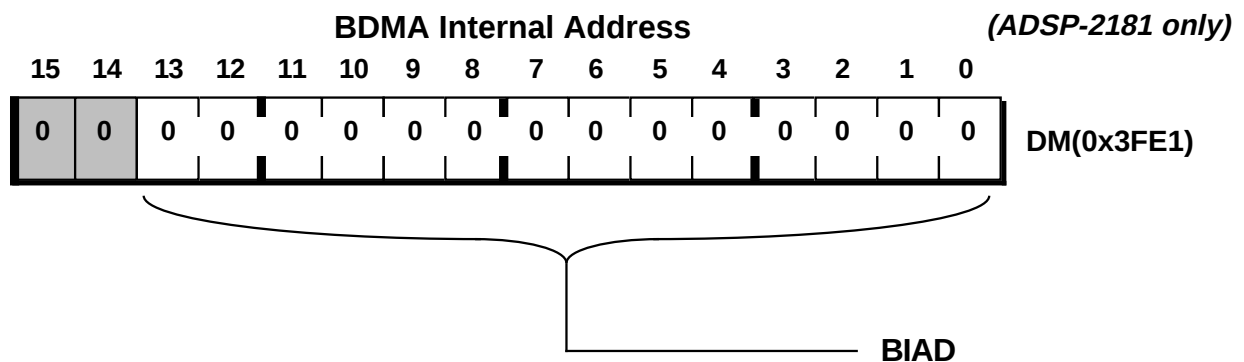
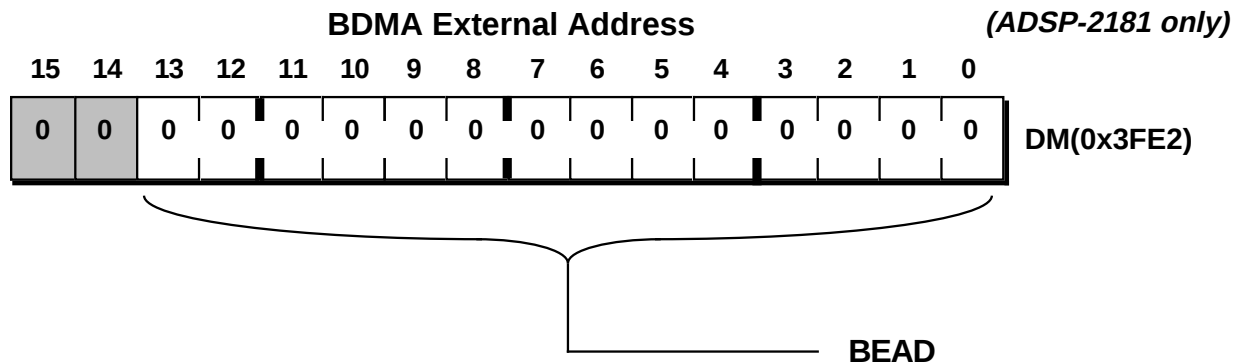
E Control/Status Registers

Memory-Mapped Registers



Control/Status Registers E

Memory-Mapped Registers

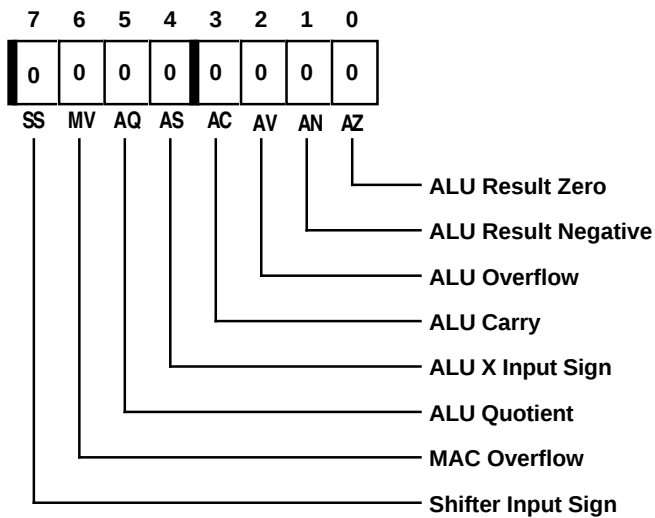


Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

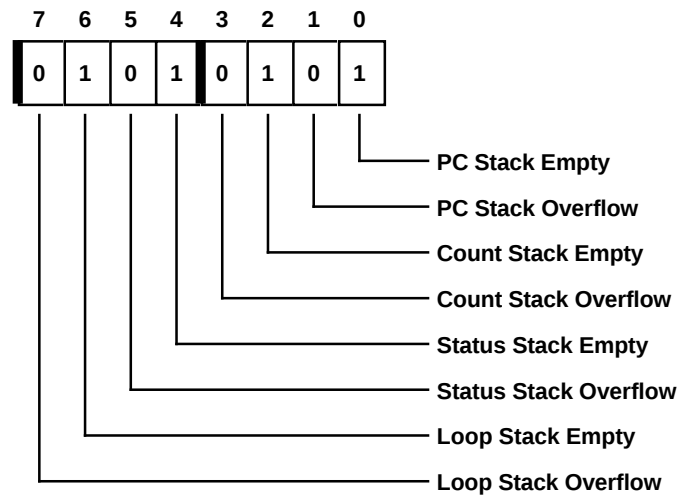
E Control/Status Registers

Non-Memory-Mapped Registers

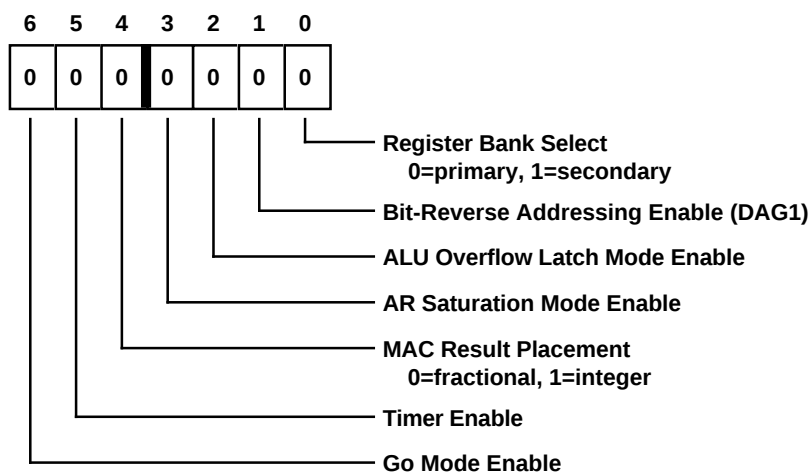
ASTAT



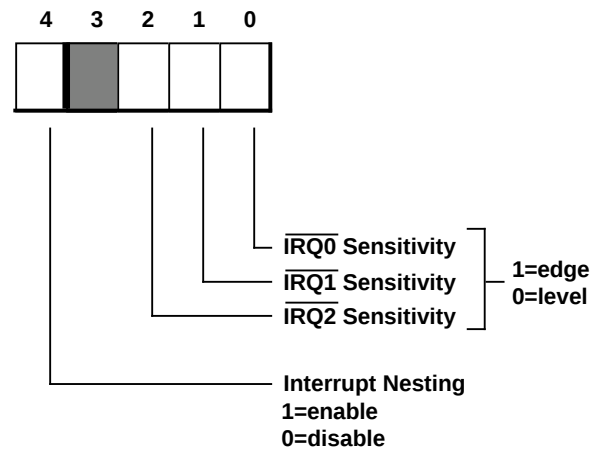
SSTAT (read-only)



MSTAT



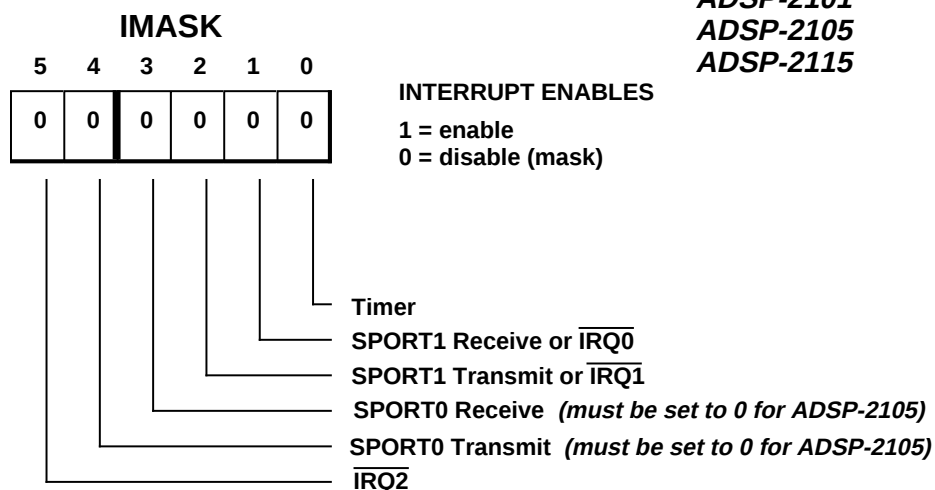
ICNTL



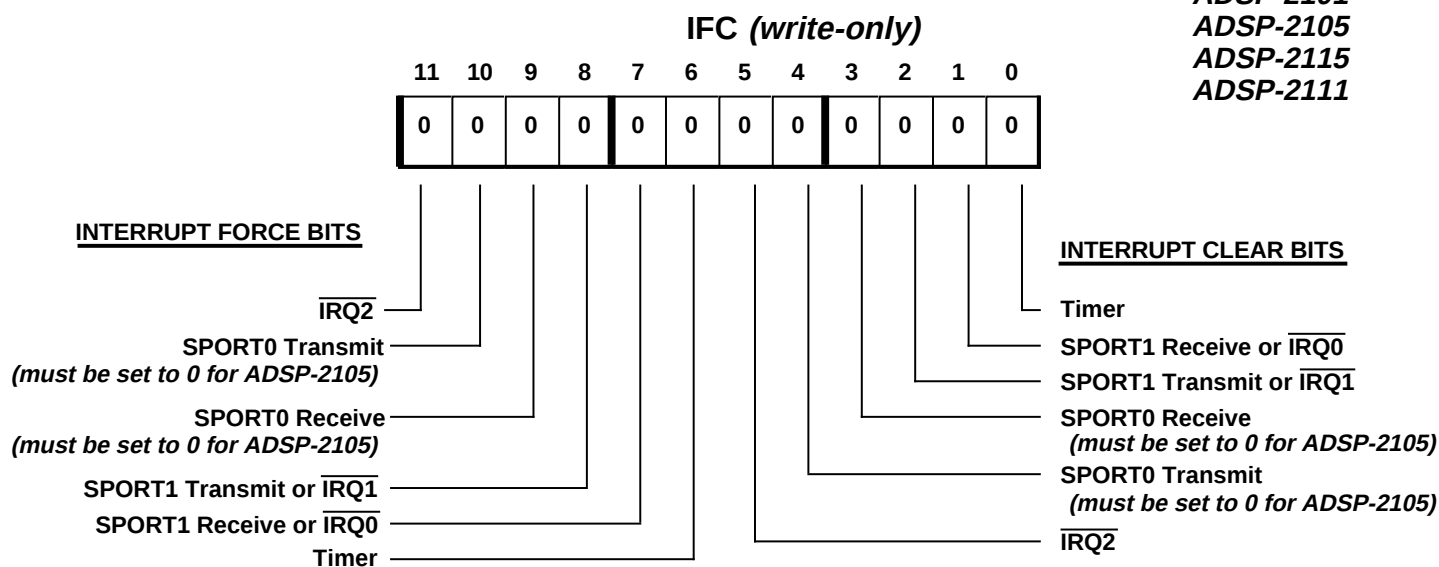
Control/Status Registers E

Non-Memory-Mapped Registers

**ADSP-2101
ADSP-2105
ADSP-2115**



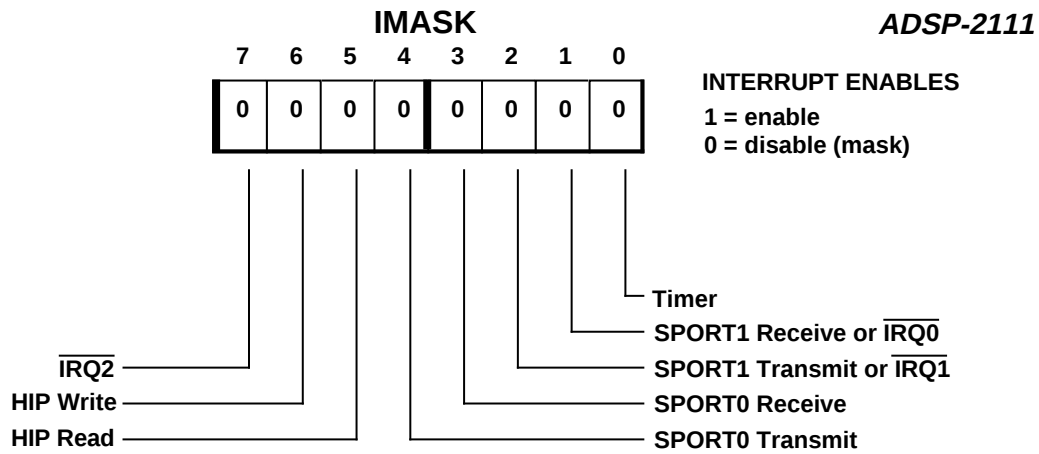
**ADSP-2101
ADSP-2105
ADSP-2115
ADSP-2111**



Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

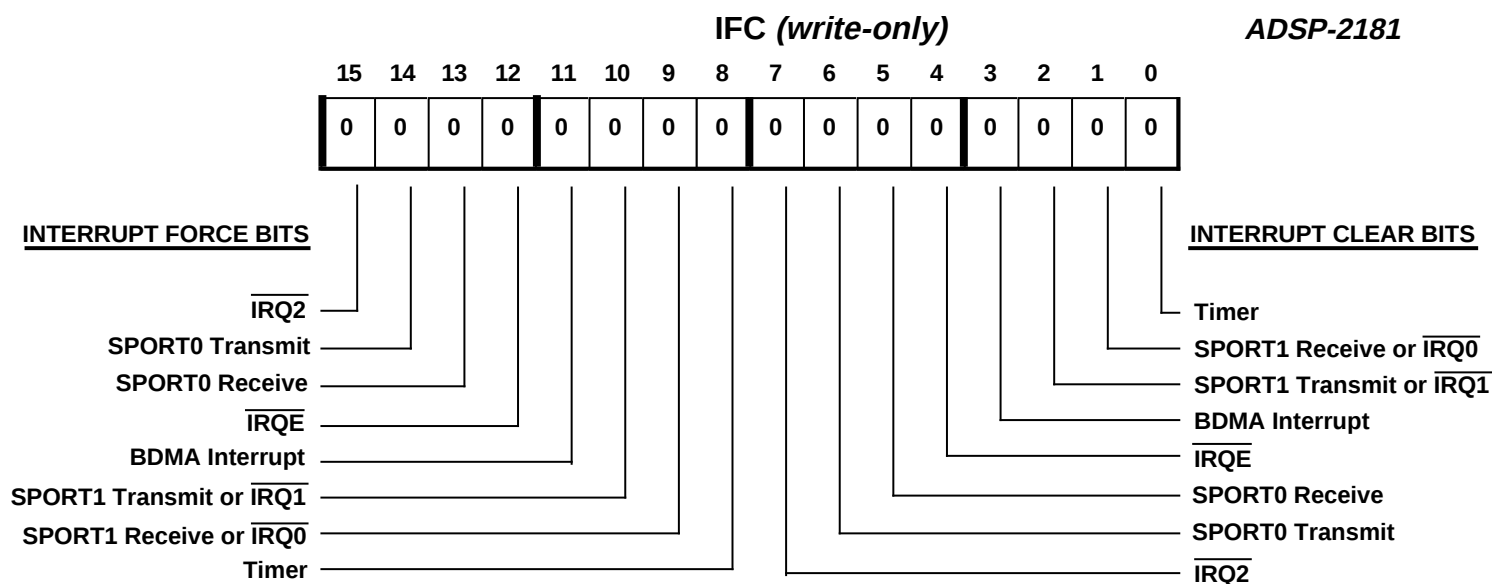
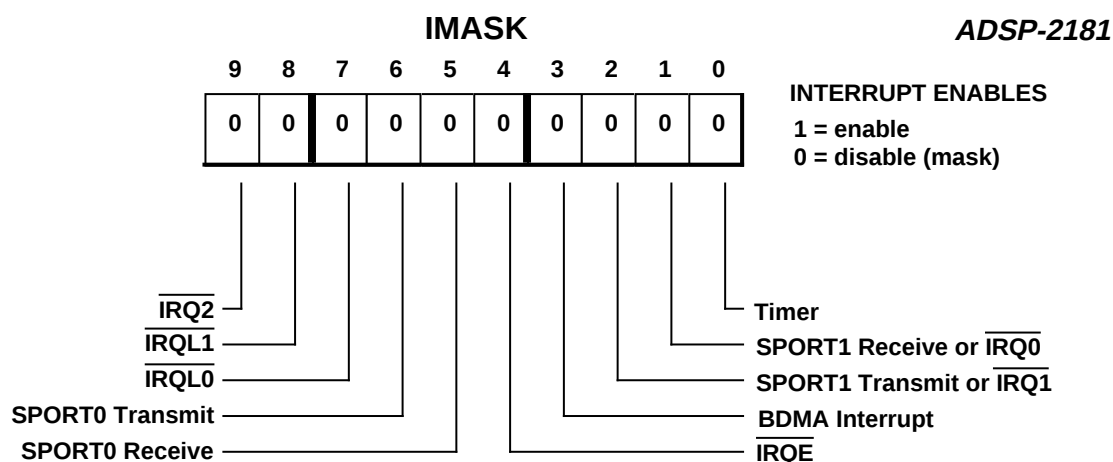
E Control/Status Registers

Non-Memory-Mapped Registers



Control/Status Registers E

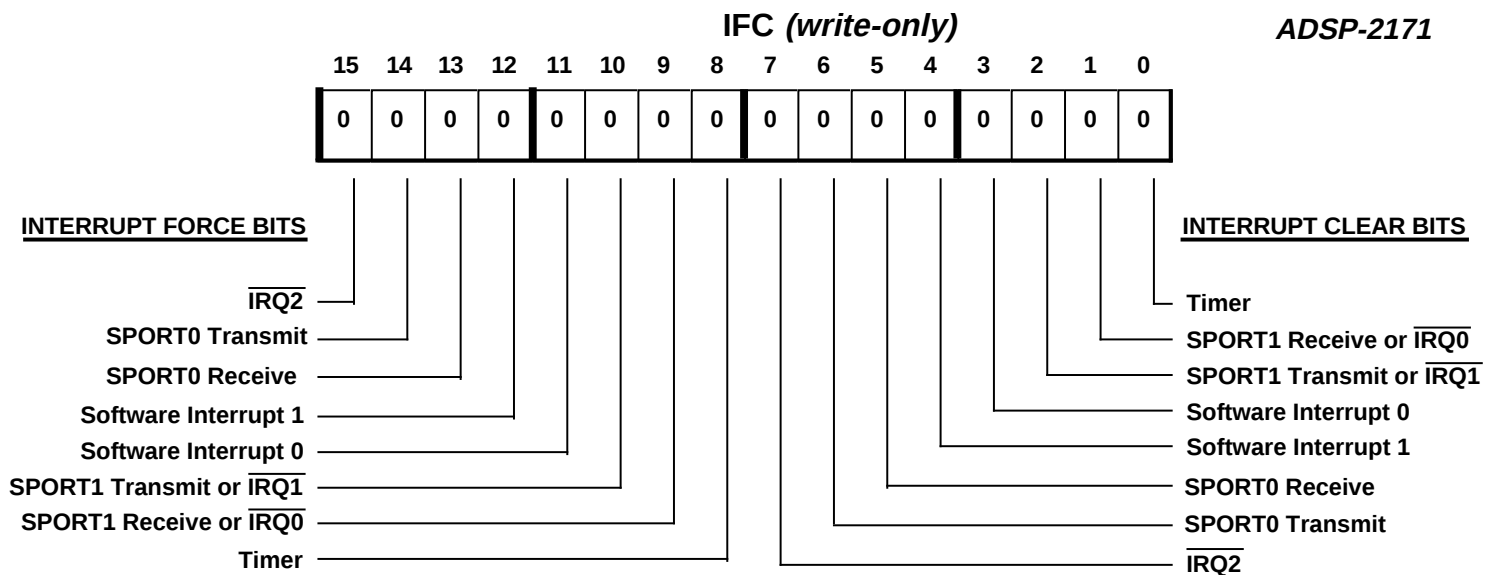
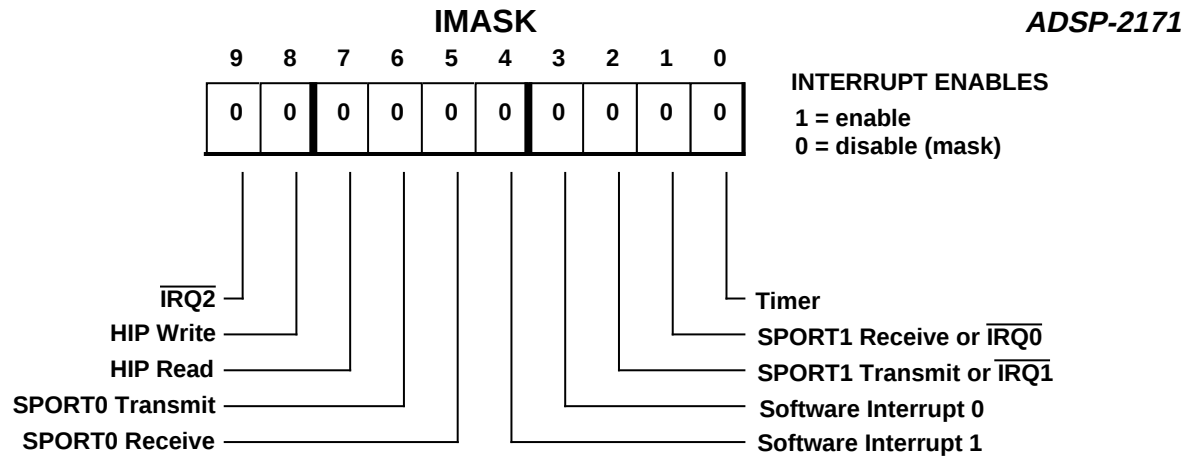
Non-Memory-Mapped Registers



Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

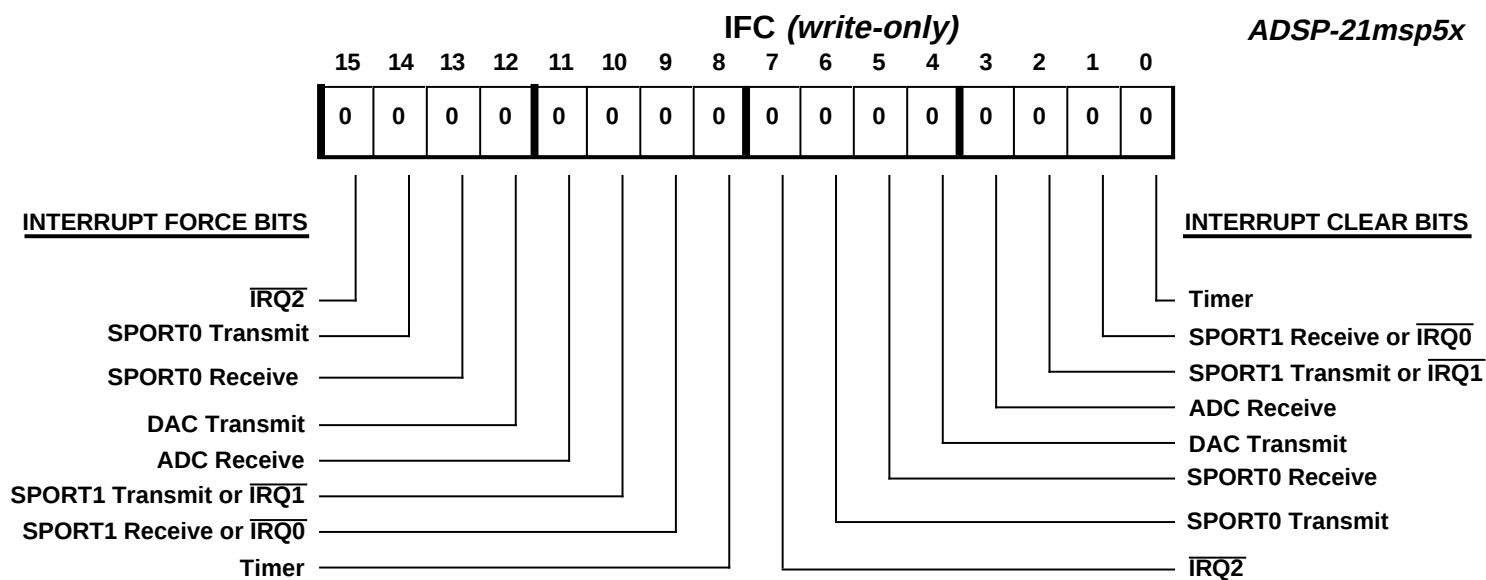
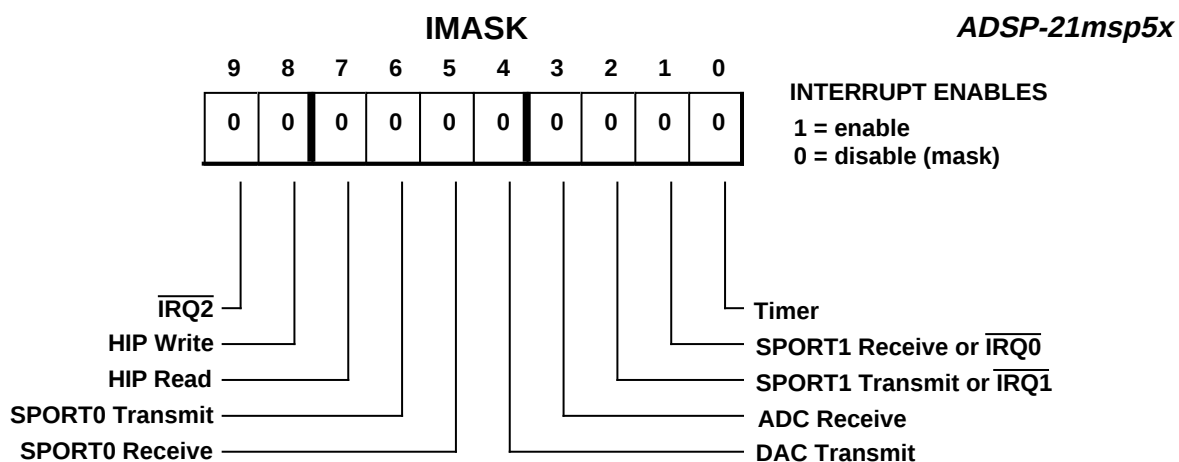
E Control/Status Registers

Non-Memory-Mapped Registers



Control/Status Registers E

Non-Memory-Mapped Registers



Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

E Control/Status Registers

Processor Core

DATA ADDRESS GENERATORS

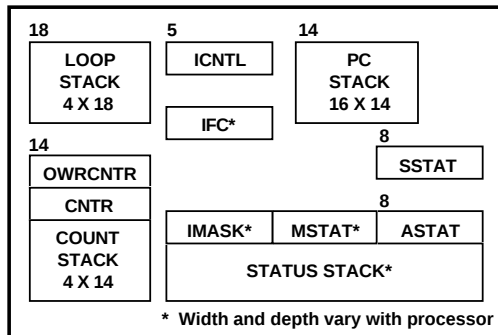
DAG1
(DM addressing only)
Bit-reverse capability

I0	L0	M0
I1	L1	M1
I2	L2	M2
I3	L3	M3
14	14	14

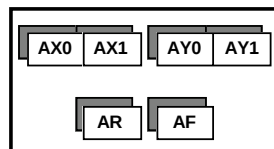
DAG2
(DM and PM addressing)
Indirect branch capability

I4	L4	M4
I5	L5	M5
I6	L6	M6
I7	L7	M7
14	14	14

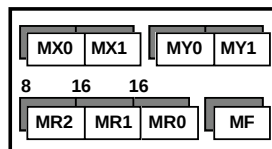
PROGRAM SEQUENCER



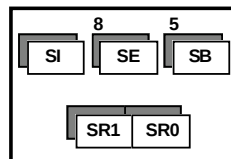
ALU



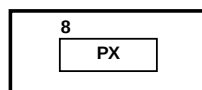
MAC



SHIFTER



BUS EXCHANGE



TIMER

0x3FFD	TPERIOD
0x3FFC	TCOUNT
0x3FFB	TSCALE

MEMORY INTERFACE

0x3FFF	System Control Register
0x3FFE	Wait States
(ADSP-2181)	
3	3
DMOVLAY	PMOVLAY

SPORT 0

RX0	TX0
Multichannel enables	
0x3FFA	RX 31-16
0x3FF9	RX 15-0
0x3FF8	TX 31-16
0x3FF7	TX 15-0
SPORT0 Control	
0x3FF6	Control
0x3FF5	SCLKDIV
0x3FF4	RFSDIV
0x3FF3	Autobuffer

ANALOG INTERFACE (ADSP-21msp5x)

0x3FEF	Autobuffer
0x3FEE	Control
0x3FED	ADC Receive
0x3FEC	DAC Transmit

SPORT 1

RX1	TX1
SPORT1 Control	
0x3FF2	Control
0x3FF1	SCLKDIV
0x3FF0	RFSDIV
0x3FEF	Autobuffer

HOST INTERFACE PORT (ADSP-2171, ADSP-2111, ADSP-21msp5x)

0x3FE8	HMASK	Data Registers	
Status Registers		0x3FE5	HDR5
		0x3FE4	HDR4
0x3FE7	HSR7	0x3FE3	HDR3
0x3FE6	HSR6	0x3FE2	HDR2
		0x3FE1	HDR1
		0x3FE0	HDR0

IDMA PORT BDMA PORT PROGRAMMABLE FLAGS (ADSP-2181)

IDMA Registers		BDMA Registers	
0x3FE0	IDMA Control Register	0x3FE4	BWCOUNT
Programmable Flag Registers		0x3FE3	BDMA Control
0x3FE6	PFTYPE	0x3FE2	BEAD
0x3FE5	PFDATA	0x3FE1	BIAD