ADSP-21375 EZ-KIT Lite®
Evaluation System Manual

Revision 1.0, September 2006

Part Number
82-000940-02

Analog Devices, Inc.
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ANALOG DEVICES

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The ADSP-21375 EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The ADSP-21375 EZ-KIT Lite evaluation system had been appended to Analog Devices Development Tools Technical Construction File referenced "DSPTOOLS1" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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PREFACE

Thank you for purchasing the ADSP-21375 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for ADSP-21375 SHARC® processors.

The SHARC processors are based on a 32-bit super Harvard architecture that includes a unique memory architecture comprised of two large on-chip, dual-ported SRAM blocks coupled with a sophisticated IO processor, which gives a SHARC processor the bandwidth for sustained high-speed computations. SHARC processors represents today's de facto standard for floating-point processing, targeted toward premium audio applications.

The evaluation system is designed to be used in conjunction with the VisualDSP++® development environment to test the capabilities of the ADSP-21375 SHARC processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-21375 assembly
- Load, run, step, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-21375 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-21375 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools/.

The ADSP-21375 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. For details about evaluation license restrictions after the 90 days, refer to "Evaluation License Restrictions" on page 1-7.

ADSP-21375 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The board features:

- Analog Devices ADSP-21375 processor
  - 208-pin MQFP package
  - 266 MHz core clock speed
- Synchronous dynamic random access memory (SDRAM)
  - 2M x 16-bit x 4 banks
- Flash memory
  - 1M x 8-bit

- Serial peripheral interface (SPI) flash memory
  - 2 Mbit
- Analog audio interface
  - AD1835A codec
  - 4x2 RCA phono jack for 4 channels of stereo output
  - 2x1 RCA phono jack for 1 channel of stereo input
  - 3.5 mm headphone jack for 1 channel stereo output
- Universal asynchronous receiver/transmitter (UART)
  - ADM3202 RS-232 driver/receiver
  - DB9 female connector
- National Instruments Educational Laboratory Virtual Instrumentation Suite (ELVIS) Interface
  - LabVIEW™-based virtual instruments
  - Multifunction data acquisition device
  - Bench-top workstation and prototype board
- LEDs
  - 11 LEDs: 1 power (green), 1 board reset (red), 1 USB monitor (amber), and 8 general purpose (amber)
- Push buttons
  - 5 push buttons: 1 reset, 2 connected to DAI, 2 connected to the `FLAG` pins of the processor

- Expansion interface (Type A)
  - Parallel port, FLAG pins, DPI, DAI
- Other features
  - JTAG ICE 14-pin header
  - Test points for processor current measurement
  - DPI header
  - DAI header

The EZ-KIT Lite board has a total of 1 MB of parallel flash memory and 2 Mbit of SPI flash memory. The flash memories can store user-specific boot code, allowing the board to run as a stand-alone unit. For more information, see "External Memory" on page 1-7 and "Boot Mode and Clock Ratio Select Switch (SW2)" on page 2-9. The board has 16 MB of SDRAM, which can be used at runtime or from which code can be executed.

The DAI port of the processor connects to the AD1835A audio codec and an external phase lock loop (PLL). The DAI interface facilitates development of digital and analog audio signal-processing applications. See "Analog Audio" on page 1-10 and for more information.

The DPI port of the processor connects to the UART interface and the SPI interface. The UART interface can connect to a standard RS-232 connection, while the SPI connects to the 2 Mbit of serial flash memory.

Additionally, the EZ-KIT Lite board provides access to all of the processor's peripheral ports. Access is provided in the form of a three-connector expansion interface. See "Expansion Interface" on page 2-7 for details.

Purpose of This Manual

The *ADSP-21375 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board) and describes the operation and configuration of the board components. The product software component is detailed in the *VisualDSP++ Installation Quick Reference Card*. The manual provides guidelines for running your own code on the ADSP-21375 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts, such as the *ADSP-2136x SHARC Processor Programming Reference* and *ADSP-21368 SHARC Processor Hardware Reference* (includes ADSP-21375) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and the VisualDSP++ user's or getting started guides. For the locations of these documents, see "Related Documents".

Manual Contents

The manual consists of:

- Chapter 1, "Using ADSP-21375 EZ-KIT Lite" on page 1-1
  Provides information on the EZ-KIT Lite from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "ADSP-21375 EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the hardware aspects of the evaluation system.
- Appendix A, "ADSP-21375 EZ-KIT Lite Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "ADSP-21375 EZ-KIT Lite Schematic" on page B-1
  Provides the resources to allow modifications to the EZ-KIT Lite or to use as a reference design.

Appendix B now is part of the online Help. The PDF version of the *ADSP-21375 EZ-KIT Lite Evaluation System Manual* is located in the `Docs\EZ-KIT Lite Manuals` folder on the installation CD. Alternatively, the schematic can be found on the Analog Devices Web site at `http://www.analog.com/processors`.

What's New in This Manual

This is the first edition of the *ADSP-21375 EZ-KIT Lite Evaluation System Manual*.

Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:

- Visit the Embedded Processing and DSP products Web site at
  http://www.analog.com/processors/technicalSupport
- E-mail tools questions to
  processor.tools.support@analog.com
- E-mail processor questions to
  processor.support@analog.com (World wide support)
  processor.europe@analog.com (Europe support)
  processor.china@analog.com (China support)
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:
  Analog Devices, Inc.
  One Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

The ADSP-21375 EZ-KIT Lite evaluation system supports the Analog Devices ADSP-21375 SHARC processors.

Product Information

You can obtain product information from the Analog Devices Web site, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at http://www.analog.com. Our Web site provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit http://www.myanalog.com to sign up. Click **Register** to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

Processor Product Information

For information on embedded processors and DSPs, visit our Web site at http://www.analog.com/processors, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- E-mail questions or requests for information to
  processor.support@analog.com (World wide support)
  processor.europe@analog.com (Europe support)
  processor.china@analog.com (China support)
- Fax questions or requests for information to
  1-781-461-3010 (North America)
  +49-89-76903-157 (Europe)

Related Documents

For information on product related development software and hardware, see these publications:

Table 1. Related Processor Publications

Title	Description
ADSP-21375: 266 MHz High Performance SHARC Processor Preliminary Data Sheet	General functional description, pinout, and timing
ADSP-21368 SHARC Processor Hardware Reference (Includes ADSP-21367, ADSP-21368, ADSP-21369, ADSP-21371, ADSP-21375)	Description of internal processor architecture, registers, and all peripheral functions
ADSP-2136x SHARC Processor Programming Reference	Description of all allowed processor assembly instructions

Table 2. Related VisualDSP++ Publications

VisualDSP++ User's Guide	Detailed description of VisualDSP++ features and usage
VisualDSP++ Assembler and Preprocessor Manual	Description of the assembler function and commands

Table 2. Related VisualDSP++ Publications (Cont'd)

VisualDSP++ C/C++ Complier and Library Manual for SHARC Processors	Description of the complier function and commands for SHARC processors
VisualDSP++ Linker and Utilities Manual	Description of the linker function and commands
VisualDSP++ Loader and Utilities Manual	Description of the loader function and commands

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

All documentation is available online. Most documentation is available in printed form.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:
`http://www.analog.com/processors/technicalSupport/technicalLibrary/index.html`.

Online Technical Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, the Dinkum Abridged C++ library, and Flexible License Manager (FlexLM) network license manager software documentation. You can easily search across the entire VisualDSP++ documentation set for any topic of interest. For easy printing, supplementary `.pdf` files of most manuals are provided in the `Docs` folder on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
.chm	Help system files and manuals in Help format
.htm or .html	Dinkum Abridged C++ library and FlexLM network license manager software documentation. Viewing and printing the .html files requires a browser, such as Internet Explorer 5.01 (or higher).
.pdf	VisualDSP++ and processor manuals in Portable Documentation Format (PDF). Viewing and printing the .pdf files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

If documentation is not installed on your system as part of the software installation, you can add it from the VisualDSP++ CD at any time by running the Tools installation. Access the online documentation from the VisualDSP++ environment, Windows® Explorer, or the Analog Devices Web site.

Accessing Documentation From VisualDSP++

To view VisualDSP++ Help, click on the **Help** menu item or go to the Windows task bar and navigate to the VisualDSP++ documentation via the **Start** menu.

To view ADSP-21375 EZ-KIT Lite Help, which is part of the VisualDSP++ Help system, use the **Contents** or **Search** tab of the Help window.

Accessing Documentation From Windows

In addition to any shortcuts you may have constructed, there are many ways to open VisualDSP++ online Help or the supplementary documentation from Windows.

Help system files (.chm) are located in the Help folder, and .pdf files are located in the Docs folder of your VisualDSP++ installation CD-ROM. The Docs folder also contains the Dinkum Abridged C++ library and the FlexLM network license manager software documentation.

Your software installation kit includes online Help as part of the Windows interface. These help files provide information about VisualDSP++ and the ADSP-21375 EZ-KIT Lite evaluation system.

Accessing Documentation From Web

Download manuals at the following Web site: http://www.analog.com/processors/technicalSupport/technicalLibrary/index.html.

Select a processor family and book title. Download archive (`.zip`) files, one for each manual. Use any archive management software, such as WinZip, to decompress downloaded files.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**) and follow the prompts.

VisualDSP++ Documentation Set

To purchase VisualDSP++ manuals, call **1-603-883-2430**. The manuals may be purchased only as a kit.

If you do not have an account with Analog Devices, you are referred to Analog Devices distributors. For information on our distributors, log onto http://www.analog.com/salesdir/continent.asp.

Hardware Tools Manuals

To purchase EZ-KIT Lite and in-circuit emulator (ICE) manuals, call **1-603-883-2430**. The manuals may be ordered by title or by product number located on the back cover of each manual.

Processor Manuals

Hardware reference and instruction set reference manuals may be ordered through the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**), or downloaded from the Analog Devices Web site. Manuals may be ordered by title or by product number located on the back cover of each manual.

Data Sheets

All data sheets (preliminary and production) may be downloaded from the Analog Devices Web site. Only production (final) data sheets (Rev. 0, A, B, C, and so on) can be obtained from the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**); they also can be downloaded from the Web site.

To have a data sheet faxed to you, call the Analog Devices Faxback System at **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. If the data sheet you want is not listed, check for it on the Web site.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 USING ADSP-21375 EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-21375 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "Package Contents" on page 1-2
  Lists the items contained in your ADSP-21375 EZ-KIT Lite package.
- "Default Configuration" on page 1-3
  Shows the default configuration of the ADSP-21375 EZ-KIT Lite.
- "Installation and Session Startup" on page 1-5
  Instructs how to start a new or open an existing ADSP-21375 EZ-KIT Lite session using VisualDSP++.
- "Evaluation License Restrictions" on page 1-7
  Describes the restrictions of the VisualDSP++ license shipped with the EZ-KIT Lite.
- "External Memory" on page 1-7
  Describes how to access external memory and defines the memory map of the EZ-KIT Lite.
- "ELVIS Interface" on page 1-9
  Describes the on-board National Instruments Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) interface.

- "Analog Audio" on page 1-10·
  Describes how to set up and communicate with the on-board audio codec.
- "LEDs and Push Buttons" on page 1-11
  Describes the board's general-purpose IO pins and buttons.
- "Example Programs" on page 1-13
  Provides information about example programs included in the ADSP-21375 EZ-KIT Lite evaluation system.
- "Background Telemetry Channel" on page 1-13
  Highlights the advantages of the Background Telemetry Channel feature of VisualDSP++.

For information on the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online Help.

For detailed information on how to program the ADSP-21375 SHARC processor, refer to the documents referenced in "Related Documents" on page -xvii.

Package Contents

Your ADSP-21375 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-21375 EZ-KIT Lite board
- *VisualDSP++ Installation Quick Reference Card*
- CD containing:
  - VisualDSP++ software
  - ADSP-21375 EZ-KIT Lite debug software

- USB driver files
- Example programs
- *ADSP-21375 EZ-KIT Lite Evaluation System Manual* (this document)

- Universal 7V DC power supply
- USB 2.0 cable
- 3.5 mm stereo headphones
- 6-foot RCA audio cable
- 6-foot 3.5 mm/RCA x 2 Y-cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-21375 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components.

To connect the EZ-KIT Lite board:

1. Remove the EZ-KIT Lite board from the package. Be careful when handling the board to avoid the discharge of static electricity, which may damage some components.
2. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before continuing.

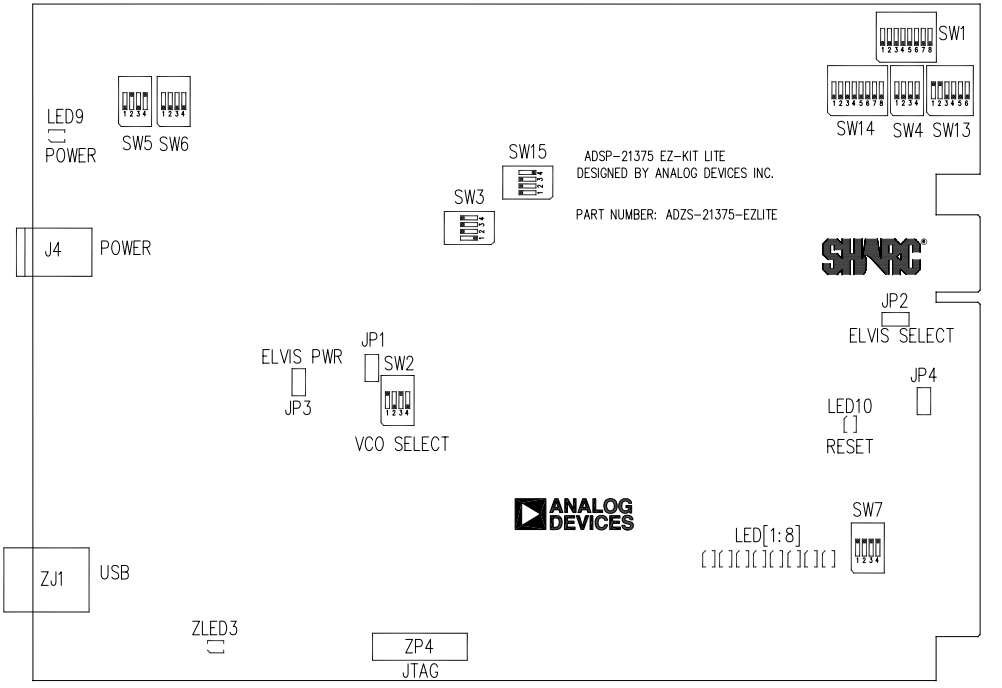

Figure 1-1. EZ-KIT Lite Hardware Setup

3. Plug the provided power supply into J4 on the EZ-KIT Lite board. Visually verify that the green power LED (LED9) is on. Also verify that the red reset LED (LED10) goes on for a moment and then goes off, and, finally, LED1 through LED8 are sequentially blinking.
4. Connect one end of the USB cable to an available full speed USB port on your PC and the other end to ZJ1 on the ADSP-21375 EZ-KIT Lite board.

Installation and Session Startup

For correct operation, install the software and hardware in the order presented in the *VisualDSP++ Installation Quick Reference Card*.

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start** –> **Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 4.

3. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.
    - From the **Session** menu, **New Session**.
    - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
    - From the **Session** menu, **Connect to Target**. Then click **New Session** from the **Session List** dialog box.
4. The **Select Processor** page of the wizard appears on the screen. Ensure **SHARC** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-21375**. Click **Next**.
5. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.
6. The **Select Platform** page of the wizard appears on the screen. In the **Select your platform** list, select **ADSP-21375 EZ-KIT Lite via Debug Agent**. In **Session name**, highlight or specify the session name.

    The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and to open a new session.

    Click **Next**.

7. The **Finish** page of the wizard appears on the screen. The page displays your selections. If you are satisfied, click **Finish**. If not, click **Back** to make changes.

To disconnect from a session, click the disconnect button  or select **Session–>Disconnect from Target**.

To delete a session, select **Session –> Session List**. Select the session name from the list and click **Delete**. Click **OK**.

Evaluation License Restrictions

The ADSP-21375 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

1. VisualDSP++ allows a connection to the ADSP-21375 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
2. The linker restricts a users program to 10922 words of internal memory for code space with no restrictions for data space.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

External Memory

The EZ-KIT Lite contains three types of memory: parallel flash (1 MB), SPI flash (2 Mbit), and SDRAM (128 Mbit). The flash memories can store user-specific boot code, allowing the board to run as a stand-alone unit. For more information about selecting the boot device for the processor, see "Boot Mode and Clock Ratio Select Switch (SW2)" on page 2-9.

Table 1-1 provides start and end addresses of the board's external memories.

Table 1-1. EZ-KIT Lite Evaluation Board External Memory

Start Address	End Address	Content
0x0020 0000	0x011F 0000	SDRAM memory (~MS0)
0x0400 0000	0x040F FFFF	Flash memory (~MS1)
0x0800 0000 0x8000 0000	0x08FF FFFF 0x0BFF FFFF	Unused chip select (~MS2) for non-SDRAM addresses Unused chip select (~MS2) for SDRAM address
0x0C00 0000 0x0C00 0000	0x0CFF FFFF 0x0FFF FFFF	Unused chip select (~MS3) for non-SDRAM addresses Unused chip select (~MS3) for SDRAM addresses

The parallel flash memory and SDRAM connect to the external memory of the processor.

The SDRAM memory connects to the SDRAM controller of the processor. A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory accesses. Care must be taken when configuring the SDRAM control registers. For more information regarding the setup of the SDRAM controller, please refer to the *ADSP-21368 SHARC Processor Hardware Reference* (includes ADSP-21375). An example program is included in the EZ-KIT Lite installation directory to demonstrate the SDRAM setup.

The SPI flash memory connects to the SPI port of the processor and designates:

- DPI pin 5 (DPI5) as a chip select
- DPI pin 3 (DPI3) as the SPI clock
- DPI pin 1 (DPI1) as the MOSI
- DPI pin 2 (DPI2) as the MISO

By default, the DPI is set up for the SPI flash, and any required changes to the SPI flash can be made by modifying the DPI of the processor. An example program is included in the EZ-KIT Lite installation directory to demonstrate the SPI flash memory reads and writes.

The parallel flash memory connects to the asynchronous memory controller of the processor. Each of their respective memory banks can be independently programmed with different timing parameters. For more information on changing wait states to speed up or slow down the asynchronous controller and other setup information, refer to the *ADSP-21368 SHARC Processor Hardware Reference* (includes ADSP-21375). Example programs are included in the EZ-KIT Lite installation directory to demonstrate the flash memory reads and writes.

ELVIS Interface

The ADSP-21375 EZ-KIT Lite board contains the National Instruments Educational Laboratory Virtual Instrumentation Suite interface. The interface features the DC voltage and current measurement modules, oscilloscope and bode analyzer modules, function generator, arbitrary waveform generator, and digital IO.

The ELVIS interface is a LabVIEW-based design and prototype environment for university science and engineering laboratories. The ELVIS interface consists of LabVIEW-based virtual instruments, a multifunction data acquisition (DAQ) device, and a custom-designed bench-top workstation and prototype board. This combination provides a ready-to-use suite of instruments found in most educational laboratories. Because the interface is based on LabVIEW and provides complete data acquisition and prototyping capabilities, the system is ideal for academic coursework that range from lower-division classes to advanced project-based curriculums.

For more information on ELVIS and example demonstration programs, visit National Instruments Web site at `www.ni.com`.

Analog Audio

The AD1835A is a high-performance, single-chip codec featuring four stereo digital-to-analog converters (DACs) for audio output and one stereo analog-to-digital converters (ADCs) for audio input. The codec can input and output data with a sample rate of up to 96 kHz on all channels. A 192 kHz sample rate can be used with one of the DAC channels.

The processor is interfaced with the AD1835A via the DAI port. The DAI interface pins can be configured to transfer serial data from the AD1835A codec in either time-division multiplexed (TDM) or two-wire interface mode (TWI). For more information on the AD1835A connection to the DAI, see "DAI Interface" on page 2-4.

The master input clock (`MCLK`) for the AD1835A device can be generated by the on-board 12.288 MHz oscillator or can be supplied by one of the DAI pins of the processor. Using one of the pins to generate the `MCLK`, as opposed to the on-board oscillator, allows synchronization of multiple devices in the system. It is possible to disable the on-board audio oscillator from driving the audio codec and the processor's input pin. For instructions on how to configure the clock, refer to "Codec Setup Switch (SW3)" on page 2-10.

The AD1835A codec can be configured as a master or as a slave, depending on the DIP switch settings. In master mode, the AD1835A drives the serial port clock and frame sync signals to the processor. In slave mode, the processor must generate and drive all of the serial port clock and frame sync signals. For information on how to set up the mode, refer to "Codec Setup Switch (SW3)" on page 2-10.

The internal configuration registers of the AD1835A codec are configured using the SPI port of the processor. The DPI pin 4 (`DPI4` register) is used as the select for the device. For information on how to configure the multichannel codec, refer to the product datasheet at `http://www.analog.com/en/prod/0,2877,AD1835A,00.html`.

The RCA connector (J10) is used to input analog audio. When using an electret microphone on this connector, configure the SW4 switch according to the instructions in "Electret Microphone Select Switch (SW4)" on page 2-12. The four output channels connect to the RCA connector J5. Channel 4 of the codec connects to the headphone jack J9. For more information about the connectors see "Connectors" on page 2-21.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to configure and use the board's analog audio interface.

LEDs and Push Buttons

The EZ-KIT Lite has eight general-purpose user LEDs and four general-purpose push buttons.

Two of the general-purpose push buttons are attached to the FLAG pins of the processor, while the other two are attached to the DAI pins. All of the push buttons connect to the processor through a DIP switch. The DIP switch allows processor pins, which connect to the push buttons, to be disconnected. See "Push Button Enable Switch (SW7)" on page 2-13 for instructions on how to disable a push button from driving its corresponding processor pin.

The state of the push buttons, connected to the FLAG pins, can be determined by reading the FLAG register. The push buttons connected to the DAI pins must be configured as interrupts. It is necessary to set up an interrupt routine to determine each pin's state. Table 1-2 shows the push button and processor connections. Refer to the related example program shipped with the EZ-KIT Lite for more information.

Table 1-2. Push Button Connections

Push Button Label	Push Button Reference Designator	Processor Pin
PB1	SW8	FLAG1/~IRQ1
PB2	SW11	FLAG0/~IRQ0
PB3	SW10	DAI19
PB4	SW9	DAI20

Table 1-3 summarizes the LED connections to the processor. To use the LEDs connected to the DAI or DPI, configure the respective registers of the processor. For more information, refer to the *ADSP-21368 SHARC Processor Hardware Reference* (includes ADSP-21375).

Table 1-3. LED Connections

LED Reference Designator	Processor Pin
LED1	DPI6
LED2	DPI7
LED3	DPI8
LED4	DPI13
LED5	DPI14
LED6	DAI15
LED7	DAI16
LED8	FLAG3/~MS3/~IRQ3

An example program is included in the EZ-KIT Lite installation directory to demonstrate the functionality of the LEDs and push buttons.

Example Programs

Example programs are provided with the ADSP-21375 EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software in the …\213xx\Examples\ADSP-21375 EZ-KIT Lite subdirectory of the VisualDSP++ installation directory. Please refer to the readme file provided with each example for more information.

Background Telemetry Channel

The ADSP-21375 USB debug agent supports the background telemetry channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting processor execution.

The BTC allows the user to view a variable as it is updated or changed, all while the processor continues to execute. For increased performance of the BTC, including faster reading and writing, please check out our latest line of SHARC processor emulators at http://www.analog.com/processors/sharc/evaluationDevelopment/crosscore/index.html. For more information about the background telemetry channel, see the *VisualDSP++ User's Guide* or online Help.

2 ADSP-21375 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-21375 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the configuration of the ADSP-21375 board and explains how the board components interface with the processor.
- "Switch Settings" on page 2-9
  Shows the location and describes the function of the board switches.
- "LEDs and Push Buttons" on page 2-15
  Shows the location and describes the function of the board LEDs and push buttons.
- "Jumpers" on page 2-18
  Shows the location and describes the function of the board jumpers.
- "Connectors" on page 2-21
  Shows the location and gives the part number for all of the connectors on the board. Also, the manufacturer and part number information is given for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board (Figure 2-1).

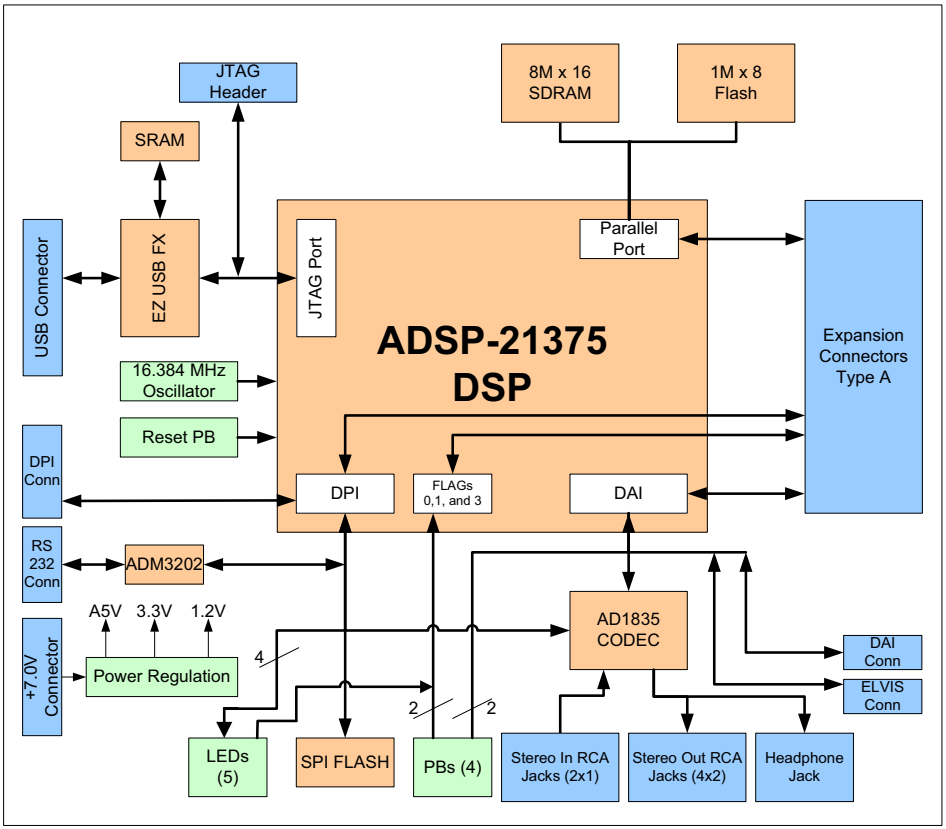

Figure 2-1. System Architecture Block Diagram

This EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-21375 processor. The processor core is powered at 1.2V, and the IO is powered at 3.3V.

The CLKIN pin of the processor connects to a 16.384 MHz oscillator. The core frequency of the processor is derived by multiplying the frequency at the CLKIN pin by a value determined by the state of the processor pins CLKCFG1 and CLKCFG0. The value at these pins is determined by the state of the SW2 switch (see "Boot Mode and Clock Ratio Select Switch (SW2)" on page 2-9). By default, the EZ-KIT Lite gives a core frequency of 262.144 MHz. It is possible to change the speed of the processor by changing the value of the PMCTL register.

The SW2 switch also configures the boot mode of the processor. The EZ-KIT Lite is capable of EPROM/flash boot and SPI boot. By default, the EZ-KIT Lite boots from the flash memory. For information about configuring the boot modes, see "Boot Mode and Clock Ratio Select Switch (SW2)" on page 2-9.

External Port

The external port of the ADSP-21375 processor consists of a 24-bit address bus, 16-bit data memory bus, and control lines. The control lines are used to select, read, and write to external memory devices.

The external port connects to an 8-bit parallel flash memory and a 16-bit SDRAM memory. See "External Memory" on page 1-7 for more information about accessing the flash and SDRAM memories.

All of the external port signals are available externally via the expansion interface connectors (J1-3). The pinout of the connectors can be found in "ADSP-21375 EZ-KIT Lite Schematic" on page B-1.

DAI Interface

The digital application interface (DAI) pins connect to the signal routing unit (SRU) of the processor. The SRU is a flexible routing system, providing a large system of signal flows within the processor. In general, the SRU allows to route the DAI pins to different internal peripherals in various combinations.

The DAI pins connect to the AD1835A audio codec, a 26-pin header, two RCA connectors, audio oscillator output, an external phase lock loop (PLL) circuit, two LEDs, and two push buttons. Figure 2-2 illustrates the EZ-KIT Lite's connections to the DAI.

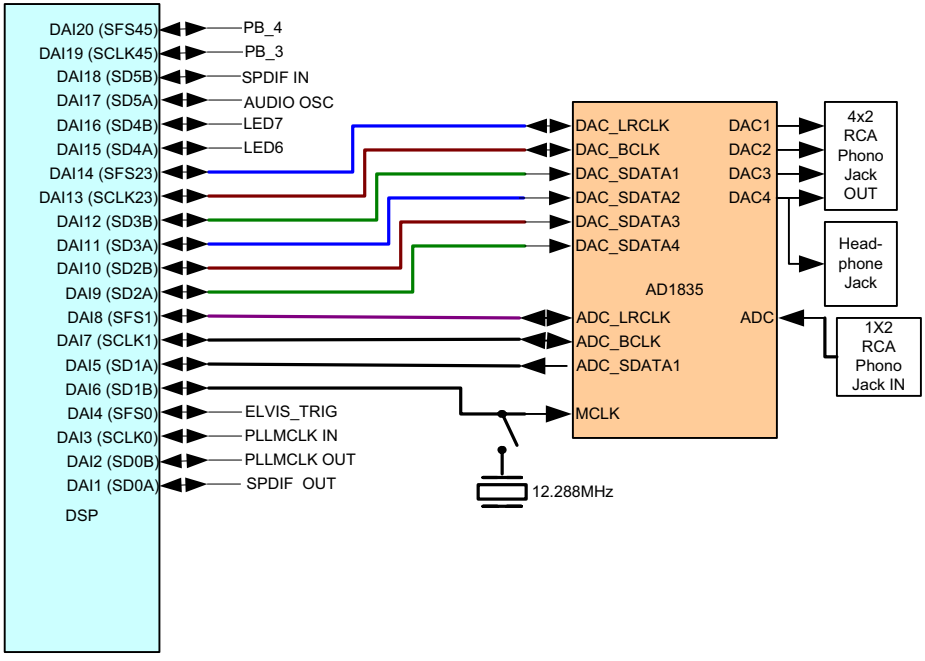

Figure 2-2. DAI Connections Block Diagram

To use the DAI for a different purpose, disable any signal driving the DAI pin with a switch (see "Codec Setup Switch (SW3)" on page 2-10). In addition, the SW3 switch allows flexible routing of the 12.288 MHz audio oscillator's output signal. By default, this signal is used as the master clock (MCLK) for the AD1835A codec.

All of the DAI signals are available externally via the expansion interface connectors (J1-3), as well as the 0.1" spaced header P4. The pinout of the connectors can be found in "ADSP-21375 EZ-KIT Lite Schematic" on page B-1.

DPI Interface

The digital peripheral interface (DPI) pins connect to a second signal routing unit of the processor (SRU2). The SRU2 unit, similar to the SRU, is a flexible routing system, providing a large system of signal flows within the processor. In general, the SRU2 allows to route the DPI pins to different internal peripherals in various combinations.

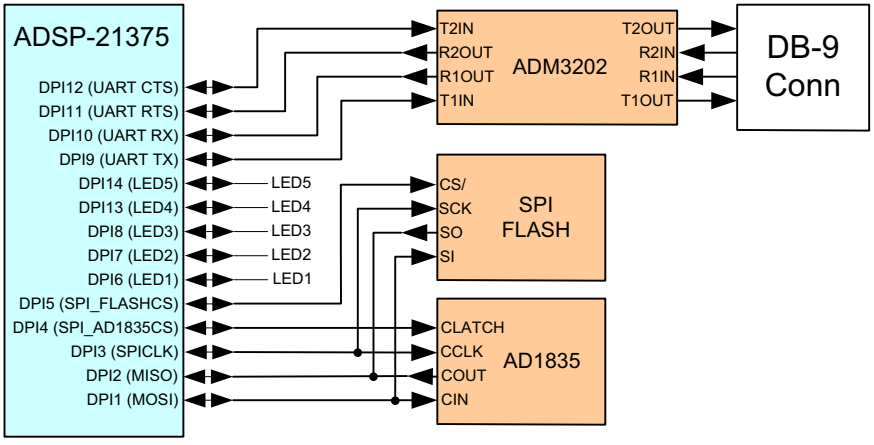

Figure 2-3. DPI Connections Block Diagram

The DPI pins connect to the SPI flash memory, the SPI interface of the AD1835A codec, a UART, a 20-pin header, and five LEDs. Figure 2-3 illustrates the EZ-KIT Lite's connections to the DPI.

To use the DPI for a different purpose, disable any signal driving the DPI pins with a switch (see "UART Enable Switch (SW5)" on page 2-12). Any DPI pin connected to a LED can be used without having to disconnect the pin. You can, however, see the respective LED turn ON and OFF when using the signal elsewhere on the board.

All of the DPI signals are available externally via the expansion interface connectors (J1-3), as well as the 0.1" spaced header P3. The pinout of these connectors can be found in "ADSP-21375 EZ-KIT Lite Schematic" on page B-1.

FLAG Pins

The processor has four general-purpose IO flag pins. Table 2-1 describes the flag connections.

Table 2-1. IO FLAG Pins

FLAG Pin	EZ-KIT Lite Function
FLAG0	Push button (SW2) input
FLAG1	Push button (SW2) input
FLAG2	SDRAM chip select
FLAG3	LED8

For information on how to disable a push button from driving its corresponding processor flag pin, see "Push Button Enable Switch (SW7)" on page 2-13.

The FLAG signals are available externally via the expansion interface connectors (J1-3). The pinout of these connectors can be found in "ADSP-21375 EZ-KIT Lite Schematic" on page B-1.

External PLL

The ADSP-21375 EZ-KIT Lite contains an external phase lock loop to help generate a faster and more stable master input clock MCLK. The PLL uses DAI pin 3 as an input clock from the ADSP-21375 processor. The new clock generated by PLL connects to the processor via DAI pin 2.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to configure and use the board's external PLL.

Expansion Interface

The expansion interface consists of the three 90-pin connectors. Table 2-2 shows the interfaces each connector provides. For the exact pinout of the connectors, refer to "ADSP-21375 EZ-KIT Lite Schematic" on page B-1. The mechanical dimensions of the connectors can be obtained from Technical or Customer Support.

Table 2-2. Expansion Interface Connectors

Connector	Interfaces
J1	5V, ADDR23-0, DATA31-0
J2	3.3V, FLAG3-0, DAIP20-1, DPI14-1, SDRAM control signals
J3	5V, 3.3V, reset, parallel port control signals

Limits to the current and to the interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry also can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the internal and external memory of the processor through a 6-pin interface. The JTAG emulation port of the processor also connects to the USB debugging interface. When an emulator connects to the board at `ZP4`, the USB debugging interface is disabled. This is not a standard connection of the JTAG interface.

For information about the standard connection of the interface, see *EE-68* published on the Analog Devices Web site. For more information about the JTAG connector, see "JTAG Header (ZP4)" on page 2-25. To learn more about available SHARC processor emulators, go to `http://www.analog.com/proces-sors/sharc/evaluationDevelopment/crosscore/index.html`.

Switch Settings

This section describes the function of the EZ-KIT Lite switches. Figure 2-4 shows the switch locations and default settings.

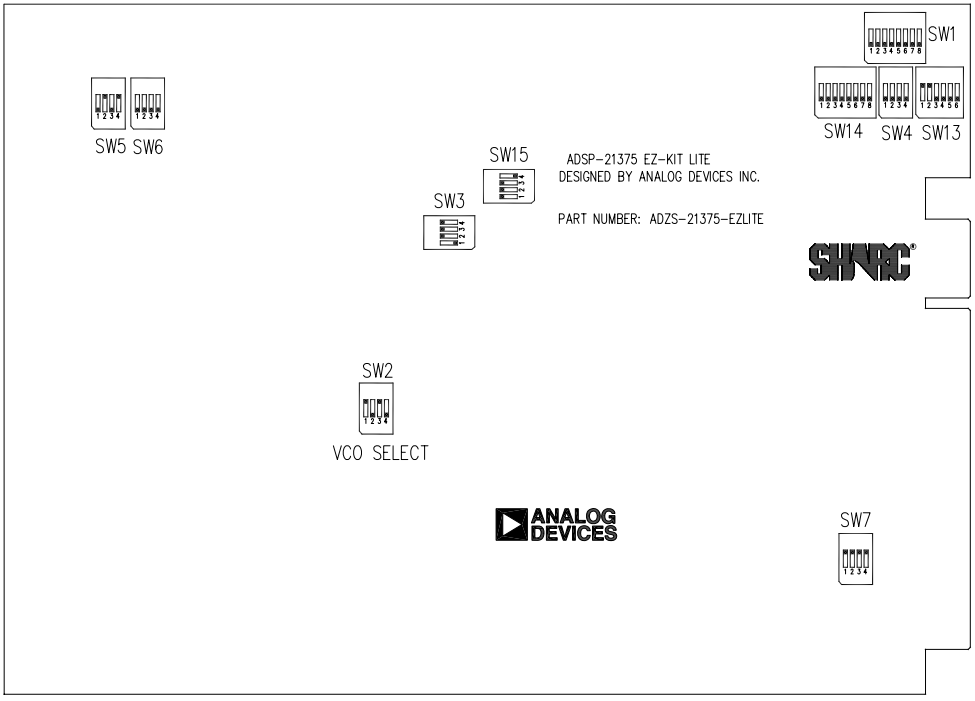

Figure 2-4. Switch Locations and Default Settings

Boot Mode and Clock Ratio Select Switch (SW2)

The SW2 switch sets the boot mode and clock multiplier ratio. Table 2-3 shows how to set up the boot mode using SW2 positions 1 and 2. By default, the EZ-KIT Lite boots in external port mode from the flash memory.

Table 2-3. Boot Mode Configuration Switch (SW2)

BOOTCFG0 Pin (Position 1)	BOOTCFG1 Pin (Position 2)	Boot Mode
ON	ON	SPI slave boot
ON	**OFF**	**Parallel flash boot (default)**
OFF	ON	SPI master boot
OFF	OFF	Reserved

Table 2-4 shows how to set up the clock multiply ratio using SW2 positions 3 and 4. By default, the processor increases the clock multiply ratio by sixteen, setting the core clock to 262.144 MHz.

Table 2-4. Core Clock Rate Configuration

CLKCFG0 (Position 3)	CLKCFG1 (Position 4)	Core to CLKIN Ratio
ON	ON	6:1
ON	**OFF**	**16:1 (default)**
OFF	ON	32:1
OFF	OFF	Reserved

The core clock frequency can be increased or decreased via software by writing to the PMCTL register. For more information on changing the core clock frequency and other setup information, refer to the *ADSP-21368 SHARC Processor Hardware Reference* (includes ADSP-21375).

Codec Setup Switch (SW3)

The codec setup switch (SW3) can be used to change the routing of some signals going to the AD1835A codec and to set up the communication protocol of the codec.

SW3 positions 1 and 2 determine the clock routing for the audio oscillator to the codec and to the processor. Figure 2-5 illustrates how the switch positions 1 and 2 connect on the board. In the default position, route the DAI_P17 pin to DAI_P6 (in software) to clock the AD1835A codec.

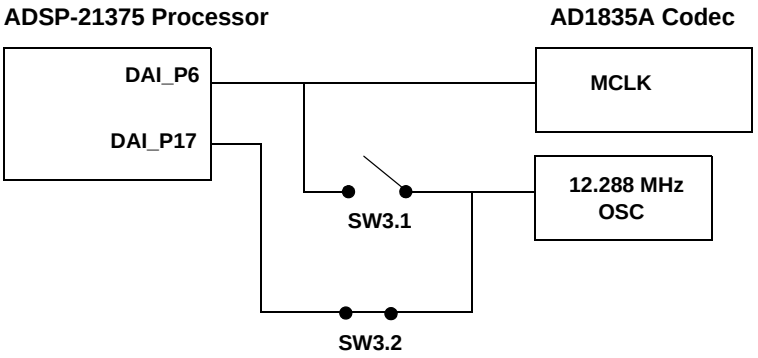

Figure 2-5. Audio Clock Routing

SW3 position 3 determines if the AD1835A device is a master or a slave. If the AD1835A is a master, the device's serial interface generates the frame sync and clock signals necessary to transfer data. When the device is a slave, the processor must generate the frame sync and clock signals. By default, position 3 is ON, and the AD1835A codec generates the control signals.

SW3 position 4 disconnects the AD1835A codec's ADC_DATA pin from the DAI interface. This is useful when the DAI interface connects to another device.

Electret Microphone Select Switch (SW4)

To connect an electret microphone to the audio input, place all positions of the SW4 switch ON. The default position of the switch is all OFF. When all of the SW4 positions are ON, a DC offset of 2.5V is added to the signal, and gain of the input amplifiers is changed from 1x to 10x.

UART Enable Switch (SW5)

The UART enable switch (SW5) disconnects UART signals from the DPI pins of the processor. When the switch is OFF, the associated DPI signal (see Table 2-5) can be used on the expansion interface.

Table 2-5. UART Enable Switch (SW5)

Switch Position	EZ-KIT Lite Signal	Processor Signal
1 (**OFF**[1])	CTS	DPI12
2 (**ON**)	RX	DPI10
3 (**OFF**)	RTS	DPI11
4 (**ON**)	T2IN tied to R2OUT	N/A

1 Bold typeface denotes the default setting.

Loop-Back Test Switches (SW6 and SW14)

The loop-back test switch SW6 is located at the top left side of the board. The second loop-back test switch, SW14, is located at the top right side of the board. These switches are used only for testing; all switch positions should remain OFF.

Push Button Enable Switch (SW7)

The push button enable switch (SW7) disconnects the push buttons from the corresponding processor pins. This allows the signals to be used elsewhere on the board. Table 2-6 shows the SW7 connections. By default, all position of the SW7 switch are ON, allowing the push buttons to function as designed.

Table 2-6. Push Button Enable Switch (SW7)

Switch Position	Push Button Label	Push Button Reference Designator	Processor Pin
1	PB1	SW8	FLAG1/~IRQ
2	PB2	SW11	FLAG0/~IRQ0
3	PB3	SW10	DAI19
4	PB4	SW9	DAI20

ELVIS Oscilloscope Configuration Switch (SW1)

The oscilloscope configuration switch (SW1) determines which audio circuit signals connect to channels A and B of the oscilloscope. The switch is used only when the board connects to the Educational Laboratory Virtual Instrumentation Suite (ELVIS) station (see "ELVIS Interface" on page 1-9). Each channel must have only one signal selected at a time, as described in Table 2-7.

Table 2-7. Oscilloscope Configuration Switch (SW1)

Channel	Switch Position	Audio Circuit Signal
A	1 (**OFF**[1])	AMP_LEFT_IN
A	2 (**OFF**)	AMP_RIGHT_IN
A	3 (**OFF**)	LEFT_OUT
A	4 (**OFF**)	RIGHT_OUT
B	5 (**OFF**)	AMP_LEFT_IN

Table 2-7. Oscilloscope Configuration Switch (SW1) (Cont'd)

Channel	Switch Position	Audio Circuit Signal
B	6 (**OFF**)	AMP_RIGHT_IN
B	7 (**OFF**)	LEFT_OUT
B	8 (**OFF**)	RIGHT_OUT

1 Bold typeface denotes the default settings.

ELVIS Function Generator Configuration Switch (SW13)

The function generator configuration switch (SW13) controls which signals connect to the left and right input signals of the audio interface. The SW13 switch is used only when the board connects to the ELVIS station (see "ELVIS Interface" on page 1-9). Each channel must have only one signal selected at a time, as described in Table 2-8.

Table 2-8. ELVIS Function Generator Configuration Switch (SW13)

Channel	Switch Position	Audio Signal
AMP_LEFT_IN	1 (**ON**[1])	LEFT_IN
AMP_RIGHT_IN	2 (**ON**)	RIGHT_IN
AMP_LEFT_IN	3 (**OFF**)	DAC0
AMP_RIGHT_IN	4 (**OFF**)	DAC1
AMP_LEFT_IN	5 (**OFF**)	FUNCT_OUT
AMP_RIGHT_IN	6 (**OFF**)	FUNCT_OUT

1 Bold typeface denotes the default settings.

AD1835A and Flash Disconnect Switch (SW15)

The AD1835A and flash disconnect switch (SW15) disconnects the following signals: DPI4_SPI_AD1835_CS, DAIP8_ADC_LRCLK, and DPI5_SPI_FLASH_CS. The switch is used only for expansion interface purposes; by default, the switch positions 1–3 are ON and position 4 is OFF.

LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 2-6 shows the LED and push button locations.

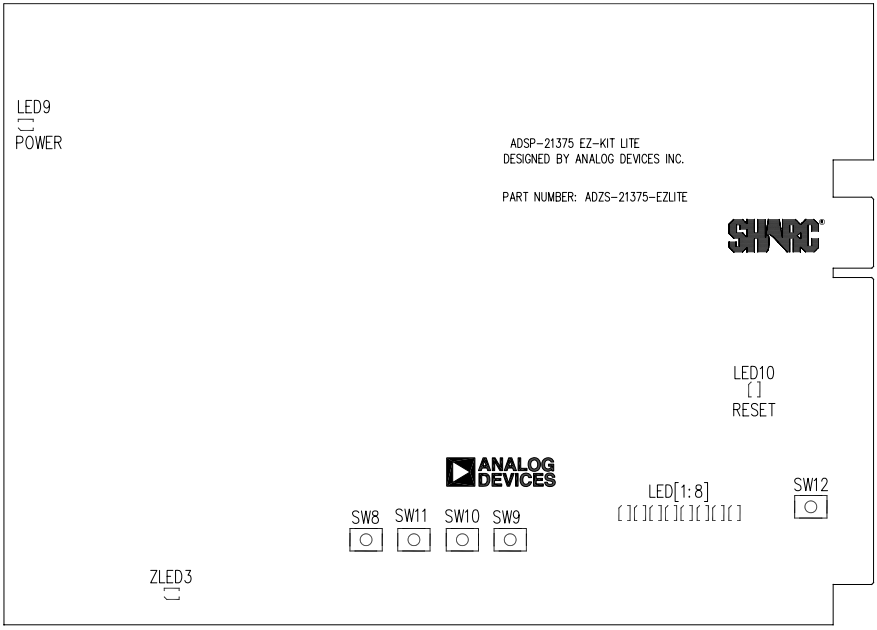

Figure 2-6. LED and Push Button Locations

General Purpose LEDs (LED1–8)

There are eight general-purpose LEDs on the board. Five LEDs connect to the DPI interface, two LEDs connect to the DAI interface, and one LED connects to FLAG3 of the processor. "LEDs and Push Buttons" on page 1-11 summarizes the LED connections. The respective registers of the processor must be programmed appropriately in order to use LEDs connected to the DAI or DPI. For more information on how to program the registers, refer to the *ADSP-21368 SHARC Processor Hardware Reference* (includes ADSP-21375).

Power LED (LED9)

When LED9 is lit (green), it indicates that power is being supplied to the board properly.

Reset LED (LED10)

When LED10 is lit (red), the master reset of all the major ICs is active.

USB Monitor LED (ZLED3)

The USB monitor LED (ZLED3) indicates that USB communication has been initialized successfully, and you can connect to the processor using a VisualDSP++ EZ-KIT Lite session. Once the USB cable is plugged into the board, it takes approximately 15 seconds for the USB monitor LED to light. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver (see the *VisualDSP++ Installation Quick Reference Card*).

When VisualDSP++ is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Push Buttons (SW8–11)

Four push buttons (SW8-11) are provided for general-purpose user input: two push buttons connect to the FLAG pins of the processor, while the other two connect to the DAI of the processor. The push buttons are active high and, when pressed, send a high (1) to the processor. Refer to "LEDs and Push Buttons" on page 1-11 for more information. The push button enable switch (SW7) is capable of disconnecting the push buttons from the corresponding processor pins (refer to "Push Button Enable Switch (SW7)" on page 2-13 for more information).

The push buttons and corresponding processor signals are summarized in Table 2-9.

Table 2-9. Push Button Connections

Push Button Label	Push Button Reference Designator	Processor Pin
PB1	SW8	FLAG1/~IRQ1
PB2	SW11	FLAG0/~IRQ0
PB3	SW10	DAI19
PB4	SW9	DAI20

Board Reset Push Button (SW12)

The RESET push button (SW12) resets all of the ICs on the board. The only exception is the USB interface chips. These chips are not being reset when the push button is pressed after the USB cable has been plugged in and communication correctly initialized with the PC. After USB communication has been initialized, the only way to reset the USB is by powering down the board.