

Blackfin FPGA EZ-Extender Manual

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Regulatory Compliance

The Blackfin FPGA EZ-Extender has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the “CE” mark.

The Blackfin FPGA EZ-Extender had been appended to Analog Devices Development Tools Technical Construction File referenced “DSPTOOLS1” dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.



The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.



CONTENTS

PREFACE

Product Overview	ix
Purpose of This Manual	xi
Intended Audience	xi
Manual Contents	xii
What's New in This Manual	xii
Technical or Customer Support	xiii
Supported Products	xiii
Product Information	xiv
Related Documents	xiv
Notation Conventions	xvi

FPGA EZ-EXTENDER INTERFACES

FPGA EZ-Extender Setup	1-1
FPGA Software and Firmware	1-2
FPGA EZ-Extender Overview	1-3

FPGA EZ-EXTENDER HARDWARE REFERENCE

System Architecture	2-2
Programming the FPGA	2-3

CONTENTS

FPGA Programming via JTAG	2-4
FPGA Programming via Serial ROM	2-5
FPGA Programming via Blackfin Application	2-6
Programming the Serial ROM	2-7
Serial ROM via JTAG Header	2-7
Power	2-8
Power In Header (P12)	2-9
3.3V Header (P13)	2-9
2.5V Header (P42)	2-10
1.2V Header (P43)	2-10
Jumpers	2-11
Serial ROM Boot Jumper (JP1)	2-12
Config Done Jumper (JP2)	2-12
Config Program Jumper (JP3)	2-13
Boot Jumper (JP4)	2-14
FPGA Input Jumpers (JP5)	2-14
Push Buttons and LEDs	2-15
Program Push Button (SW1)	2-15
PB1 Push Button (SW3)	2-15
PB2 Push Button (SW4)	2-16
Status LEDs (LED1–8)	2-17
Power LED (LED9)	2-17
Done LED (LED10)	2-17
Connectors	2-18

Expansion Interface (P1–3 and J1–3)	2-19
IDC Connectors (P8, P14, P16, and P17)	2-19
IDC Connectors (P5 and P7)	2-20
High-Speed Connector (P4)	2-20

BILL OF MATERIALS

SCHEMATICS

INDEX

CONTENTS

PREFACE

Thank you for purchasing the Blackfin[®] Field-Programmable Gate Array (FPGA) EZ-Extender, Analog Devices, Inc. (ADI) extension board to the EZ-KIT Lite[®] evaluation system for ADSP-BF533, ADSP-BF537, and ADSP-BF561 Blackfin processors.

The Blackfin processors are embedded processors that support a Media Instruction Set Computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing characteristics towards delivering signal processing performance in a microprocessor-like environment.

The EZ-KIT Lite and FPGA EZ-Extender are designed to be used in conjunction with the VisualDSP++[®] development environment. VisualDSP++ offers a powerful programming tool with new flexibility that significantly decreases the time required to port software code to a processor, reducing time-to-market.

To learn more about Analog Devices development software, go to <http://www.analog.com/processors/tools/>.

Product Overview

The Blackfin FPGA EZ-Extender is a separately sold extension board that plugs onto the expansion interface of the ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite evaluation system. The extension board aids the design and prototyping phases of ADSP-BF533, ADSP-BF537, or ADSP-BF561 processor targeted applications.

Product Overview

The board extends the capabilities of the evaluation system by providing a Xilinx FPGA with external memory, IDC connectors for off-board connections, and a small bread board area.

The Blackfin FPGA EZ-Extender features:

- Xilinx Spartan III Field-Programmable Gate Array
 - ✓ XC3S1000
 - ✓ FG456 package
- Asynchronous static random access memory (SRAM)
 - ✓ Directly connected to FPGA
 - ✓ 2 MB (512K x 16 bits x 2 chips)
 - ✓ TSOP44 package
- 25 MHz oscillator
 - ✓ Directly connected to global clock of FPGA
- Socket for auxiliary oscillator
 - ✓ Directly connected to global clock of FPGA
- IDC thru-hole connectors
 - ✓ Allows quick access to Blackfin and FPGA pins for probing
 - ✓ Allows access to Blackfin and FPGA pins for off-board connections
- High-speed connector
 - ✓ Allows access to Blackfin and FPGA pins for high-speed application
- Expansion interface connectors
 - ✓ Allows access to ADI's family of Blackfin EZ-Extenders

- Two push buttons
 - ✓ Directly connected to FPGA
 - ✓ One with external debounce circuitry and one without
- Eight flag LEDs
 - ✓ Directly connected to FPGA

Before using any of the interfaces, follow the setup procedure in [“FPGA EZ-Extender Setup” on page 1-1](#).

Example programs are available to demonstrate the capabilities of the Blackfin FPGA EZ-Extender board.

Purpose of This Manual

The *Blackfin FPGA EZ-Extender Manual* describes the operation and configuration of the components on the extension board. A schematic and a bill of materials are provided as a reference for future Blackfin processor board designs.

Intended Audience

This manual is a user’s guide and reference to the Blackfin FPGA EZ-Extender. Programmers who are familiar with the Analog Devices Blackfin processor architecture, operation, and development tools are the primary audience for this manual. The user should also be familiar with basic FPGA development and Xilinx’s Spartan III family of FPGAs.

Programmers who are unfamiliar with VisualDSP++ or EZ-KIT Lite evaluation software should refer to the *ADSP-BF533*, *ADSP-BF537*, or *ADSP-BF561 Evaluation System Manual*, VisualDSP++ online Help, and user’s or getting started guides. For the locations of these documents, refer to [“Related Documents”](#).

Manual Contents

The manual consists of:

- Chapter 1, “[FPGA EZ-Extender Interfaces](#)” on page 1-1
Provides basic board information.
- Chapter 2, “[FPGA EZ-Extender Hardware Reference](#)” on page 2-1
Provides information on the hardware aspects of the board.
- Appendix A, “[Bill Of Materials](#)” on page A-1
Provides a list of components used to manufacture the EZ-Extender board.
- Appendix B, “[Schematics](#)” on page B-1
Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.



This appendix is not part of the online Help. The online Help viewers should go to the PDF version of the *Blackfin FPGA EZ-Extender Manual* located in the Docs\EZ-KIT Lite Manuals folder on the installation CD to see the schematics. Alternatively, the schematics can be found on the Analog Devices Web site, www.analog.com/processors.

What's New in This Manual

This is the first edition of the *Blackfin FPGA EZ-Extender Manual*.

Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:

- Visit the Embedded Processing and DSP products Web site at <http://www.analog.com/processors/technicalSupport>
- E-mail tools questions to processor.tools.support@analog.com
- E-mail processor questions to processor.support@analog.com (World wide support)
processor.europe@analog.com (Europe support)
processor.china@analog.com (China support)
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:
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USA

Supported Products

The Blackfin FPGA EZ-Extender is designed as an extension board to the ADSP-BF533, ADSP-BF537, and ADSP-BF561 EZ-KIT Lite evaluation systems.

Product Information

You can obtain product information from the Analog Devices Web site, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at www.analog.com. Our Web site provides information about a broad range of products—analogue integrated circuits, amplifiers, converters, and digital signal processors.

Related Documents

For information on product related development software, see the following publications.

Table 1. Related Processor Publications

Title	Description
<ul style="list-style-type: none">• <i>ADSP-BF533 Embedded Processor Datasheet</i>• <i>ADSP-BF536/ADSP-BF537 Embedded Processor Datasheet</i>• <i>ASP-BF561 Blackfin Embedded Symmetric Multi-Processor Datasheet</i>	General functional description, pinout, and timing.
<ul style="list-style-type: none">• <i>ADSP-BF533 Blackfin Processor Hardware Reference</i>• <i>ADSP-BF537 Blackfin Processor Hardware Reference</i>• <i>ASP-BF561 Blackfin Processor Hardware Reference</i>	Description of internal processor architecture and all register functions
<i>Blackfin Processor Instruction Set Reference</i>	Description of all allowed processor assembly instructions.

Table 2. Related VisualDSP++ Publications

Title	Description
<ul style="list-style-type: none"> • <i>ADSP-BF533 EZ-KIT Lite Evaluation System Manual</i> • <i>ADSP-BF537 EZ-KIT Lite Evaluation System Manual</i> • <i>ADSP-BF561 EZ-KIT Lite Evaluation System Manual</i> 	Description of the EZ-KIT Lite features and usage. Note: For the ADSP-BF537 EZ-KIT Lite, there is additional <i>Getting Started with ADSP-BF537 EZ-KIT Lite</i> .
<i>VisualDSP++ User's Guide</i>	Description of VisualDSP++ features and usage
<i>VisualDSP++ Assembler and Preprocessor Manual</i>	Description of the assembler function and commands
<i>VisualDSP++ C/C++ Compiler and Library Manual for Blackfin Processors</i>	Description of the compiler function and commands for Blackfin processors
<i>VisualDSP++ Linker and Utilities Manual</i>	Description of the linker function and commands
<i>VisualDSP++ Loader Manual</i>	Description of the loader function and commands

All documentation is available online. Most documentation is available in printed form.




Visit the Technical Library Web site to access all processor and tools manuals and data sheets:


<http://www.analog.com/processors/resources/technicalLibrary>.

For more information on the Xilinx Spartan III FPGA, refer to the datasheet located at www.xilinx.com.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
{this that}	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as <i>this</i> or <i>that</i> . One or the other is required.
[this that]	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional <i>this</i> or <i>that</i> .
[this,...]	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipsis; read the example as an optional comma-separated list of <i>this</i> .
.SECTION	Commands, directives, keywords, and feature names are in text with letter gothic font.
<i>filename</i>	Non-keyword placeholders appear in text with italic style format.
	Note: For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word Note appears instead of this symbol.
	Caution: Incorrect device operation may result if ... Caution: Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word Caution appears instead of this symbol.
	Warning: Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word Warning appears instead of this symbol.

 Additional conventions, which apply only to specific chapters, may appear throughout this document.

1 FPGA EZ-EXTENDER INTERFACES

This chapter provides the setup procedures for both the Blackfin Field-Programmable Gate Array (FPGA) EZ-Extender and EZ-KIT Lite (ADSP-BF533, ADSP-BF537 or ADSP-BF561). It also provides an overview of the extender board.

The information is presented in the following order.

- [“FPGA EZ-Extender Setup” on page 1-1](#)
- [“FPGA Software and Firmware” on page 1-2](#)
- [“FPGA EZ-Extender Overview” on page 1-3](#)

FPGA EZ-Extender Setup

It is very important to set up all of the components of the system containing the FPGA EZ-Extender before applying power to that system. The following procedure is recommended.

Power your system when these steps are completed:

1. Read the applicable design interface section in this chapter—the text provides an overview of the capabilities of the EZ-Extender.
2. Read [“System Architecture” on page 2-2](#) to understand the physical connections of the extender board. For detailed information, refer to [“Schematics on page B-1”](#).

FPGA Software and Firmware

3. Remove any rubber feet attached to the EZ-KIT Lite if the feet cover the printed circuit board (PCB) mounting holes. In place of the rubber feet, install the four nylon feet and screws provided with the FPGA EZ-Extender. Install the nylon feet in the mounting holes of the EZ-KIT Lite's PCB. Flip the EZ-KIT Lite upside down so that the three expansion headers (J1-3) are facing up.
4. Set the switches and jumpers on the FPGA EZ-Extender board. Use the block diagram in [Figure 2-1 on page 2-2](#) in conjunction with ["Jumpers" on page 2-11](#).
5. Set the switches and jumpers on the EZ-KIT Lite board. If not already, familiarize yourself with the documentation and schematics of the EZ-KIT Lite (see ["Related Documents" on page -xiv](#)). Compare the expansion interface signals of the FPGA EZ-Extender board with the signals of the EZ-KIT Lite board to ensure there is no contention. For example, it may be necessary to disable other devices connected to the expansion interface of the processor and disable the push buttons on the EZ-KIT Lite.
6. Install the FPGA EZ-Extender on the EZ-KIT Lite via the three-connector expansion interface. [Figure 1-1](#) shows how an FPGA EZ-Extender plugs onto an EZ-KIT Lite.
7. Configure any other interfacing boards, for example, another EZ-Extender.

FPGA Software and Firmware

For information on the FPGA software, refer to the `FPGA Software Readme.txt` file located in the `...\Blackfin\EZ-KITs\FPGA EZ-EXTENDER` subdirectory of the VisualDSP++ installation directory.

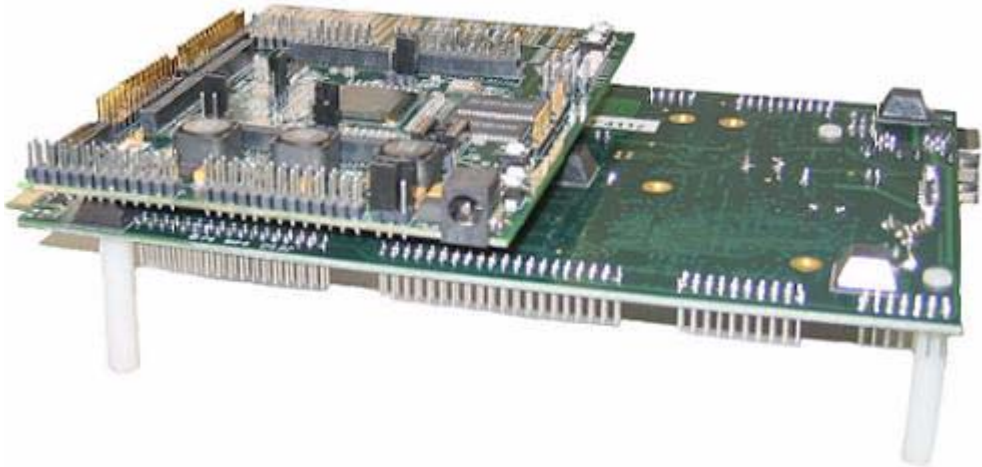


Figure 1-1. FPGA EZ-Extender Setup

FPGA EZ-Extender Overview

The Blackfin FPGA EZ-Extender connects a Xilinx[®] Spartan III Field-Programmable Gate Array (FPGA for short) to the ADSP-BF533, ADSP-BF537, or the ADSP-BF561 EZ-KIT Lite. The FPGA connects to the Blackfin processor via the expansion interface.

The extender board, by default, is powered by an external 7V power supply provided with the product. You can also power the FPGA EZ-Extender by the expansion interface of the EZ-KIT Lite or an external power supply. An external supply must be used whenever application code exceeds the recommended core and IO power supported by the FPGA EZ-Extender. For more information on the jumper and connector settings required to power the extender, review [“Power” on page 2-8](#) as well as the schematics in Appendix C.

FPGA EZ-Extender Overview

The FPGA EZ-Extender contains 2 MB of asynchronous SRAM memory, powered by a 3.3V supply. The SRAM memory connects to banks 6 and 7 of the FPGA and can perform simple data storage instructions in application-specific code.

The FPGA EZ-Extender includes a 25 MHz oscillator (U6) connected to the FPGA via the dedicated global clock 1 (GCLK1) pin, facilitating development of applications that require a clock. A second clock socket (U7) is left unpopulated to allow a user to place an oscillator with a specific frequency for the FPGA. The second clock socket connects to the global clock 6 (GCLK6) pin of the FPGA.

The extender has eight LEDs (LED1-8) and two push buttons (SW3-4) for applications that require status reporting and user control. The push buttons are active `low` and when pressed, provide a logic 0 to the respective FPGA nets. For inputs that require a permanent input `low`, use the jumper inputs on JP4. When a jumper is populated on one of the four nets of JP4, the respective pin is hard wired to a logic 0. For more information about the LEDs, push button switches, and jumper inputs, refer to [“FPGA EZ-Extender Hardware Reference” on page 2-1](#).

There are various ways to program the FPGA. By default, the FPGA is programmed in its slave serial mode by the flash programming utility in VisualDSP++. The program configures the FPGA using the Blackfin processor’s flag pins and/or serial port pins. For more information on how to use the flash programming utility within VisualDSP++, refer to the `FPGA Software Readme.txt` file located in the `...\\Blackfin\\EZ-KITs\\FPGA EZ-EXTENDER` subdirectory of the VisualDSP++ installation directory.

A second method of programming the FPGA is by using a Xilinx JTAG cable and software. The Xilinx JTAG cable connects to the FPGA JTAG header (P15). For more information about programming the FPGA via a Xilinx JTAG cable, refer to the manufacturer’s website at www.xilinx.com.

The third and final way to program the FPGA is via the Xilinx serial ROM on the FPGA EZ-Extender. The serial ROM used for FPGA is shipped with the extender and is pre-programmed. If the serial ROM needs to be re-programmed with new code, use an Xilinx JTAG cable and software and connect the Xilinx JTAG cable to the flash JTAG header (P6).

More information about programming the serial ROM can be found at www.xilinx.com. More details about the different ways to program the FPGA can be found in “[FPGA EZ-Extender Hardware Reference](#)” on [page 2-1](#).

FPGA EZ-Extender Overview

2 FPGA EZ-EXTENDER HARDWARE REFERENCE

This chapter describes the hardware design of the Field-Programmable Gate Array (FPGA) EZ-Extender.

The following topics are covered.

- [“System Architecture” on page 2-2](#)
Describes the configuration of the extender board and explains how the board components interface with the processor and EZ-KIT Lite.
- [“Programming the FPGA” on page 2-3](#)
Describes the different methods of programming the FPGA.
- [“Programming the Serial ROM” on page 2-7](#)
Describes the method of programming the serial ROM.
- [“Power” on page 2-8](#)
Describes the methods to power the extender board.
- [“Jumpers” on page 2-11](#)
Describes the function of the configuration jumpers.
- [“Push Buttons and LEDs” on page 2-15](#)
Describes the function of the push buttons and LEDs.
- [“Connectors” on page 2-18](#)
Describes the function of the extender connectors.

System Architecture

A block diagram of the Blackfin FPGA EZ-Extender is shown in [Figure 2-1](#).

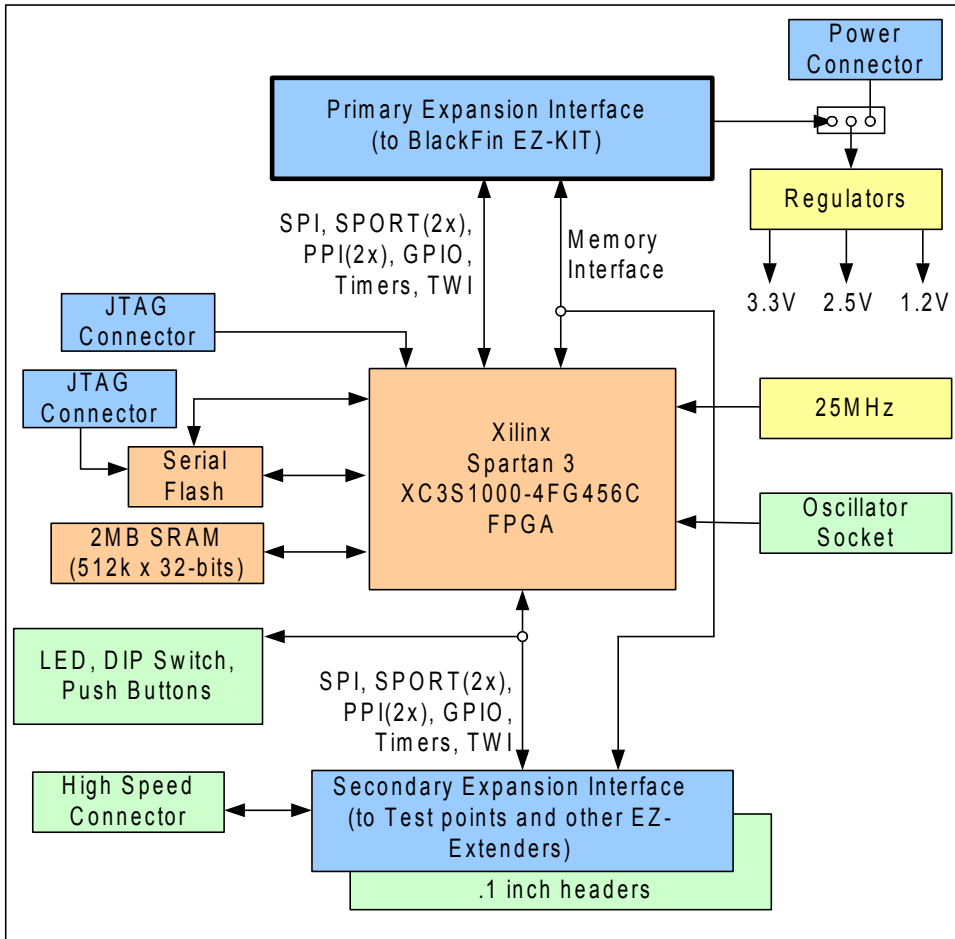


Figure 2-1. Block Diagram

Programming the FPGA

Before using the Blackfin FPGA EZ-Extender, follow the steps in “[FPGA EZ-Extender Setup](#)” on page 1-1.

Figure 2-2 is a block diagram of the FPGA programming connections.

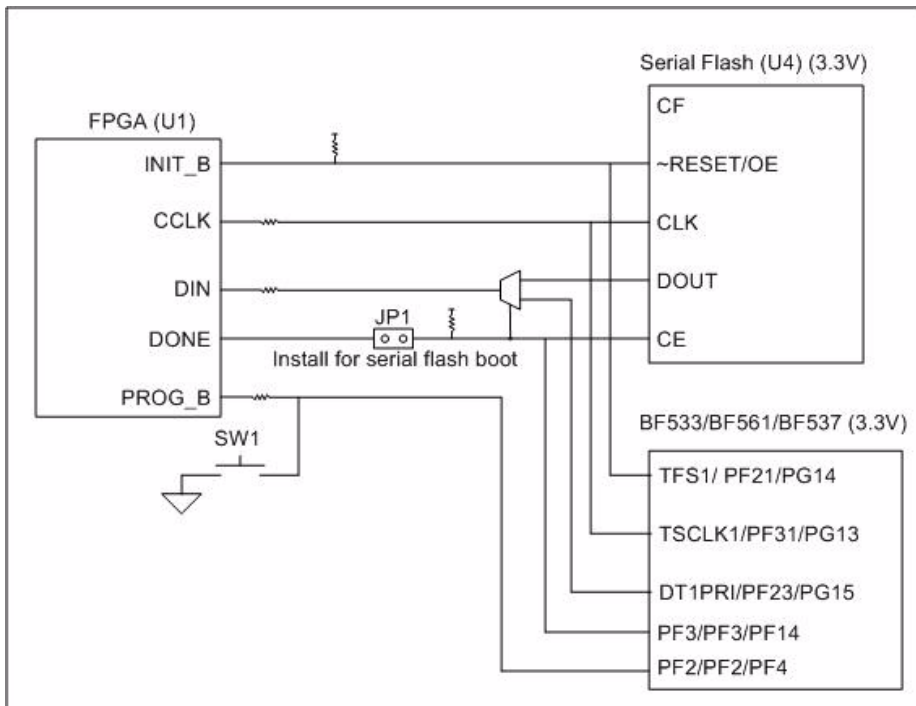


Figure 2-2. FPGA Programming Block Diagram

Programming the FPGA

There are three ways to program the FPGA:

- Using the FPGA JTAG header, as described in [“FPGA Programming via JTAG” on page 2-4](#)
- Using the Xilinx serial ROM, as described in [“FPGA Programming via Serial ROM” on page 2-5](#)
- Using the Blackfin processor, as described in [“FPGA Programming via Blackfin Application” on page 2-6](#)

The done LED (LED10) lights up once the FPGA is programmed, signifying that the task is complete. To erase the contents of the FPGA at any time, de-press the program switch SW1.

FPGA Programming via JTAG

To program the FPGA via the JTAG header, create the appropriate program file using the Xilinx ISE software provided at www.xilinx.com. Once the program file is created, use a Xilinx JTAG cable and connect it to P15 of the FPGA EZ-Extender (the P15 connections are shown in [Table 2-1](#)).

Table 2-1. P15 Connections for PFGA Programming via JTAG

P15 Pin Number	Signal Name
1	3.3V
2	GND
3	TCK
4	TDO
5	TDI
6	TMS

In addition to removing JP1 (serial ROM boot jumper) as shown in [Table 2-2](#), set the boot jumper, JP4, to JTAG mode. The JP4 settings for JTAG boot are shown in [Table 2-3](#). See “[Boot Jumper \(JP4\)](#)” on [page 2-14](#) for more information.

Table 2-2. JP1 Settings for FPGA Programming via JTAG

JP1 Pin Name	Pins Connected	Jumper Setting
Flash done	JP1.1 and JP1.2	Unpopulated

Table 2-3. JP4 Settings for FPGA Programming via JTAG

JP4 Pin Name	Pins Connected	Jumper Setting
M0	JP4.1 and JP4.2	Unpopulated
M1	JP4.3 and JP4.4	Populated
M2	JP4.5 and JP4.6	Unpopulated

FPGA Programming via Serial ROM

To program the FPGA with the contents of the serial ROM, populate the JP1 jumper. When populated, JP1 connects the chip enable pin of the serial ROM to the done bit of the FPGA. Once the FPGA is programmed, the done bit automatically goes high, and the enable pin of the serial ROM chip becomes a logic 1. The JP1 settings for serial ROM boot are shown in [Table 2-4](#). See “[Programming the Serial ROM](#)” on [page 2-7](#) for more information.

The done LED (LED10) remains lit to signify that the FPGA is programmed. See “[Done LED \(LED10\)](#)” on [page 2-17](#) for more information.

Table 2-4. JP1 Settings for FPGA Programming via Serial ROM

JP1 Pin Name	Pins Connected	Jumper Setting
Flash done	JP1.1 and JP1.2	Populated

Programming the FPGA


In addition to JP1, set the boot mode jumper, JP4, to master serial mode. The JP4 settings for serial ROM boot are shown in [Table 2-5](#). See “[Boot Jumper \(JP4\)](#)” on [page 2-14](#) for more information.

Table 2-5. JP4 Settings for FPGA Programming in Master Serial Mode

JP4 Pin Name	Pins Connected	Jumper Setting
M0	JP4.1 and JP4.2	Populated
M1	JP4.3 and JP4.4	Populated
M2	JP4.5 and JP4.6	Populated

FPGA Programming via Blackfin Application

By default, the FPGA EZ-Extender is configured by the flash programming utility within VisualDSP++. The software is located in the `...\\Blackfin\\EZ-KITs\\FPGA EZ-EXTENDER` subdirectory of the VisualDSP++ installation directory. The `FPGA Software Readme.txt` file located in the same subdirectory provides all the necessary instructions required for running the application.

 When generating a program file using the Xilinx software tools, remember to generate a slave serial program file in the Intel MCS-86 Hexadecimal Object (.mcs) file format.

To boot the FPGA from the Blackfin processor, unpopulate jumper JP1 and set jumper JP4 to slave serial mode, as shown in [Table 2-6](#) and [Table 2-7](#). See “[Serial ROM Boot Jumper \(JP1\)](#)” on [page 2-12](#) and “[Boot Jumper \(JP4\)](#)” on [page 2-14](#) for more information.

Table 2-6. JP1 Settings for FPGA Programming via Blackfin Processor

JP1 Pin Name	Pins Connected	Jumper Setting
Flash done	JP1.1 and JP1.2	Unpopulated

Table 2-7. JP4 Settings for FPGA Programming via Blackfin Processor

JP4 Pin Name	Pins Connected	Jumper Setting
M0	JP4.1 and JP4.2	Unpopulated
M1	JP4.3 and JP4.4	Unpopulated
M2	JP4.5 and JP4.6	Unpopulated

Programming the Serial ROM

The FPGA EZ-Extender allows the user to program the serial ROM. The serial ROM can be programmed by using a Xilinx JTAG cable, ISE software, and the flash JTAG header on the FPGA EZ-Extender.

Serial ROM via JTAG Header

To program the serial ROM via the JTAG header, create the appropriate program file using the Xilinx software provided at www.xilinx.com. Once the program file is created, use a Xilinx JTAG cable and connect it to P6. The P6 connections are shown in [Table 2-8](#).

Table 2-8. P6 Connections for Serial ROM

P6 Pin Number	Signal Name	P6 Pin Number	Signal Name
1	3.3V	4	TDO
2	GND	5	TDI
3	TCK	6	TMS

Power

The FPGA EZ-Extender can be powered from the enclosed power supply, EZ-KIT Lite, or external power supply. The power source for the extender is selected based on the power requirements of the application.

An external 7V power supply is shipped with the extender board. The power supply uses three switching regulators: VR1 is used to power the 2.5V power plane, VR2 is used to power the 1.2V power plane, and VR3 is used to power the 3.3V plane. All of the regulators can supply a maximum current of 2 Amps. To understand the power requirements of your application, run the Xilinx power estimator software. The software can be located at www.xilinx.com.

Table 2-9 states the current limitations of each method. Each method requires a correctly configured header, described in the following sections.

Table 2-9. Power Limitations

Power Source	1.2V Supply	2.5V Supply	3.3V Supply
ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite	500 mA	500 mA	500 mA
FPGA EZ-Extender power supply ¹	2A	2A	2A
External power supply	2A	2A	2A

¹ Default setting

Power In Header (P12)

The P12 header supplies the power to the on board 1.2V and the 2.5V regulators. The P42 and P43 headers supply the power to the external 1.2V and 2.5V planes, as described in “2.5V Header (P42)” and “1.2V Header (P43)” on page 2-10.

Power Source	P12 Setting
FPGA EZ-Extender power supply ¹	Jumper on P12.1 and P12.2
ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite 5V power supply	Jumper on P12.2 and P12.3

¹ Default setting

3.3V Header (P13)

Power Source	P13 Setting
ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite 3.3V power supply	Jumper on P13.1 and P13.2
FPGA EZ-Extender power supply ¹	Jumper on P13.2 and P13.3
External power supply	No jumper; connect supply to P13.2 and GND

¹ Default setting




When using an external power supply, *do not* plug in the power supply shipped with the FPGA EZ-Extender. This can seriously damage the board. As an extra measure of precaution, remove all jumpers from P12.

Power

2.5V Header (P42)

Power Source	P42 Setting
FPGA EZ-Extender Power Supply ¹	No Jumper
External power supply	Connect P42.1 to external 2.5V Connect P42.2 to external GND


¹ Default setting

 When using an external power supply, *do not* plug in the power supply shipped with the FPGA EZ-Extender. This can seriously damage the board. As an extra measure of precaution, remove all jumpers from P12.

1.2V Header (P43)

Power Source	P43 Setting
FPGA EZ-Extender power supply ¹	No Jumper
External power supply	Connect P42.1 to external 2.5V Connect P42.2 to external GND

¹ Default setting

 When using an external power supply, *do not* plug in the power supply shipped with the FPGA EZ-Extender. This can seriously damage the board. As an extra measure of precaution, remove all jumpers from P12.

Jumpers

Before using the Blackfin FPGA EZ-Extender, follow the steps in “[FPGA EZ-Extender Setup](#)” on page 1-1.

Figure 2-3 shows the locations of all jumper headers. A two-pin jumper can be placed on the respective jumper header for different functionality. The following sections describe all possible jumper settings and associated functionality.

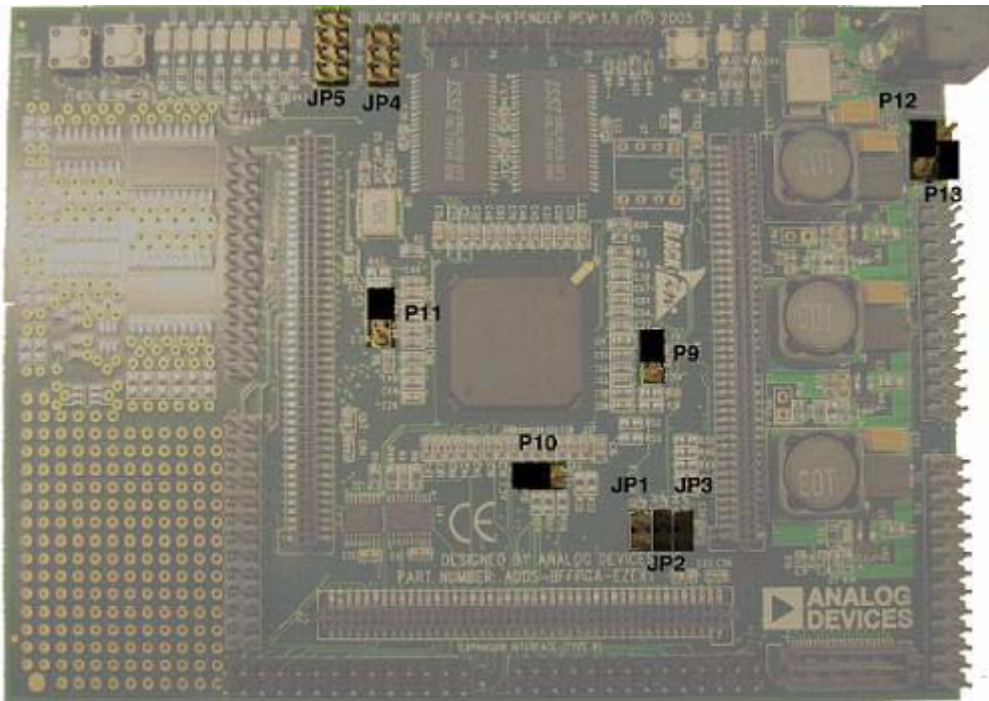


Figure 2-3. Jumper Locations

Serial ROM Boot Jumper (JP1)

By default, the serial ROM boot jumper, JP1, is unpopulated. When unpopulated, the FPGA EZ-Extender programs via the Blackfin processor or the Xilinx JTAG header.

When JP1 is left populated, the jumper connects the serial ROM chip enable pin to the done bit of the FPGA. At power-up, the done bit is driven low by the FPGA, causing the FPGA to enable the serial ROM as a programming source. After the FPGA is programmed, the done bit is driven high by the FPGA, causing the FPGA to drive high the chip enable pin of the serial ROM.

Both JP1 and JP4 must be set up for correct FPGA programming. “[Boot Jumper \(JP4\)](#)” on page 2-14 summarizes the JP4 settings. [Table 2-10](#) summarizes the JP1 settings. See [Table 2-4 on page 2-5](#) and [Table 2-6 on page 2-6](#) for more information on JP1.

Table 2-10. JP1 Settings

Boot Source	JP1 Setting
ADSP-BF533, ADSP-BF537, or ADSP-BF561 processor via VisualDSP++ ¹	Unpopulated
JTAG header	Unpopulated
Serial ROM	Populated

¹ Default setting

Config Done Jumper (JP2)

The configuration done jumper, JP2, connects the done bit of the FPGA to the Blackfin processor’s PF3 flag pin of the ADSP-BF533 and ADSP-BF561 EZ-KIT Lites or PF14 flag pin of the ADSP-BF537 EZ-KIT

Lite. By default, the jumper is populated and acts as a monitor for the done bit by the Blackfin processor (the bit indicates that the FPGA programming is complete).

Table 2-11 summarizes the jumper settings.

Table 2-11. JP2 Settings

Functionality	JP2 Setting
Done bit connected to Blackfin processor's PF3 flag pin ¹	Populated
Done bit disconnected from Blackfin processor's PF3 flag pin	Unpopulated

¹ Default setting

Config Program Jumper (JP3)

The configuration program jumper, JP3, connects the program bit of the FPGA to the Blackfin processor's flag pin. By default, JP3 is populated. The jumper assures that the program bit is asserted by the Blackfin processor to initiate the FPGA programming through VisualDSP++ software.

Table 2-12 summarizes the jumper settings.

Table 2-12. JP3 Settings

Functionality	JP3 Setting
Program bit connected to the Blackfin processor's flag pin ¹	Populated
Program bit disconnected from the Blackfin processor's flag pin	Unpopulated

¹ Default setting

Jumpers

Boot Jumper (JP4)

The boot jumper, JP4, configures the FPGA mode pins (M[2:0]). Based on the jumper settings, the FPGA is set to be programmed by the JTAG header, serial ROM, or Blackfin processor.

Table 2-13 summarizes the jumper settings. See Table 2-3 on page 2-5 for the JTAG header boot settings, Table 2-5 on page 2-6 for the serial ROM boot settings, and Table 2-7 on page 2-7 for the Blackfin processor boot settings.

Table 2-13. JP4 Settings

Boot Source	JP4.1 and JP4.2 M0	JP4.3 and JP4.4 M1	JP4.5 and JP4.6 M2
ADSP-BF533, ADSP-BF537, or ADSP-BF561 processor ¹	Unpopulated	Unpopulated	Unpopulated
JTAG header	Unpopulated	Populated	Unpopulated
Serial ROM	Populated	Populated	Populated

¹ Default setting

FPGA Input Jumpers (JP5)

The FPGA input jumpers, JP5.2-5.8, drive select FPGA nets to a logic 0 and can be used for any user logic that requires a steady state input. You can set internal pull-ups on these nets in the FPGA and, when a low is required, populate the respective jumper.

Table 2-14 summarizes the jumper settings.

Table 2-14. JP5 Settings

Reference Designator	FPGA Pin Number
JP5.2	Y3
JP5.4	Y2
JP5.6	U10
JP5.8	AB11

Push Buttons and LEDs

Before using the Blackfin FPGA EZ-Extender, follow the steps in [“FPGA EZ-Extender Setup” on page 1-1](#).

[Figure 2-4](#) shows the locations of all push buttons and LEDs. The following sections describe the associated functionality of all the push buttons and LEDs.

Program Push Button (SW1)

The program push button, SW1, erases the contents of the FPGA. The push button can be used as a hard reset—the FPGA must be completely re-programmed once SW1 is de-pressed. See [“Programming the FPGA” on page 2-3](#) for more information.

PB1 Push Button (SW3)

The PB1 push button, SW3, is a general-purpose input push button. The switch with a connected debounce circuit eliminates the need to re-create it in the FPGA. The push button connects to pin C11 of the FPGA.

Push Buttons and LEDs

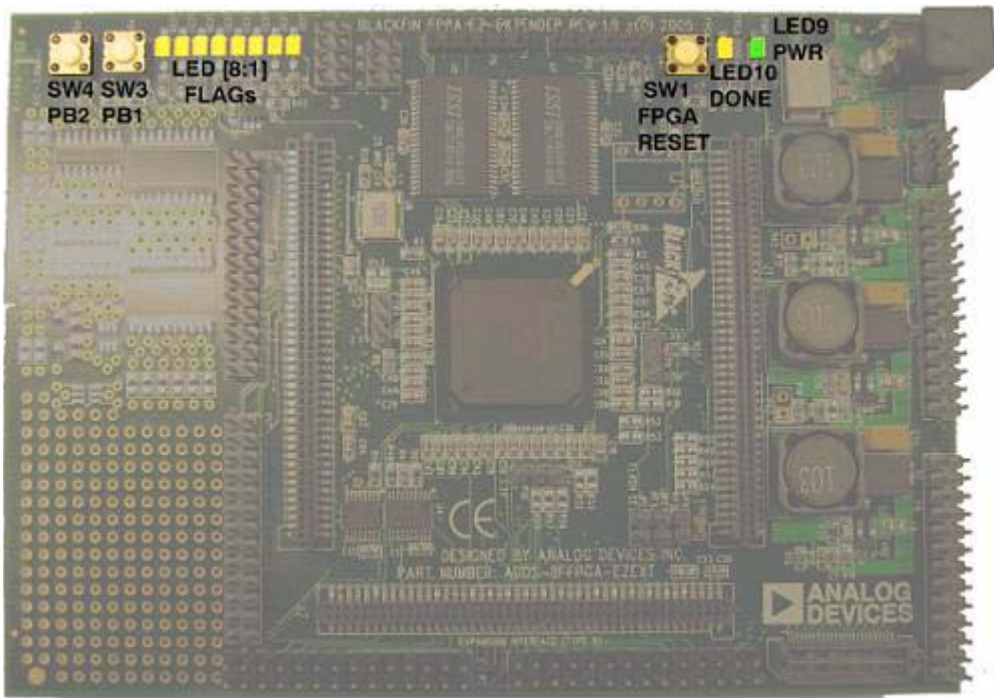


Figure 2-4. Push Button and LED Locations

PB2 Push Button (SW4)

The PB2 push button, SW4, is a general-purpose input push button. The switch does not have a connected debounce circuit; you may need to create it in the FPGA if required by a specific application. The push button connects to pin H5 of the FPGA.

Status LEDs (LED1–8)

Eight status LEDs, LED1–8, connect to the FPGA and act as status flags in any application that requires it. [Table 2-15](#) shows the LED/FPGA connections.

Table 2-15. Status LED (LED1–8) Settings

Reference Designator	FPGA Pin Number
LED1	U11
LED2	W11
LED3	AB10
LED4	Y10
LED5	AB9
LED6	W9
LED7	AB8
LED8	V10

Power LED (LED9)

The power LED, LED9, connects to the 2.5V power supply and, when lit, signifies that the FPGA EZ-Extender is powered properly.

Done LED (LED10)

The done LED, LED10, connects to the done pin of the FPGA. At power-up, the FPGA is blank and needs to be programmed. When lit, the LED indicates that the FPGA is programmed successfully.

Connectors

Before using the Blackfin FPGA EZ-Extender, follow the steps in “[FPGA EZ-Extender Setup](#)” on page 1-1.

This section describes the connector functionality and provides information about the mating connectors. The connector locations are shown in [Figure 2-5](#).

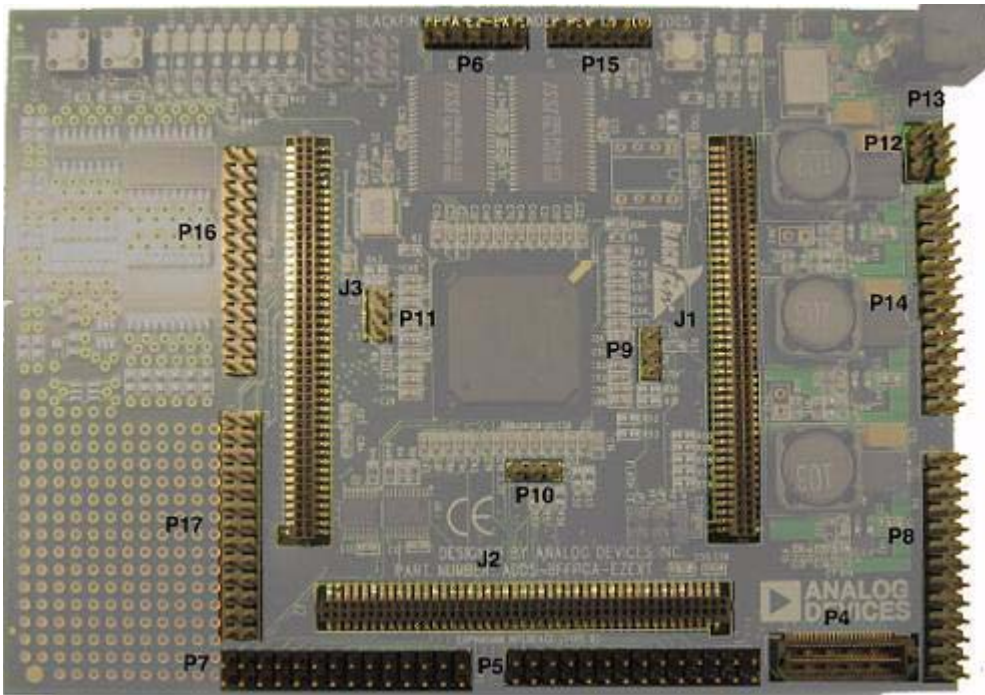


Figure 2-5. Connector Locations

Expansion Interface (P1-3 and J1-3)

Connectors P1-3 of the expansion interface are used to plug in the EZ-Extender to the ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite.

Connectors J1-3 of the expansion interface are used to plug in another extender board, such as the Blackfin USB-LAN EZ-Extender. Your own custom board can be plugged into J1-3 as well.

- ⊘ Plugging in another EZ-Extender or a customer board to the expansion interface can de-grade the overall system performance. The extra overall load can cause the user to add wait states or slow down the system bus to get all of the boards to work properly.

For the J1-3 and P1-3 connector availability and pricing, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05" spacing, SMT (J1, J2, J3)	Samtec	SFC-145-T2-F-D-A
90-position 0.05" spacing (P1, P2, P3)	Samtec	TFC-145-32-F-D

IDC Connectors (P8, P14, P16, and P17)

The P8, P14, P16, and P17 connectors are standard 0.1" IDC headers. The connectors are in a 13 x 2 configuration and designed for signal probing, bread boarding, and other signal accesses.

Part Description	Manufacturer	Part Number
IDC13x2 0.1" header	Berg	54102-T08-13
Mating Connector		
IDC 13x2 0.1" plug	Samtec	SSW-113-01-T-D

Connectors

IDC Connectors (P5 and P7)

The P5 and P7 connectors are standard 0.1” IDC headers. The connectors are in a 14 x 2 configuration and designed for signal probing, bread boarding, and other signal accesses.

Part Description	Manufacturer	Part Number
IDC14x2 0.1” header	FCI	68737-428HLF
IDC14x2 0.1” header	Sullins	GEC14DAAN
Mating Connector		
IDC 14x2 0.1” plug	Samtec	SSW-114-01-T-D

High-Speed Connector (P4)

The high-speed connector, P4, facilitates development of applications where use of the standard IDC connectors is complicated due to signal integrity issues.

For the P4 connector and cable assembly availability and pricing, contact Samtec.

Part Description	Manufacturer	Part Number
QTS 25x2 high-speed connector	Samtec	QTS-025-01-F-D-A
Mating Connector		
QSS 25x2 high-speed connector	Samtec	QSS-025-01-F-D-A

A BILL OF MATERIALS

The bill of materials corresponds to the board schematics on page B-1. Please check the latest schematics on the Analog Devices website, <http://www.analog.com/Processors/Processors/DevelopmentTools/technicalLibrary/manuals/DevToolsIndex.html#Evaluation%20Kit%20Manuals>.

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
1	1	SN74LVC1G125 SOT23-5 SINGLE-3STATE-BUFFER	U8	TI	SN74LVC1G125DBVR
2	1	25MHZ SMT OSC003	U6	EPSON	SG-8002CA-PWT 25MHZ
3	1	74LVC157 TSSOP16 QUAD MUX	U2	PHILIPS	74LVC157APW
4	1	XC3S1000 FG456 SPARTAN3-FPGA	U1	XILINX	XC3S1000-4FGG456C
5	3	LM3475MF SOT23-5 BUCK-CONTROLLER	VR1-3	NATIONAL	LM3475MF
6	1	XCF04S TSSOP20 XILINX_4MBIT_FLASH	U4	XILINX	XCF04SVOG20C
7	2	IS61LV51216 TSOP44 512KX16_SRAM	U3,U5	ISSI	IS61LV51216-10TTLI
8	3	SI2343DS SOT23D PFET_30V	Q1-3	VISHAY	SI2343DS-T1-E3
9	1	PWR 2.5MM_JACK CON005 RA	J4	SWITCHCRAFT	SC1152-ND12
10	1	8 PIN DIP TH-TH CARRIER SOCKETED PIN	U7	MILL-MAX	614-93-308-31-007

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
11	3	SPST-MOMENTARY SWT013 6MM	SW1,SW3-4	PANASONIC	EVQ-PAD04M
12	3	0.05 45x2 CON018 HEADER	P1-3	SAMTEC	TFC-145-32-F-D
13	3	0.05 45X2 CON019 SMT SOCKET	J1-3	SAMTEC	SFC-145-T2-F-D-A
14	2	IDC 14X2 IDC14X2 HEADER	P5,P7	FCI	68737-428HLF
15	2	IDC 6X1 IDC6X1 HEADER	P6,P15	FCI	90726-406HLF
16	1	QTS 25X2 CON041 SMT	P4	SAMTEC	QTS-025-01-F-D-A
17	9	AMBER-SMT LED001 GULL-WING	LED1-8,LED10	PANASONIC	LN1461C-TR
18	1	10uF 16V 10% C TANT	C4	AVX	TAJ106K025R
19	3	3A HSM350J DO214AB SCHOT_RECT	D1-3	MICRO-SEMI	HSM350J
20	1	600 100MHZ 200MA 0603 0.50 BEAD	FER2	MURATA	BLM11A601SPT

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
21	1	2A S2A_RECT DO-214AA SILICON RECTIFIER	D5	VISHAY	S2A
22	1	3.9NF 50V 5% 805	C6	PANASONIC	ECH-U1C392JB5
23	1	190 100MHZ 5A FER002	FER1	MURATA	DLW5BSN191SQ2
24	7	10UF 6.3V 10% 805 X7R	C14-16,C35,C55,C83,C86	AVX	080560106KAT2A
25	4	1000PF 10V 20% 805	C1-2,C10,C74	YAGEO	1206CG229C9B200
26	3	100UF 10V 10% C TANT-LOW-ESR	CT1-3	AVX	TPSC107K010R0075
27	5	0.1UF 16V 10% 0603 X7R	C3,C38,C56,C84-85	AVX	0603YC104KAT2A
28	56	0.01UF 16V 10% 0603 X7R	C11-13,C17-34,C36-37,C39-54,C57-70,C80-82	AVX	0603YC103KAT2A
29	1	1UF 16V 10% 0603	C5	PANASONIC	ECJ-1V/B1C105K
30	3	10UH 17 20% IND005	L1-3	COILCRAFT	MSS1278-103MXB
31	8	10K 1/10W 5% 0603	R1,R6,R21-22,R28-29,R46-47	PANASONIC	ERJ-3GEYJ103V
32	10	330 1/10W 5% 0603	R10,R24,R34-41	VISHAY	CRCW0603331JRT1

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
33	9	0 1/10W 5% 0603	R3-4,R9,R12,R15-16, R27,R58-59	PANASONIC	ERJ-3GEY0R00V
34	1	10 1/10W 5% 0603	R42	PANASONIC	ERJ-3GEYJ100V
35	1	200K 1/16W 1% 0603	R20	VISHAY	CRCW06032003FRT1
36	2	10K 1/10W 1% 0603	R14,R19	PANASONIC	P10.0KHTR-ND
37	2	33 1/10W 1% 0603	R2,R26	YAGEO	9C06031A33R0FKHFT
38	5	100 1/16W 5% 402	R5,R7-8,R23,R44	PANASONIC	ERJ-2GEJ101X
39	1	390PF 25V 5% 0603 NPO	C7	AVX	06033A391FAT2A
40	1	4.99K 1/16W 1% 0603	R13	STACKPOLE	RMC 1/16 4.99K 1% R
41	1	31.6K 1/16W 1% 0603	R17	PANASONIC	ERJ-3EKF3162V
42	1	1.05K 1/16W 1% 0603	R11	PANASONIC	ERJ-3EKF1051V
43	1	2.15K 1/16W 1% 0603	R18	PANASONIC	ERJ-3EKF2151V
44	1	GREEN-SMT LED001 GULL-WING	LED9	PANASONIC	LN1361C
45	3	IDC 2X1 IDC2X1 GOLD	JP1-3		

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
46	5	IDC 3X1 IDC3X1	P9-13	BERG	54101-T08-03
47	1	IDC 3X2 IDC3X2	JP4	BERG	54102-T08-03
48	1	IDC 4X2 IDC4X2	JP5	SULLINS	S2012-04
49	4	IDC 13X2 IDC13X2	P8,P14,P16-17	BERG	54102-T08-13
50	1	2.5A RESETTABLE FUS001	F1	RAYCHEM CORP.	SMD250-2
51	3	10UF 10V 10% 805	C8, C9, C71	PANASONIC	ECJ-2FB1A106K

A

B

C

D

BLACKFIN FPGA EZ-EXTENDER Schematic

DNP = Do Not Populate

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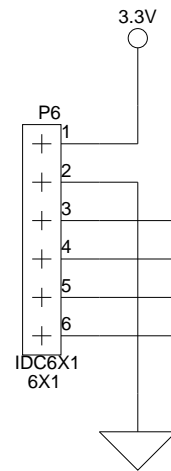
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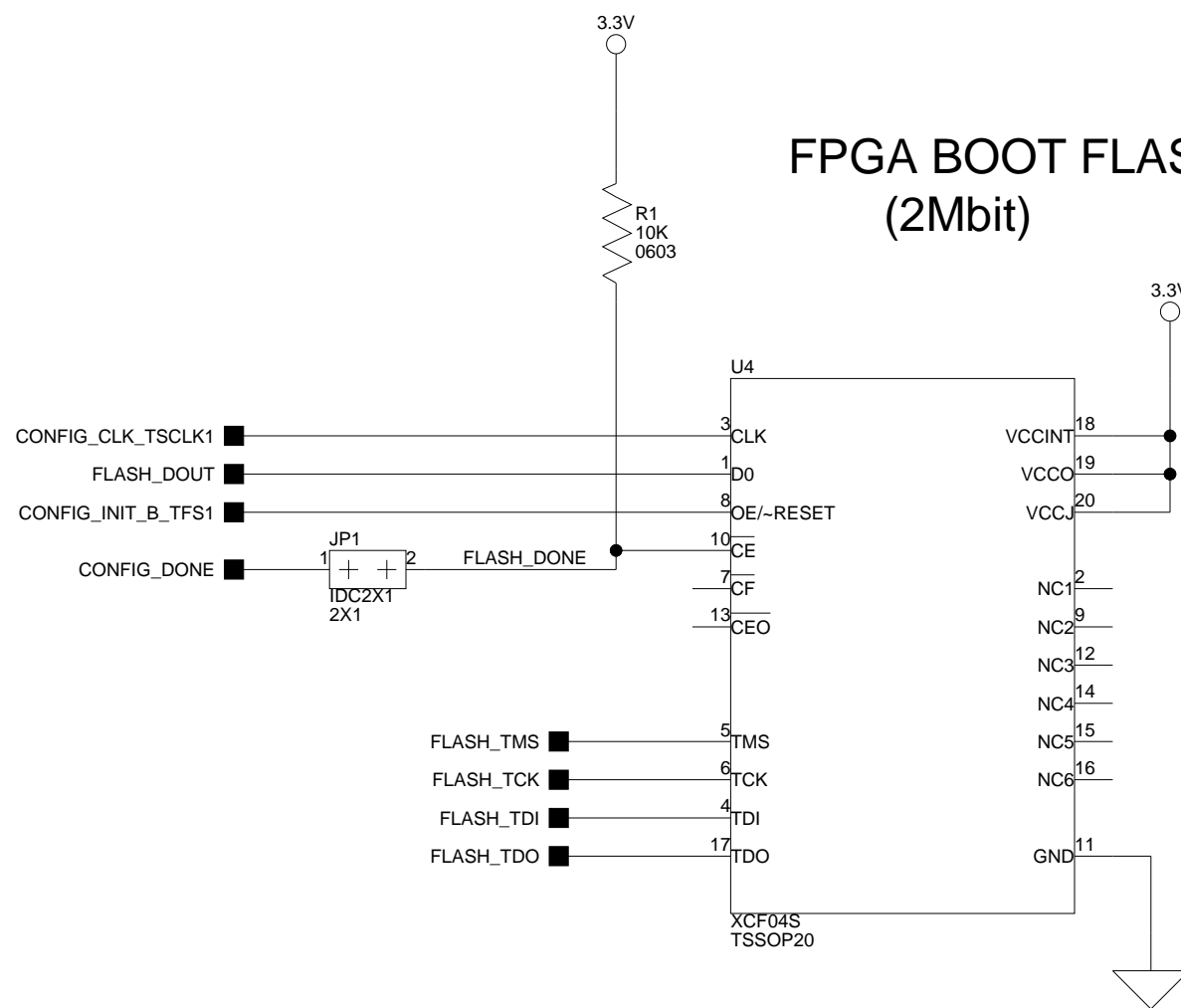
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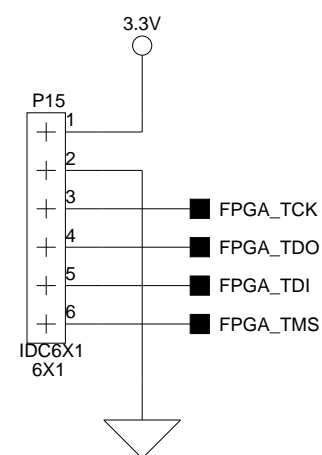
FLASH JTAG HEADER



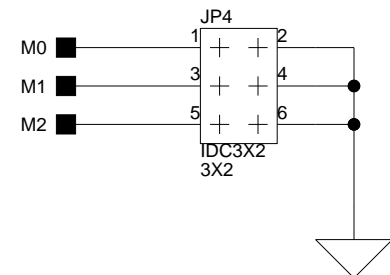
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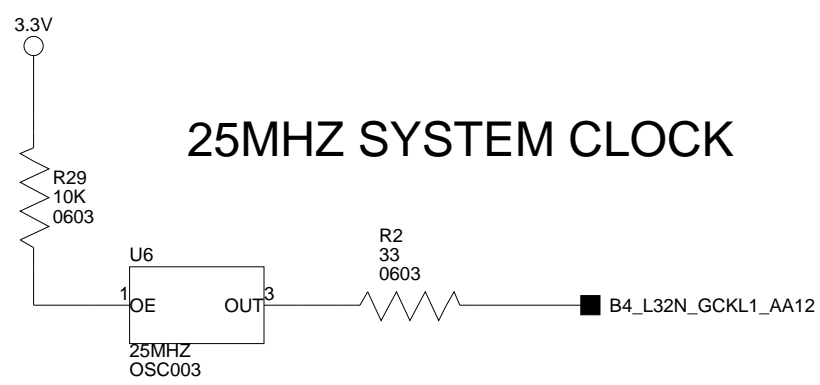
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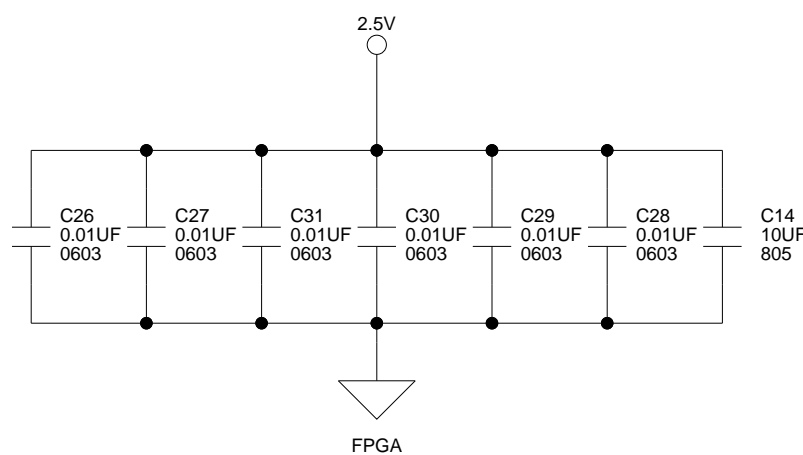
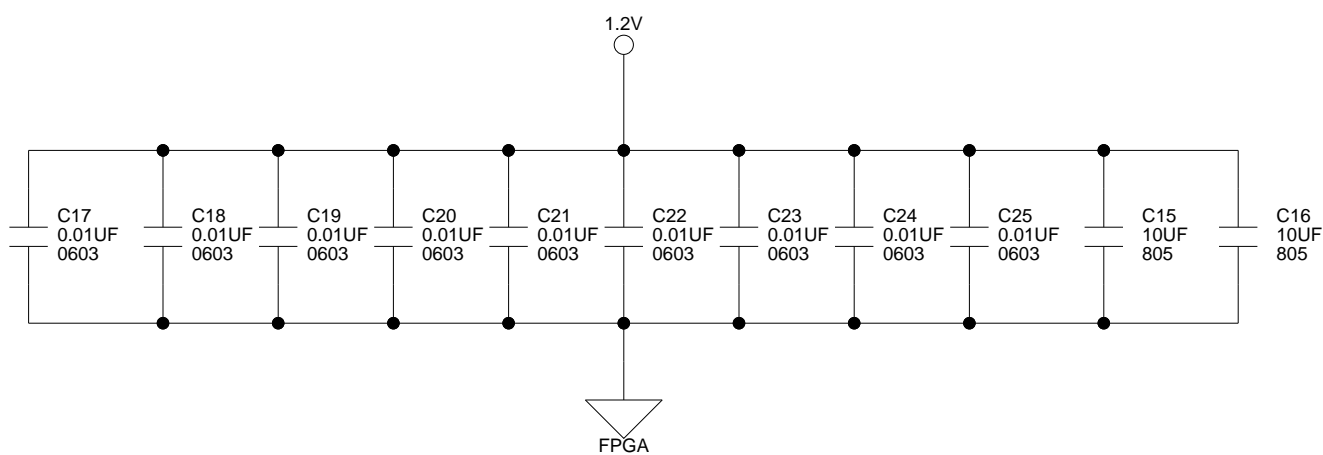
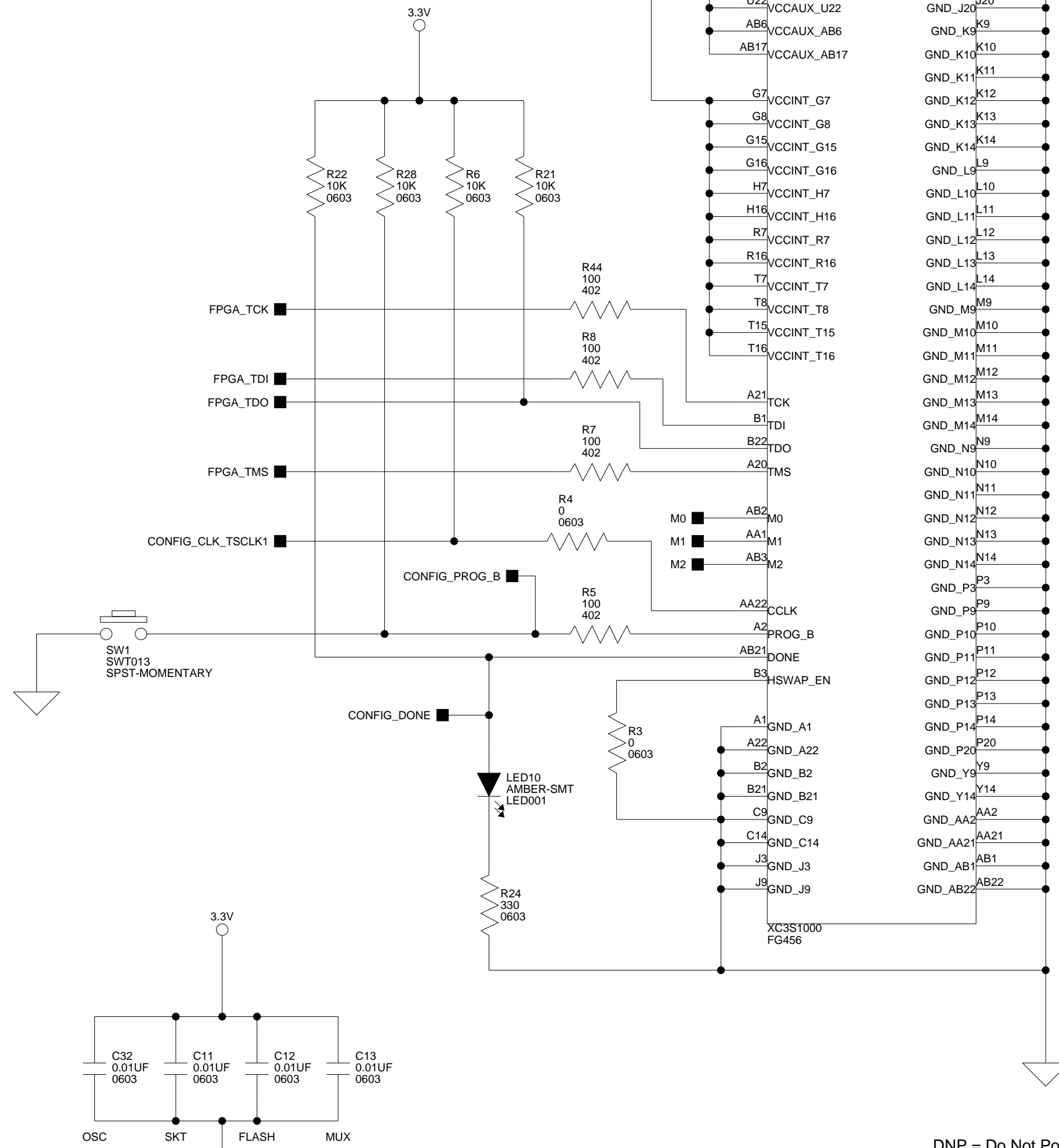
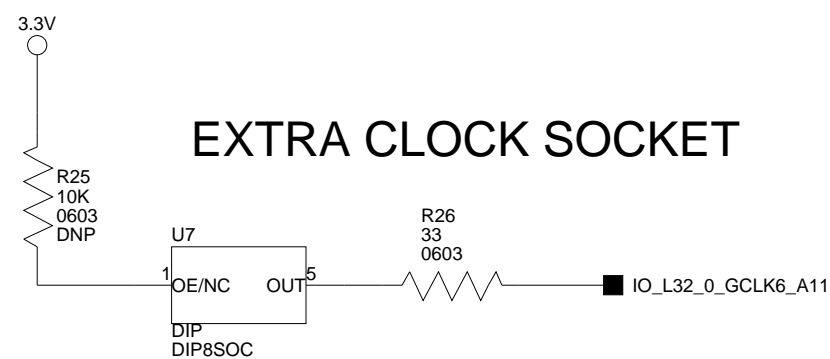
BOOTMODE JUMPER



25MHZ SYSTEM CLOCK



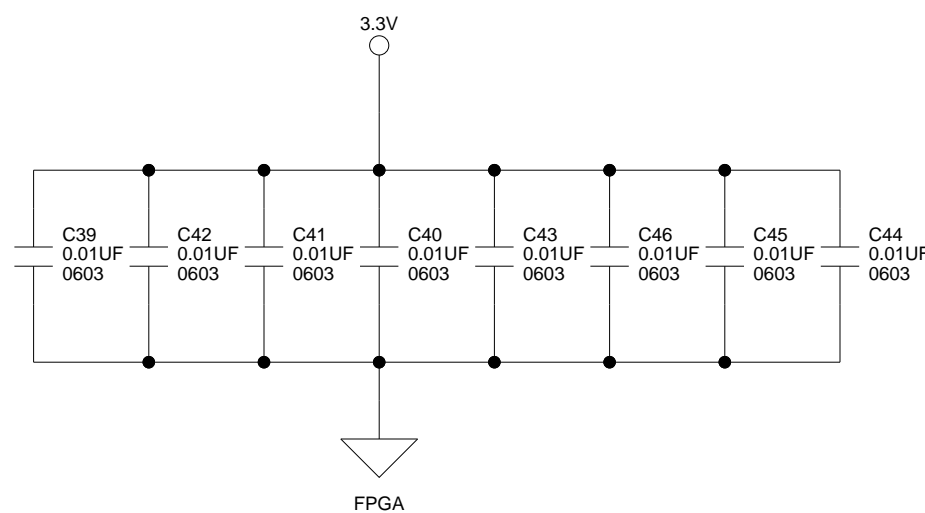
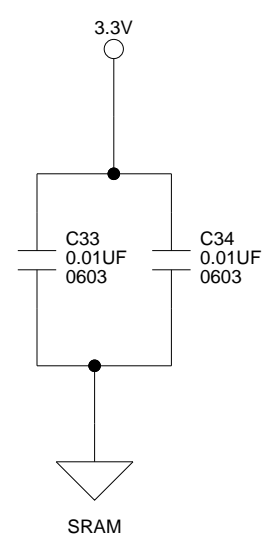
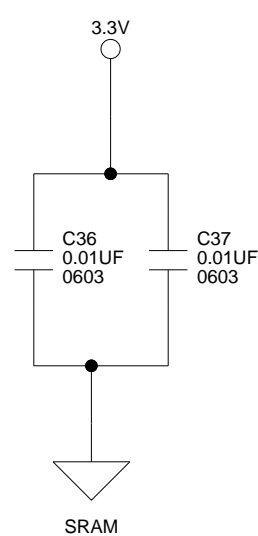
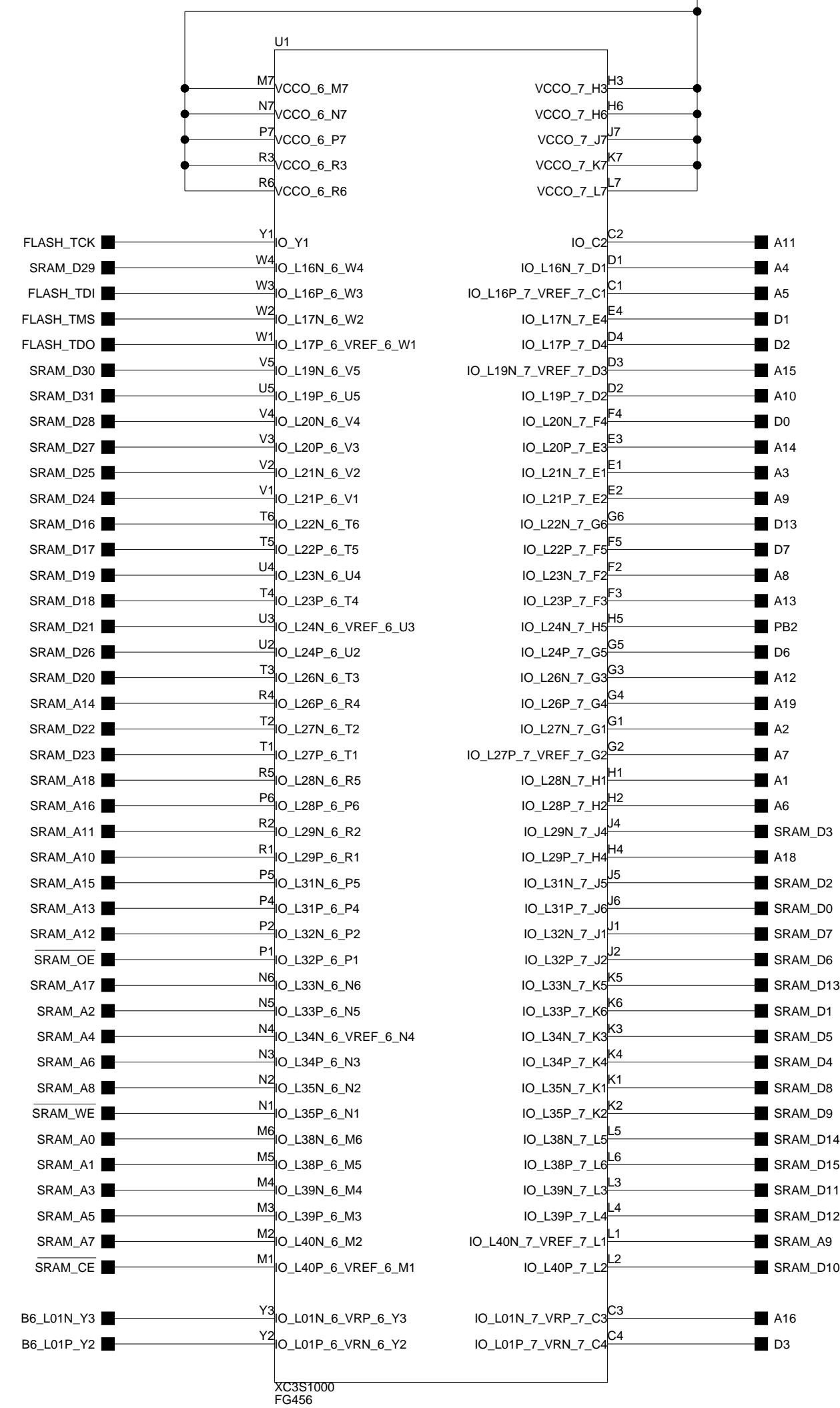
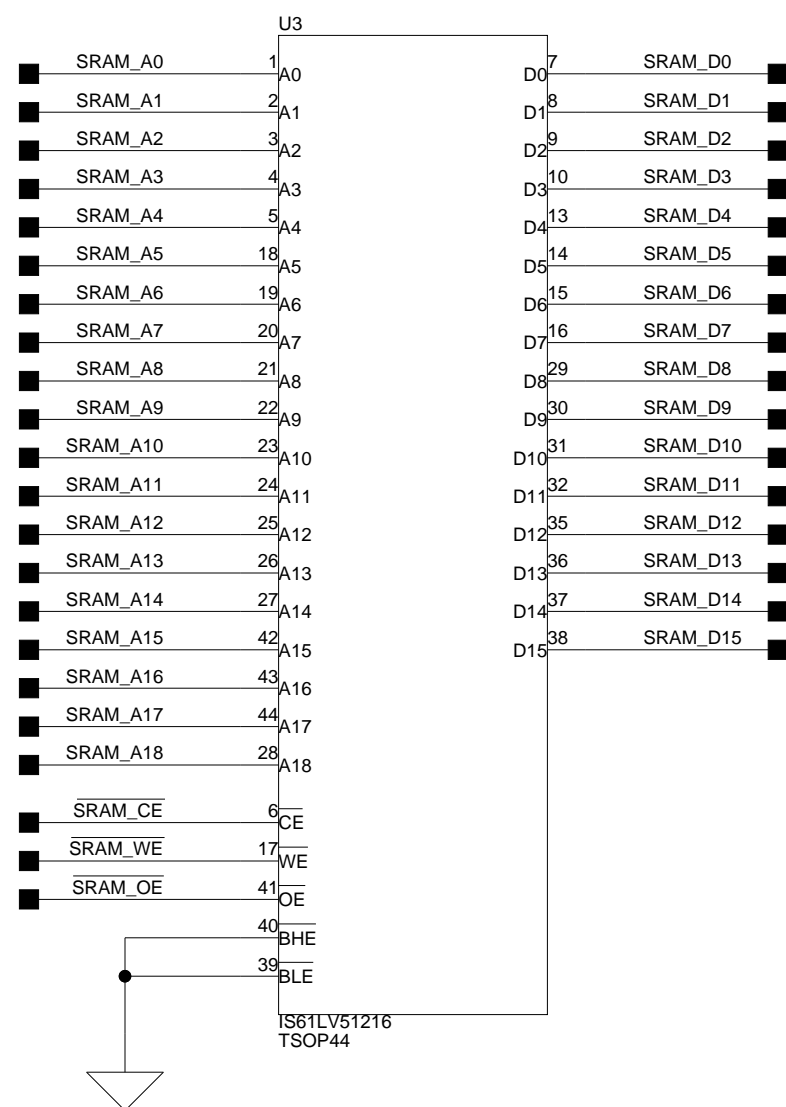
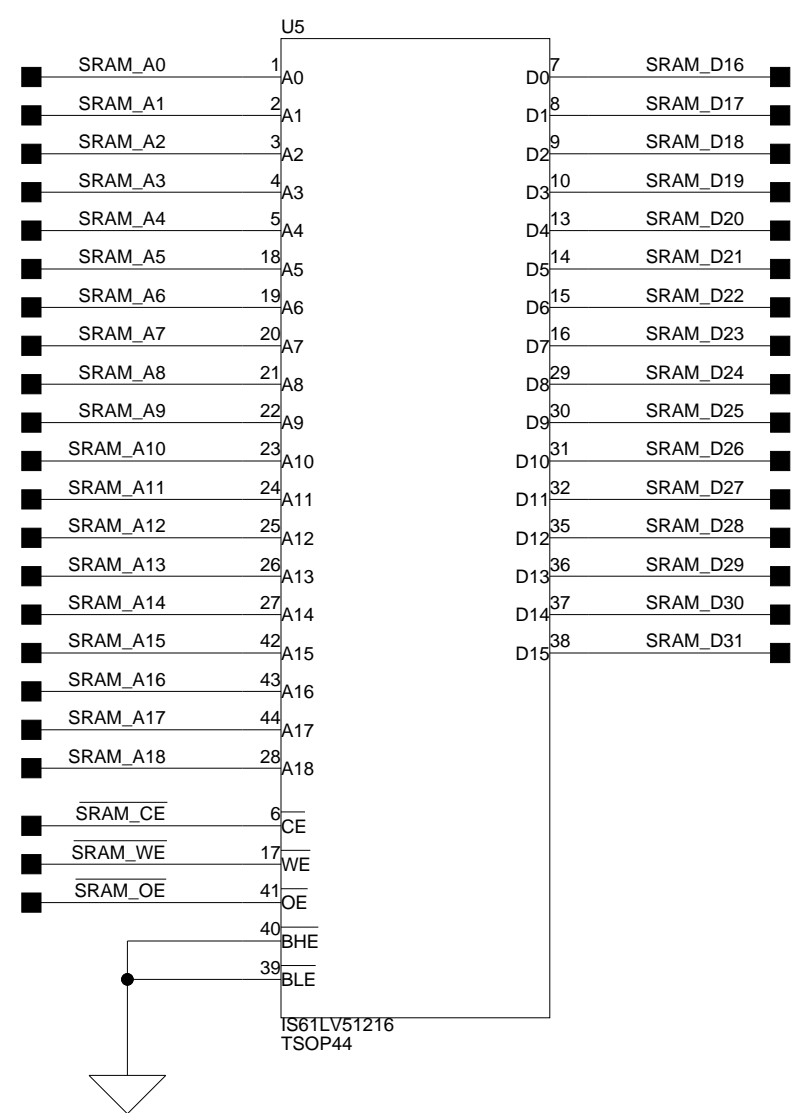
EXTRA CLOCK SOCKET



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Date	9-27-2005_11:44	Sheet	2 of 12

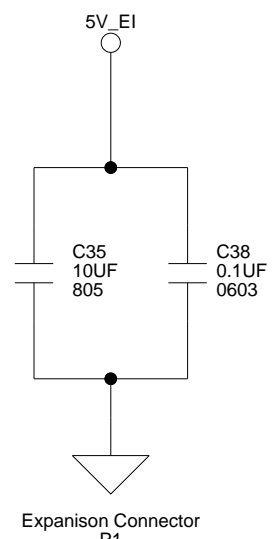
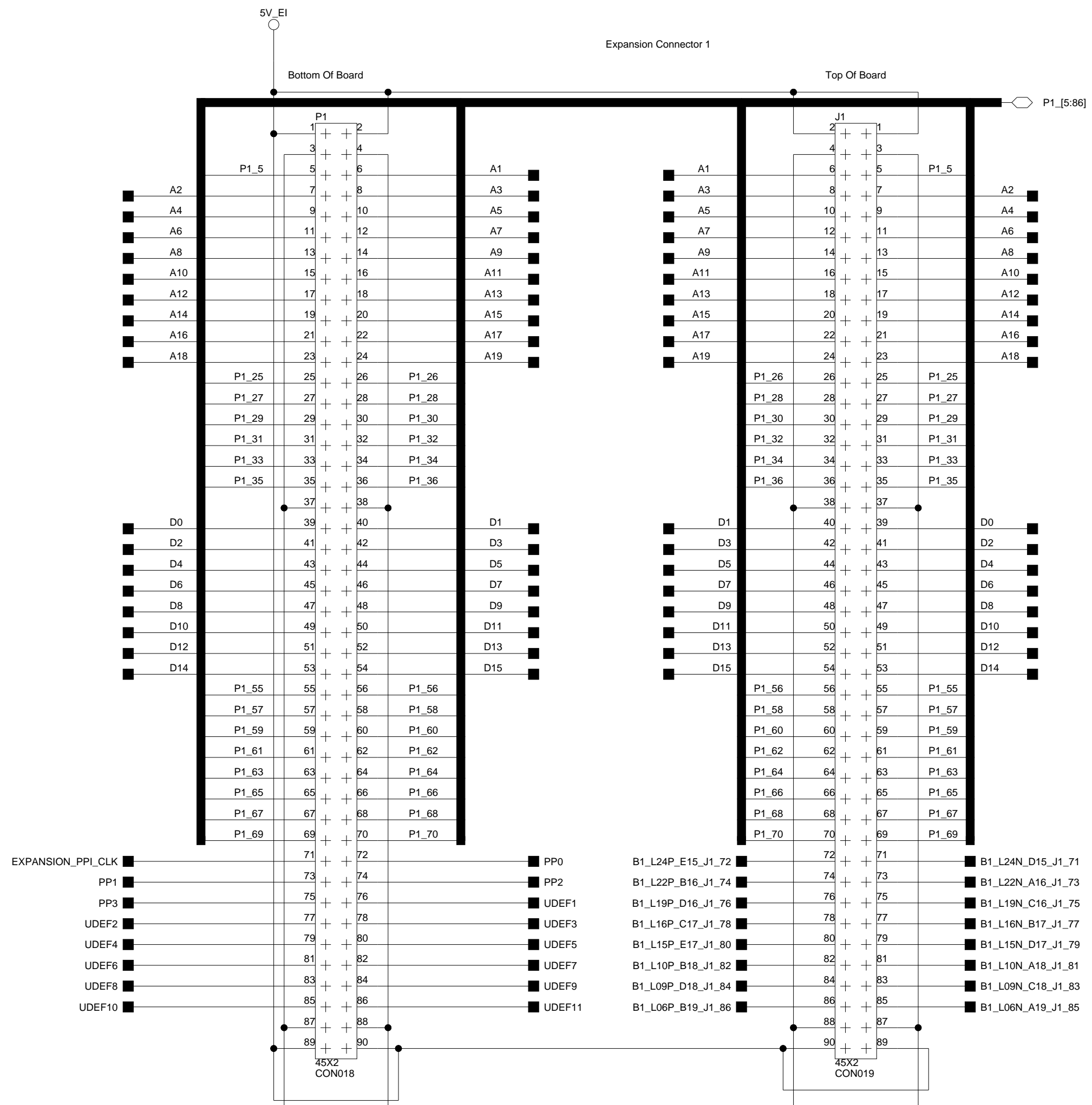
2MBYTES FPGA SRAM (512k x 16bits x 2chips)



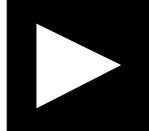
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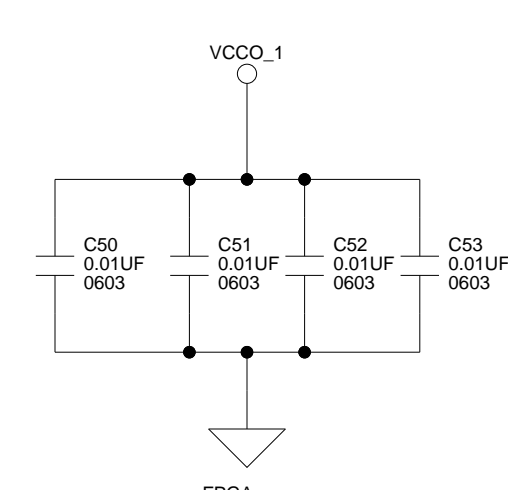
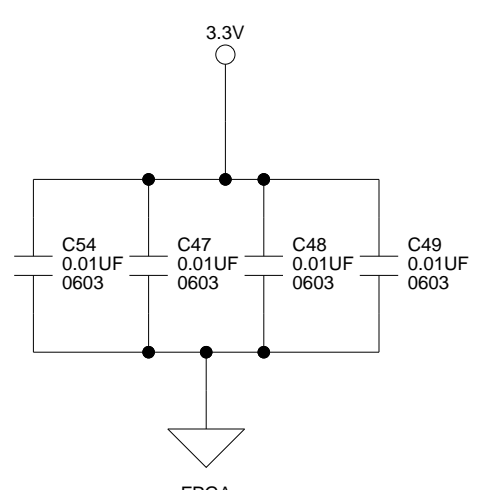
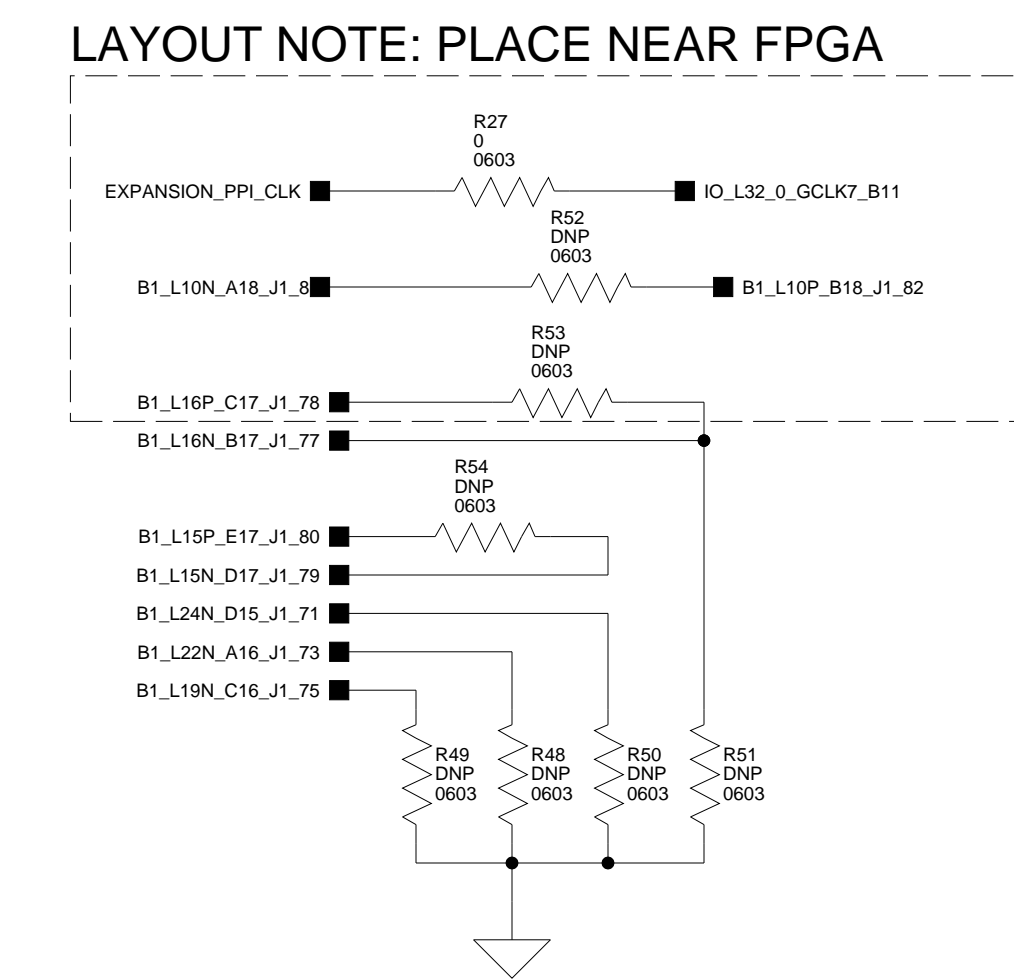
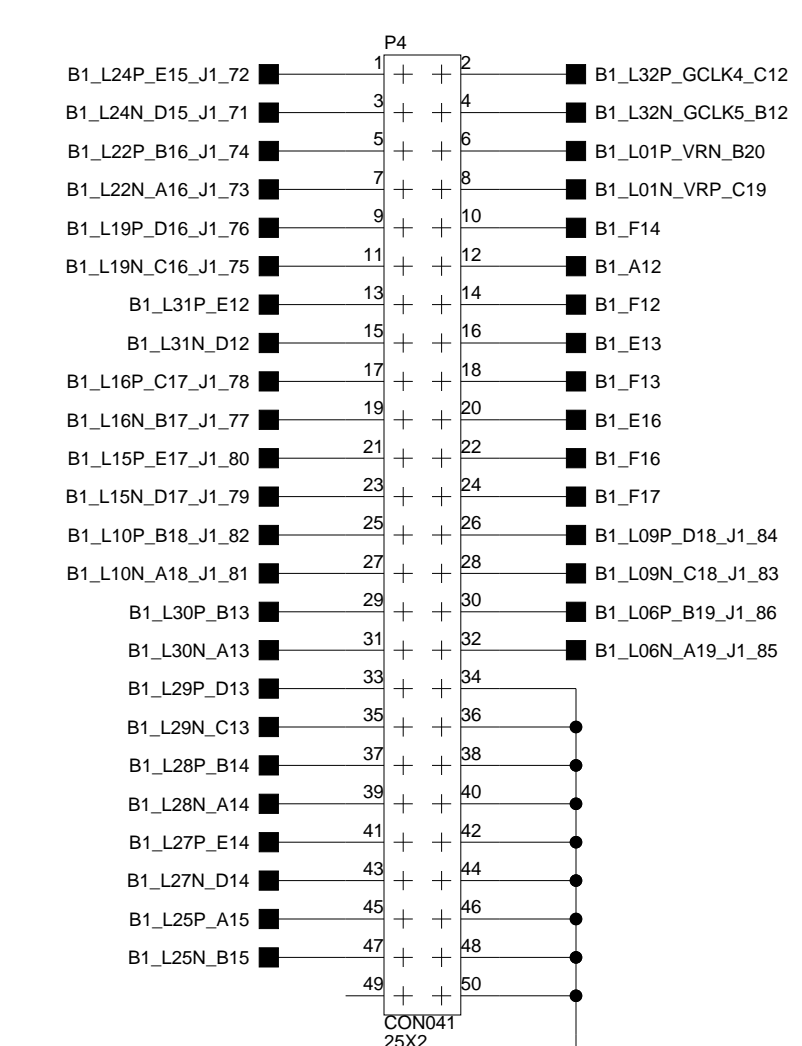
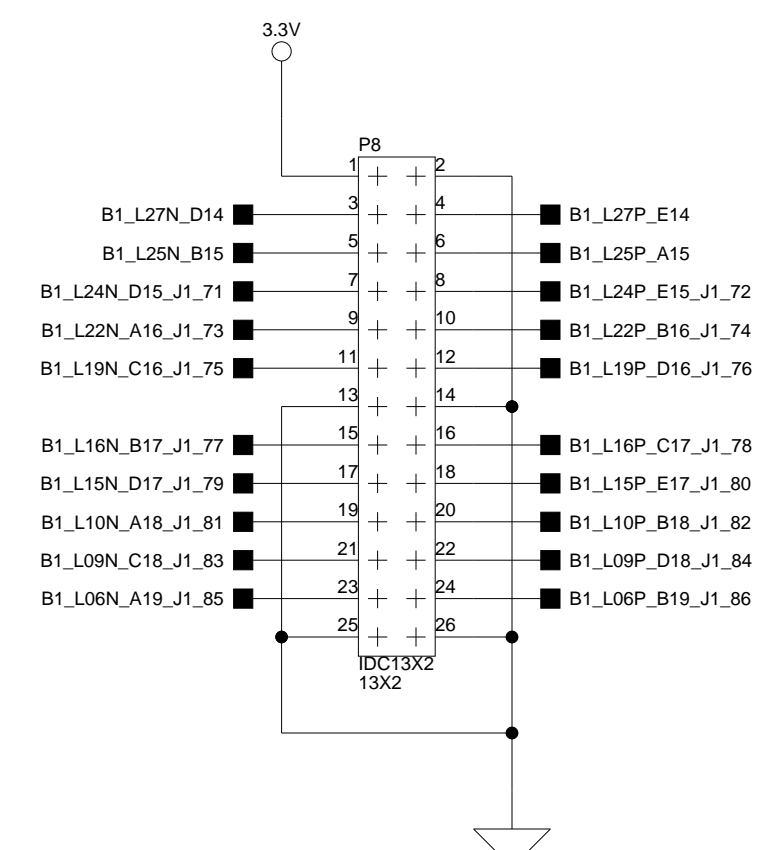
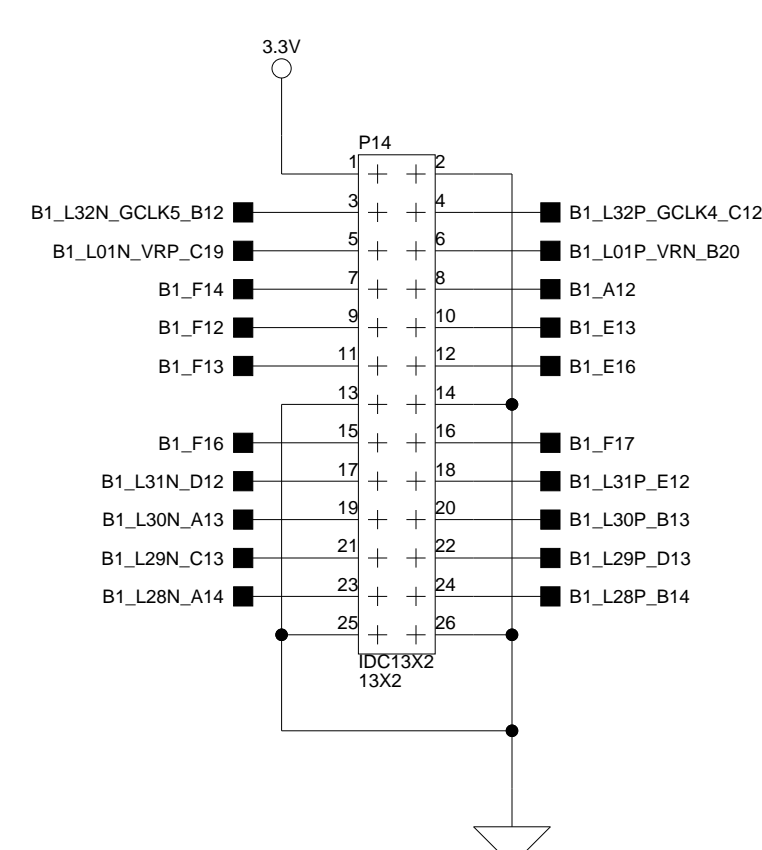
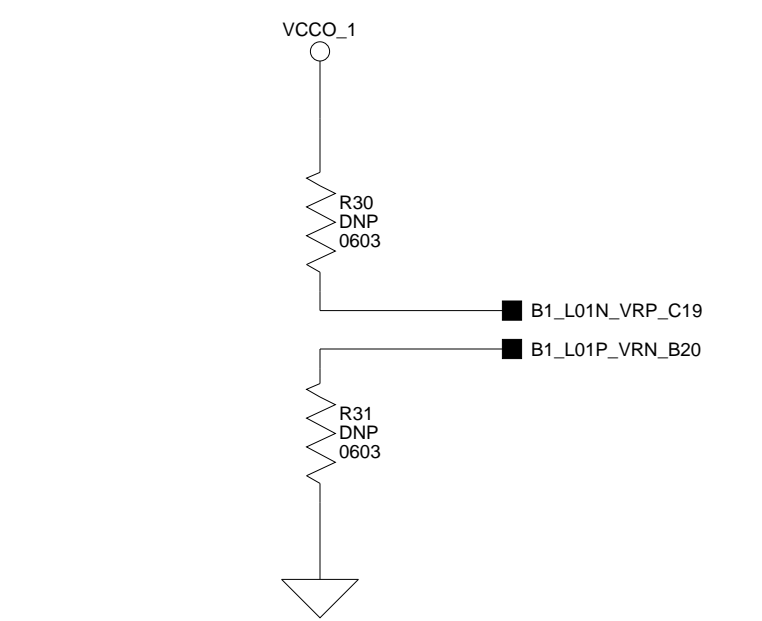
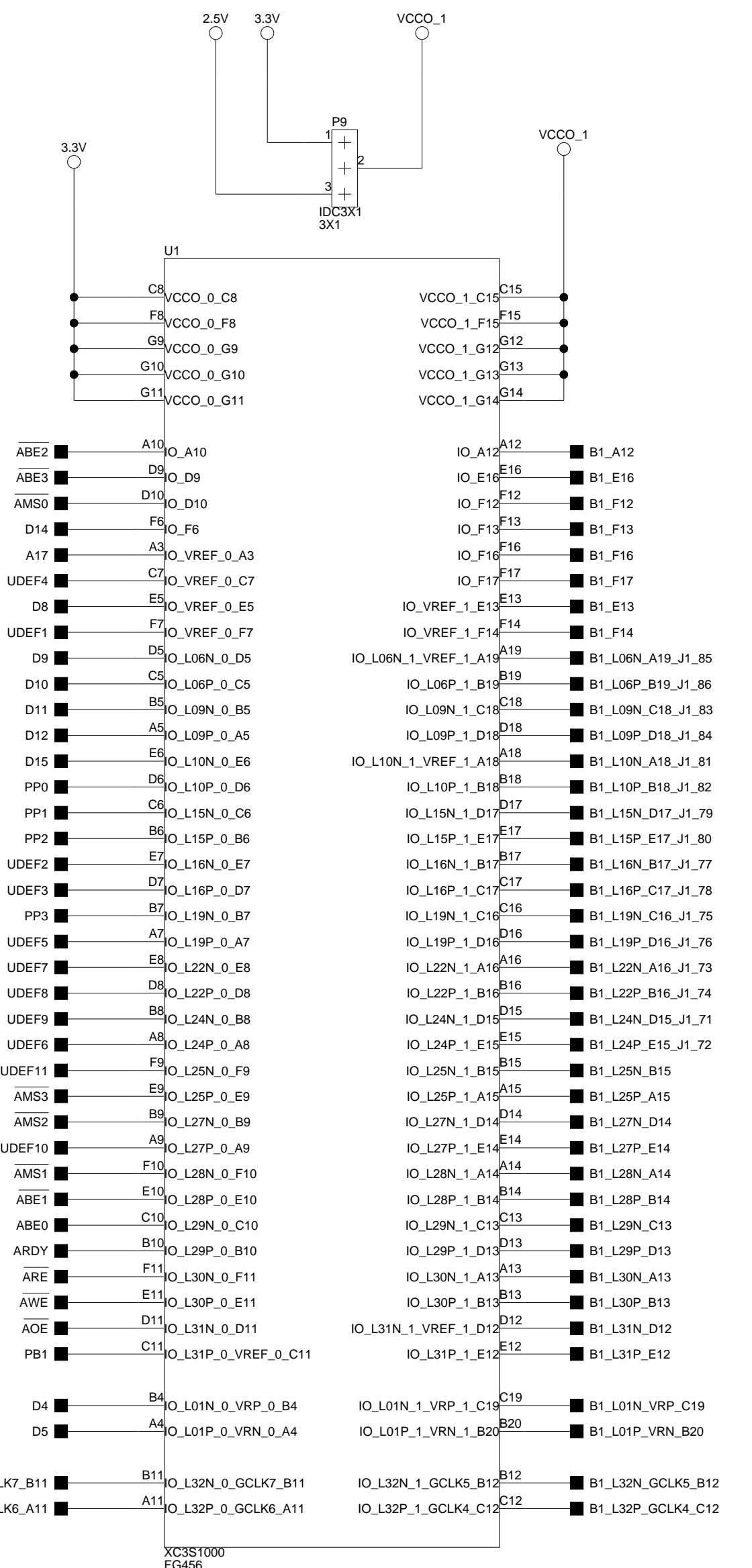
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Size C	Rev	
Date	9-27-2005_11:44	Sheet 3 of 12

EXPANSION INTERFACE TYPE B



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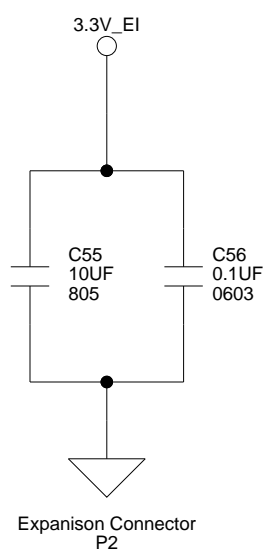
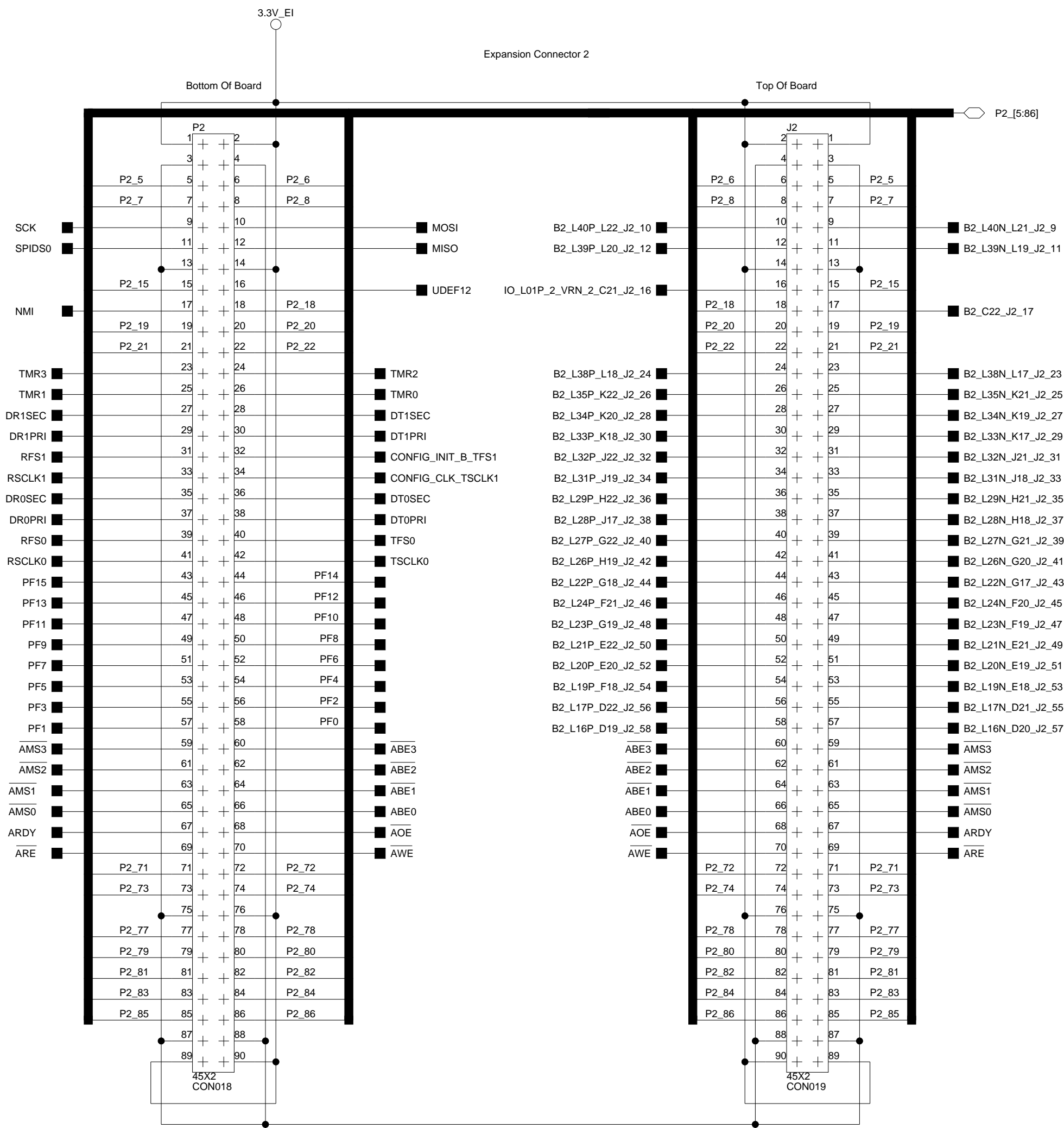
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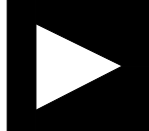
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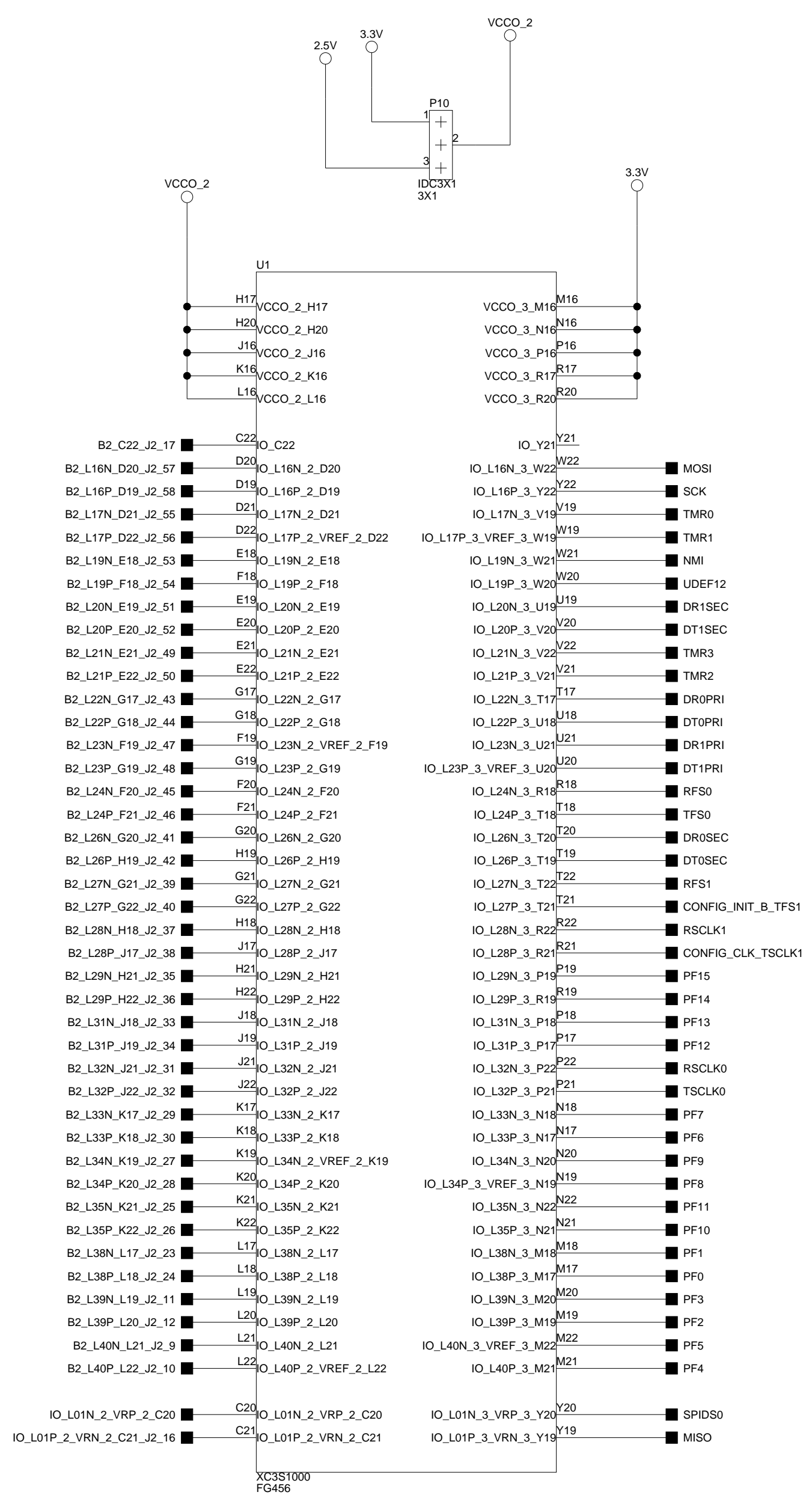
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PH: 1-800-ANALOGD

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C				1.0	
Date	9-27-2005_11:44	Sheet	5 of	12	

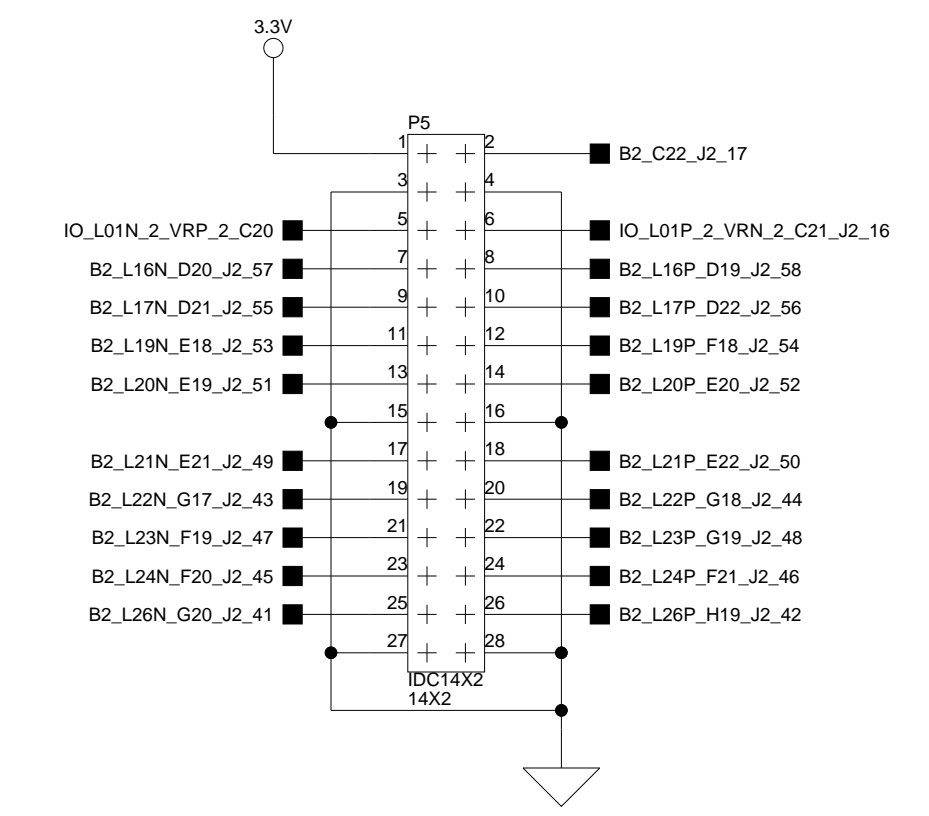
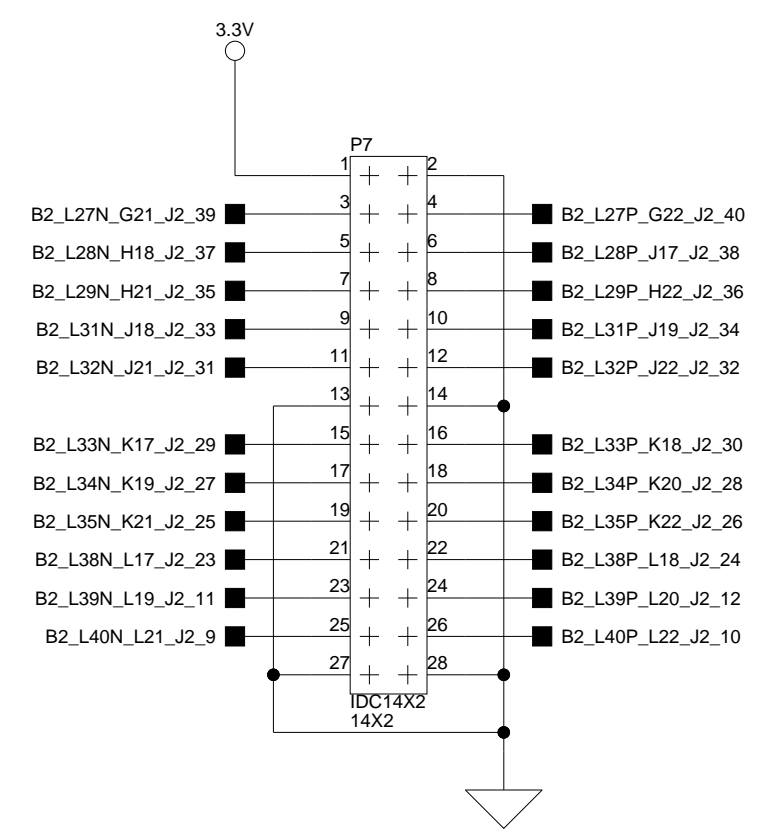
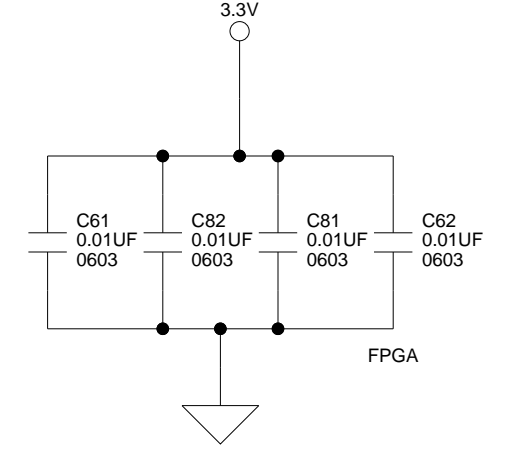
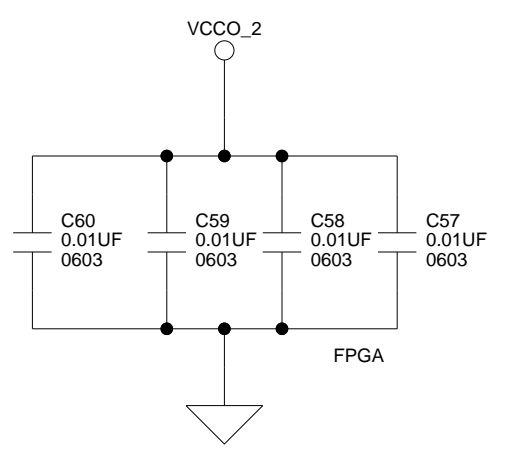
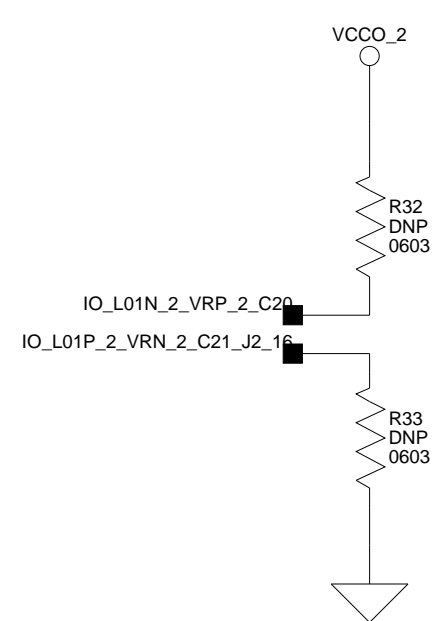
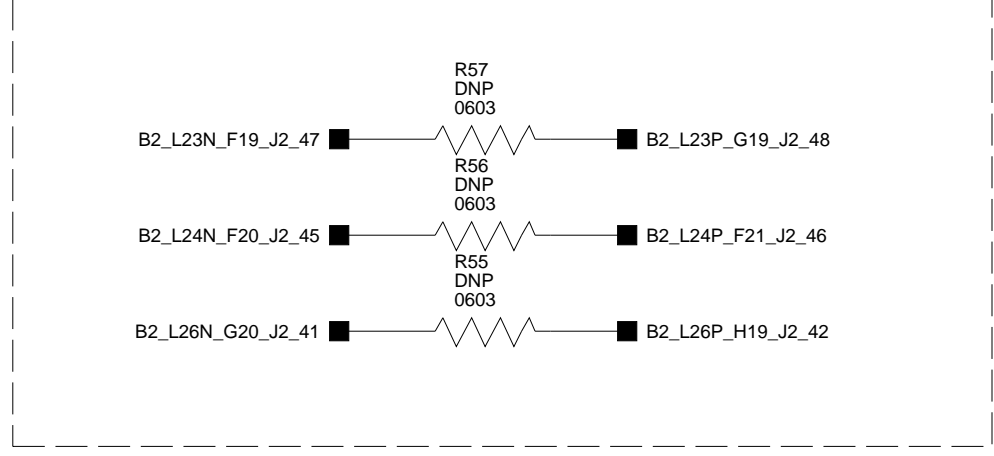


DNP = Do Not Populate

 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title BLACKFIN FPGA EZ-EXTENDER EXPANSION INTERFACE CONNECTOR 2	
Size C	Board No. A0199-2005	Rev 1.0	
Date 9-14-2005_12:03	Sheet 6 of 12		



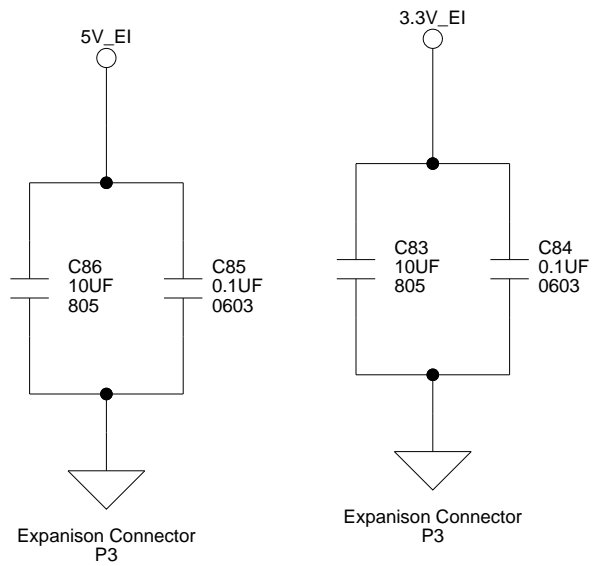
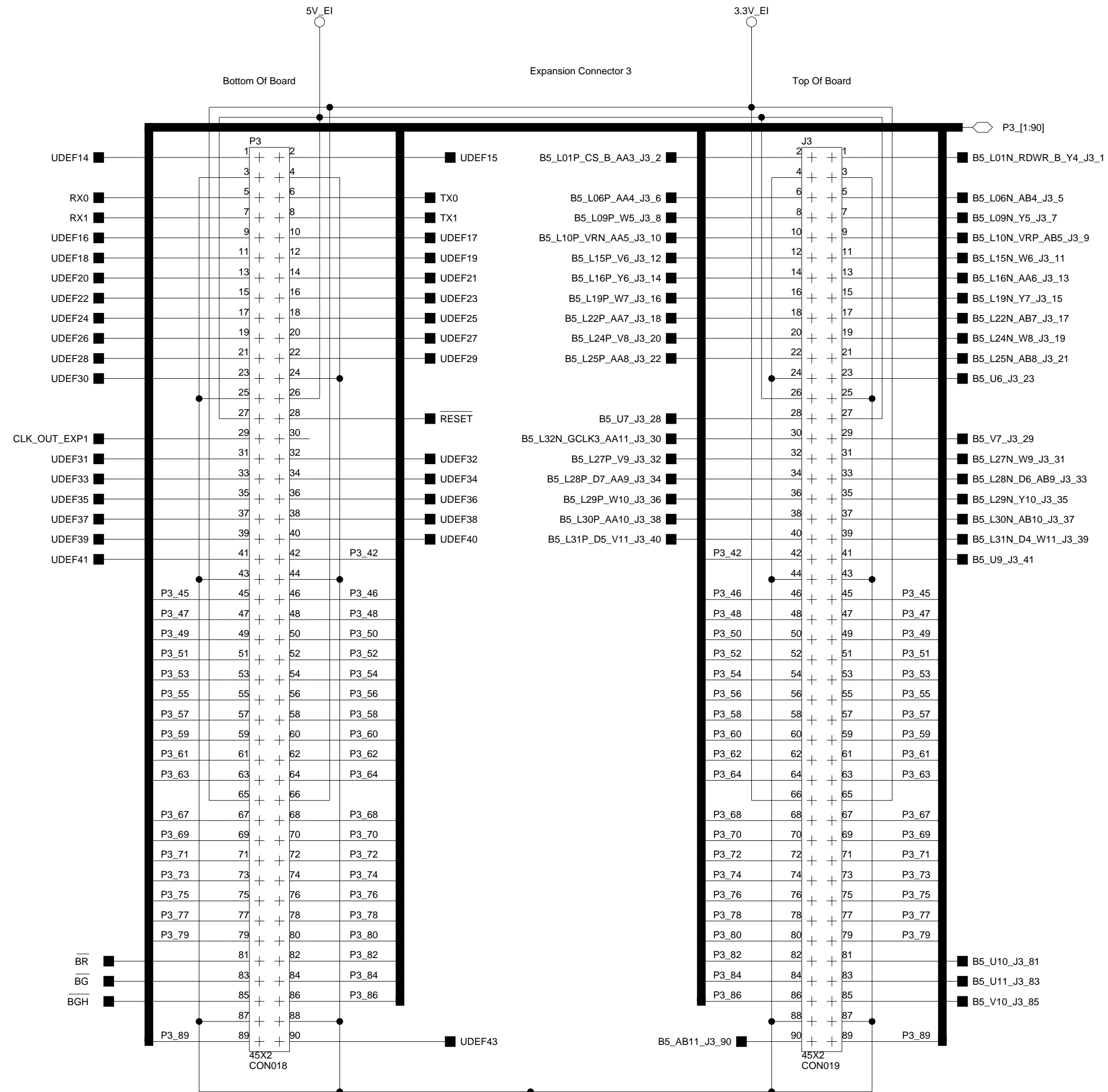
LAYOUT NOTE: PLACE NEAR FPGA



DNP = Do Not Populate

		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title BLACKFIN FPGA EZ-EXTENDER FPGA BANKS 2 + 3	
Size C	Board No. A0199-2005	Rev 1.0	
Date 9-27-2005_11:44	Sheet 7 of 12		

EXPANSION INTERFACE (TYPE B)

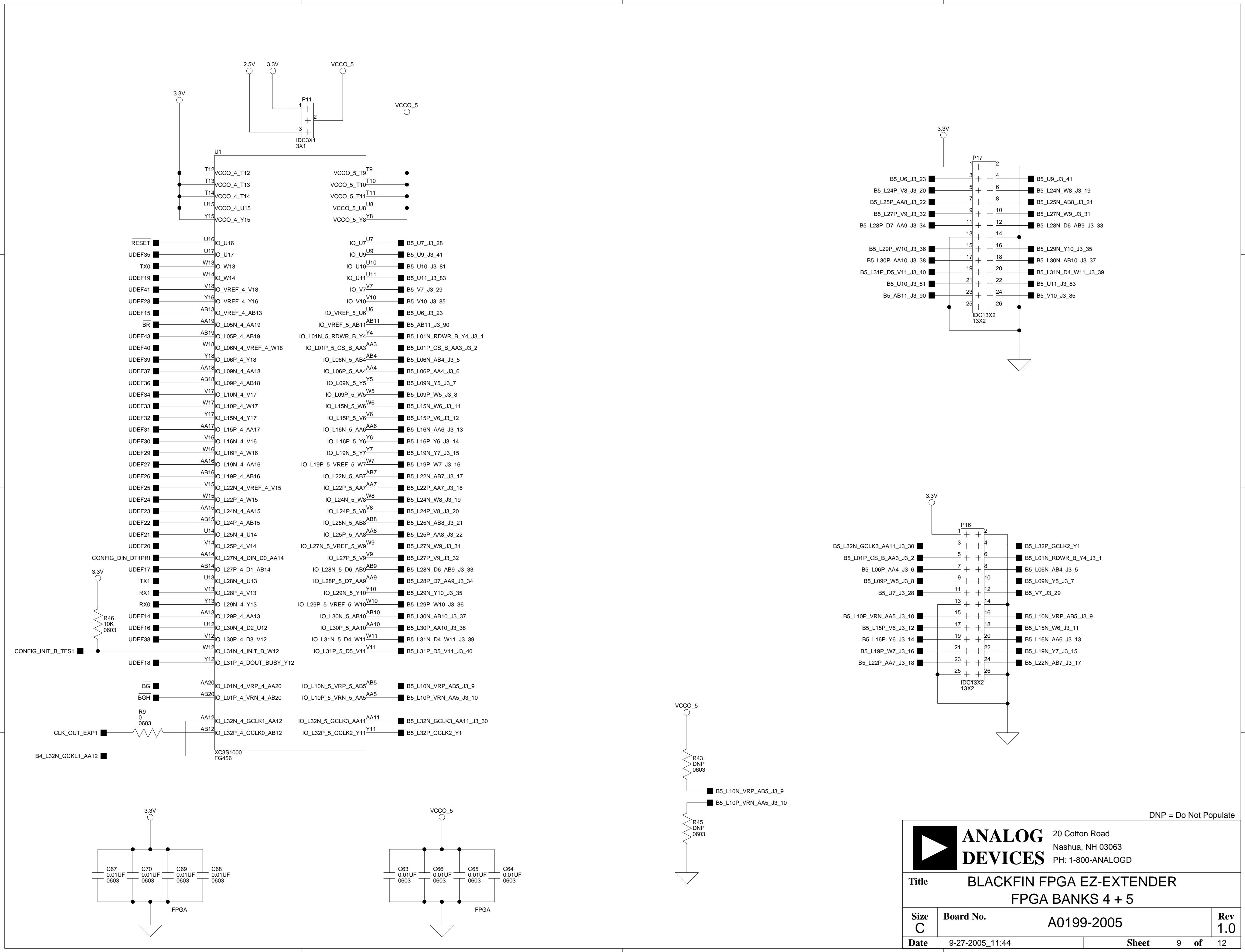


DNP = Do Not Populate

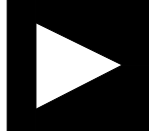
ANALOG DEVICES

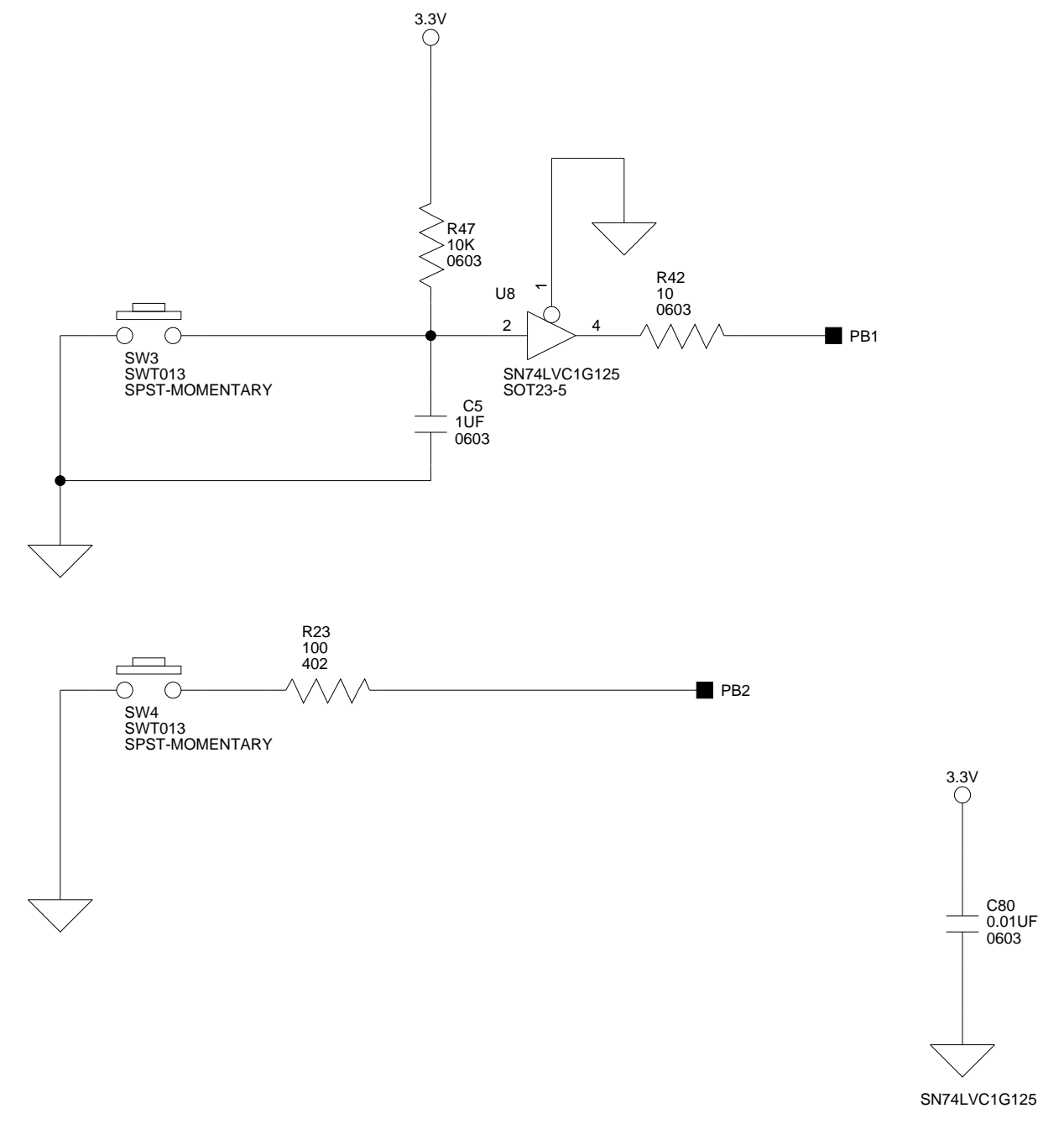
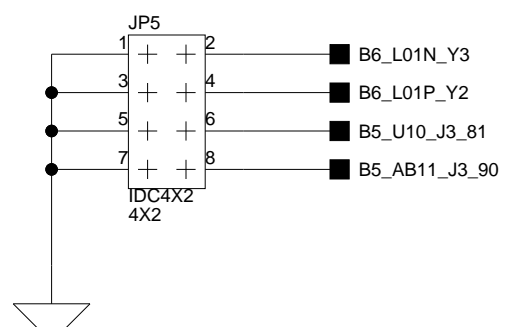
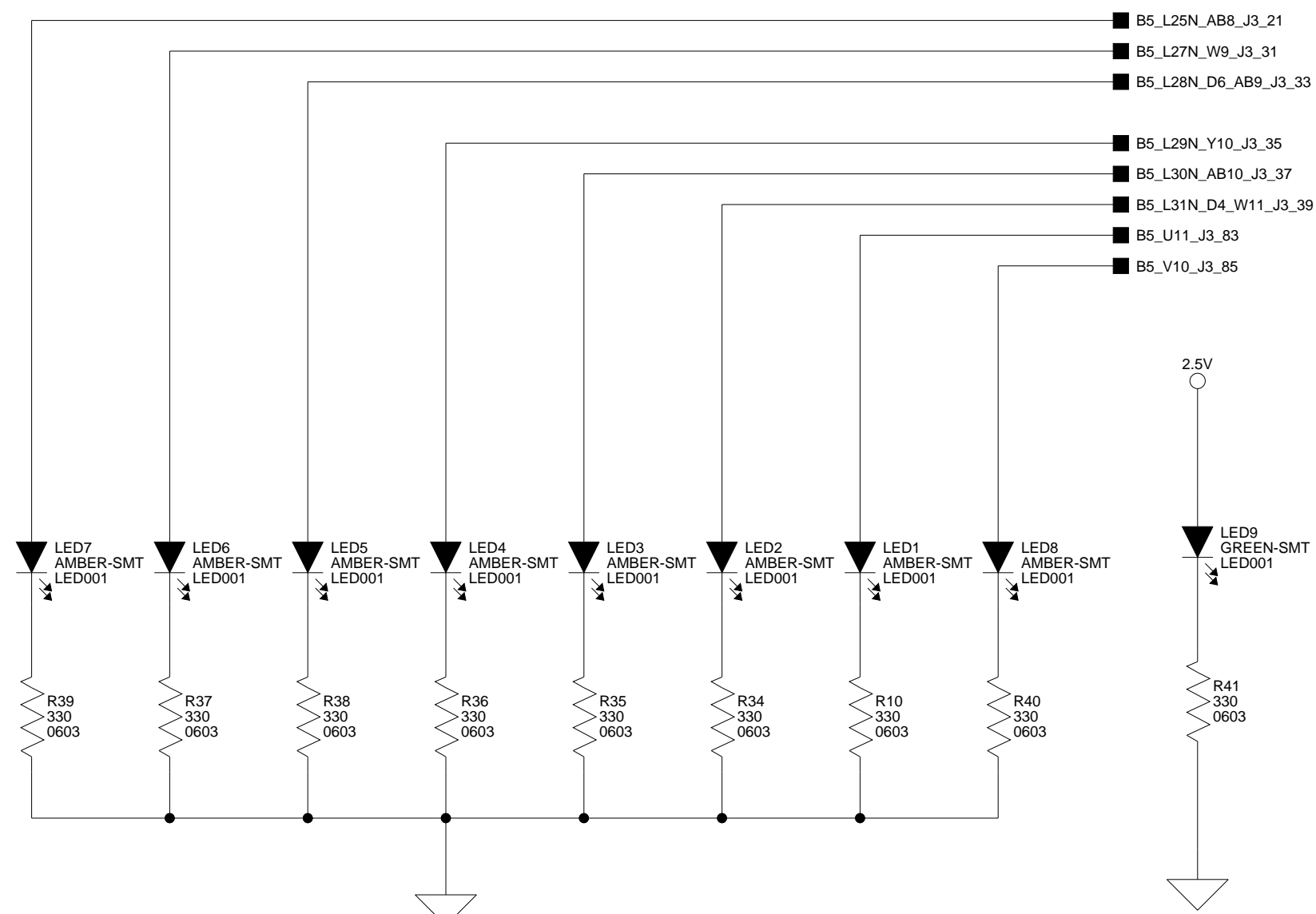
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title BLACKFIN FPGA EZ-EXTENDER EXPANSION INTERFACE CONNECTOR 1		
Size C	Board No. A0199-2005	Rev 1.0
Date 9-9-2005_10:29	Sheet 8 of 12	

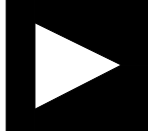


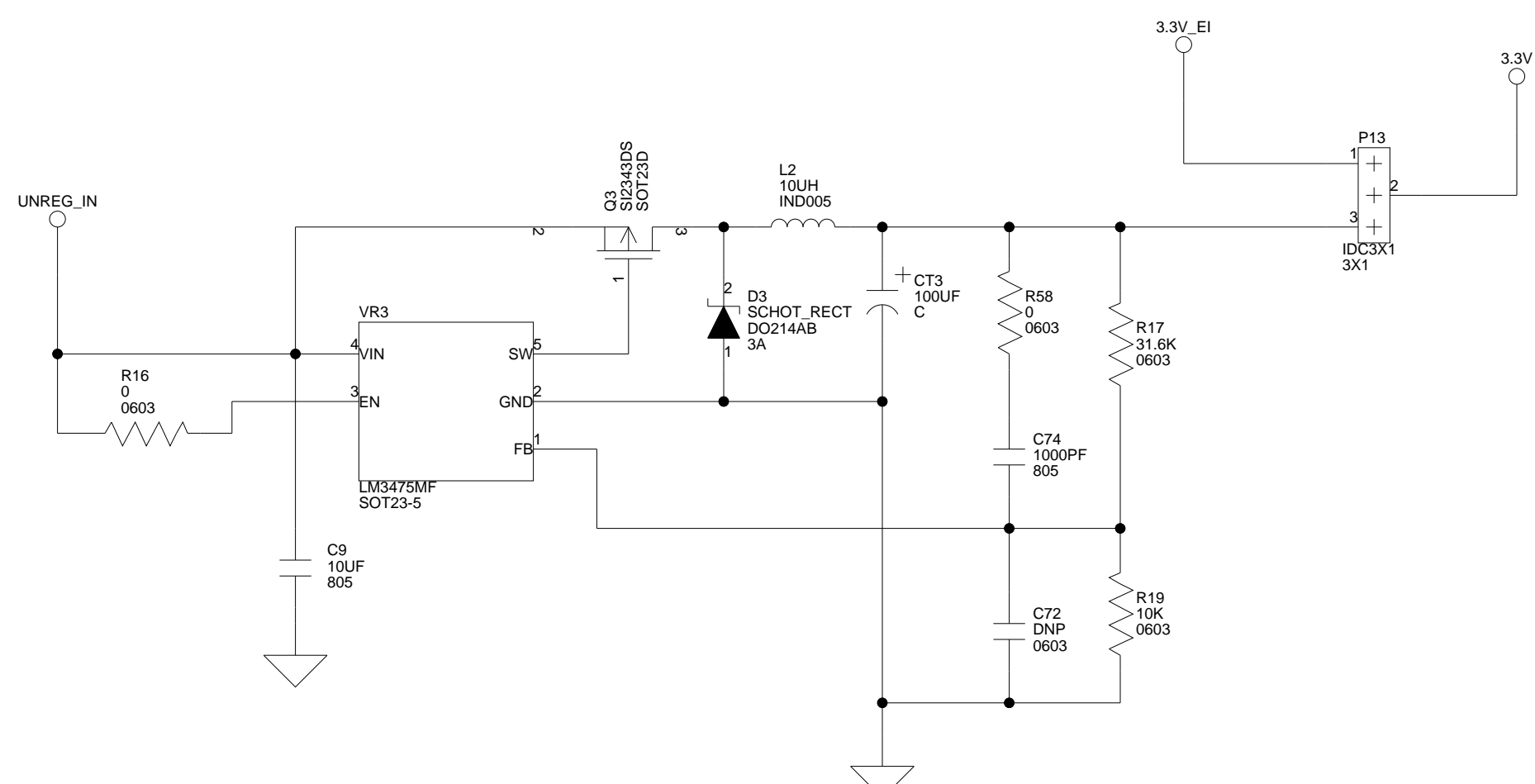
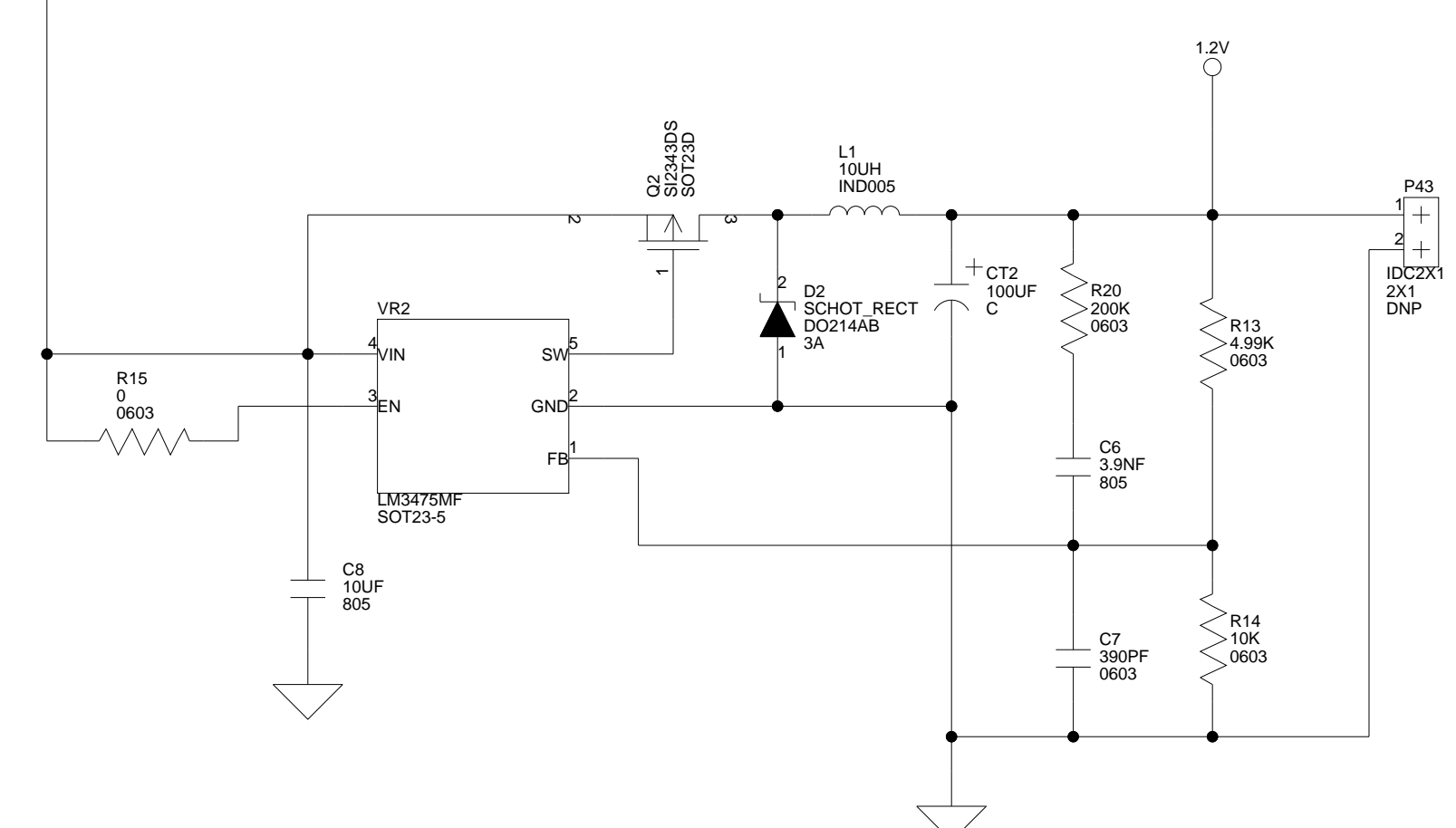
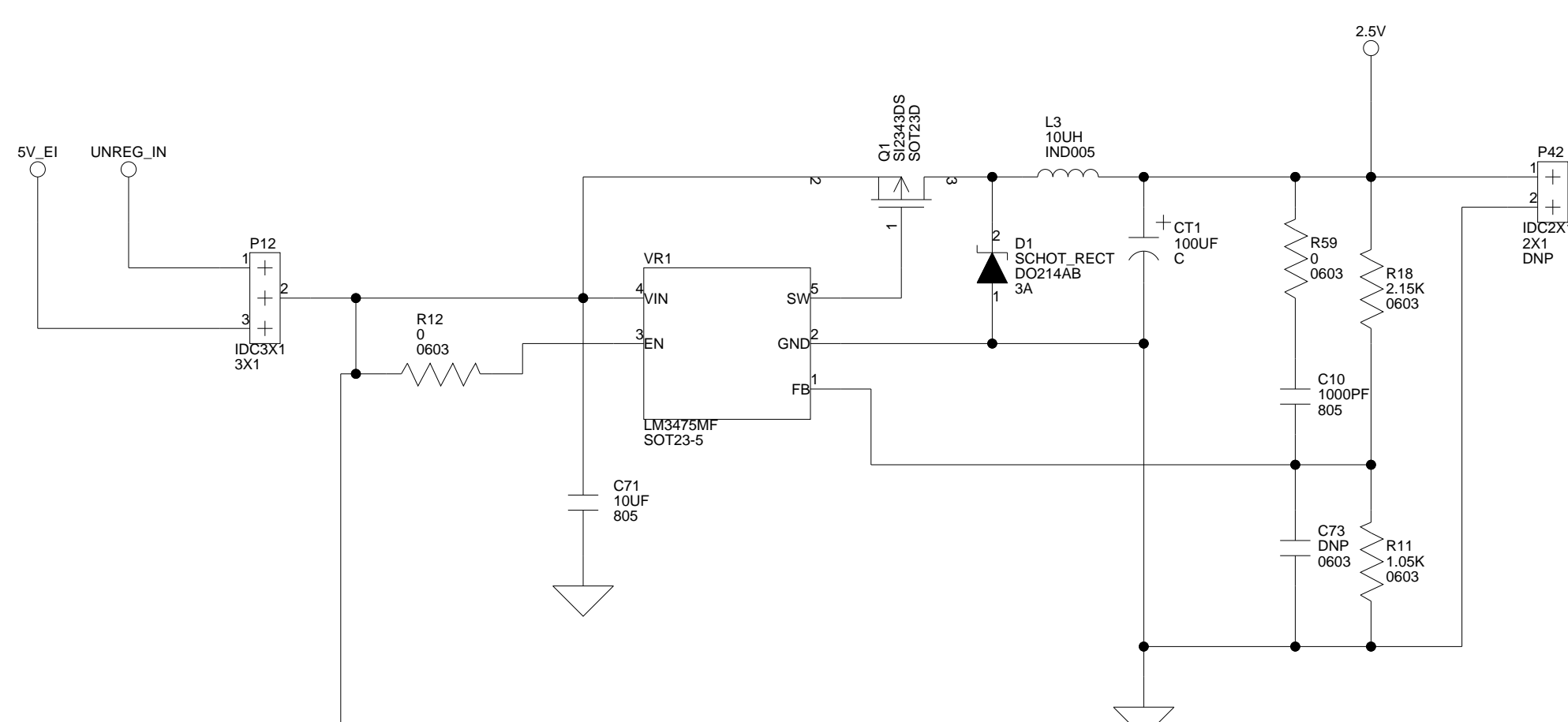
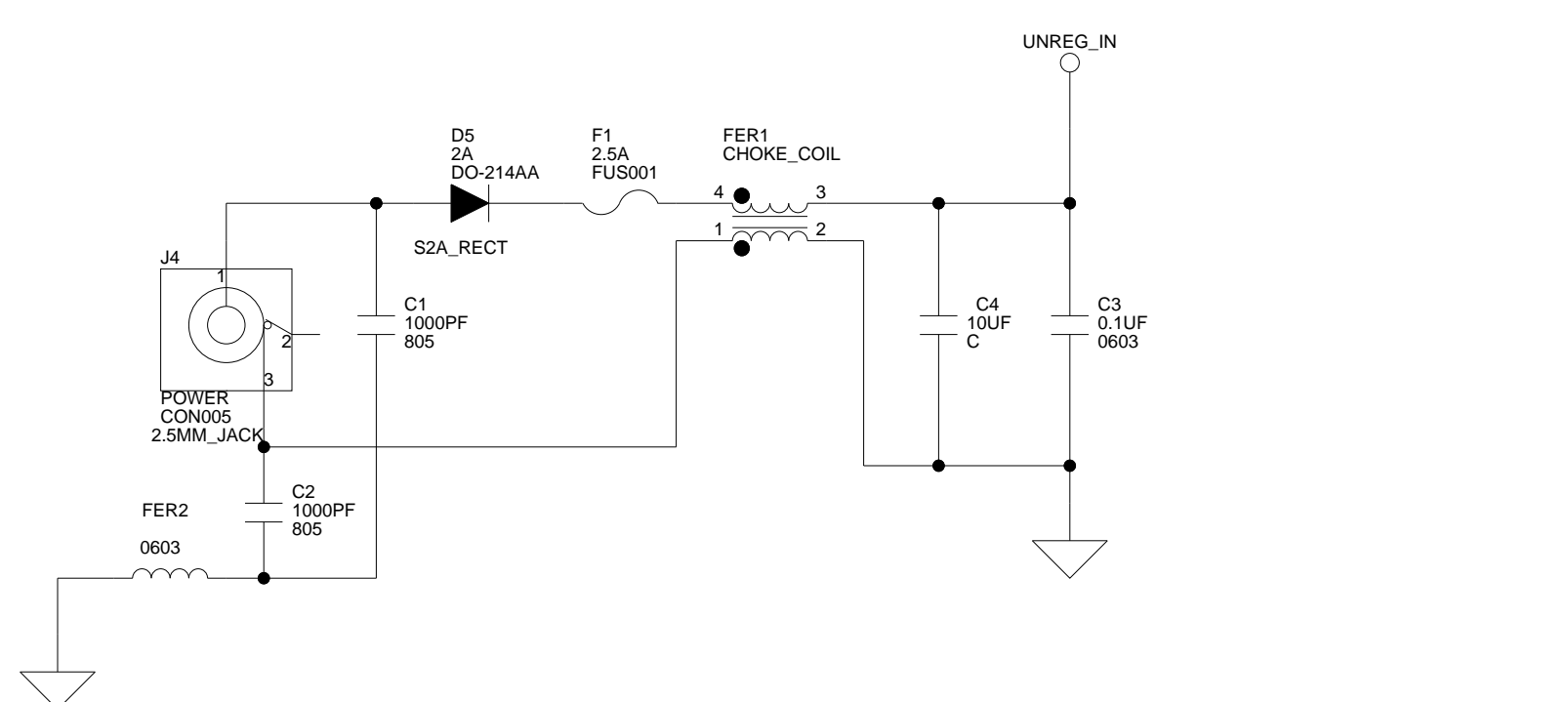
DNP = Do Not Populate

 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title BLACKFIN FPGA EZ-EXTENDER FPGA BANKS 4 + 5	
Size C	Board No. A0199-2005	Rev 1.0	
Date 9-27-2005_11:44	Sheet 9 of 12		



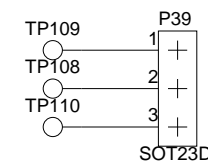
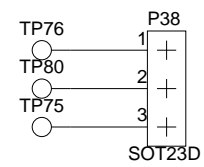
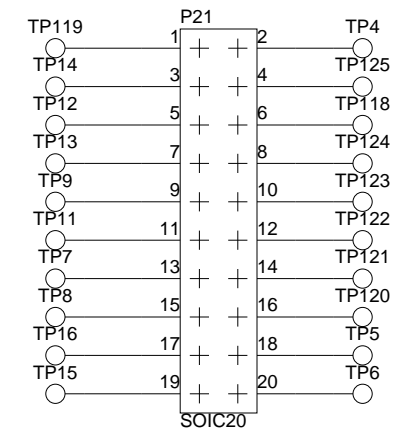
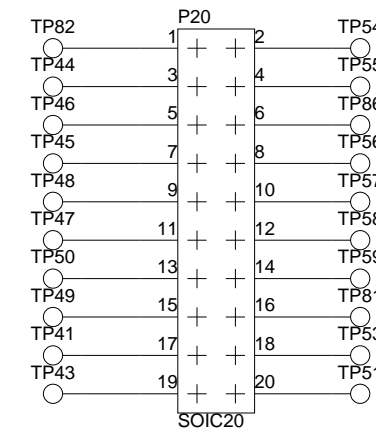
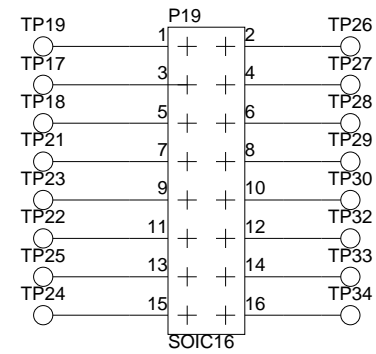
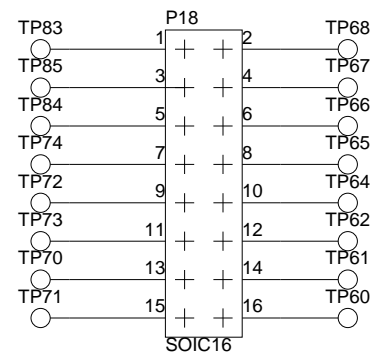
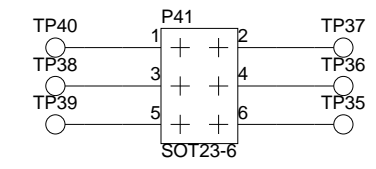
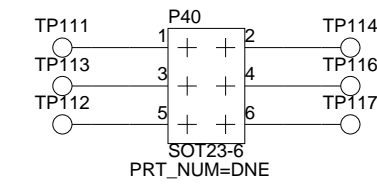
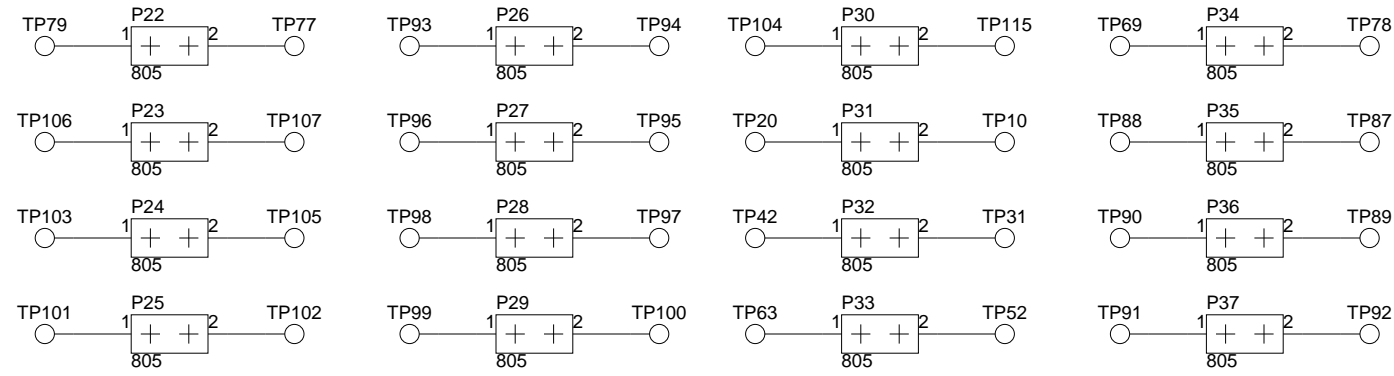
DNP = Do Not Populate

 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title BLACKFIN FPGA EZ-EXTENDER USER IO	
Size C	Board No. A0199-2005	Rev 1.0	
Date 9-27-2005_11:44	Sheet 10 of 12		



DNP = Do Not Populate

 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title BLACKFIN FPGA EZ-EXTENDER POWER	
Size C	Board No.	A0199-2005	Rev
Date	9-27-2005_11:24	Sheet	11 of 12



DNP = Do Not Populate

 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title BLACKFIN FPGA EZ-EXTENDER PROTO AREA	
Size C	Board No. A0199-2005	Rev 1.0	
Date 9-14-2005_12:04	Sheet 12 of 12		

I INDEX

Numerics

2.5V header (P42), [2-17](#)

A

ADSP-BF533/37/61 EZ-KIT Lite interface, [2-1](#)

ADSP-BF533/37/61 processors, boot mode settings, [2-14](#)

architecture, of this EZ-Extender, [2-2](#)

asynchronous static random access memory (SRAM), [x](#)

auxiliary oscillator, [x](#)

B

bill of materials, [A-1](#)

block diagram, of this EZ-Extender, [2-2](#)

boot jumper, *See* JP4

C

configuration jumpers, *See* JP2, JP3

connectors

map of locations, [2-18](#)

J1-3 (expansion), [2-19](#)

P1-3 (expansion), [2-19](#)

P14 (IDC), [2-19](#)

P15 (JTAG header), [2-4](#)

P16-17 (IDC), [2-19](#)

P4 (high-speed), [2-20](#)

P5 (IDC), [2-20](#)

P6 (JTAG), [2-7](#)

P7 (IDC), [2-20](#)

P8 (IDC), [2-19](#)

customer support, [xiii](#)

D

done LED (LED10), [2-17](#)

E

expansion interface

connectors (P1-3, J1-3), [2-19](#)

of ADSP-BF533/37/61 EZ-KIT Lites, [ix](#), [1-3](#)

external power supply, [1-3](#), [2-8](#)

F

Field-Programmable Gate Array, *See* FPGA

INDEX

FPGA

- documentation, [1-2](#)
- input jumpers (JP5), [2-14](#)
- software/firmware, [1-2](#)
- Xilinx Spartan package, [x, 1-3](#)

FPGA pins

- AB10 (LED3), [2-17](#)
- AB11 (JP5.8), [2-15](#)
- AB8 (LED7), [2-17](#)
- AB9 (LED5), [2-17](#)
- C11 (PB1/SW3), [2-15](#)
- H5 (PB2/SW3), [2-16](#)
- M2-0 (JP4), [2-14](#)
- U10 (JP5.6), [2-15](#)
- U11 (LED1), [2-17](#)
- V10 (LED8), [2-17](#)
- W11 (LED2), [2-17](#)
- W9 (LED6), [2-17](#)
- Y10 (LED4), [2-17](#)
- Y3-2 (JP5.2-5.4), [2-15](#)

FPGA programming

- block diagram, [2-3](#)
- via ADSP-BF533/37/6 processors, [2-6](#)
- via JTAG header, [2-4](#)
- via serial ROM, [2-5](#)

G

- GCLK1 (global clock 1) pin, [1-4](#)
- GCLK6 (global clock 6) pin, [1-4](#)
- general-purpose input push buttons, [2-15, 2-16](#)

H

- high-speed connector (P4), [2-20](#)

I

- IDC connectors, [x, 2-19, 2-20](#)
- installation, of this EZ-Extender, [1-1](#)

J

JTAG

- cable, [1-4, 2-7](#)
- header (P6), [1-5, 2-4, 2-7, 2-14](#)
- jumpers

- map of locations, [2-11](#)
- JP1 (boot jumper), [2-5, 2-12](#)
- JP2 (config done), [2-12](#)
- JP3 (config program), [2-13](#)
- JP4.1-4.6 (boot mode select), [2-5, 2-6, 2-14](#)
- JP5.2-5.6 (FPGA input), [2-14](#)

L

LEDs

- map of locations, [2-15](#)
- LED10 (FPGA done pin), [2-4, 2-5, 2-17](#)
- LED1-8 (status), [2-17](#)
- LED9 (power), [2-17](#)

M

- M2-0 (JP4) pins, [2-5](#)
- master serial boot mode, [2-6](#)
- MCS-86 Hexadecimal Object (.mcs) file format, [2-6](#)

N

- notation conventions, [xvi](#)

O

- oscillator, [x, 1-4](#)

P

- P12 (power in) header, [2-9](#)
- P13 (3.3V header), [2-9](#)
- P42 (2.5V header), [2-10](#)
- P43 (1.2V header), [2-10](#)
- PB1 push button (SW3), [2-15](#)

- PB2 push button (SW4), [2-16](#)
 - PF14 flag pin (ADSP-BF537 EZ-KIT Lite),
[2-12](#)
 - PF3 flag pin (ADSP-BF533/61 EZ-KIT Lite),
[2-12](#)
 - power
 - 1.2V header (P43), [2-10](#)
 - 2.5V header (P42), [2-10](#)
 - 3.3V header (P13), [2-9](#)
 - in header (P12), [2-9](#)
 - LED (LED9), [2-17](#)
 - limitations, [2-8](#)
 - supplies, [1-3](#), [2-8](#)
 - printed circuit board (PCB), [1-2](#)
 - product overview, [ix](#)
 - program push button (SW1), [2-4](#), [2-15](#)
 - push buttons
 - See also* SWx
 - map of locations, [2-15](#)
- S**
- serial ROM, [1-5](#)
 - boot jumper (JP1), [2-12](#), [2-14](#)
 - programming via JTAG Header, [2-7](#)
 - setup, of this EZ-Extender, [1-1](#)
 - slave serial mode, [2-6](#)
- SRAM memory banks, [1-4](#)
 - status reporting, [1-4](#), [2-17](#)
 - SW1 (program) push button, [2-4](#), [2-15](#)
 - SW3 (PB1) push button, [2-15](#)
 - SW4 (PB2) push button, [2-16](#)
 - switching regulators, [2-8](#)
- T**
- TCK signal, [2-7](#)
 - TDI signal, [2-7](#)
 - TDO signal, [2-7](#)
 - TMS signal, [2-7](#)
- V**
- VisualDSP++
 - flash programming utility, [1-4](#), [2-6](#)
 - FPGA documentation, [2-6](#)
 - VR1-3 regulators, [2-8](#)
- X**
- Xilinx
 - JTAG cable/software, [1-4](#), [2-4](#), [2-7](#)
 - JTAG header, [2-12](#)
 - serial ROM, [1-5](#)

INDEX