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Printed in the USA.

Limited Warranty

The EZ-KIT Lite evaluation system is warranted against defects in materials and workmanship for a period of one year from the date of purchase from Analog Devices or from an authorized dealer.

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Regulatory Compliance

The ADSP-21161N EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the “CE” mark.

The ADSP-21161N EZ-KIT Lite evaluation system had been appended to the Technical Construction File referenced “DSPTOOLS1” dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body as listed below.

Technical Certificate No: Z600ANA1.005

Issued by: Technology International (Europe) Limited
41 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TZ, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.
CONTENTS

PREFACE

Purpose of This Manual ................................................................. xiv
Intended Audience ......................................................................... xiv
Manual Contents ............................................................................ xv
What’s New in This Manual ............................................................ xv
Technical or Customer Support ...................................................... xvi
Supported Processors ...................................................................... xvi
Product Information ................................................................... xvi
    MyAnalog.com ........................................................................ xvii
    DSP Product Information ....................................................... xvii
    Related Documents .............................................................. xviii
    Online Documentation ............................................................ xix
    Printed Manuals ..................................................................... xix
        VisualDSP++ Documentation Set ...................................... xix
        Hardware Manuals ............................................................. xx
        Data Sheets ..................................................................... xx
    Contacting DSP Publications .................................................. xx
    Notation Conventions .............................................................. xxi
## GETTING STARTED

<table>
<thead>
<tr>
<th>Contents of EZ-KIT Lite Package</th>
<th>1-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC Configuration</td>
<td>1-3</td>
</tr>
<tr>
<td>Installation Tasks</td>
<td>1-3</td>
</tr>
<tr>
<td>Installing VisualDSP++ and EZ-KIT Lite Software</td>
<td>1-4</td>
</tr>
<tr>
<td>Installing and Registering VisualDSP++ License</td>
<td>1-4</td>
</tr>
<tr>
<td>Setting Up EZ-KIT Lite Hardware</td>
<td>1-5</td>
</tr>
<tr>
<td>Installing EZ-KIT Lite USB Driver</td>
<td>1-6</td>
</tr>
<tr>
<td>Windows 98 USB Driver</td>
<td>1-7</td>
</tr>
<tr>
<td>Windows 2000 USB Driver</td>
<td>1-11</td>
</tr>
<tr>
<td>Windows XP USB Driver</td>
<td>1-12</td>
</tr>
<tr>
<td>Verifying Driver Installation</td>
<td>1-14</td>
</tr>
<tr>
<td>Starting VisualDSP++</td>
<td>1-16</td>
</tr>
</tbody>
</table>

## USING EZ-KIT LITE

<table>
<thead>
<tr>
<th>EZ-KIT Lite License Restrictions</th>
<th>2-2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Map</td>
<td>2-2</td>
</tr>
<tr>
<td>Using SDRAM Memory</td>
<td>2-3</td>
</tr>
<tr>
<td>Using FLAG Pins</td>
<td>2-5</td>
</tr>
<tr>
<td>Using Interrupt Pins</td>
<td>2-6</td>
</tr>
<tr>
<td>Using Audio Interface</td>
<td>2-6</td>
</tr>
<tr>
<td>Example Programs</td>
<td>2-8</td>
</tr>
<tr>
<td>Using Flash Programmer Utility</td>
<td>2-8</td>
</tr>
<tr>
<td>Using EZ-KIT Lite VisualDSP++ Interface</td>
<td>2-9</td>
</tr>
</tbody>
</table>
CONTENTS

Boot Load ........................................................................................................... 2-9
Target Options ................................................................................................. 2-9
  While Target is Halted and On Emulator Exit Options .......................... 2-10
  Other Options ............................................................................................... 2-10
Core Hang Conditions ....................................................................................... 2-11
Hardware Breakpoints ...................................................................................... 2-12
  Common Hardware Breakpoint Attributes .............................................. 2-13
  Global Hardware Breakpoint Options ...................................................... 2-13
  Data Hardware Breakpoints ....................................................................... 2-15
  Instruction Hardware Breakpoints ............................................................. 2-16
  Other Breakpoints ....................................................................................... 2-17
Tips and Tricks Using Hardware Breakpoints .............................................. 2-18
  Latency ......................................................................................................... 2-18
  Restrictions ................................................................................................. 2-18
  Setting a Breakpoint on a Single Address .............................................. 2-18
Restricted Software Breakpoints ................................................................. 2-19

EZ-KIT LITE HARDWARE REFERENCE

System Architecture .......................................................................................... 3-2
External Port ....................................................................................................... 3-3
Host Processor Interface (HPI) ........................................................................ 3-3
SPORT Audio Interface ..................................................................................... 3-3
SPI Audio Interface ........................................................................................... 3-4
Breadboard Area ............................................................................................... 3-4
JTAG Emulation Port ......................................................................................... 3-5
CONTENTS

Jumper Settings ................................................................. 3-5

SDRAM Disable Jumper (JP1) .............................................. 3-5
SPDIF Selection Jumper (JP2) ............................................ 3-5
MCLK Selection Jumper (JP3) ............................................ 3-6
FLAG0 Enable Jumper (JP4) ............................................. 3-7
FLAG1 Enable Jumper (JP5) ............................................. 3-7
Sample Frequency Jumper (JP6) ...................................... 3-7
ADC2 Input Mode Selection Jumpers (JP7–8) ...................... 3-8
MIC Gain Selection Jumpers (JP9–10) ......................... 3-8
ADC1 Input Selection Jumper (JP11) .............................. 3-9
Processor ID Jumper (JP19) ........................................... 3-10
Boot Mode Selection Jumper (JP20) .................................. 3-10
Clock Mode Selection Jumper (JP21) .............................. 3-11
~BMS Enable Jumper (JP22) ........................................... 3-12
AD1836 Control Selection Jumper (JP23) ...................... 3-12
SW1 Enable Jumper (JP26) ............................................. 3-12
SW2 Enable Jumper (JP27) ............................................. 3-12

LEDs and Push Buttons .................................................... 3-13
Reset LEDs (LED1 and LED8) ........................................ 3-14
FLAG LEDs (LED2–7) .................................................... 3-14
VERF LED (LED9) ...................................................... 3-14
USB Monitor LED (LED10) ......................................... 3-15
Power LED (LED11) ..................................................... 3-15
Programmable FLAG Push Buttons (SW1–4) ............... 3-15
CONTENTS

Interrupt Push Buttons (SW5–7) ........................................... 3-15
Board Reset Push Button (SW8) ............................................. 3-16
Connectors .............................................................................. 3-16
USB Connector (P2) ............................................................. 3-16
Audio Connectors (P4–8, P17) ........................................... 3-18
External Port Connector (P9) ................................................ 3-18
Host Processor Interface Connector (P10) .............................. 3-19
JTAG Connector (P12) .......................................................... 3-19
Link Port Connectors (P13–14) ............................................. 3-19
SPORT1 and SPORT3 Connector (P15) ............................... 3-20
Power Connector (P16) ......................................................... 3-20
Specifications ........................................................................... 3-21
Power Supply ........................................................................ 3-21
Board Current Measurements ................................................ 3-21

BILL OF MATERIALS

INDEX
Thank you for purchasing the ADSP-21161N EZ-KIT Lite®, Analog Devices (ADI) evaluation system for SHARC® processors.

The SHARC processors are based on a 32-bit super Harvard architecture that includes a unique memory architecture comprised of two large on-chip, dual-ported SRAM blocks coupled with a sophisticated IO processor, which gives SHARC the bandwidth for sustained high-speed computations. SHARC represents today’s de facto standard for floating-point DSP targeted for premium audio applications.

The evaluation system is designed to be used in conjunction with the VisualDSP++® development environment to test the capabilities of the ADSP-21161N SHARC processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-21161N assembly
- Load, run, step, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-21161N processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-21161N processor and the
evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and DSP development tools, go to http://www.analog.com/dsp/tools/.

ADSP-21161N EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The VisualDSP++ license provided with this EZ-KIT Lite evaluation system limits the size of a user program to 5K words of internal memory.

The board features:

- Analog Devices ADSP-21161N processor
  - 100 MHz Core Clock Speed
  - Core Clock Mode Jumper Configurable

- Analog Devices AD1836 96 kHz Audio Codec
  - Jumper Selectable Line-In or Mic-In 3.5 mm Stereo Jack
  - Line-Out 3.5 mm Stereo Jack
  - 4 RCA Jacks for Audio Input
  - 8 RCA Jacks for Audio Output

- Analog Devices AD1852 192 kHz Auxiliary DAC

- Crystal Semiconductor CS8414 96 kHz SPDIF Receiver
  - Optical and Coaxial Connectors for SPDIF Input

- Flash Memory
  - 512K x 8-bits
Interface Connectors

- 14-Pin Emulator Connector for JTAG Interface
- SPORT Connectors
- Link Port 0 and Link Port 1
- External Port Connectors (not populated)

General-Purpose IO

- 4 Push Button Flags
- 3 Push Button Interrupts
- 6 LED Outputs

Analog Devices ADP3338 and ADP3339 Voltage Regulators

Breadboard area with typical SMT footprints

The EZ-KIT Lite board has a Flash memory device that can be used to store user-specific boot code. By configuring the jumpers for EPROM boot, the board can run as a stand-alone unit. The ADSP-21161N EZ-KIT Lite package contains a Flash programmer utility, which allows you to program the flash memory. The “Using Flash Programmer Utility” is described on page 2-8.

SPORT0 and SPORT2 connect to the audio codec, facilitating creation of audio-signal processing applications. SPORT1 and SPORT3 connect to off-board connectors of other serial devices.

Additionally, the EZ-KIT Lite board provides un-installed expansion connector footprints that allow you to connect to the processor’s External Port (EP) and Host Processor Interface (HPI).
Purpose of This Manual

The ADSP-21161N EZ-KIT Lite Evaluation System Manual provides instructions for using the hardware and installing the software on your PC. The text includes guidelines for running your own code on the ADSP-21161N EZ-KIT Lite. The manual also describes the board’s configuration and components. Finally, a schematic and a bill of materials are provided as a reference for future ADSP-21161N board designs.

Intended Audience

This manual is a user’s guide and reference to the ADSP-21161N EZ-KIT Lite evaluation system. Programmers who are familiar with the Analog Devices SHARC processor architecture, operation, and programming are the primary audience for this manual.

Programmers who are unfamiliar with Analog Devices SHARC processors can use this manual in conjunction with the ADSP-21161 SHARC Processor Hardware Reference and ADSP-21160 SHARC Processor Instruction Set Reference, which describe the DSP’s architecture and instruction set. Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and the VisualDSP++ user’s or getting started guides. For the locations of these documents, see “Related Documents” on page -xviii.
Preface

Manual Contents

The manual consists of:

- Chapter 1, “Getting Started” on page 1-1
  Provides software and hardware installation procedures, PC system requirements, and basic board information.

- Chapter 2, “Using EZ-KIT Lite” on page 2-1
  Provides information on the EZ-KIT Lite from a programmer’s perspective and provides a simplified memory map.

- Chapter 3, “EZ-KIT Lite Hardware Reference” on page 3-1
  Provides information on the hardware aspects of the evaluation system.

- Appendix A, “Bill Of Materials” on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.

- Appendix B, “Schematics” on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.
  The appendix is not part of the online Help. The online Help viewers should go the PDF version of the ADSP-21161N EZ-KIT Lite Evaluation System Manual located in the Docs\EZ-KIT Lite Manuals folder on the installation CD to see the schematics.

What’s New in This Manual

This is the third edition of the ADSP-21161N EZ-KIT Lite Evaluation System Manual. The new edition includes the updated installation and license registration procedures.
Technical or Customer Support

You can reach DSP Tools Support in the following ways.

- Visit the DSP Development Tools website at
  

- Email questions to
  
  dsptools.support@analog.com

- Phone questions to 1-800-ANALOGD

- Contact your ADI local sales office or authorized distributor

- Send questions by mail to
  
  Analog Devices, Inc.
  One Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

The ADSP-21161N EZ-KIT Lite evaluation system supports Analog Devices ADSP-21161N SHARC processors.

Product Information

You can obtain product information from the Analog Devices website, from the product CD-ROM, or from the printed publications (manuals).
Analog Devices is online at www.analog.com. Our website provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices website that allows customization of a webpage to display only the latest information on products you are interested in. You can also choose to receive weekly email notification containing updates to the webpages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit www.myanalog.com to sign up. Click Register to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your email address.

DSP Product Information

For information on digital signal processors, visit our website at www.analog.com/dsp, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- Email questions or requests for information to dsp.support@analog.com

- Fax questions or requests for information to 1-781-461-3010 (North America) or +49 (0) 89 76903-157 (Europe)
Product Information

Related Documents

For information on product related development software, see the following publications.

Table 1. Related DSP Publications

<table>
<thead>
<tr>
<th>Title</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADSP-21161N DSP Data Sheet</td>
<td>General functional description, pinout, and timing</td>
</tr>
<tr>
<td>ADSP-21161 SHARC Processor Hardware Reference</td>
<td>Description of internal processor architecture, registers, and all peripheral functions</td>
</tr>
<tr>
<td>ADSP-21160 SHARC Processor Instruction Set Reference</td>
<td>Description of all allowed processor assembly instructions</td>
</tr>
</tbody>
</table>

Table 2. Related VisualDSP++ Publications

<table>
<thead>
<tr>
<th>Title</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VisualDSP++ 3.5 User’s Guide for 32-Bit Processors</td>
<td>Detailed description of VisualDSP++ 3.5 features and usage</td>
</tr>
<tr>
<td>VisualDSP++ 3.5 Assembler and Preprocessor Manual for SHARC Processors</td>
<td>Description of the assembler function and commands for SHARC processors</td>
</tr>
<tr>
<td>VisualDSP++ 3.5 C/C++ Compiler and Library Manual for SHARC Processors</td>
<td>Description of the compiler function and commands for SHARC processors</td>
</tr>
<tr>
<td>VisualDSP++ 3.5 Linker and Utilities Manual for 32-Bit Processors</td>
<td>Description of the linker function and commands for the 32-bit processors</td>
</tr>
<tr>
<td>VisualDSP++ 3.5 Loader Manual for 32-Bit Processors</td>
<td>Description of the loader function and commands for the 32-bit processors</td>
</tr>
</tbody>
</table>
Preface

The listed documents can be found through online Help or in the Docs folder of your VisualDSP++ installation. Most documents are available in printed form.

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, refer to the documentation that accompanies the emulator.

Online Documentation

Your software installation kit includes online Help as part of the Windows® interface. These help files provide information about VisualDSP++ and the ADSP-21161N EZ-KIT Lite evaluation system.

To view VisualDSP++ Help, click on the Help menu item or go to the Windows task bar and select Start —> Programs —> Analog Devices —> VisualDSP++ for 32-bit Processors —> VisualDSP++ Documentation.

To view ADSP-21161N EZ-KIT Lite Help, which now is a part of the VisualDSP++ Help system, go the Contents tab of the Help window and select Manuals —> Hardware Tools —> EZ-KIT Lite Evaluation Systems.

For more documentation, please go to http://www.analog.com/technology/dsp/library.html.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at 1-800-ANALOGD (1-800-262-5643) and follow the prompts.

VisualDSP++ Documentation Set

Printed copies of VisualDSP++ manuals may be purchased through Analog Devices Customer Service at 1-781-329-4700; ask for a Customer Service representative. The manuals can be purchased only as a kit. For additional information, call 1-603-883-2430.
**Product Information**

If you do not have an account with Analog Devices, you will be referred to Analog Devices distributors. To get information on our distributors, log onto [www.analog.com/salesdir/continent.asp](http://www.analog.com/salesdir/continent.asp).

**Hardware Manuals**

Printed copies of hardware reference and instruction set reference manuals can be ordered through the Literature Center or downloaded from the Analog Devices website. The phone number is **1-800-ANALOGD** (1-800-262-5643). The manuals can be ordered by a title or by product number located on the back cover of each manual.

**Data Sheets**

All data sheets can be downloaded from the Analog Devices website. As a general rule, printed copies of data sheets with a letter suffix (L, M, N, S) can be obtained from the Literature Center at **1-800-ANALOGD** (1-800-262-5643) or downloaded from the website. Data sheets without the suffix can be downloaded from the website only—no hard copies are available. You can ask for the data sheet by part name or by product number.

If you want to have a data sheet faxed to you, the phone number for that service is **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. Call the Literature Center first to find out if requested data sheets are available.

**Contacting DSP Publications**

Please send your comments and recommendations on how to improve our manuals and online Help. You can contact us at dsp.techpubs@analog.com.
## Notation Conventions

The following table identifies and describes text conventions used in this manual.

> Additional conventions, which apply only to specific chapters, may appear throughout this document.

<table>
<thead>
<tr>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Close command</strong> (File menu) or <strong>OK</strong></td>
<td>Text in <strong>bold</strong> style indicates the location of an item within the VisualDSP++ environment's and boards' menu system and user interface items.</td>
</tr>
<tr>
<td>`{this</td>
<td>that}`</td>
</tr>
<tr>
<td>`[this</td>
<td>that]`</td>
</tr>
<tr>
<td><code>[this,...]</code></td>
<td>Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipsis; read the example as an optional comma-separated list of <strong>this</strong>.</td>
</tr>
<tr>
<td><strong>PF9-0</strong></td>
<td>Registers, connectors, pins, commands, directives, keywords, code examples, and feature names are in text with <strong>letter gothic</strong> font.</td>
</tr>
<tr>
<td><strong>filename</strong></td>
<td>Non-keyword placeholders appear in text with italic style format.</td>
</tr>
<tr>
<td>!</td>
<td>A note providing information of special interest or identifying a related topic. In the online version of this book, the word <strong>Note</strong> appears instead of this symbol.</td>
</tr>
<tr>
<td>☢</td>
<td>A caution providing information about critical design or programming issues that influence operation of a product. In the online version of this book, the word <strong>Caution</strong> appears instead of this symbol.</td>
</tr>
</tbody>
</table>
Notation Conventions
1 GETTING STARTED

This chapter provides information you need to begin using ADSP-21161N EZ-KIT Lite evaluation system. For correct operation, install the software and hardware in the order presented in “Installation Tasks” on page 1-3.

The chapter includes the following sections.

- “Contents of EZ-KIT Lite Package” on page 1-1
  Provides a list of the components shipped with this EZ-KIT Lite evaluation system.

- “PC Configuration” on page 1-3
  Describes the minimum requirements for the PC to work with the EZ-KIT Lite.

- “Installation Tasks” on page 1-3
  Describes the step-by-step procedures for setting up the hardware and software.

Contents of EZ-KIT Lite Package

Your ADSP-21161N EZ-KIT Lite evaluation system package contains the following items.

- ADSP-21161N EZ-KIT Lite board
- EZ-KIT Lite Installation Procedure
- VisualDSP++ 3.5 Installation Quick Reference Card
Contents of EZ-KIT Lite Package

- CD containing:
  - VisualDSP++ 3.5 for 32-bit processors with a limited license
  - ADSP-21161N EZ-KIT Lite debug software
  - USB driver files
  - Example programs
  - ADSP-21161N EZ-KIT Lite Evaluation System Manual (this document)
- Universal 7V DC power supply
- USB 2.0 type cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.
**PC Configuration**

For correct operation of the VisualDSP++ software and the EZ-KIT Lite, your computer must have the minimum configuration:

<table>
<thead>
<tr>
<th>Windows 98, Windows 2000, Windows XP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel (or comparable) 166MHz processor</td>
</tr>
<tr>
<td>VGA Monitor and color video card</td>
</tr>
<tr>
<td>2-button mouse</td>
</tr>
<tr>
<td>50 MB free on hard drive</td>
</tr>
<tr>
<td>32 MB RAM</td>
</tr>
<tr>
<td>Full-speed USB port</td>
</tr>
<tr>
<td>CD-ROM Drive</td>
</tr>
</tbody>
</table>

EZ-KIT Lite does not run under Windows 95 or Windows NT.

**Installation Tasks**

The following task list is provided for the safe and effective use of the ADSP-21161N EZ-KIT Lite. Follow the instructions in the presented order to ensure correct operation of your software and hardware.

1. VisualDSP++ and EZ-KIT Lite software installation
2. VisualDSP++ license installation and registration
3. EZ-KIT Lite hardware setup
4. EZ-KIT Lite USB driver installation
5. USB driver installation verification
6. VisualDSP++ startup
Installation Tasks

Installing VisualDSP++ and EZ-KIT Lite Software

This EZ-KIT Lite comes with the latest version of VisualDSP++ 3.5 for 32-bit processors. VisualDSP++ installation includes EZ-KIT Lite installations.

To install VisualDSP++ and EZ-KIT Lite software:

1. Insert the VisualDSP++ installation CD into the CD-ROM drive.

2. If Autoplay is enabled on your PC, you see the Install Shield Wizard Welcome screen. Otherwise, choose Run from the Start menu, and enter D:\ADI_Setup.exe in the Open field, where D is the name of your local CD-ROM drive.

3. Follow the on-screen instructions to continue installing the software.

4. At the Custom Setup screen, select your EZ-KIT Lite from the list of available systems and choose the installation directory. Click an icon in the Feature Description field to see the selected system’s description. When you have finished, click Next.

5. At the Ready to Install screen, click Back to change your install options, click Install to install the software, or click Cancel to exit the install.

6. When the EZ-KIT Lite installs, the Wizard Completed screen appears. Click Finish.

Installing and Registering VisualDSP++ License

VisualDSP++ and EZ-KIT Lites are licensed products. You may run only one copy of the software for each license purchased. Once a new copy of the VisualDSP++ or EZ-KIT Lite software is installed on your PC, you must install, register, and validate your licence.
Getting Started

The VisualDSP++ 3.5 Installation Quick Reference Card included in your package will guide you through the licence installation and registration process (refer to Tasks 1, 2, and 3).

Setting Up EZ-KIT Lite Hardware

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-21161N EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

To connect the EZ-KIT Lite board:

1. Remove the EZ-KIT Lite board from the package. Be careful when handling the board to avoid the discharge of static electricity, which may damage some components.

2. Figure 1-1 shows the default jumper settings, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before moving to the next step.

3. Plug the provided power supply into P16 on the EZ-KIT Lite board. Visually verify that the green power LED (LED11) is on. Also verify that the two red RESET LEDs (LED1 and LED8) go on for a moment and then go off.
Installation Tasks

4. Connect one end of the USB cable to an available full-speed USB port on your PC and the other end to P2 on the ADSP-21161N EZ-KIT Lite board.

Installing EZ-KIT Lite USB Driver

The EZ-KIT Lite evaluation system installed on the following platforms requires one full-speed USB port.

- “Windows 98 USB Driver” on page 1-7 describes the installation on Windows 98.
“Windows XP USB Driver” on page 1-12 describes the installation on Windows XP.

The USB driver used by the debug agent is not Microsoft certified because it is intended for a development or laboratory environment, not a commercial environment.

Windows 98 USB Driver

Before using the ADSP-21161N EZ-KIT Lite for the first time, the Windows 98 USB driver must first be installed.

To install the USB driver:

1. Insert the CD into the CD-ROM drive.
   The connection of the device to the USB port activates the Windows 98 Add New Hardware Wizard shown in Figure 1-2.

2. Click Next.

Figure 1-2. Windows 98 – Add New Hardware Wizard
Installation Tasks

3. Select **Search for the best driver for your device**, as shown in Figure 1-3.

![Figure 1-3. Windows 98 – Searching for Driver](image)

4. Click **Next**.

5. Select **CD-ROM drive**, as shown in Figure 1-4.

![Figure 1-4. Windows 98 – Searching for CD-ROM](image)
6. Click Next.
Windows 98 locates the WmUSBEz.inf file on the installation CD, as shown in Figure 1-5.

![Figure 1-5. Windows 98 – Locating Driver](image)

7. Click Next.
The Coping Files dialog box appears (Figure 1-6).

![Figure 1-6. Windows 98 – Searching for .SYS File](image)
Installation Tasks

8. Click Browse.
   The Open dialog box, shown in Figure 1-7, appears on the screen.


10. Click OK. The Copying Files dialog box (Figure 1-8) appears.

Figure 1-7. Windows 98 – Opening .SYS File

Figure 1-8. Windows 98 – Copying .SYS File
11. Click OK.
   The driver installation is now complete, as shown in Figure 1-9.

![Add New Hardware Wizard](image)

Figure 1-9. Windows 98 – Completing Software Installation

12. Click Finish to exit the wizard.

13. Verify the installation by following the instructions in “Verifying Driver Installation” on page 1-14.

**Windows 2000 USB Driver**

VisualDSP++ 3.5 installation software pre-installs the necessary drivers for the selected EZ-KIT Lite. The install also upgrades an older driver if such is detected in the system.

⚠️ Prior to running the VisualDSP++ 3.5 installer, ensure there are no other Hardware Wizard windows running in the background. If there are any wizard windows running, close them before starting the installer.
Installation Tasks

To install the USB driver:

1. If VisualDSP++ 3.5 is already installed on your system, go to step 2.
   Otherwise, run VisualDSP++ 3.5 installation. Refer to the VisualDSP++ 3.5 Installation Quick Reference Card for a detailed installation description.
   When installing VisualDSP++ 3.5 on Windows 2000, make sure the appropriate EZ-KIT Lite component is selected for the installation.

2. Connect the EZ-KIT Lite device to your PC's USB port.
   Windows 2000 automatically detects an EZ-KIT device and automatically installs the appropriate driver for the selected device (see step 1).

3. Verify the installation by following the instructions in “Verifying Driver Installation” on page 1-14.

Windows XP USB Driver

VisualDSP++ 3.5 installation software pre-installs the necessary drivers for the selected EZ-KIT Lite. The install also upgrades an older driver if such is detected in the system.

Prior to running the VisualDSP++ 3.5 installer, ensure there are no other Hardware Wizard windows running in the background. If there are any wizard windows running, close them before starting the installer.

To install the USB driver:

1. If VisualDSP++ 3.5 is already installed on your system, go to step 2.
   Otherwise, run VisualDSP++ 3.5 installation. Refer to the VisualDSP++ 3.5 Installation Quick Reference Card for a detailed
Getting Started

installation description.
When installing VisualDSP++ 3.5 on Windows XP, make sure the appropriate EZ-KIT Lite component is selected for the installation.

2. Connect the EZ-KIT Lite device to your PC’s USB port.
By connecting the device to the USB port you activate the Windows XP Found New Hardware Wizard, shown in Figure 1-10.

![Figure 1-10. Windows XP – Found New Hardware Wizard](image)

3. Select Install the software automatically (Recommended) and click Next.
Installation Tasks

When Windows XP completes the driver installation for the selected device (see step 1), a window shown in Figure 1-11 appears on the screen.

![Image of driver installation](image)

Figure 1-11. Windows XP – Completing Driver Installation

4. Verify the installation by following the instructions in “Verifying Driver Installation”.

Verifying Driver Installation

Before launching the EZ-KIT Lite evaluation system, verify that the USB driver software is installed properly:

1. Ensure that the USB cable connects to the evaluation board and the PC.
2. Press and release the RESET button (SW8) on the evaluation board.
3. Verify that the red DSP RESET LED (LED8) blinks once and then blinks again in 15 seconds.
4. After the DSP RESET LED (LED8) blinks for the second time, verify that the yellow USB monitor LED (LED10) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

5. Verify that the USB driver software is installed properly. Open Windows Device Manager and verify that ADSP-21161N EZ-KIT Lite shows under ADI Development Tools with no exclamation point, as in Figure 1-12.

Figure 1-12. Device Manager Window

⚠️ If using an EZ-KIT Lite on Windows 98, disconnect the USB cable from the board before booting the PC. When Windows 98 is booted and you are logged on, re-connect the USB cable to the board. The operation should continue normally from this point.
Installation Tasks

Starting VisualDSP++

To set up a session in VisualDSP++:

1. Verify that the yellow USB monitor LED (LED10, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

2. Hold down the Control (CTRL) key.


   If you are running VisualDSP++ for the first time, go to step 4. If you already have existing sessions, the Session List dialog box appears on the screen.

4. Click New Session.

5. The New Session dialog box, shown in Figure 1-13, appears on the screen.

Figure 1-13. New Session Dialog Box

6. In Debug Target, choose EZ-KIT Lite (ADSP-21161N).
7. In Processor, choose the appropriate processor, ADSP-21161N.

8. Type a new target name in Session Name or accept the default name.

9. Click OK to return to the Session List. Highlight the new session and click Activate.
Installation Tasks
2 USING EZ-KIT LITE

This chapter provides specific information to assist you with developing programs for the ADSP-21161N EZ-KIT Lite evaluation system. This information appears in the following sections.

- “EZ-KIT Lite License Restrictions” on page 2-2
  Describes the restrictions of the VisualDSP++ license shipped with the EZ-KIT Lite.

- “Memory Map” on page 2-2
  Defines the ADSP-21161N EZ-KIT Lite’s memory map.

- “Using SDRAM Memory” on page 2-3
  Defines the register values to configure the on-board SDRAM.

- “Using FLAG Pins” on page 2-5
  Describes the board’s FLAG pins.

- “Using Interrupt Pins” on page 2-6
  Describes the board’s interrupt pins.

- “Using Audio Interface” on page 2-6
  Describes the board’s audio interface.

- “Example Programs” on page 2-8
  Provides information about example programs included in the ADSP-21161N EZ-KIT Lite.

- “Using Flash Programmer Utility” on page 2-8
  Provides information on the Flash Programmer utility included with the EZ-KIT Lite software.
EZ-KIT Lite License Restrictions

- “Using EZ-KIT Lite VisualDSP++ Interface” on page 2-9
  Describes the trace, performance monitoring, boot loading, context switching, and target options facilities of the EZ-KIT Lite system.

For detailed information on how to program the ADSP-21161N SHARC processor, refer to the documents referenced in “Related Documents”.

EZ-KIT Lite License Restrictions

The license shipped with the EZ-KIT Lite imposes the following restrictions.

- The size of a user program’s code is limited to 5K words (1/4) of the ADSP-21161N processor’s program memory space.
- No connections to simulator or emulator sessions are allowed.
- The EZ-KIT Lite hardware must be connected and powered up in order to use VisualDSP++ with a kit license.

Memory Map

The ADSP-21161N processors includes 1 Mbit of internal SRAM for program storage or data storage. The configuration of internal SRAM is detailed in the ADSP-21161 SHARC Processor Hardware Reference.

The ADSP-21161N EZ-KIT Lite board contains 512K x 8-bits of external Flash memory. The Flash memory is connected to the processors’s ~MS1 and ~BMS memory select pins. The Flash memory can be accessed in either the boot memory space or the external memory space. The external memory interface is also connected to 1M x 48-bit SDRAM memory. The Flash memory is connected to the ~MS0 pin.
Using SDRAM Memory

To use the SDRAM memory, set the two SDRAM control registers to the values shown in Listing 2-1.

Listing 2-1. ADSP-21161N EZ-KIT Lite – SDRAM Settings

/* SDRAM Controller Setup for the ADSP-21161N EZ-KIT Lite */
/* Assumes SDRAM part# Micron MT48LC16M16A1-7SE (1Mx16-bit, 2 banks) */
/* Default Factory Hardware settings (rev2.3) */
/* LK_CFG[1:0]= 10,~CLDBL=1 */
/* CLKIN=25 MHz, => CCLK=100 MHz */
/* 3 SDRAMs by 16 bits wide total = 3x(1Mx16-bit) = 1M x 48-bit */

Table 2-1. EZ-KIT Lite Evaluation Board Memory Map

<table>
<thead>
<tr>
<th>Start Address</th>
<th>End Address</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000 0000</td>
<td>0x0001 FFFF</td>
<td>IOP Registers (Internal)</td>
</tr>
<tr>
<td>0x0002 0000</td>
<td>0x0002 1FFF</td>
<td>Block 0 Long Word Addressing</td>
</tr>
<tr>
<td>0x0002 8000</td>
<td>0x0002 9FFF</td>
<td>Block 1 Long Word Addressing</td>
</tr>
<tr>
<td>0x0004 0000</td>
<td>0x0004 3FFF</td>
<td>Block 0 Normal Word Addressing</td>
</tr>
<tr>
<td>0x0005 0000</td>
<td>0x0005 3FFF</td>
<td>Block 1 Normal Word Addressing</td>
</tr>
<tr>
<td>0x0008 0000</td>
<td>0x0008 7FFF</td>
<td>Block 0 Short Word Addressing</td>
</tr>
<tr>
<td>0x000A 0000</td>
<td>0x000A 7FFF</td>
<td>Block 1 Short Word Addressing</td>
</tr>
<tr>
<td>0x0010 0000</td>
<td>0x001F FFFF</td>
<td>Multi-processor Memory Space</td>
</tr>
<tr>
<td>0x0020 0000</td>
<td>0x002F FFFF</td>
<td>External Memory Space Bank 0 (SDRAM)</td>
</tr>
<tr>
<td>0x0400 0000</td>
<td>0x047F FFFF</td>
<td>External Memory Space Bank 1 (FLASH)</td>
</tr>
<tr>
<td>0x0800 0000</td>
<td>0x08FF FFFF</td>
<td>External Memory Space Bank 2</td>
</tr>
<tr>
<td>0x0C00 0000</td>
<td>0x0FFF FFFF</td>
<td>External Memory Space Bank 3</td>
</tr>
</tbody>
</table>

Using EZ-KIT Lite
Using SDRAM Memory

/* Mapped to MS0 addresses 0x00200000-0x002fffff */
/* Estimated SDCLK 50 MHz => SDCKR=0 */
/* Settings must be double counted for SDCKR-bit=0, except CAS Latency */
/* 50 MHz min @ CL=2 -> SDCL=2 [CAS Latency] */
/* tRAS=42ns min -> SDTRAS=5*2=10 [precharge delay] */
/* tRP=21ns min -> SDTRP=3*2=6 [active delay] */
/* tRCD=20ns min -> SDTRCD=2*2=4 [CAS-to-RAS delay] */
/* tREF=64ms/4K rows -> */
/* -> SDRDIV= (100MHz*64ms/4096) - 13 = 1549 = 0x60D cycles */
/* Note: If you change any clock, you have to change all settings for best performance */

init_21161_SDRAM_controller:
ustat1=dm(WAIT);
bit clr ustat1 0x000FFFFF; /* clear MS0 wait state count */
dm(WAIT)=ustat1;
ustat1=0x60D; /* refresh rate */
dm(SDRDIV)=ustat1;
ustat1=0x040146A2; /* mask in SDRAM settings */
dm(SDCTL)=ustat1;
init_21161_SDRAM_controller.end:
rts;

The SDRAM registers are configured automatically through the debugger. Checking the Manual External Mem configuration box in the Target Options dialog box, as shown in Figure 2-1 on page 2-10, disables the automatic setting.
Using FLAG Pins

The ADSP-21161N holds 12 asynchronous FLAG IO pins. Ten of these pins (FLAG0–9) are available for interaction with the running program.

After the processor is reset, the FLAGs are configured as inputs. The directions of the FLAGs are configured though the MODE2 register and are set and read though the FLAG registers. The FLAG registers are summarized in Table 2-2. For more information on FLAGs, refer to the ADSP-21161 SHARC Processor Hardware Reference.

Table 2-2. FLAG Pin Summary

<table>
<thead>
<tr>
<th>FLAG(^1)</th>
<th>Connects To</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLAG0</td>
<td>SW1/AD1836_SPI_SELECT</td>
<td>FLAG0 connects to push button SW1 for user input and to the SPI select pin on the AD1836 audio codec.</td>
</tr>
<tr>
<td>FLAG1</td>
<td>SW2/AD1852_SPI_SELECT</td>
<td>FLAG1 connects to push button SW2 for user input and to the SPI select pin on the AD1852 auxiliary DAC.</td>
</tr>
<tr>
<td>FLAG2</td>
<td>SW3</td>
<td>FLAG2 connects to push button SW3 for user input.</td>
</tr>
<tr>
<td>FLAG3</td>
<td>SW4</td>
<td>FLAG3 connects to push button SW4 for user input.</td>
</tr>
<tr>
<td>FLAG4–FLAG9</td>
<td>LED2–LED7</td>
<td>FLAG4–9 connect to LEDs on the EZ-KIT Lite board and are for user output.</td>
</tr>
<tr>
<td>FLAG10 and FLAG11</td>
<td>Not connected</td>
<td>Not available</td>
</tr>
</tbody>
</table>

\(^1\) FLAG0–FLAG3 are available on connector P10.
Using Interrupt Pins

The ADSP-21161N holds three interrupt pins (IRQ0–2) that let you interact with the running program. Each of the three external interrupts is directly accessible through the push button switches SW5–SW7 on the EZ-KIT Lite board. Interrupt pins are summarized in Table 2-3. For more information, refer to the ADSP-21161 SHARC Processor Hardware Reference.

Table 2-3. Interrupt Pin Summary

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Connects To</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0</td>
<td>SW5</td>
<td>IRQ0-2 connect to the push buttons and supply feedback for program execution. For instance, you can write your code to trigger a FLAG when a routine is complete.</td>
</tr>
<tr>
<td>IRQ1</td>
<td>SW6</td>
<td></td>
</tr>
<tr>
<td>IRQ2</td>
<td>SW7</td>
<td></td>
</tr>
</tbody>
</table>

1. IRQ0-2 are available on connector P10.

Using Audio Interface

The audio interface consists of the AD1836 audio codec, the AD1852 auxiliary DAC and the CS8414 SPDIF receiver. SPORT0 and SPORT2 connect to the audio devices and provide 3 channels of stereo input (1 channel digital, 2 channels analog) and 4 channels of stereo output.

Analog audio input is facilitated by a 3.5 mm stereo jack (P7) and four RCA mono jacks (P6). One of the AD1836 stereo input channels is dedicated to two of the RCA mono jacks. The other stereo input channels can either be supplied by the 3.5 mm stereo jack or the other two RCA mono jacks. JP11 determines which jack is used for audio input. Digital audio input can be provided on either a single RCA mono jack (P5) or an optical input connector (P4). JP2 determines the source. Three of the stereo out-
Using EZ-KIT Lite

Put channels come from the AD1836, while the final channel is from the AD1852. See “Audio Connectors (P4–8, P17)” on page 3-18 for more information about the connectors.

The AD1836 multi-channel codec features six digital-to-analog converters (DACs) and four analog-to-digital converters (ADCs) and supports multiple digital stereo channels with 24-bit conversion resolution and a 96 kHz sample rate. The AD1836 features a 108 dB dynamic range for each of its six DACs and a 104 dB dynamic range for its four ADCs. The AD1836 is configured through its SPI port. The ADSP-21161N processor is capable of accessing the AD1836’s SPI port through the SPI port as well as through SPORT1. For more information, see “AD1836 Control Selection Jumper (JP23)” on page 3-12.

The AD1852 is a complete 18/20/24-bit single-chip stereo digital audio playback system. It is comprised of a multibit sigma-delta modulator, digital interpolation filters, and analog output drive circuitry. Other features include an on-chip stereo attenuator and mute, programmed through an SPI-compatible serial control port. The AD1852 is fully compatible with all known DVD formats, including 192 kHz and 96 kHz sample frequencies and 24 bits. It also is backwards compatible by supporting 50/15µs digital de-emphasis intended for “redbook” Compact Discs, as well as de-emphasis at 32 kHz and 48 kHz sample rate.

The CS8414 is a monolithic CMOS device that receives and decodes audio data up to 96 kHz, according to the AES/EBU, IEC958, S/PDIF, and EIAJ CP340/1201 interface standards. The CS8414 receives data from a transmission line, recovers the clock and synchronization signals, and de-multiplexes the audio and digital data. The CS8414 is setup to operate in I2S compatible mode.

The Microphone and Line-In jacks connect to the left and right ADC1 channel on the AD1836, depending on the setting of jumpers. See “MIC Gain Selection Jumpers (JP9–10)” on page 3-8 and “ADC1 Input Selection Jumper (JP11)” on page 3-9 for more information. Two RCA jacks
Example Programs

connect to ADC2 on the AD1836. This input is configured though the input mode selection jumpers, See “ADC2 Input Mode Selection Jumpers (JP7–8)” on page 3-8 for more information.

The Line-Out jacks connect to the left and right DAC outputs of the AD1836 and AD1852.

The CS8414 includes an error flag (VERF) to indicate that the audio output may not be valid. This signal connects to a LED (LED9) on the board. This signal may also be used by interpolation filters to provide error correction.

Example Programs

Example programs are provided with the ADSP-21161N EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in \VisualDSP 3.5 32-Bit\AD18xx\Examples. Please refer to the readme file provided with each example for more information.

Using Flash Programmer Utility

The ADSP-21161N EZ-KIT Lite evaluation system includes a Flash Programmer utility. The utility allows you to program the Flash memory on the EZ-KIT Lite. The Flash Programmer is installed with VisualDSP++. Once the utility is installed, it is accessible from the Tools pull-down menu.

Using EZ-KIT Lite VisualDSP++ Interface

This section provides information about the following parts of the VisualDSP++ graphical user interface:

- “Boot Load” on page 2-9
- “Target Options” on page 2-9
- “Core Hang Conditions” on page 2-11
- “Hardware Breakpoints” on page 2-12
- “Restricted Software Breakpoints” on page 2-19

Boot Load

Choosing Boot Load from the Settings menu runs the processor and performs a hard reset on the board. This command saves you from having to shut down VisualDSP++, reset the EZ-KIT Lite board, and bring up VisualDSP++ again when you want to perform a hard reset.

Use this feature when loading debug boot code from an external part or when you want to put the device into a known state.

Target Options

Choosing Target Options from the Settings menu opens the Target Options dialog box (Figure 2-1). Use target options to control certain aspects of the processor on the ADSP-21161N EZ-KIT Lite evaluation system.
Using EZ-KIT Lite VisualDSP++ Interface

While Target is Halted and On Emulator Exit Options

This target option controls the processor’s behavior when VisualDSP++ relinquishes DSP control (for example, when exiting VisualDSP++). The options are detailed in Table 2-4 and Table 2-5.

Table 2-4. While Target is Halted Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stop I/O DMA</td>
<td>Stops IO DMAs in emulator space. This option disables DMA requests when the emulator has control of the DSP. Data in the EP, LINK, or SPORT DMA buffers are held there unless the internal DMA request was already granted. This option holds off incoming data and ceases outgoing data. Because SPORT-receive data cannot be held off, it is lost, and the overrun bit is set. The direct write buffer (internal memory write) and the EP pad buffer are allowed to flush any remaining data to internal memory.</td>
</tr>
</tbody>
</table>

Other Options

Table 2-6 describes other available target options.
Using EZ-KIT Lite

Core Hang Conditions

Certain peripheral devices, such as host ports, DMA, and link ports, can hold off the execution of processor instructions. This is known as a hung condition and commonly occurs when reading from an empty port or writing to a full port. If an attempt to halt the processor is made during one of these conditions, the EZ-KIT Lite may encounter a core hang.

Table 2-5. On Emulator Exit Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>On Emulator Exit</td>
<td>Determines the state the DSP is left in when the emulator relinquishes control of the DSP:</td>
</tr>
<tr>
<td></td>
<td>Reset DSP and Run causes the DSP to reset and begin execution from its reset vector location.</td>
</tr>
<tr>
<td></td>
<td>Run from current PC causes the DSP to begin running from its current location.</td>
</tr>
</tbody>
</table>

Table 2-6. Other Target Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset before loading executable</td>
<td>Resets registers before loading a DSP executable. Clear this option when DSP registers must not change to their reset values when a file load occurs.</td>
</tr>
<tr>
<td>Verify all writes to target memory</td>
<td>Validates all memory writes to the DSP. After each write, a read is performed and the values are checked for a matching condition. Enable this option during initial program development to locate and fix initial build problems (such as attempting to load data into non-existent memory). Clear this option to increase performance while loading executable files since VisualDSP++ does not perform the extra reads that are required to verify each write.</td>
</tr>
<tr>
<td>Reset cycle counters on run</td>
<td>Resets the cycle count registers to zero before a Run command is issued. Select this option to count the number of cycles executed between breakpoints in a program.</td>
</tr>
<tr>
<td>Manual Extern Mem configuration</td>
<td>Disables the automatic configuration of the SDRAM registers (done through the debugger).</td>
</tr>
</tbody>
</table>

ADSP-21161N EZ-KIT Lite Evaluation System Manual 2-11
Using EZ-KIT Lite VisualDSP++ Interface

Normally, a core hang can be cleared by the board using a special clear/abort bit. However, there are cases in which it is desirable or possible not to clear the core hang. Sometimes it is desirable to wait for the core hang to clear itself, such as when waiting for a host processor to read or write data. In other cases, it is not possible to clear the core hang, and a DSP reset must occur to continue the debugging session.

Table 2-7 describes the EZ-KIT Lite’s core hang operations.

Table 2-7. Core Hang Operations

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abort</td>
<td>Abort the hung operation. This causes the offending instruction to be aborted in the pipeline.</td>
</tr>
<tr>
<td>Retry</td>
<td>Allows you to remedy the hung operation. For example, if a host processor is holding off the DSP, you can cause the host to clear the hung condition.</td>
</tr>
<tr>
<td>Ignore</td>
<td>Performs a software reset on the target board.</td>
</tr>
<tr>
<td>Clear</td>
<td>Aborts the hung operation. This causes the offending instruction to be aborted in the pipeline.</td>
</tr>
<tr>
<td>Acknowledge</td>
<td>Allows you to remedy the hung operation. For example, if a host processor is holding off the DSP, you can cause the host to clear the hung condition.</td>
</tr>
<tr>
<td>Reset</td>
<td>Performs a software reset on the target board.</td>
</tr>
</tbody>
</table>

**Hardware Breakpoints**

Hardware breakpoints work similarly to watchpoints. Set hardware breakpoints on:

- Data transfers within a user-defined memory range
- Instructions
- Register reads and writes
To enable hardware breakpoints for ADSP-21161N DSPs:

1. From the Settings menu, choose Hardware Breakpoints.

2. The Hardware Breakpoints dialog box appears. The dialog box has three tabbed pages: Data, Instruction, and Other (Figure 2-2).

![Hardware Breakpoints Dialog Box](image)

Figure 2-2. Hardware Breakpoints Dialog Box

Refer to the following sections for information about hardware breakpoints.

- “Common Hardware Breakpoint Attributes” on page 2-13
- “Global Hardware Breakpoint Options” on page 2-13
- “Data Hardware Breakpoints” on page 2-15
- “Instruction Hardware Breakpoints” on page 2-16
- “Other Breakpoints” on page 2-17
- “Tips and Tricks Using Hardware Breakpoints” on page 2-18

### Common Hardware Breakpoint Attributes

Each of the three tabs in the Hardware Breakpoints dialog box has common attributes. The common attributes are described in Table 2-8.

### Global Hardware Breakpoint Options

For ADSP-21161N DSPs, the options listed in Table 2-9 apply to all hardware breakpoints, regardless of their type.
Using EZ-KIT Lite VisualDSP++ Interface

Table 2-8. Common Hardware Breakpoint Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable</td>
<td>Enables each individual breakpoint.</td>
</tr>
<tr>
<td>Start Address</td>
<td>Specify inclusive start and end addresses.</td>
</tr>
<tr>
<td>End Address</td>
<td>Each pair of addresses sets up an address range for the particular breakpoint.</td>
</tr>
<tr>
<td>Exclusive</td>
<td>Enables breaks outside of the specified (inclusive) address range.</td>
</tr>
<tr>
<td>Mode</td>
<td>Data page and Other page only. This option specifies the modes that trigger hardware breakpoints. The available choices are: Disabled—disables the breakpoint On Write—triggers the breakpoint on any write operation to the specified address range On Read—triggers the breakpoint on any read operation from the specified address range Any Access—triggers the breakpoint on any read or write access to the specified address range.</td>
</tr>
</tbody>
</table>

Table 2-9. Global Hardware Breakpoint Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Skip N Breakpoint</td>
<td>Specifies the number of breakpoint events to be ignored before stopping the processor. Each time a hardware breakpoint condition occurs, the count decrements. When the count reaches zero (0), the DSP processes the hardware break. Use this option to count the number of times a break operation occurs. Breakpoints within the group are ORed together to create this condition.</td>
</tr>
<tr>
<td>Events</td>
<td></td>
</tr>
<tr>
<td>Restore Skip Count</td>
<td>Enables skip-count decrement as specified in Skip N Breakpoint Events.</td>
</tr>
<tr>
<td>on Break</td>
<td></td>
</tr>
<tr>
<td>Restore Skip Count</td>
<td>Causes the emulator to restore the Skip Count to the value at program RESTART. Otherwise, the Skip Count remains at its current value.</td>
</tr>
<tr>
<td>on Break</td>
<td></td>
</tr>
<tr>
<td>AND All Breakpoints</td>
<td>ANDs the interrupts to form the composite interrupt. Normally, the group interrupts are ORed to create a composite interrupt.</td>
</tr>
</tbody>
</table>
Data Hardware Breakpoints

For ADSP-21161N DSPs, use data breakpoints to break on accesses to internal memory, IOP registers, the external port (EP), and multiprocessor memory space (MMS).

The following actions trigger a data breakpoint:

- DAG1 access
- DM() modifier access

The two data breakpoints are ORed to generate a single data breakpoint condition.

The **Data** page of the **Hardware Breakpoints** dialog box, which permits the specification of two data breakpoints, is shown in Figure 2-3.

Figure 2-3. Data Page of Hardware Breakpoints Dialog Box
Using EZ-KIT Lite VisualDSP++ Interface

Instruction Hardware Breakpoints

For ADSP-21161N DSPs, an instruction breakpoint occurs when an instruction is executed within one of the specified address ranges. The four individual instruction breakpoints are ORed to generate a single instruction breakpoint condition.

Shown below is the Instruction page of the Hardware Breakpoints dialog box, which permits the specification of four individual instruction breakpoints.

![Figure 2-4. Instruction Page of Hardware Breakpoints Dialog Box](image)

Other Breakpoints

For SHARC DSPs, the Other page of the Data Breakpoints dialog box permits the specification of hardware breakpoints triggered by access to PM data, IO, or the external port.

Table 2-10. Other Hardware Breakpoint Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PM DataEvents</td>
<td>Enables PM data breakpoints. PM data breakpoints are similar to data breakpoints (Data page), except accesses that trigger a PM breakpoint are made by DAG2 or the PM() modifier. Like data breakpoints, PM data breakpoints cause a break on accesses to internal memory, IOP registers, the external port (EP), and multiprocessor memory space (MMS).</td>
</tr>
<tr>
<td>I/O</td>
<td>Enables IO breakpoints. IO breakpoints are triggered by accesses made on the IO Address Bus. Use an IO breakpoint to break on accesses made during DMA transfers, MMS accesses, and Host accesses.</td>
</tr>
</tbody>
</table>
Using EZ-KIT Lite VisualDSP++ Interface

Table 2-10. Other Hardware Breakpoint Options (Cont'd)

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Port</td>
<td>Enables external port breakpoints. External port (EP) breakpoints are triggered by accesses made through the External Port. Use an EP breakpoint to break on accesses made to any external device that may be tied to the EP, such as external memory.</td>
</tr>
<tr>
<td>AND All Breakpoints</td>
<td>ANDs the interrupts to form the composite interrupt. Normally, the group interrupts are ORed to create a composite interrupt.</td>
</tr>
</tbody>
</table>

Tips and Tricks Using Hardware Breakpoints

Be aware of the following tips and tricks when using hardware breakpoints on ADSP-21161N processors.

Latency

For SHARC processors, hardware breakpoints do not assert until two (2) instruction cycles after the actual break condition occurs.

Restrictions

When using hardware breakpoints, do not place breaks at any address where a JUMP, CALL, or IDLE instruction would be illegal.

Do not place breaks in the last few instructions of a DO LOOP or in the delay slots of a delayed branch. For more information on these illegal locations, refer to your DSP’s Hardware Reference.

Setting a Breakpoint on a Single Address

To set a breakpoint on a single address, set the Start Address equal to the End Address.
Using EZ-KIT Lite

Restricted Software Breakpoints

The EZ-KIT Lite development system restricts breakpoint placement when certain conditions are met. That is, under some conditions, breakpoints cannot be placed effectively. Such conditions depend on bus architecture, pipeline depth, and ordering of the EZ-KIT Lite and its target processor.
Using EZ-KIT Lite VisualDSP++ Interface
3 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-21161N EZ-KIT Lite board. The following topics are covered.

- “System Architecture” on page 3-2
  Describes the configuration of the ADSP-21161N EZ-KIT Lite board and explains how the board components interface with the processor.

- “Jumper Settings” on page 3-5
  Shows the location and describes the function of the on-board jumpers.

- “LEDs and Push Buttons” on page 3-13
  Shows the location and describes the function of the LEDs and push buttons.

- “Connectors” on page 3-16
  Shows the location and gives the part number for the on-board connectors. Also, the manufacturer and part number information is given for the mating parts.

- “Specifications” on page 3-21
  Provides the board’s measurements and power supply specifications.
System Architecture

This section describes the processor’s configuration on the EZ-KIT Lite board.

![System Architecture Block Diagram](image)

Figure 3-1. System Architecture Block Diagram

The ADSP-21161N processor’s core voltage is 1.8V, and the external interface voltage is 3.3V.

A 25 MHz through-hole oscillator supplies the input clock to the processor. Footprints are provided on the board for a surface-mount oscillator and a through-hole crystal for alternate user-installed clocks. The speed at
which the core operates is determined by the location of the clock mode jumper (JP21) as described on page 3-11. By default, the processor core runs at 100 MHz.

**External Port**

The External Port (EP) of the processor connects to a 512K x 8-bit Flash memory. The Flash memory connects to the boot memory select (\~BMS) pin and the memory select 1 (\~MS1) pin. The connection allows the Flash memory to be used to boot the processor as well as to store information during normal operation.

The external memory interface also connects to 1M x 48-bit SDRAM memory. The SDRAM memory connects to the memory select 0 (\~MS0) pin. Refer to “SDRAM Disable Jumper (JP1)” on page 3-5 for information on how to configure the width of the SDRAM. Refer to “Using SDRAM Memory” on page 2-3 for a summary of the processor’s memory map.

Some of the address, data, and control signals are available externally via two off-board connectors. The EP connectors’ pinout (P9 and P10) can be found in Appendix B, “Schematics”.

**Host Processor Interface (HPI)**

The Host Port Interface (HPI) signals are brought to an unpopulated off-board connector (P9). This allows the HPI to interface with a user application. The pinout of the host port connector can be found in Appendix B, “Schematics”.

**SPORT Audio Interface**

SPORT0 and SPORT2 are connected to the AD1836 codec (U10). A 3.5 mm stereo jack and four RCA mono jacks facilitate an audio input, while a 3.5 mm stereo jack and eight RCA mono jacks facilitate an audio output.
System Architecture

The codec contains two input channels. One channel connects to a 3.5 mm stereo jack and two RCA jacks. The 3.5 mm stereo jack connects to a microphone. The two RCA jacks can connect to a LINE-OUT from an audio device. You can supply an audio input to the codec microphone input channel (MIC1) or to the LINE_IN input channel. The jumper settings of JP11 determine whether the LINE_IN channel of the codec is driven by the P6 connector or by the P7 connector.

SPI Audio Interface

The SPI port is connected to the AD1836 and AD1852. The SPI port is used for writing and reading the control registers of the audio devices.

Breadboard Area

Use the breadboard area to add external circuitry to:

- All board voltages and grounds
- Package footprints:
  - 1x SOIC16
  - 1x SOIC20
  - 4x SOT23-6
  - 1x PSOP44
  - 2x SOT23
  - 27x 0805

⚠️ Analog Devices does not support and is not responsible for the effects of additional circuitry.
JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor’s internal and external memory, as well as the special function registers, through a 14-pin header.

For a detailed description of the interface’s connectors, see EE-68 published on the Analog Devices website. For more information, see “JTAG Connector (P12)” on page 3-19. For more information about available emulators, contact Analog Devices (see “Product Information”).

Jumper Settings

This section describes the function of all the jumpers. Figure 3-2 shows the locations of all the jumpers.

SDRAM Disable Jumper (JP1)

The JP1 jumper is used to enable or disable the third SDRAM device. When the jumper is installed, the ADSP-21161N can access the SDRAM as 48-bit-wide external memory.

The upper 16 bits of data are multiplexed with the Link Ports and the external data bus; therefore, when the jumper is installed, the Link Ports are not available. To use the Link Ports, the JP1 jumper must be removed.

SPDIF Selection Jumper (JP2)

The JP2 jumper is used select the SPDIF input to the CS8414 digital audio receiver. When the jumper is configured for an optical connection, the TOSLINK optical input connector (P4) should be used. When the jumper is configured for a coax connection, the RCA input connector (P5) should be used.
MCLK Selection Jumper (JP3)

The JP3 jumper is used to select the MCLK source for the AD1836 and AD1852.
Table 3-1. SPDIFF Modes

<table>
<thead>
<tr>
<th>Jumper Location</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 and 2</td>
<td>Optical (factory default)</td>
</tr>
<tr>
<td>2 and 3</td>
<td>Coax</td>
</tr>
</tbody>
</table>

Table 3-2. MCLK Selection

<table>
<thead>
<tr>
<th>Jumper Location</th>
<th>MCLK Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 and 2</td>
<td>Audio Oscillator (12.288 MHz) (factory default)</td>
</tr>
<tr>
<td>2 and 3</td>
<td>Derived clock from SPDIF Stream</td>
</tr>
</tbody>
</table>

**FLAG0 Enable Jumper (JP4)**

In standard configuration, FLAG0 is connected to the AD1836 and used as a select for the SPI port. This jumper should be removed to use the push button switch or the signal on the expansion connector (P10). Once the jumper is removed, the SPI can no longer communicate with the AD1836.

**FLAG1 Enable Jumper (JP5)**

In standard configuration, FLAG1 is connected to the AD1852 and used as a select for the SPI port. The JP5 jumper should be removed to use the push button switch or the signal on the expansion connector (P10). Once the jumper is removed, the SPI can no longer communicate with the AD1852.

**Sample Frequency Jumper (JP6)**

The JP6 jumper is used to select the sample frequency for the AD1852 device. Table 3-3 shows the valid frequency modes.
Jumper Settings

Table 3-3. Sample Frequencies

<table>
<thead>
<tr>
<th>Jumper Location</th>
<th>Sample Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>None installed</td>
<td>Not allowed</td>
</tr>
<tr>
<td>3 and 4</td>
<td>192 kHz (2x Interpolator)</td>
</tr>
<tr>
<td>1 and 2</td>
<td>96 kHz (4x Interpolator)</td>
</tr>
<tr>
<td>1 and 2, 3 and 4</td>
<td>48 kHz (8x Interpolator)  (factory default)</td>
</tr>
</tbody>
</table>

ADC2 Input Mode Selection Jumpers (JP7–8)

The JP7 and JP8 jumpers control the input mode to ADC2 on the AD1836 (see Table 3-4). In high-performance mode, the signal is routed straight in to the ADC. In PGA mode, the signal goes through a multiplexer and a programmable gain amplifier inside of the codec.

Table 3-4. ADC Input Mode

<table>
<thead>
<tr>
<th>Jumper Location</th>
<th>Input Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 and 5, 4 and 6</td>
<td>PGA (factory default)</td>
</tr>
<tr>
<td>1 and 3, 2 and 4</td>
<td>High Performance</td>
</tr>
</tbody>
</table>

MIC Gain Selection Jumpers (JP9–10)

The JP9 and JP10 jumpers are used to select the pre-amp gain for the microphone circuit (see Table 3-5). The gain for the left and right channel should be configured the same.

Table 3-5. MIC Pre Amp Gain

<table>
<thead>
<tr>
<th>Jumper Position</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Not Installed</td>
<td>0 dB</td>
</tr>
</tbody>
</table>
ADC1 Input Selection Jumper (JP11)

The JP11 jumper is used to select the input source for ADC2. If the input source for ADC2 is LINE-IN, then the RCA connector P6 should be used. If the input source for ADC2 is a microphone, then the mini stereo plug P7 should be used. If a microphone is used, the gain of the circuit may be increased, as described in “MIC Gain Selection Jumpers (JP9–10)” on page 3-8.

When the JP11 jumpers are between pins 1 and 3 and between pins 2 and 4, the connection is to P7. When the jumpers are between pins 3 and 5 and between pins 4 and 6, the connection is to P6. The jumper settings are illustrated in Table 3-6. (The words MIC and LINE are on the board as a reference.)

Table 3-6. Audio Input Jumper Settings

<table>
<thead>
<tr>
<th>Microphone Input</th>
<th>Stereo LINE_IN (Default)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC 1 2</td>
<td>MIC 1 2</td>
</tr>
<tr>
<td>LINE</td>
<td>LINE</td>
</tr>
<tr>
<td>JP11</td>
<td>JP11</td>
</tr>
</tbody>
</table>
Jumper Settings

Processor ID Jumper (JP19)

The JP19 jumper is used to select a different ID for the processor. During typical operation of the EZ-KIT Lite board, there is only a single DSP in the system. The jumper should be set to the single processor setting. When a second processor is attached to the board though the link port, these jumpers should be changed to configure one board for processor 1 and the other board for processor 2. System configuration options are shown in Table 3-7.

Table 3-7. Processor ID Modes

<table>
<thead>
<tr>
<th>Jumper Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 and 2, 3 and 4, 5 and 6</td>
<td>Single processor (default)</td>
</tr>
<tr>
<td>3 and 4, 5 and 6</td>
<td>Processor 1</td>
</tr>
<tr>
<td>1 and 2, 5 and 6</td>
<td>Processor 2</td>
</tr>
<tr>
<td>Other</td>
<td>Invalid</td>
</tr>
</tbody>
</table>

Boot Mode Selection Jumper (JP20)

The JP20 jumper determines how the ADSP-21161N processor boots. Table 3-8 shows the jumper setting for the boot modes.

Table 3-8. Boot Mode Select Jumper (JP20) Settings

<table>
<thead>
<tr>
<th>EBOOT Pins 1 &amp; 2</th>
<th>LBOOT Pins 3 &amp; 4</th>
<th>BMS Pins 5 &amp; 6</th>
<th>Boot Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Not installed</td>
<td>Installed</td>
<td>Not installed</td>
<td>EPROM BOOT (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(output)</td>
<td></td>
</tr>
<tr>
<td>Installed</td>
<td>Installed</td>
<td>Not installed</td>
<td>Host Processor Boot</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(input)</td>
<td></td>
</tr>
<tr>
<td>Installed</td>
<td>Not installed</td>
<td>Installed</td>
<td>Serial Boot via SPI</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(input)</td>
<td></td>
</tr>
</tbody>
</table>
Clock Mode Selection Jumper (JP21)

The JP21 jumper controls the speed for the core and external port of the ADSP-21161N processor. The frequency supplied to CLKIT of the DSP may be changed by removing the 25 MHz oscillator (U24) that is shipped with the board and replacing it with a different oscillator or crystal (Y2). A clock mode and frequency should be selected so that the minimum and maximum specs of the ADSP-21161N processor are not exceeded. For more information on clock modes, see the ADSP-21161 SHARC Processor Hardware Reference. Table 3-9 shows the jumper setting for the clock modes.

Table 3-9. Clock Mode Selections

<table>
<thead>
<tr>
<th>CLKDBL Pins 1 &amp; 2</th>
<th>CLK_CFG1 Pins 3 &amp; 4</th>
<th>CLK_CFG0 Pins 5 &amp; 6</th>
<th>Core Clock Ratio</th>
<th>External Port Clock Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Not installed</td>
<td>Installed</td>
<td>Installed</td>
<td>2:1</td>
<td>1x</td>
</tr>
<tr>
<td>Not installed</td>
<td>Installed</td>
<td>Not installed</td>
<td>3:1</td>
<td>1x</td>
</tr>
<tr>
<td>Not installed</td>
<td>Not installed</td>
<td>Installed</td>
<td>4:1</td>
<td>1x (default)</td>
</tr>
<tr>
<td>Installed</td>
<td>Installed</td>
<td>Installed</td>
<td>4:1</td>
<td>2x</td>
</tr>
<tr>
<td>Installed</td>
<td>Not installed</td>
<td>Installed</td>
<td>6:1</td>
<td>2x</td>
</tr>
<tr>
<td>Installed</td>
<td>Not installed</td>
<td>Installed</td>
<td>8:1</td>
<td>2x</td>
</tr>
</tbody>
</table>
Jumper Settings

~BMS Enable Jumper (JP22)

The JP22 jumper is used to control the routing of the Boot Memory Select (~BMS) signal. When the jumper is installed, the ~BMS signal is routed to the Flash memory interface and can be used for reading, writing, and booting. The jumper should be installed when using EPROM boot mode. The jumper should be removed when using the serial boot or no-boot mode. If the jumper remains “ON” in serial boot or no-boot modes, the ~BMS signal is grounded, and the flash memory is selected.

AD1836 Control Selection Jumper (JP23)

The AD1836 control registers are programmed through an SPI port. The SPI port can be configured to be connected to the processor’s SPI port or SPORT1. When the jumper is installed at JP23, the AD1836 SPI port is connected to SPORT1 of the processor. When the jumper is removed, the AD1836 SPI port connects to the processor’s SPI port. By default, the jumper is installed.

SW1 Enable Jumper (JP26)

The SW1 push button is attached though a driver to FLAG0 of the processor. To disconnect the driver from FLAG0 (for example, to use FLAG1 as an output), remove JP26.

SW2 Enable Jumper (JP27)

The SW2 push button is attached though a driver to FLAG1 of the processor. To disconnect the driver from (for example, to use FLAG1 as an output), remove JP27.
LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 3-3 shows the locations of the LEDs and push buttons.

Figure 3-3. LED and Push Button Locations
LEDs and Push Buttons

Reset LEDs (LED1 and LED8)

When LED1 is lit, the master reset of all the major ICs is active.

When LED8 is lit, the ADSP-21161N processor (U1) is being reset. The USB interface resets the processor during USB communication initialization.

FLAG LEDs (LED2–7)

The FLAG LEDs connect to the processor’s flag pins (FLAG4–9). The LEDs are active HIGH and are lit by an output of “1” from the processor. Refer to “LEDs and Push Buttons” on page 3-13 for more information on how to use the programmable flags to program the DSP. Table 3-10 shows the FLAG signals and the corresponding LEDs.

Table 3-10. FLAG LEDs

<table>
<thead>
<tr>
<th>FLAG Pin</th>
<th>LED Reference Designator</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLAG4</td>
<td>LED7</td>
</tr>
<tr>
<td>FLAG5</td>
<td>LED6</td>
</tr>
<tr>
<td>FLAG6</td>
<td>LED5</td>
</tr>
<tr>
<td>FLAG7</td>
<td>LED4</td>
</tr>
<tr>
<td>FLAG8</td>
<td>LED3</td>
</tr>
<tr>
<td>FLAG9</td>
<td>LED2</td>
</tr>
</tbody>
</table>

VERF LED (LED9)

The VERF LED indicates that there is a possible error in the audio stream of the CS8414 digital receiver. The error may occur when digital audio cables disconnect from the optical or coaxial SPDIF connectors.
USB Monitor LED (LED10)

The USB monitor LED (LED10) indicates that USB communication has been initialized successfully, and you may connect to the processor using a VisualDSP++ EZ-KIT Lite session. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver (see “Installing EZ-KIT Lite USB Driver” on page 1-6).

Power LED (LED11)

When LED11 is lit (green), it indicates that power is being properly supplied to the board.

Programmable FLAG Push Buttons (SW1–4)

Four push buttons (SW1–4) are provided for general-purpose user input. The push buttons connect to the processor’s FLAG pins. The push buttons are active “HIGH” and, when pressed, send a High (1) to the processor. Refer to “Using FLAG Pins” on page 2-5 for more information. The push button reference designators and corresponding FLAGs are summarized in Table 3-11.

Table 3-11. FLAG Switches

<table>
<thead>
<tr>
<th>FLAG Pin</th>
<th>Push Button Reference Designator</th>
<th>FLAG Pin</th>
<th>Push Button Reference Designator</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLAG0</td>
<td>SW1</td>
<td>FLAG2</td>
<td>SW3</td>
</tr>
<tr>
<td>FLAG1</td>
<td>SW2</td>
<td>FLAG3</td>
<td>SW4</td>
</tr>
</tbody>
</table>

Interrupt Push Buttons (SW5–7)

Three push buttons are provided for general-purpose user interrupts. SW5–SW7 connect to the processor's programmable FLAG pins. The push buttons are active “HIGH” and, when pressed, send a High (1) to the
Connectors

The ADSP-21161N EZ-KIT Lite evaluation system manual contains information about the processor. Refer to “Using FLAG Pins” on page 2-5 for more information. The push button reference designators and corresponding interrupt signals are summarized in Table 3-12.

Table 3-12. Interrupt Switches

<table>
<thead>
<tr>
<th>Interrupt Signal</th>
<th>Push Button Reference Designator</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0</td>
<td>SW5</td>
</tr>
<tr>
<td>IRQ1</td>
<td>SW6</td>
</tr>
<tr>
<td>IRQ2</td>
<td>SW7</td>
</tr>
</tbody>
</table>

**Board Reset Push Button (SW8)**

The RESET push button (SW8) resets all of the ICs on the board. During reset, the USB interface is automatically reinitialized.

⚠️ Pressing the RESET push button (SW8) while VisualDSP++ is running disrupts communication and causes errors in the current debug session. VisualDSP++ must be closed and re-opened.

Connectors

This section describes the connector functionality and provides information about mating connectors. Figure 3-4 shows the connector locations.

**USB Connector (P2)**

The USB connector (P2) is a standard Type B USB receptacle.
Figure 3-4. Connector Locations

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type B USB receptacle</td>
<td>Mill-Max</td>
<td>897-30-004-90-000</td>
</tr>
<tr>
<td></td>
<td>Digi-Key</td>
<td>ED90003-ND</td>
</tr>
<tr>
<td><strong>Mating Connector</strong></td>
<td><strong>provided with the EZ-KIT Lite</strong></td>
<td></td>
</tr>
<tr>
<td>USB cable</td>
<td>Assmann</td>
<td>AK672-5</td>
</tr>
<tr>
<td></td>
<td>Digi-Key</td>
<td>AK672-5ND</td>
</tr>
</tbody>
</table>
Connectors

Audio Connectors (P4–8, P17)

There are two 3.5 mm stereo audio jacks, 13 RCA jacks, and one optical connector.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5 mm stereo jack (P7 and P17)</td>
<td>Shogyo</td>
<td>SJ-0359AM-5</td>
</tr>
<tr>
<td>RCA Jacks (P6)</td>
<td>SWITCHCRAFT</td>
<td>PJRAS2X2S01</td>
</tr>
<tr>
<td>RCA Jacks (P8)</td>
<td>SWITCHCRAFT</td>
<td>PJRAS4X2U01</td>
</tr>
<tr>
<td>‘TORX (P4)</td>
<td>TOSHIBA</td>
<td>TORX173</td>
</tr>
<tr>
<td>Coaxial (P5)</td>
<td>SWITCHCRAFT</td>
<td>PJRAN1X1U01</td>
</tr>
</tbody>
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Mating Connectors

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5mm stereo plug to 3.5mm stereo cable (P7 and P17)</td>
<td>Radio Shack</td>
<td>L12-2397A</td>
</tr>
<tr>
<td>Two channel RCA interconnect cable (P6 and P8)</td>
<td>Monster Cable</td>
<td>BH100-1M</td>
</tr>
<tr>
<td>Digital Fiber-Optic Cable (P4)</td>
<td>Monster Cable</td>
<td>ILS100-1M</td>
</tr>
<tr>
<td>Digital Coaxial Cable (P5)</td>
<td>Monster Cable</td>
<td>IDL100-1M</td>
</tr>
</tbody>
</table>

External Port Connector (P9)

A 40-pin 0.05’ spacing connector provides access to some of the processor’s External Port signals. By default, this connector is not populated.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>40-pin 0.05’ (male)</td>
<td>Samtec</td>
<td>FTSH-120-01-F-D-K</td>
</tr>
</tbody>
</table>

Mating Connector

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Female to female cable</td>
<td>Samtec</td>
<td>FFSD-20-D-5.000-01-N</td>
</tr>
</tbody>
</table>
Host Processor Interface Connector (P10)

A 20-pin 0.05' spacing connector provides access to some of the processor’s External Port signals. By default, this connector is not populated.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>20-pin 0.05' (male)</td>
<td>Samtec</td>
<td>FTSH-110-01-F-D-K</td>
</tr>
<tr>
<td>Mating Connector</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Female to female cable</td>
<td>Samtec</td>
<td>FFSD-10-D-5.000-01-N</td>
</tr>
</tbody>
</table>

JTAG Connector (P12)

The JTAG header (P12) is the connecting point for a JTAG in-circuit emulator pod. When an emulator is connected to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>14-pin IDC Header (P12)</td>
<td>Berg</td>
<td>54102-T08-07</td>
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</table>

Link Port Connectors (P13–14)

Each link port is connected to a 26-pin connector. Refer to EE-106 found on the ADI website at http://www.analog.com for more information about the link port connectors.
Connectors

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>26 position connector</td>
<td>Honda</td>
<td>RMCA-26JL-AD</td>
</tr>
</tbody>
</table>

**Mating Connector**

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cable connector</td>
<td>Honda</td>
<td>RMCA-E26F1S-A</td>
</tr>
<tr>
<td>Shroud</td>
<td>Honda</td>
<td>RMCA-E26L1A</td>
</tr>
<tr>
<td>Coaxial cable</td>
<td>Gore</td>
<td>DXN2132</td>
</tr>
</tbody>
</table>

**SPORT1 and SPORT3 Connector (P15)**

SPORT1 and SPORT3 are connected to a 20-pin connector.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 position AMPMODU system 50 receptacle</td>
<td>AMP</td>
<td>104069-1</td>
</tr>
</tbody>
</table>

**Mating Connector**

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 position AMPMODU system 20 connector</td>
<td>AMP</td>
<td>2-487937-0</td>
</tr>
<tr>
<td>20 position AMPMODU system 20 connector (w/o lock)</td>
<td>AMP</td>
<td>2-487938-0</td>
</tr>
<tr>
<td>Flexible film contacts (20 per connector)</td>
<td>AMP</td>
<td>487547-1</td>
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</tbody>
</table>

**Power Connector (P16)**

The power connector (P16) provides all of the power necessary to operate the EZ-KIT Lite board.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 mm Power Jack (P16)</td>
<td>SWITCHCRAFT</td>
<td>RAPC712</td>
</tr>
<tr>
<td></td>
<td>Digi-Key</td>
<td>SC1152-ND</td>
</tr>
</tbody>
</table>
Specifications

This section provides the requirements for powering the board.

Power Supply

The power connector supplies DC power to the EZ-KIT Lite board. Table 3-13 shows the power supply specifications.

Table 3-13. Power Supply Specifications

<table>
<thead>
<tr>
<th>Terminal</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center pin</td>
<td>+7V@2 amps</td>
</tr>
<tr>
<td>Outer Ring</td>
<td>GND</td>
</tr>
</tbody>
</table>

Board Current Measurements

The ADSP-21161N EZ-KIT Lite board provides two zero-ohm resistors that may be removed to measure current draw. Table 3-14 shows the resistor number, the voltage plane, and a description of the components on the plane.

Table 3-14. Current Measurement Resistors

<table>
<thead>
<tr>
<th>Resistor</th>
<th>Voltage Plane</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R168</td>
<td>VDDINT</td>
<td>Core Voltage of the DSP</td>
</tr>
<tr>
<td>R169</td>
<td>VDDEXT</td>
<td>IO Voltage of the DSP</td>
</tr>
</tbody>
</table>

Mating Power Supply

(shipped with EZ-KIT Lite)

5V Power Supply CUI Stack DTS070175SUDC-p6-SZ
Specifications
## BILL OF MATERIALS

<table>
<thead>
<tr>
<th>Reference</th>
<th>Quantity</th>
<th>Description</th>
<th>Reference Design</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
</table>
| 1         | 1        | M29W040 PLCC32  
FLASH-512K-X-8-3V | U5           | ST MICRO       | M29W040B120K6 |
| 2         | 2        | 74LVC14A SOIC14  
HEX-INVER-SCHMITT-T  
RIGGER | U21-22       | TI            | 74LVC14AD    |
| 3         | 3        | MT48LC1M16A1TG  
TSOP50  
1MX16-SDRAM-143MHZ | U2-4         | MICRON        | MT48LC1M16A1TG-7S |
| 4         | 1        | CS8414 SOIC28  
96KHZ-DIGITAL-AUDIO-RECVR | U8           | CIRRUS LOGIC  | CS8414      |
| 5         | 1        | CY7C64603-128 PQFP128  
USB-TX/RX MICROCONTROLLER | U6           | CYPRESS       | CY7C64603-128NC |
| 6         | 1        | MMBT4124 SOT-23  
NPN TRANSISTOR 1A | Q2           | FAIRCHILD     | MMBT4124    |
| 7         | 1        | MMBT4401 SOT-23  
NPN TRANSISTOR 200MA | Q1           | FAIRCHILD     | MMBT4401    |
| 8         | 2        | 74LVC00AD SOIC14 | U9, U27      | PHILIPS      | 74LVC00AD   |
| 9         | 1        | CY7C1019BV33-15VC  
SOJ32  
128K X 8 SRAM | U30          | CYPRESS       | CY7C1019BV33-12VC |
<table>
<thead>
<tr>
<th>Reference</th>
<th>Quantity</th>
<th>Description</th>
<th>Reference Design</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1</td>
<td>AD8532AR SOIC8 DUAL AMP 250MA</td>
<td>U29</td>
<td>ANALOG DEVICES</td>
<td>AD8532AR</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>12.288MHZ 1/2 OSC001</td>
<td>U25</td>
<td>DIG01</td>
<td>SG-8002DC-PCC-ND 12.288MH</td>
</tr>
<tr>
<td>12</td>
<td>2</td>
<td>SN74AHC1G02 SOT23-5 SINGLE-2 INPUT-NOR</td>
<td>U34,U37</td>
<td>TI</td>
<td>SN74AHC1G02DBVR</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>SN74LV164A SOIC14 8-BIT-PARALLEL-Serial</td>
<td>U33</td>
<td>TI</td>
<td>SN74LV164AD</td>
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<tr>
<td>14</td>
<td>1</td>
<td>CY7C4201V-15AC TQFP32 64-BYTE-FIFO</td>
<td>U32</td>
<td>CYPRESS</td>
<td>CY7C4201V-15AC</td>
</tr>
<tr>
<td>15</td>
<td>1</td>
<td>25MHZ 1/2 OSC01 OSC</td>
<td>U24</td>
<td>DIGI-KEY</td>
<td>SG-8002DC-PCC-ND</td>
</tr>
<tr>
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<td>12.0MHZ THR OSC006 CRYSTAL</td>
<td>Y1</td>
<td>DIG01</td>
<td>300-6027-ND</td>
</tr>
<tr>
<td>17</td>
<td>1</td>
<td>21161 24LC00 U7** SEE 1000127</td>
<td>U7</td>
<td>MICROCHIP</td>
<td>24LC00-SN</td>
</tr>
<tr>
<td>18</td>
<td>2</td>
<td>1000pF 50V 5% 1206 CERM</td>
<td>C85-86</td>
<td>AVX</td>
<td>12065A102JAT2A</td>
</tr>
<tr>
<td>19</td>
<td>8</td>
<td>2200pF 50V 5% 1206 NPO</td>
<td>C40, C46, C52, C58, C64, C70, C76, C82</td>
<td>AVX</td>
<td>12065A222JAT050</td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>ADM708SAR SOIC8 VOLTAGE-SUPERVISOR</td>
<td>U26</td>
<td>ANALOG DEVICES</td>
<td>ADM708SAR</td>
</tr>
<tr>
<td>21</td>
<td>1</td>
<td>AD1852 SSOP28 MULTI-BIT-SIGMA-DELTA-DAC</td>
<td>U11</td>
<td>ANALOG DEVICES</td>
<td>AD1852JRS</td>
</tr>
<tr>
<td>22</td>
<td>1</td>
<td>AD1836AS MQFP52 MULTI-CHANNEL-96KHZ-CODEC</td>
<td>U10</td>
<td>ANALOG DEVICES</td>
<td>AD1836AS</td>
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</tbody>
</table>
## Bill Of Materials

<table>
<thead>
<tr>
<th>Reference</th>
<th>Quantity</th>
<th>Description</th>
<th>Reference Design</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>23 1</td>
<td>1</td>
<td>ADSP-21161NKCA100 PBGA225 1MM SPACING REV. X1.2</td>
<td>U1</td>
<td>ANALOG DEVICES</td>
<td>ADSP-21161NCCA100</td>
</tr>
<tr>
<td>24 1</td>
<td>1</td>
<td>ADP3338AKC-33 SOT-223 3.3V-1.0AMP REGULATOR</td>
<td>VR2</td>
<td>ANALOG DEVICES</td>
<td>ADP3338AKC-3.3</td>
</tr>
<tr>
<td>25 2</td>
<td>2</td>
<td>ADP3339AKC-5 SOT-223 5V-1.5A REGULATOR</td>
<td>VR1, VR5</td>
<td>ANALOG DEVICES</td>
<td>ADP3339AKC-5-REEL</td>
</tr>
<tr>
<td>26 1</td>
<td>1</td>
<td>ADP3338AKC-18 SOT-223 1.8V-1A REGULATOR</td>
<td>VR3</td>
<td>ANALOG DEVICES</td>
<td>ADP3338AKC-1.8</td>
</tr>
<tr>
<td>27 10</td>
<td>1</td>
<td>LMV722M SOIC8 DUAL AUDIO OP AMP</td>
<td>U12-20, U28</td>
<td>NATIONAL SEMI</td>
<td>LMV722M</td>
</tr>
<tr>
<td>28 3</td>
<td>4.7uF 25V 10% C TANT</td>
<td>CT23-25</td>
<td>AVX</td>
<td>TAJC475K025R</td>
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<tr>
<td>29 1</td>
<td>1</td>
<td>PWR 2.5MM_JACK CON005 RA</td>
<td>P16</td>
<td>SWITCH-CRAFT</td>
<td>SC1152-ND12</td>
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<td>30 1</td>
<td>1</td>
<td>USB 4PIN CON009 USB</td>
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<td>MILL-MAX</td>
<td>897-30-004-90-000000</td>
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<td>1</td>
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<td>TORX173</td>
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<td>1</td>
<td>RCA 4X2 CON011 RA</td>
<td>P8</td>
<td>SWITCH-CRAFT</td>
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<tr>
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<td>1</td>
<td>RCA 1X1 CON012 BLK</td>
<td>P5</td>
<td>SWITCH-CRAFT</td>
<td>PJRAN1X1U01</td>
</tr>
<tr>
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<td>RCA 2X2 CON013</td>
<td>P6</td>
<td>SWITCH-CRAFT</td>
<td>PJRAS2X2S01</td>
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<td>1</td>
<td>LNKPRT 12X2 CON010</td>
<td>P13-14</td>
<td>HONDA (TSUSHINK)</td>
<td>RMCA-EA26LMY-0M03-A</td>
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<td>Quantity</td>
<td>Description</td>
<td>Reference Design</td>
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<td>0.05 10X2  CON014 RA</td>
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<td>AMP</td>
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<td>8</td>
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<td>PANASONIC</td>
<td>EVQ-PAD04M</td>
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<td>1</td>
<td>DIP8 SWT016</td>
<td>SW9</td>
<td>C&amp;K</td>
<td>CKN1365-ND</td>
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<tr>
<td>39</td>
<td>1</td>
<td>10 1/8W 5% 1206</td>
<td>R2</td>
<td>PANASONIC</td>
<td>P10ECT-ND</td>
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<tr>
<td>40</td>
<td>6</td>
<td>0.00 1/8W 5% 1206</td>
<td>R153, R154, R168-169, R217, R218</td>
<td>YAGEO</td>
<td>0.0ECT-ND</td>
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<tr>
<td>41</td>
<td>8</td>
<td>AMBER-SMT LED001 GULL-WING</td>
<td>LED2-7, LED9-10</td>
<td>PANASONIC</td>
<td>LN1461C-TR</td>
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<tr>
<td>42</td>
<td>8</td>
<td>330pF 50V 5% 805 NPO</td>
<td>C36, C42, C48, C54, C60, C66, C72, C78</td>
<td>AVX</td>
<td>08055A331JAT</td>
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<tr>
<td>43</td>
<td>80</td>
<td>0.01uF 100V 10% 805 CERM</td>
<td>C2, C6-7, C91-149, C154-155, C165-171, C184-C186, C174-179</td>
<td>AVX</td>
<td>08051C103KAT2A</td>
</tr>
<tr>
<td>44</td>
<td>11</td>
<td>0.22uF 25V 10% 805 CERM</td>
<td>C156-164, C172, C183</td>
<td>AVX</td>
<td>08053C224FAT</td>
</tr>
<tr>
<td>45</td>
<td>16</td>
<td>0.1uF 50V 10% 805 CERM</td>
<td>C1,C5,C9-11, C33,C87-90, C150-153, C173,C180</td>
<td>AVX</td>
<td>08055C104KAT</td>
</tr>
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<td>Reference</td>
<td>Quantity</td>
<td>Description</td>
<td>Reference Design</td>
<td>Manufacturer</td>
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<td>------------------</td>
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</tr>
<tr>
<td>46</td>
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<td>0.001uF 50V 5% 805 NPO</td>
<td>C14-15, C19-20, C24-25, C29-30</td>
<td>AVX</td>
<td>08055A102JAT2A</td>
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<tr>
<td>47</td>
<td>5</td>
<td>10uF 16V 10% C TANT</td>
<td>CT19-22, CT36</td>
<td>SPRAGUE</td>
<td>293D106X9025C2T</td>
</tr>
<tr>
<td>49</td>
<td>4</td>
<td>33 100MW 5% 805</td>
<td>R1, R150, R176, R152</td>
<td>AVX</td>
<td>CR21-330JTR</td>
</tr>
<tr>
<td>50</td>
<td>5</td>
<td>4.7K 100MW 5% 805</td>
<td>R184, R188, R189, R191, R165</td>
<td>AVX</td>
<td>CR21-4701F-T</td>
</tr>
<tr>
<td>51</td>
<td>11</td>
<td>680 100MW 5% 805</td>
<td>R137-147</td>
<td>AVX</td>
<td>CR21-6800F-T</td>
</tr>
<tr>
<td>52</td>
<td>1</td>
<td>1M 100MW 5% 805</td>
<td>R12</td>
<td>AVX</td>
<td>CR21-1004F-T</td>
</tr>
<tr>
<td>Reference</td>
<td>Quantity</td>
<td>Description</td>
<td>Reference Design</td>
<td>Manufacturer</td>
<td>Part Number</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>-------------</td>
<td>------------------</td>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>53</td>
<td>1</td>
<td>475 100MW 5% 805</td>
<td>R16</td>
<td>AVX</td>
<td>CR21-471J-T</td>
</tr>
<tr>
<td>54</td>
<td>1</td>
<td>1.5K 100MW 5% 805</td>
<td>R7</td>
<td>AVX</td>
<td>CR21-1501F-T</td>
</tr>
<tr>
<td>55</td>
<td>2</td>
<td>2.00K 1/8W 1% 1206</td>
<td>R49-50</td>
<td>DALE</td>
<td>CRCW1206-2001FRT1</td>
</tr>
<tr>
<td>56</td>
<td>10</td>
<td>49.9K 1/8W 1% 1206</td>
<td>R66, R74, R82, R90, R98, R106, R114, R122, R192, R206</td>
<td>AVX</td>
<td>CR32-4992F-T</td>
</tr>
<tr>
<td>57</td>
<td>2</td>
<td>2.21K 1/8W 1% 1206</td>
<td>R10-11</td>
<td>AVX</td>
<td>CR32-2211F-T</td>
</tr>
<tr>
<td>58</td>
<td>24</td>
<td>100pF 100V 5% 1206 NPO</td>
<td>C12, C16-17, C21-22, C26-27, C31, C35, C38, C41, C44, C47, C50, C53, C56, C59, C62, C65, C68, C71, C74, C80, C77</td>
<td>AVX</td>
<td>12061A101JAT2A</td>
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<td>59</td>
<td>5</td>
<td>10uF 16V 10% B TANT</td>
<td>CT1-4, CT11</td>
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<td>60</td>
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<td>22K 100MW 5% 805</td>
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<td>61</td>
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<td>R123, R125, R127, R129, R131, R133, R135</td>
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<td>62</td>
<td>8</td>
<td>220pf 50V 10% 1206 NPO</td>
<td>C39, C45, C51, C57, C63, C69, C75, C81</td>
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<td>1000 100MHz 1.5A FER002 0.06 CHOKE</td>
<td>FER13</td>
<td>MURATA</td>
<td>PLM250S40T1</td>
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<td>64</td>
<td>2</td>
<td>2A S2A RECT DO-214AA SILICON RECTIFIER</td>
<td>D1-2</td>
<td>GENERAL-ALSEMI</td>
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<td>65</td>
<td>11</td>
<td>600 100MHz 500MA 1206 0.70 BEAD</td>
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<td>R23, R27, R30, R34, R40-41, R47-48</td>
<td>KOA</td>
<td>P11.0FCT-ND</td>
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<td>4</td>
<td>750K 1/8W 1% 1206</td>
<td>R25, R32, R38, R45</td>
<td>KOA</td>
<td>RK73H2BT7503F</td>
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<td>5.76K 1/8W 1% 1206</td>
<td>R21, R22, R24, R26, R28-29, R31, R33, R35-37, R39, R42-44, R46</td>
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<td>C13, C18, C23, C28, C187-190</td>
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<td>C32, C34</td>
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<td>R60, R61, R68, R69, R76, R77, R84, R85, R92, R93, R100, R101, R108, R109, R116, R117</td>
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<td>100 1/8W 1% 1206</td>
<td>R54, R57</td>
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<td>R64, R72, R80, R88, R96, R104, R112, R120</td>
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<td>81</td>
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<td>CT5-10</td>
<td>DIG01</td>
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<td>GENERAL</td>
<td>SL22</td>
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<td>10K 100MW 2% RNET16 BUSSED</td>
<td>RN1-2</td>
<td>CTS</td>
<td>767-161-103G</td>
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<td>R53, R56</td>
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<td>DALE</td>
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<td>ADG774ABRQ</td>
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<td>IDC 2X1 IDC2X1 2X1 TIN</td>
<td>JP1, JP4-5, JP22-23, JP26, JP27</td>
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<td>SULLINS</td>
<td>PTC02DAAN</td>
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<td>JP7-8, JP11, JP19-21</td>
<td>BERG</td>
<td>54102-T08-03</td>
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<td>102</td>
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<td>BERG</td>
<td>54102-T08-07</td>
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<td>F1</td>
<td>RAYCHEM CORP.</td>
<td>SMD250-2</td>
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<td>104</td>
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<td>3.5MM STEREO_JACK CON001</td>
<td>P7, P17</td>
<td>SHOGYO</td>
<td>SJ-0359AM-5</td>
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</table>
ADSP-21161 EZ-KIT LITE
Schematic
INSTALL JUMPER TO READ/WRITE OR BOOT FROM FLASH

REMOVE JUMPER WHEN USING SPI OR NO BOOT MODE

FLASH
512K X 8
JTAG HEADER

PIN 3 SHOULD BE CUT

JTAG HEADER CIRCUIT FOR EZ-KIT LITE ONLY
REFER TO EE-68 FOR STANDARD JTAG HEADER CONNECTION. THIS CAN BE FOUND AT HTTP://WWW.ANALOG.COM
OPERATING IN I S COMPATIBLE MODE

PLACE JUMPER ON 1&2 FOR COAX INPUT
PLACE JUMPER ON 2&3 FOR OPTICAL INPUT

MCLK SOURCE FOR AD1836 AND AD1852
INSTALL JUMPER ON 1 & 2 TO USE AUDIO OSCILLATOR
INSTALL JUMPER ON 2 & 3 TO USE CS8414 MCK

TOSLINK OPTICAL INPUT
SPDIF COAX INPUT

Analog Devices
20 Cotton Road
Nashua, NH 03063
MIC PRE AMP GAIN
1&2 20dB
3&3 40dB
NONE 0 dB

SHORTING JUMPER DEFAULT=1&2

ADC2 RIGHT/LEFT
INSTALL JUMPERS ON 3-5 & 4-6 FOR LINE IN
INSTALL JUMPERS ON 1-3 & 2-4 FOR MIC IN

MIC INPUT

ADC2 INPUT SELECTOR

MIC INPUT

AVCC

MIC INPUT

1.00K
R56
1206

R57
1206
10.0K

R55
1206
10.0K

U16

MIC PRE AMP GAIN
1&2 20dB
3&3 40dB
NONE 0 dB

SHORTING JUMPER DEFAULT=1&2

SHORTING JUMPER DEFAULT=3&5

SHORTING JUMPER DEFAULT=4&6

ADC2 RIGHT/LEFT
DAC1 LEFT

DAC1 RIGHT

ANALOG DEVICES
21161N EZ-KIT LITE - DAC1 OUTPUT
OSCILLATOR OR CRYSTAL CAN BE USED FOR THE 21161N

LED9 INDICATES AUDIO OUTPUT MAY NOT BE VALID
LED10 INDICATES MONITOR FIRMWARE IS RUNNING

18 OF 24
JP1 SHOULD NOT BE INSTALLED WHEN USING THE LINK PORT

JP1 SHOULD NOT BE INSTALLED WHEN USING THE LINK PORT
Symbols
- BMS, memory select pin, 2-2, 3-3
- MS0, memory select pin, 2-2, 3-3
- MS1, memory select pin, 2-2, 3-3

A
abort, hang operations, 2-12
acknowledge, hang operation, 2-12
AD1836, xii, 2-6, 3-3, 3-4, 3-6
control registers, 3-12
MIC1 input channel, 3-4
SPI port, 2-7
SPI select pin, 2-5
AD1852, xii, 2-7, 3-4, 3-6
sampling frequency, 3-7
SPI port, 2-7
SPI select pin, 2-5
ADC1 input selector (JP11), 3-9
ADC2 mode selection (JP7, JP8), 3-8
Add New Hardware Wizard, Windows 98, 1-7
ADSP-21161N processor
boot modes, 3-10
clock jumper (JP21), 3-11
core speed, 3-3
core voltage, 3-2
external voltage, 3-2
ID jumper (JP19), 3-10
internal memory restrictions, 2-2
interrupt pins, 2-6
memory map, 2-2
reset, 2-5
SPI port, 2-7
analog audio
input, 2-6
interface, xii
asynchronous FLAGs, 2-5
audio
connectors (P4-8, P17), 3-18
input, 2-6, 3-3
interface, 2-6
output, 2-8, 3-3
stream, 3-14

B
bill of materials, A-1
BMS pin
enabling (JP22), 3-12
see -BMS, select pin
board measurements, 3-21
boot
code, xiii
load, 2-9
memory select pin (-BMS), 3-3, 3-12
INDEX

memory space, 2-2
mode select (JP20), 3-10
breadboard area, xiii
breakpoints, 2-12

C
clear, hang operations, 2-12
CLK_CFG pins, 3-11
CLKDBL pins, 3-11
clock
frequency, 3-11
mode jumper (JP21), 3-3, 3-11
modes, 3-11
common attributes, hardware
breakpoints, 2-13
configuring SDRAM, 2-3
connecting, EZ-KIT Lite board, 1-5
connectors, -xii, 1-5, 3-16
JP11 (analog audio input), 2-6
JP2 (digital audio input), 2-6
P10 (external port), 2-5, 2-6, 3-3,
3-19
P12 (JTAG header), 3-19
P13 (link port), 3-19
P14 (link port), 3-19
P15 (SPORT1, SPORT3), 3-20
P16 (power), 1-5, 3-20
P2 (USB), 1-6, 3-16
P4 (optical input), 2-6, 3-5
P5 (mono jack), 2-6, 3-5
P6 (mono jack), 2-6, 3-4, 3-9
P7 (stereo jack), 2-6, 3-4, 3-9
P9 (external port), 3-3, 3-18
contents, EZ-KIT Lite package, 1-1

core
conventions, manual, -xxi
converters, 2-7

D
data hardware breakpoints, 2-15
Device Manager window, 1-15
digital
audio playback, 2-7
data, 2-7
stereo channels, 2-7
DSP signals, DAL_P, 3-15
DVD formats, 2-7

E
EBOOT pins, 3-10
electrostatic discharge, 1-2
emulator connector, xiii
enable attribute, 2-14
end address, attribute, 2-14
EPROM boot mode, 3-10, 3-12
example programs, 2-8
exclusive, attribute, 2-14
expansion connector footprints, xiii
external
data bus, 3-5
interrupts, 2-6
memory, EZ-KIT Lite, 2-3
port clock ratio, 3-11
port connectors, 3-3
port interface, xiii, 3-3
port signals, 3-18, 3-19
EZ-KIT Lite board
architecture, 3-2
features, xii
specifications, 3-21

F
features, EZ-KIT Lite board, -xii
FLAG
directing, 2-5
pins, 2-5, 3-15
registers, 2-5
FLAG0, 2-5, 3-12, 3-15
enable jumper (JP4), 3-7
FLAG1, 2-5, 3-12, 3-15
enable jumper (JP5), 3-7
FLAG10, 2-5
FLAG11, 2-5
FLAG2, 2-5, 3-15
FLAG3, 2-5, 3-15
FLAG4, 3-14
FLAG4-9, 2-5, 3-14
FLAG5, 3-14
FLAG6, 3-14
FLAG7, 3-14
FLAG8, 3-14
FLAG9, 3-14
flash
memory, xii, 2-2, 3-3, 3-12
programmer, 2-8

Found New Hardware Wizard
Windows 2000, 1-13
frequency jumper (JP6), 3-7

G
general-purpose IO, xiii
global options, hardware breakpoints, 2-13
graphical user interface (GUI), 2-9

H
hard reset, 2-9
hardware breakpoints, 2-12, 2-17, 2-18
dialog box, 2-13
Help, online, xix, 2-8
host
processor booting, 3-10
processor interface, xiii, 3-3
processor interface connector (P10), 3-19
hung conditions, 2-11

I
I2S mode, 2-7
ignore, hang operations, 2-12
input clock, 3-2
installation, summary, 1-3
installing
EZ-KIT Lite USB driver, 1-6
VisualDSP++ and EZ-KIT Lite
license, 1-4
VisualDSP++ and EZ-KIT Lite
software, 1-4
instruction hardware breakpoints, 2-16
INDEX

interface connectors, xiii
interfaces
  see graphical user interface (GUI)
internal memory, EZ-KIT Lite, 2-3
interrupt
  pins, 2-6
  push buttons, xiii
  see also push buttons
IO
  input push buttons (SW1-4), 3-15
  pins see FLAGs
  voltage, 3-21
  IRQ0-2 pins, 2-6, 3-16

J
JTAG
  connector (P12), 3-19
  emulation port, 3-5
  emulator, 3-19
jumper settings, 1-5
jumpers, 2-7
  JP1 (SDRAM disable), 3-5
  JP10 (microphone), 3-8
  JP11 (audio in), 3-4, 3-9
  JP19 (processor ID), 3-10
  JP2 (SPDIF), 3-5
  JP20 (boot mode), 3-10
  JP21 (clock), 3-11
  JP22 (~BMS), 3-12
  JP26 (SW1 enable), 3-12
  JP27 (SW2 enable), 3-12
  JP3 (MCLK source), 3-6
  JP6 (frequency), 3-7
  JP7 (ADC2), 3-8
  JP8 (ADC2), 3-8
  JP9 (microphone), 3-8

L
  latency, 2-18
  LBOOT pins, 3-10
  LEDs, xiii, 1-5, 2-5, 3-13, 3-14
    LED1 (reset), 1-5, 3-14
    LED10 (USB monitor), 1-15, 1-16,
      3-15
    LED11 (power), 1-5, 3-15
    LED2 (FLAG9), 3-14
    LED2-LED7 (FLAGs), 3-14
    LED3 (FLAG8), 3-14
    LED4 (FLAG7), 3-14
    LED5 (FLAG6), 3-14
    LED6 (FLAG5), 3-14
    LED7 (FLAG4), 3-14
    LED8 (DSP reset), 1-5, 1-14, 3-14
    LED9 (VERF), 2-8, 3-14
  line-in
    input channel, 3-4
    jacks, 2-7
  line-out jacks, 2-8
  link port, 3-5, 3-10
    booting, 3-11
    connectors, 3-19

M
  MCLK, selecting (JP3), 3-6
  measurements, EZ-KIT Lite, 3-21
  memory
    restrictions, 2-2
    select pins, 3-3
microphone
   circuit, 3-8
   jacks, 2-7
mode, attribute, 2-14
MODE2 register, 2-5

N
no-boot mode, 3-11, 3-12

O
oscillator, 3-11
   surface-mount, 3-2
   through-hole, 3-2
   through-hole crystal, 3-2

P
package contents, 1-1
PC configuration, 1-3
power
   connector (P16), 3-20
   LED (LED11), 3-15
   specifications, 3-21
   supply, 3-21
processor external memory, see
   ADSP-21161N processor
programmable FLAGs
   see FLAGs
push buttons, xiii, 2-6, 3-13, 3-15
   SW1 (FLAG0), 3-15
   SW2 (FLAG1), 3-15
   SW3 (FLAG2), 3-15
   SW4 (FLAG3), 3-15
   SW5 (IRQ0), 3-15
   SW6 (IRQ1), 3-15
   SW7 (IRQ2), 3-15
   SW8 (reset), 3-16

R
RCA jacks, 2-7, 3-3
registering, this product, 1-2, 1-4
reset
   board, 2-9
   hang operation, 2-12
   processor, 3-14
   push button (SW8), 3-16
retry, hang operation, 2-12

S
sample frequencies, 2-7
SDRAM
   configuration, 2-3
   control registers, 2-3
   disabling (JP1), 3-5
   memory, 2-2, 2-3, 3-3
   semiconductor receiver, xii
   serial booting, 3-10, 3-12
setting
   breakpoints, 2-18
   EZ-KIT Lite hardware, 1-5
   target options, 2-9
SMT footprints, xiii
SPDIF
   connectors, 3-14
   modes, 3-7
   selecting (JP2), 3-5
   specifications, 3-21
SPI
   audio interface, 3-4
INDEX

port, 3-4, 3-12
select pin, 2-5
SPORT
    audio interface, 3-3
    connectors, 3-3
SPORT0, xiii
SPORT1, xiii, 3-12, 3-20
SPORT2, xiii
SPORT3, xiii, 3-20
SRAM memory, 2-2
start address, attribute, 2-14
starting VisualDSP++, 1-16
stereo
    jack (P7), 2-6, 3-3
    output channels, 2-6
SW1 (FLAG0) push button, 2-5
SW1 (JP26) enable push button, 3-12
SW2 (FLAG1) push button, 2-5
SW3 (FLAG2) push button, 2-5
SW4 (FLAG3) push button, 2-5
SW5 (interrupt) push button, 2-6, 3-16
SW6 (interrupt) push button, 2-6, 3-16
SW7 (interrupt) push button, 2-6, 3-16
SW8 (reset) push button, 1-14
system
    architecture, EZ-KIT Lite board, 3-2
    requirements, PC, 1-3
T
target options
    dialog box, 2-9
    miscellaneous, 2-10
on emulator exit, 2-10
while target is halted, 2-10

U
UART, 3-11
USB
    cable, 1-2
    connector (P2), 3-16
    debug interface, 3-19
driver installation, Windows 2000, 1-11
driver installation, Windows 98, 1-7
driver installation, Windows XP, 1-12
interface, 3-14, 3-16
monitor LED (LED10), 3-15
user
    input, 2-5
    output, 2-5

V
VERF flag (LED9), 2-8, 3-14
verifying USB driver installation, 1-14
VisualDSP++
    documentation, xix
    installation, 1-4
    license, 1-4
    online Help, xix
    requirements, 1-3
    starting, 1-16
    voltage regulators, xiii