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Limited Warranty

The EZ-KIT Lite evaluation system is warranted against defects in materials and workmanship for a period of one year from the date of purchase from Analog Devices or from an authorized dealer.

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Regulatory Compliance

The ADSP-BF561 EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the “CE” mark.

The ADSP-BF561 EZ-KIT Lite evaluation system had been appended to the Technical Construction File referenced “DSPTOOLS1” dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body as listed below.

Technical Certificate No: Z600ANA1.016

Issued by: Technology International (Europe) Limited
41 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TZ, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.
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## BILL OF MATERIALS

## INDEX
Thank you for purchasing the ADSP-BF561 EZ-KIT Lite®, Analog Devices (ADI) evaluation system for Blackfin® embedded media processors.

The Blackfin processors are embedded processors that support a Media Instruction Set Computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics towards delivering signal processing performance in a microprocessor-like environment.

The evaluation board is designed to be used in conjunction with the VisualDSP++™ development environment to test the capabilities of the ADSP-BF561 Blackfin processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C and ADSP-BF561 assembly
- Load, run, step, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF561 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF561 processor and the
evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and DSP development tools, go to http://www.analog.com/dsp/tools/.

ADSP-BF561 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The VisualDSP++ license provided with this EZ-KIT Lite evaluation system limits the size of a user program to 41 KB of internal memory.

The board features:

- Analog Devices ADSP-BF561 processor
  - 256-pin Mini-BGA package
  - 30 MHz CLKIN oscillator
- Synchronous Dynamic Random Access Memory (SDRAM)
  - 64 MB (16M x 16 bits x 2 chips)
- Flash Memory
  - 8 MB (4M x 16 bits)
- Analog Audio Interface
  - AD1836 A – Analog Devices 96 kHz audio codec
  - 4 input RCA phono jacks (2 Stereo Channels)
  - 6 output RCA phono jacks (3 Stereo Channels)
- Analog Video Interface
  - ADV7183A video decoder w/ 3 input RCA phono jacks
  - ADV7179 video encoder w/ 3 output RCA phono jacks
Universal Asynchronous Receiver/Transmitter (UART)
  - ADM3202 RS-232 line driver/receiver
  - DB9 male connector

LEDs
  - 20 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 16 general purpose (amber), and 1 USB monitor (amber)

Push Buttons
  - 5 push buttons with debounce logic: 1 reset, 4 programmable flags

Expansion Interface
  - PPI0, PPI1, SPI, EBIU, Timers11-0, UART, Programmable Flags, SPORT0, SPORT1

Other Features
  - JTAG ICE 14-pin header

The EZ-KIT Lite board holds 8 MB of Flash memory, which can be used to store user-specific boot code, allowing the board to run as a stand-alone unit. The board also holds 512-Mb SDRAM, which can be used at runtime. For more information see “Using External Memory” on page 2-2.

SPORT0 interfaces with the AD1836A audio codec, allowing you to create audio signal processing applications. SPORT0 also attaches to an off-board connector to allow communication with other serial devices. For information about SPORT0, see “SPORT0 Audio Interface” on page 3-3.

The Parallel Peripheral Interfaces (PPIs) of the DSP connect to both a video encoder and video decoder, allowing you to create video signal processing applications. For information on how the board utilizes the processor’s PPIs, see “PPI Interfaces” on page 3-6.
Purpose of This Manual

The UART of the DSP connects to an RS232 Line Driver and a DB9 male connector, allowing you to interface with a PC or other serial device. For information about the UART, see “UART Port” on page 3-8.

Additionally, the EZ-KIT Lite board provides access to most of the processor’s peripheral ports. Access is provided in the form of a three-connector expansion interface. For information about the expansion interface, see “Expansion Interface” on page 3-8.

Purpose of This Manual

The ADSP-BF561 EZ-KIT Lite Evaluation System Manual provides instructions for using the hardware and installing the software on your PC. This manual provides guidelines for running your own code on the ADSP-BF561 EZ-KIT Lite. The manual also describes the operation and configuration of the evaluation board’s components. Finally, a schematic and a bill of materials are provided as a reference for future ADSP-BF561 board designs.

Intended Audience

This manual is a user’s guide and reference to the ADSP-BF561 EZ-KIT Lite evaluation system. Programmers who are familiar with the Analog Devices Blackfin processor architecture, operation, and programming are the primary audience for this manual.

Programmers who are unfamiliar with Analog Devices Blackfin processors can use this manual in conjunction with the ADSP-BF561 Blackfin Processor Hardware Reference and the Blackfin Processor Instruction Set Reference, which describe the processor’s architecture and instruction set. Programmers who are unfamiliar with VisualDSP++ should refer to the
Preface

VisualDSP++ online Help and the VisualDSP++ user’s or getting started guides. For the locations of these documents, refer to “Related Documents”.

Manual Contents

The manual consists of:

- **Chapter 1, “Getting Started” on page 1-1**
  Provides software and hardware installation procedures, PC system requirements, and basic board information.

- **Chapter 2, “Getting Started” on page 1-1**
  Provides information on the EZ-KIT Lite from a programmer’s perspective and provides an easy-to-access memory map.

- **Chapter 3, “EZ-KIT Lite Hardware Reference” on page 3-1**
  Provides information on the hardware aspects of the evaluation system.

- **Appendix A, “Bill Of Materials” on page A-1**
  Provides a list of components used to manufacture the EZ-KIT Lite board.

- **Appendix B, “Schematics” on page B-1**
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.

  This appendix is not part of the online Help. The online Help viewers should go the PDF version of the ADSP-BF561 EZ-KIT Lite Evaluation System Manual located in the Docs\EZ-KIT Lite Manuals folder on the installation CD to see the schematics.
What’s New in This Manual

This is the first edition of the ADSP-BF561 EZ-KIT Lite Evaluation System Manual. The manual documents the tools support for ADSP-BF561 Blackfin processors.

Technical or Customer Support

You can reach DSP Tools Support in the following ways.

- Email questions to dsptools.support@analog.com
- Phone questions to 1-800-ANALOGD
- Contact your ADI local sales office or authorized distributor
- Send questions by mail to

  Analog Devices, Inc.
  One Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

The ADSP-BF561 EZ-KIT Lite evaluation system supports ADSP-BF561 Blackfin Analog Devices embedded processors.
Product Information

You can obtain product information from the Analog Devices website, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at www.analog.com. Our website provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices website that allows customization of a webpage to display only the latest information on products you are interested in. You can also choose to receive weekly email notification containing updates to the webpages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit www.myanalog.com to sign up. Click Register to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your email address.

DSP Product Information

For information on digital signal processors, visit our website at www.analog.com/dsp, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.
Product Information

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- Email questions or requests for information to dsp.support@analog.com
- Fax questions or requests for information to 1-781-461-3010 (North America) or +49 (0) 89 76903-157 (Europe)

Related Documents

For information on product related development software, see the following publications.

Table 1. Related DSP Publications

<table>
<thead>
<tr>
<th>Title</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADSP-BF561 Blackfin Processor Hardware Reference</td>
<td>Description of internal processor architecture and all register functions.</td>
</tr>
<tr>
<td>Blackfin Processor Instruction Set Reference</td>
<td>Description of all allowed processor assembly instructions.</td>
</tr>
</tbody>
</table>

Table 2. Related VisualDSP++ Publications

<table>
<thead>
<tr>
<th>Title</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VisualDSP++ 3.5 Assembler and Preprocessor Manual for Blackfin Processors</td>
<td>Description of the assembler function and commands for Blackfin processors.</td>
</tr>
<tr>
<td>VisualDSP++ 3.5 C/C++ Compiler and Library Manual for Blackfin Processors</td>
<td>Description of the compiler function and commands for Blackfin processors.</td>
</tr>
</tbody>
</table>
Preface

Table 2. Related VisualDSP++ Publications (Cont’d)

<table>
<thead>
<tr>
<th>Title</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VisualDSP++ 3.5 Linker &amp; Utilities Manual for 16-Bit Processors</td>
<td>Description of the linker function and commands for 16-bit processors.</td>
</tr>
<tr>
<td>VisualDSP++ 3.5 Loader Manual for 16-Bit Processors</td>
<td>Description of the loader/splitter function and commands for 16-bit processors.</td>
</tr>
</tbody>
</table>

The listed documents can be found through online Help or in the Docs folder of your VisualDSP++ installation. Most documents are available in printed form.

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, refer to the documentation that accompanies the emulator.

Online Documentation

Your software installation kit includes online Help as part of the Windows® interface. These help files provide information about VisualDSP++ and the ADSP-BF561 EZ-KIT Lite evaluation system.

To view VisualDSP++ Help, click on the Help menu item or go to the Windows task bar and select Start --> Programs --> Analog Devices --> VisualDSP++ 3.5 for 16-bit Processors --> VisualDSP++ Documentation.

To view ADSP-BF561 EZ-KIT Lite Help, which now is a part of the VisualDSP++ Help system, go the Contents tab of the Help window and select Manuals --> ADSP-BF561 EZ-KIT Lite.

For more documentation, please go to http://www.analog.com/technology/dsp/library.html.
Product Information

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at 1-800-ANALOGD (1-800-262-5643) and follow the prompts.

VisualDSP++ Documentation Set

Printed copies of VisualDSP++ manuals may be purchased through Analog Devices Customer Service at 1-781-329-4700; ask for a Customer Service representative. The manuals can be purchased only as a kit. For additional information, call 1-603-883-2430.

If you do not have an account with Analog Devices, you will be referred to Analog Devices distributors. To get information on our distributors, log onto www.analog.com/salesdir/continent.asp.

Hardware Manuals

Printed copies of hardware reference and instruction set reference manuals can be ordered through the Literature Center or downloaded from the Analog Devices website. The phone number is 1-800-ANALOGD (1-800-262-5643). The manuals can be ordered by a title or by product number located on the back cover of each manual.

Data Sheets

All data sheets can be downloaded from the Analog Devices website. As a general rule, printed copies of data sheets with a letter suffix (L, M, N, S) can be obtained from the Literature Center at 1-800-ANALOGD (1-800-262-5643) or downloaded from the website. Data sheets without the suffix can be downloaded from the website only—no hard copies are available. You can ask for the data sheet by part name or by product number.
If you want to have a data sheet faxed to you, the phone number for that service is 1-800-446-6212. Follow the prompts and a list of data sheet code numbers will be faxed to you. Call the Literature Center first to find out if requested data sheets are available.

**Contacting DSP Publications**

Please send your comments and recommendations on how to improve our manuals and online Help. You can contact us at dsp.techpubs@analog.com.

**Notation Conventions**

The following table identifies and describes text conventions used in this manual.

Additional conventions, which apply only to specific chapters, may appear throughout this document.

<table>
<thead>
<tr>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Close command (File menu) or OK</td>
<td>Text in <strong>bold</strong> style indicates the location of an item within the VisualDSP++ environment's and boards' menu system and user interface items.</td>
</tr>
<tr>
<td>{this</td>
<td>that}</td>
</tr>
<tr>
<td>[this</td>
<td>that]</td>
</tr>
<tr>
<td>[this,...]</td>
<td>Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipsis; read the example as an optional comma-separated list of <strong>this</strong>.</td>
</tr>
<tr>
<td>PF9-0</td>
<td>Registers, connectors, pins, commands, directives, keywords, code examples, and feature names are in text with <strong>letter gothic font</strong>.</td>
</tr>
<tr>
<td>filename</td>
<td>Non-keyword placeholders appear in text with <strong>italic style format</strong>.</td>
</tr>
</tbody>
</table>
## Notation Conventions

<table>
<thead>
<tr>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Note:" /></td>
<td>A note providing information of special interest or identifying a related topic. In the online version of this book, the word Note appears instead of this symbol.</td>
</tr>
<tr>
<td><img src="image" alt="Caution:" /></td>
<td>A caution providing information about critical design or programming issues that influence operation of a product. In the online version of this book, the word Caution appears instead of this symbol.</td>
</tr>
</tbody>
</table>
1 GETTING STARTED

This chapter provides the information you need to begin using ADSP-BF561 EZ-KIT Lite evaluation system. For correct operation, install the software and hardware in the order presented in “Installation Tasks” on page 1-3.

The chapter includes the following sections.

- “Contents of EZ-KIT Lite Package” on page 1-1
  Provides a list of the components shipped with this EZ-KIT Lite evaluation system.

- “PC Configuration” on page 1-3
  Describes the minimum requirements for the PC to work with the EZ-KIT Lite evaluation system.

- “Installation Tasks” on page 1-3
  Describes the step-by-step procedures for setting up the hardware and software.

Contents of EZ-KIT Lite Package

Your ADSP-BF561 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF561 EZ-KIT Lite board
- EZ-KIT Lite Quick Start Guide
- VisualDSP++ 3.5 Installation Quick Reference Card
Contents of EZ-KIT Lite Package

- CD containing VisualDSP++ 3.5 for 16-bit processors with a limited license
- CD containing:
  - ADSP-BF561 EZ-KIT Lite debug software
  - USB driver files
  - Example programs
  - *ADSP-BF561 EZ-KIT Lite Evaluation System Manual* (this document)
- Universal 7.5V DC power supply
- USB 2.0 type cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.
Getting Started

PC Configuration

For correct operation of the VisualDSP++ software and the EZ-KIT Lite, your computer must have the minimum configuration:

<table>
<thead>
<tr>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Windows 98, Windows 2000, Windows XP</td>
</tr>
<tr>
<td>Intel (or comparable) 166 MHz processor</td>
</tr>
<tr>
<td>VGA Monitor and color video card</td>
</tr>
<tr>
<td>2-button mouse</td>
</tr>
<tr>
<td>50 MB free on hard drive</td>
</tr>
<tr>
<td>32 MB RAM</td>
</tr>
<tr>
<td>Full-speed USB port</td>
</tr>
<tr>
<td>CD-ROM Drive</td>
</tr>
</tbody>
</table>

EZ-KIT Lite does not run under Windows 95 or Windows NT.

Installation Tasks

The following task list is provided for the safe and effective use of the ADSP-BF561 EZ-KIT Lite. Follow the instructions in the presented order to ensure correct operation of your software and hardware.

1. VisualDSP++ and EZ-KIT Lite software installation
2. VisualDSP++ license installation and registration
3. EZ-KIT Lite hardware setup
4. EZ-KIT Lite USB driver installation
5. USB driver installation verification
6. VisualDSP++ startup
Installation Tasks

Installing VisualDSP++ and EZ-KIT Lite Software

The ADSP-BF561 EZ-KIT Lite Update CD installs all of the files necessary to use the EZ-KIT Lite. The ADSP-BF561 EZ-KIT Lite requires the VisualDSP++ 3.5 for 16-bit processors software (included in the package) pre-installed on your PC.

To install the ADSP-BF561 EZ-KIT Lite software:

1. If VisualDSP++ 3.5 for 16-bit processors is installed already on your system, go to step 2.
   If VisualDSP++ 3.5 for 16-bit processors is not installed on your system, install the software prior to installing the ADSP-BF561 EZ-KIT Lite evaluation system. Refer to the VisualDSP++ 3.5 Installation Quick Reference Card for instructions.

2. Insert the ADSP-BF561 EZ-KIT Lite installation CD into the CD-ROM drive.

3. If Autoplay is enabled on your PC, you see the Install Shield Wizard Welcome screen. Otherwise, choose Run from the Start menu, and enter D:\Update.exe in the Open field, where D is the name of your local CD-ROM drive.

4. Follow the on-screen instructions to continue installing the software.

5. When the EZ-KIT Lite installs, the Wizard Completed screen appears. Click Finish.
Getting Started

Installing and Registering VisualDSP++ License

VisualDSP++ and EZ-KIT Lites are licensed products. You may run only one copy of the software for each license purchased. Once a new copy of the VisualDSP++ or EZ-KIT Lite software is installed on your PC, you must install, register, and validate your licence.

The VisualDSP++ 3.5 Installation Quick Reference Card included in your package will guide you through the licence installation and registration process (refer to Tasks 1, 2, and 3).

Setting Up EZ-KIT Lite Hardware

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF561 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

To connect the EZ-KIT Lite board:

1. Remove the EZ-KIT Lite board from the package. Be careful when handling the board to avoid the discharge of static electricity, which may damage some components.

2. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before continuing.
3. Plug the provided power supply into J4 on the EZ-KIT Lite board. Visually verify that the green power LED (J7) is on. Also verify that the two red reset LEDs (LED2 and LED3) go on for a moment and then go off.

4. Connect one end of the USB cable to an available full speed USB port on your PC and the other end to J5 on the ADSP-BF561 EZ-KIT Lite board.
Getting Started

Installing EZ-KIT Lite USB Driver

The EZ-KIT Lite evaluation system installed on the following platforms requires one full-speed USB port.

- “Windows 98 USB Driver” on page 1-8 describes the installation on Windows 98.
- “Windows XP USB Driver” on page 1-13 describes the installation on Windows XP.

The USB driver used by the debug agent is not Microsoft certified because it is intended for a development or laboratory environment, not a commercial environment.
Installation Tasks

Windows 98 USB Driver

Before using the ADSP-BF561 EZ-KIT Lite for the first time, the Windows 98 USB driver must first be installed.

To install the USB driver:

1. Insert the CD into the CD-ROM drive. The connection of the device to the USB port activates the Windows 98 Add New Hardware Wizard, as shown in Figure 1-2.

2. Click Next.
Getting Started

3. Select **Search for the best driver for your device**, as shown in Figure 1-3.

![Figure 1-3. Windows 98 – Searching for Driver](image)

4. Click **Next**.

5. Select **CD-ROM drive**, as shown in Figure 1-4.

![Figure 1-4. Windows 98 – Searching for CD-ROM](image)
Installation Tasks

6. Click Next. Windows 98 locates the WmUSB Ez.inf file on the installation CD, as shown in Figure 1-5.

![Figure 1-5. Windows 98 – Locating Driver](image)

7. Click Next. The Coping Files dialog box appears (Figure 1-6).

![Figure 1-6. Windows 98 – Searching for .SYS File](image)
8. Click **Browse**.

The **Open** dialog box, shown in Figure 1-7, appears on the screen.

![Figure 1-7. Windows 98 – Opening .SYS File](image)


10. Click **OK**.

The **Copying Files** dialog box (Figure 1-8) appears.

![Figure 1-8. Windows 98 – Copying .SYS File](image)
Installation Tasks

11. Click **OK**.
   The driver installation is now complete, as shown in Figure 1-9.

![Add New Hardware Wizard](image)

Figure 1-9. Windows 98 – Completing Software Installation

12. Click **Finish** to exit the wizard.

Verify the installation by following the instructions in “Verifying Driver Installation” on page 1-15.

**Windows 2000 USB Driver**

VisualDSP++ 3.5 installation software pre-installs the necessary drivers for the EZ-KIT Lite. The install also upgrades an older driver if such is detected in the system.

⚠ Prior to running the VisualDSP++ 3.5 installer, ensure there are no other Hardware Wizard windows running in the background. If there are any wizard windows running, close them before starting the installer.
To install the USB driver:

1. If VisualDSP++ 3.5 is already installed on your system, go to step 2.
   Otherwise, run VisualDSP++ 3.5 installation. Refer to the VisualDSP++ 3.5 Installation Quick Reference Card for a detailed installation description.

2. Connect the EZ-KIT Lite device to your PC’s USB port.
   Windows 2000 automatically detects an EZ-KIT device and automatically installs the appropriate driver for the device.

3. Verify the installation by following the instructions in “Verifying Driver Installation” on page 1-15.

Windows XP USB Driver

VisualDSP++ 3.5 installation software pre-installs the necessary drivers for the EZ-KIT Lite. The install also upgrades an older driver if such is detected in the system.

Prior to running the VisualDSP++ 3.5 installer, ensure there are no other Hardware Wizard windows running in the background. If there are any wizard windows running, close them before starting the installer.

To install the USB driver:

1. If VisualDSP++ 3.5 is already installed on your system, go to step 2.
   Otherwise, run VisualDSP++ 3.5 installation. Refer to the VisualDSP++ 3.5 Installation Quick Reference Card for a detailed installation description.
Installation Tasks

2. Connect the EZ-KIT Lite device to your PC’s USB port. By connecting the device to the USB port you activate the Windows XP Found New Hardware Wizard, shown in Figure 1-10.

![Figure 1-10. Windows XP – Found New Hardware Wizard](image1)

3. Select Install the software automatically (Recommended) and click Next. When Windows XP completes the driver installation for the device, a window shown in Figure 1-11 appears on the screen.

![Figure 1-11. Windows XP –Completing Driver Installation](image2)

1-14 ADSP-BF561 EZ-KIT Lite Evaluation System Manual
4. Verify the installation by following the instructions in “Verifying Driver Installation”.

**Verifying Driver Installation**

Before you use the EZ-KIT Lite evaluation system, verify that the USB driver software is installed properly:

1. Ensure that the USB cable is connected to the evaluation board and the PC.

2. Verify that the yellow USB monitor LED (LED4) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

3. Verify that the USB driver software is installed properly. Open Windows Device Manager and verify that ADSP-BF561 EZ-KIT Lite shows under ADI Development Tools with no exclamation point, as in Figure 1-12.

![Device Manager Window](image)

Figure 1-12. Device Manager Window
Installation Tasks

If using an EZ-KIT Lite on Windows 98, disconnect the USB cable from the board before booting the PC. When Windows 98 is booted and you are logged on, re-connect the USB cable to the board. The operation should continue normally from this point.

Starting VisualDSP++

First, verify that the yellow USB monitor LED (LED4, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

If you do not have an existing EZ-KIT Lite session, create one based on the existing EZ-KIT Lite platform template:


2. Double click the ADSP-BF561 EZ-KIT Lite in the list of available Platform Templates. The Platform Properties dialog box for the chosen platform appears on the screen.

3. Click OK to close the Platform Properties dialog box.

4. Click OK to close the VisualDSP++ Configurator dialog box. Your new EZ-KIT Lite session is set.

Lastly, open your new or existing EZ-KIT Lite session:

1. From the Start menu, choose Programs-->Analog Devices-->VisualDSP++ 3.5 for 16-bit Processors-->VisualDSP++ Environment. If you running VisualDSP++ for the first time, press the Ctrl key to bring up the Session List dialog box. Otherwise, the last opened session appears on the screen (skip the rest of the procedure).

2. Click the New Session button.
3. In **Debug Target**, select **Blackfin Emulators/EZ-KITs**.
   In **Platform**, select the platform you created in **VisualDSP++ Configurator**.
   In **Multiprocessor System** (the ADSP-BF561 EZ-KIT Lite is an example of a multiprocessor system), select a core for your session.

4. Click **OK** to return to the **Session List**.

5. From the **Session List** dialog box, highlight the session and click **Activate**.
Installation Tasks
2 USING EZ-KIT LITE

This chapter provides specific information to assist you with developing programs for the ADSP-BF561 EZ-KIT Lite evaluation system. This information appears in the following sections.

- “EZ-KIT Lite License Restrictions” on page 2-2
  Describes the restrictions of the VisualDSP++ license shipped with the EZ-KIT Lite.

- “Using External Memory” on page 2-2
  Defines the ADSP-BF561 EZ-KIT Lite’s external memory map.

- “Using LEDs and Push Buttons” on page 2-5
  Describes the board’s LEDs and push buttons.

- “Using Audio” on page 2-6
  Describes the board’s audio interface.

- “Using Video” on page 2-7
  Describes the board’s video interface.

- “Example Programs” on page 2-8
  Provides information about the example programs included in the ADSP-BF561 EZ-KIT Lite evaluation system.

- “Using Background Telemetry Channel” on page 2-8
  Highlights the advantages of the Background Telemetry Channel feature of VisualDSP++.

- “Using EZ-KIT Lite VisualDSP++ Interface” on page 2-9
  Describes the target options facilities of the EZ-KIT Lite system.
EZ-KIT Lite License Restrictions

For more detailed information about programming the ADSP-BF561 Blackfin processor, see the documents referred to as “Related Documents”.

EZ-KIT Lite License Restrictions

The license shipped with the EZ-KIT Lite imposes the following restrictions.

- The size of a user program is limited to 41 KB of the ADSP-BF561 processor's internal memory space.
- No connections to a simulator or emulator session are allowed.
- The EZ-KIT Lite hardware must be connected and powered up in order to use VisualDSP++ with a kit license.

Using External Memory

EZ-KIT Lite board includes two types of external memory, 64-MB SDRAM and 8-MB Flash. Table 2-1 shows the memory map of these devices. The complete configuration of the ADSP-BF561 processor internal SRAM is detailed in Figure 2-1.

Table 2-1. EZ-KIT Lite External Memory Map

<table>
<thead>
<tr>
<th>Start Address</th>
<th>End Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000</td>
<td>0x3FFFFFF</td>
<td>SDRAM Bank 0; see “Using External Memory” on page 2-2</td>
</tr>
<tr>
<td>0x20000000</td>
<td>0x207FFFFFF</td>
<td>ASYNC Memory Bank 0; see “Using External Memory” on page 2-2.</td>
</tr>
<tr>
<td>All other locations</td>
<td>Not used</td>
<td></td>
</tr>
</tbody>
</table>
Using EZ-KIT Lite

The 8 MB of Flash memory is organized as 4M x 16 bit and mapped into a ADSP-BF561 processor’s ASYNC Memory Bank 0 (~AMS0, memory select signal connects to the Flash memory’s output enable pin).

The 64 MB of SDRAM is organized as 16M x 32 bits wide. The processor’s memory select pin ~SMS0 is configured for the SDRAM. Three SDRAM control registers must be initialized in order to access the SDRAM memory.

When in a VisualDSP++ EZ-KIT Lite session, you can automatically configure the SDRAM registers by selecting the Use XML reset values box on the Target Options dialog box, which is accessible through the Settings.
Using External Memory

The values for the EBU_SDGCTL, EBU_SDBCTL, and EBU_SDRRC registers have been set in the ADSP-BF561.xml file found in your VisualDSP\system folder under the RegReset tag. These values can be changed to be more optimal depending on the SCLK frequency. The values in Table 2-2 are programmed by default whenever Bank 0 is accessed through the debugger (for example, when viewing memory windows or loading a program). The numbers are derived for maximum flexibility and work for a system clock frequency between 60 MHz and 133 MHz.

Table 2-2. EZ-KIT Lite Session SDRAM Default Settings

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>EBU_SDGCTL</td>
<td>0x009199BD</td>
<td>Calculated with SCLK = 133 MHz1s</td>
</tr>
<tr>
<td>EBU_SDBCTL</td>
<td>0x00000013</td>
<td></td>
</tr>
<tr>
<td>EBU_SDRRC</td>
<td>0x000001CF</td>
<td>Calculated with SCLK = 120 MHz</td>
</tr>
</tbody>
</table>

The EBU_SDGCTL register can only be written once after the processor comes out of reset. Therefore, the user code should not reinitialize this register. Clearing the Use XML reset values checkbox allows manual configuration of the EBU registers. For more information, see “Target Options” on page 2-9.

Automatic configuration of the SDRAM is not optimized for a specific SCLK frequency. Table 2-3 shows the optimized configuration for the SDRAM registers using a 120 MHz SCLK. The frequency of 120 MHz is the maximum SCLK frequency when using a 600 MHz core frequency, the maximum frequency for the EZ-KIT Lite. Only the SDRRC register needs to be modified in the user code to achieve maximum performance.

Table 2-3. SDRAM Optimum Settings

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>EBU_SDGCTL</td>
<td>0x009199BD</td>
</tr>
</tbody>
</table>

1 Automatic configuration of SDRAM is not optimized for a specific SCLK frequency.
Table 2-3. SDRAM Optimum Settings\(^1\) (Cont’d)

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>EBIU_SDBCTL</td>
<td>0x00000013</td>
</tr>
<tr>
<td>EBIU_SDRRC</td>
<td>0x000003A0</td>
</tr>
</tbody>
</table>

\(^1\) SCLK = 120 MHz

For more information about the memory connection on the EZ-KIT Lite, see “External Bus Interface Unit” on page 3-3.

An example program is included in the EZ-KIT installation directory to demonstrate how to set up the SDRAM interface.

**Using LEDs and Push Buttons**

The EZ-KIT Lite provides four push buttons and sixteen LEDs for general-purpose IO.

Sixteen LEDs labeled LED5 through LED20 are controlled by the processor’s programmable flags PF32 through PF47 (equivalent to PPI0 D15-8 and PPI1 D15-8). These LEDs are accessed through the Flag 2 registers. First, the direction must be set to output by setting the bits of the FIO2_DIR register to “1”. Then the value of the LEDs can be modified using one the FIO2_FLAG_D, FIO2_FLAG_C, FIO2_FLAG_S, or FIO2_FLAG_T registers.

The four general-purpose push buttons are labeled SW6 through SW9. These are connected to the programmable flags, PF8-5. A status of each individual button can be read through the FIO0_FLAG_D register. When the corresponding bit of the register reads “1”, a switch is being pressed-on. When the switch is released, the bit reads “0”. A connection between the push button and PF input is established through the SW4 DIP switch. For information on how to disconnect the switch from the programmable flag and use the flag for something else, see “Push Button Enable Switch (SW4)”. 
Using Audio

An example program is included in the EZ-KIT installation directory to demonstrate the functionality of the LEDs and push buttons.

Using Audio

The AD1836A audio codec provides three channels of stereo audio output and two channels of multichannel 96 kHz input. The SPORT0 interface of the processor links with the stereo audio data input and output pins of the AD1836A codec. The processor is capable of transferring data to the audio codec in time-division multiplexed (TDM) or I²S mode.

The I²S mode allows the codec to operate with a 96 kHz sample rate but only allows you to use two channels of output. TDM mode can operate at a maximum of 48 kHz sample rate but allows simultaneous use of all input and output channels. When using I²S mode, the TSCLKO and RSCLK0 pins, as well as the TFS0 and RFS0 pins of the processor, must be tied together externally to the processor. This is accomplished with the SW4 DIP switch. See “Push Button Enable Switch (SW4)” on page 3-12 for more information.

The AD1836A audio codec’s internal configuration registers are configured using the processor’s PF4 programmable flag pin is used as the select for this device. For more information on how to configure the multichannel codec, download the datasheet from Analog Devices website, www.analog.com.

The AD1836A codec reset is controlled by the processor’s programmable flag PF15. When PF15 is “0”, the reset is asserted. When PF15 is “1”, the reset is de-asserted. Note, when PF15 is not driven (configured as input), the AD1836A reset is asserted due to the pull-down resistor. See “Programmable Flags” on page 3-4 for more information.

Example programs are included in the EZ-KIT installation directory to demonstrate the AD1836A codec operation.
Using Video

The board supports video input and output applications. The ADV7179 video encoder provides up to three output channels of analog video, while the ADV7183A video decoder provides up to three input channels of analog video. The video encoder connects to the Parallel Peripheral Interface 1 (PPI1), while the video decoder connects to the Parallel Peripheral Interface 0, (PPI0). Each PPI interface has an individual clock that is configured by the SW5 switch’s settings. See “PPI Clock Select Switch (SW5)” on page 3-13 for more information.

Both the encoder and the decoder connect to the Parallel Peripheral Interfaces (PPI input clock) of the ADSP-BF561 processor. For additional information on the video interface hardware, refer to “PPI Interfaces” on page 3-6.

For the video interface to be operational, the following basic steps must be performed.

1. Configure the SW2 DIP switch as required by the application. Refer to “Video Configuration Switch (SW2)” on page 3-10 for details.

2. De-assert the video device’s reset by setting a corresponding programmable flag “High”. Note that PF14 controls the ADV7179 encoder’s reset, while PF13 controls the ADV7183A decoder’s reset.

3. If using the decoder:
   - Enable device by driving programmable flag output PF2 to “0”.
   - Select PPI0 clock; for details, refer to “PPI Clock Select Switch (SW5)” on page 3-13.

4. Program internal registers of the video device in use. Both video encoder and decoder use a 2-wire serial interface to access internal registers. The PF0 programmable flag functions as a serial clock
Example Programs

(SCL), and PF1 functions as a serial data (SDAT).

5. Program the ADSP-BF561 processor’s PPI interfaces (configuration registers, DMA, and so on).

Example programs are included in the EZ-KIT installation directory to demonstrate the capabilities of the video interface.

Example Programs

Example programs are provided with the ADSP-BF561 EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in \...\VisualDSP\Blackfin\EZ-KITs\ADSP-BF561\Examples. Please refer to the readme file provided with each example for more information.

Using Background Telemetry Channel

The ADSP-BF561 USB debug agent supports the Background Telemetry Channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting DSP execution.

The BTC allows to view a variable as it is updated or changed, all while the processor continues to execute. For increased performance of the BTC, including faster reading and writing, please check out our latest line of DSP emulators at www.analog.com/Analog_ROOT/productPage/productHome/0,2121,EMULATORS,00.html. For more information about the Background Telemetry Channel, see the VisualDSP++ 3.5 User’s Guide for 16-Bit Processors or online Help.
Using EZ-KIT Lite VisualDSP++ Interface

This section provides information on the following parts of the VisualDSP++ graphical user interface:

- “Target Options” on page 2-9
- “Restricted Software Breakpoints” on page 2-12

Target Options

Choosing Target Options from the Settings menu opens the Target Options dialog box (Figure 2-2). Use target options to control certain aspects of the processor on the ADSP-BF561 EZ-KIT Lite evaluation system.

![Target Options Dialog Box](image)

Figure 2-2. Target Options Dialog Box

Reset Options

Reset options control how the processor behaves when a reset occurs. The reset options are described in Table 2-4.
Using EZ-KIT Lite VisualDSP++ Interface

Table 2-4. Reset Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core reset</td>
<td>Resets the core when the debugger executes a reset.</td>
</tr>
<tr>
<td>System reset</td>
<td>Resets the peripherals when the debugger executes a reset.</td>
</tr>
</tbody>
</table>

On Emulator Exit

This target option controls processor behavior when VisualDSP++ relinquishes DSP control (for example, when exiting VisualDSP++). The option is described in Table 2-5.

Table 2-5. On Emulator Exit Target Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>On Emulator Exit</td>
<td>Determines the state the DSP is left in when the board relinquishes control of the DSP:</td>
</tr>
<tr>
<td></td>
<td><strong>Reset DSP and Run</strong> causes the DSP to reset and begin execution from its reset vector location.</td>
</tr>
<tr>
<td></td>
<td><strong>Run from current PC</strong> causes the DSP to begin running from its current location.</td>
</tr>
<tr>
<td></td>
<td><strong>Stall the DSP</strong> resets the DSP and then writes a JUMP 0 to the first location in internal memory so the DSP is stuck in a tight loop after exiting.</td>
</tr>
</tbody>
</table>

XML File

These read-only fields show the version information for the processor-specific XML file, \VisualDSP\system\ADSP-BF561.xml, as well as the parser program (Table 2-6).

Table 2-6. XML File Information

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XML File Version</td>
<td>The version of the processor’s XML file.</td>
</tr>
<tr>
<td>XML Parser Version</td>
<td>The version of the program that parses the XML file.</td>
</tr>
</tbody>
</table>
Other Options

Table 2-7 describes other available target options.

Table 2-7. Miscellaneous Target Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset before loading executable</td>
<td>Resets registers before loading a DSP executable. Clear this option when DSP registers must not change to their reset values when a file load occurs.</td>
</tr>
<tr>
<td>Verify all writes to target memory</td>
<td>Validates all memory writes to the DSP. After each write, a read is performed and the values are checked for a matching condition. Enable this option during initial program development to locate and fix initial build problems (such as attempting to load data into non-existent memory). Clear this option to increase performance while loading executable files, since VisualDSP++ does not perform the extra reads that are required to verify each write.</td>
</tr>
<tr>
<td>Reset cycle counters on run</td>
<td>Resets the cycle count registers to zero before a Run command is issued. Select this option to count the number of cycles executed between breakpoints in a program.</td>
</tr>
<tr>
<td>Use opcode scan method</td>
<td>Enables the debugger to use a highly optimized JTAG scan method. This provides extremely fast communication between the EZ-KIT Lite and the processor. In certain circumstances, this causes JTAG scan failures. Typically, JTAG scan failures occur when using this method combined with debugging situations that hold off or stall the core (such as debugging, loading, or viewing external memory). Clearing this option uses a less optimized JTAG scan method.</td>
</tr>
<tr>
<td>Use XML reset values</td>
<td>Uses a section in the processor-specific XML file located in the VisualDSP/system folder. The file defines registers that are to be reset to certain values when a reset is done through VisualDSP++.</td>
</tr>
</tbody>
</table>
Using EZ-KIT Lite VisualDSP++ Interface

Restricted Software Breakpoints

The EZ-KIT Lite development system restricts breakpoint placement when certain conditions are met. That is, under some conditions, breakpoints cannot be placed effectively. Such conditions depend on bus architecture, pipeline depth, and ordering of the EZ-KIT Lite and its target processor.
This chapter describes the hardware design of the ADSP-BF561 EZ-KIT Lite board. The following topics are covered.

- **“System Architecture” on page 3-2**
  Describes the configuration of the ADSP-BF561EZ-KIT Lite and explains how the board components interface with the processor.

- **“Jumper and DIP Switch Settings” on page 3-10**
  Shows the location and describes the function of the configuration jumpers and DIP switches.

- **“LEDs and Push Buttons” on page 3-14**
  Shows the location and describes the function of the LEDs and push buttons.

- **“Connectors” on page 3-17**
  Shows the location and gives the part number for all of the connectors on the board. Also, the manufacturer and part number information is given for the mating parts.
System Architecture

This section describes the processor’s configuration on the EZ-KIT Lite board.

Figure 3-1. System Architecture

The EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-BF561 Blackfin processor. The processor has IO voltage of 3.3V. The core voltage and the core clock rate can be set on the fly by the processor. The input clock is 30 MHz.
External Bus Interface Unit

The External Bus Interface Unit (EBIU) connects an external memory to the ADSP-BF561 processor. It includes a 32-bit wide data bus, an address bus ($A_{25}$–$A_2$), and a control bus. All 8-bit, 16-bit, and 32-bit accesses are supported. On the EZ-KIT Lite board, the EBI unit is connected to SDRAM and Flash memory. For more information on using the external memory see “Using External Memory” on page 2-2.

All of the address, data, and control signals are available externally via the extender connectors ($J_3$–$J_1$). The pinout of these connectors can be found in Appendix B, “Schematics” on page B-1.

SPORT0 Audio Interface

The SPORT0 interface connects to the AD1836A audio codec, the SPORT connector ($P_3$), and the expansion interface. The AD1836A codec uses both the primary and secondary data transmit and receive pins to input and output data from the audio input and outputs.

The pinout of the SPORT connector and the expansion interface connectors can be found in Appendix B, “Schematics” on page B-1.

SPI Interface

The processor’s Serial Peripheral Interconnect (SPI) interface connects to the AD1836A audio codec and the expansion interface. The SPI connection to the AD1836A is used to access the control registers of the device. The $PF4$ flag of the processor acts as the devices select for the SPI port.

The SPI signals are available on the expansion interface. The pinout for the expansion interface can be found in Appendix B, “Schematics” on page B-1.
Programmable Flags

The processor has 48 programmable flag pins (PFs). Many of the flags have a multiple functionality, depending on the processor’s setup. Table 3-1 shows how the programmable flag pins are used on the EZ-KIT Lite.

Table 3-1. Programmable Flag Connections

<table>
<thead>
<tr>
<th>DSP PF Pin</th>
<th>DSP Function</th>
<th>EZ-KIT Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF0</td>
<td>SPI Select S, Timer 0</td>
<td>Serial clock for programming ADV7179 video encoder and ADV7183A video decoder.</td>
</tr>
<tr>
<td>PF1</td>
<td>SPI Select 1, Timer 1</td>
<td>Serial data for programming ADV7179 video encoder and ADV7183A video decoder.</td>
</tr>
<tr>
<td>PF2</td>
<td>SPI Select 2, Timer 2</td>
<td>ADV7183A video decoder’s −OE.</td>
</tr>
<tr>
<td>PF3</td>
<td>SPI Select 3, Timer 3</td>
<td>ADV7183A Field pin. See “Video Configuration Switch (SW2)” on page 3-10.</td>
</tr>
<tr>
<td>PF4</td>
<td>SPI Select 4, Timer 4</td>
<td>AD1836A audio codec’s SPI Select.</td>
</tr>
<tr>
<td>PF5</td>
<td>SPI Select 5, Timer 5</td>
<td>Push Button (SW6). See “Using LEDs and Push Buttons” on page 2-5 and “Push Button Enable Switch (SW4)” on page 3-12 for information on how to disable the push button.</td>
</tr>
<tr>
<td>PF6</td>
<td>SPI Select 6, Timer 6</td>
<td>Push Button (SW7). See “Using LEDs and Push Buttons” on page 2-5 and “Push Button Enable Switch (SW4)” on page 3-12 for information on how to disable the push button.</td>
</tr>
<tr>
<td>PF7</td>
<td>SPI Select 7, Timer 7</td>
<td>Push Button (SW8). See “Using LEDs and Push Buttons” on page 2-5 and “Push Button Enable Switch (SW4)” on page 3-12 for information on how to disable the push button.</td>
</tr>
<tr>
<td>PF8</td>
<td></td>
<td>Push Button (SW9). See “Using LEDs and Push Buttons” on page 2-5 and “Push Button Enable Switch (SW4)” on page 3-12 for information on how to disable the push button.</td>
</tr>
<tr>
<td>PF9-PF12</td>
<td></td>
<td>Not used</td>
</tr>
</tbody>
</table>
Table 3-1. Programmable Flag Connections  (Cont’d)

<table>
<thead>
<tr>
<th>DSP PF Pin</th>
<th>DSP Function</th>
<th>EZ-KIT Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF13</td>
<td>ADV7183A video decoder’s reset</td>
<td></td>
</tr>
<tr>
<td>PF14</td>
<td>ADV7179 video encoder’s reset</td>
<td></td>
</tr>
<tr>
<td>PF15</td>
<td>AD1836 codec’s reset</td>
<td></td>
</tr>
<tr>
<td>PF16</td>
<td>Sport 0 Transmit Frame Sync</td>
<td></td>
</tr>
<tr>
<td>PF17</td>
<td>Sport 0 Transmit Data Secondary</td>
<td></td>
</tr>
<tr>
<td>PF18</td>
<td>Sport 0 Transmit Data Primary</td>
<td></td>
</tr>
<tr>
<td>PF19</td>
<td>Sport 0 Receive Frame Sync</td>
<td></td>
</tr>
<tr>
<td>PF20</td>
<td>Sport 0 Receive Data Secondary</td>
<td></td>
</tr>
<tr>
<td>PF21</td>
<td>Sport 1 Transmit Frame</td>
<td></td>
</tr>
<tr>
<td>PF22</td>
<td>Sport 1 Transmit Data Secondary</td>
<td></td>
</tr>
<tr>
<td>PF23</td>
<td>Sport 1 Transmit Data Primary</td>
<td></td>
</tr>
<tr>
<td>PF24</td>
<td>Sport 1 Receive Frame Sync</td>
<td></td>
</tr>
<tr>
<td>PF25</td>
<td>Sport 1 Receive Data Secondary</td>
<td></td>
</tr>
<tr>
<td>PF26</td>
<td>UART Transmit</td>
<td></td>
</tr>
<tr>
<td>PF27</td>
<td>UART Receive</td>
<td></td>
</tr>
<tr>
<td>PF28</td>
<td>Sport 0 Receive Serial Clock</td>
<td></td>
</tr>
<tr>
<td>PF29</td>
<td>Sport 0 Transmit Serial Clock</td>
<td></td>
</tr>
<tr>
<td>PF30</td>
<td>Sport 1 Receive Serial Clock</td>
<td></td>
</tr>
<tr>
<td>PF31</td>
<td>Sport 1 Transmit Serial Clock</td>
<td></td>
</tr>
<tr>
<td>PF39-32</td>
<td>PP11 data 15-8</td>
<td>LED20-13</td>
</tr>
<tr>
<td>PF47-40</td>
<td>PP10 data 15-8</td>
<td>LED12-5</td>
</tr>
</tbody>
</table>
PPI Interfaces

The ADSP-BF561 processor employs two independent Parallel Peripheral Interfaces (PPIs), PPI0 and PPI1. Each PPI interface is a half-duplex, bi-directional bus consisting of 16 bits of data, a dedicated input clock, and synchronization signals. The ADSP-BF561 EZ-KIT Lite board utilizes the PPI interfaces for video input and video output.

The PPI0 interface is configured to input video data from the ADV7183A video decoder device: bits 7-0 connect to the video decoder’s data outputs. The PPI1 interface is configured to output video data to the ADV7179 video encoder device: bits 7-0 connect to the video encoder’s data inputs.

Each PPI interface has a dedicated clock input configured independently by the SW5 switch. The clock source can be one of the following: 27 MHz crystal oscillator, ADV7183A video decoder’s clock output, or external clock from the expansion interface. See “PPI Clock Select Switch (SW5)” on page 3-13 for more information about the switch.

The SW2 switch allows flexible connectivity between dedicated synchronization IOs (SYNC1 and SYNC2 of each PPI interface) and the encoder’s and decoder’s horizontal and vertical synchronization pins. See “Video Configuration Switch (SW2)” on page 3-10 for more information about the switch. For a detailed description of the ADSP-BF561 processor’s PPI interfaces, refer to the ADSP-BF561 Blackfin Processor Hardware Reference.

Table 3-2 describes the PPI pins and their use on the EZ-KIT Lite board.

<table>
<thead>
<tr>
<th>DSP PPI Pin</th>
<th>Other DSP Function</th>
<th>EZ-KIT Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI0 bits 7-0</td>
<td>ADV7183A data outputs P15-8</td>
<td></td>
</tr>
<tr>
<td>PPI1 bits 7-0</td>
<td>ADV7179 data inputs P7-0</td>
<td></td>
</tr>
</tbody>
</table>
| PPI0 SYNC1 | Timer 8 | ADV7179 HSYNC. For more information, see “Video Configuration Switch (SW2)” on page 3-10.
Video Output (PPI1)

The PPI1 interface is configured as output and connects to the on-board video encoder device, ADV7179. The ADV7179 encoder generates three analog video channels on DAC A, DAC B, and DAC C. The PPI1 bits 7–0 connect to P7–0 of the encoder’s pixel inputs. The encoder’s input clock is fixed and comes from an on-board 27 MHz oscillator.

The encoder’s synchronization signals, HSYNC and VSYNC, can be configured as inputs or outputs. Video Blanking control signal is at level “1”. The HSYNC and VSYNC signals can connect to the ADSP-BF561 processor’s PPI1 interface SYNC1 and SYNC2 via the SW2 switch, as described in “Video Configuration Switch (SW2)” on page 3-10.

Table 3-2. PPI Connections (Cont’d)

<table>
<thead>
<tr>
<th>DSP PPI Pin</th>
<th>Other DSP Function</th>
<th>EZ-KIT Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI 0 SYNC2</td>
<td>Timer 9</td>
<td>ADV7179 VSYNC. For more information, see “Video Configuration Switch (SW2)” on page 3-10.</td>
</tr>
<tr>
<td>PPI 0 Clock</td>
<td></td>
<td>A choice of ADV7183A output clock, a local 27 MHz oscillator, or an external clock from ADSP-BF533/BF561 EZ-KIT Extender 1 board.</td>
</tr>
<tr>
<td>PPI 1 SYNC1</td>
<td>Timer 10</td>
<td>ADV7183A HSYNC. For more information, see “Video Configuration Switch (SW2)” on page 3-10.</td>
</tr>
<tr>
<td>PPI 1 SYNC2</td>
<td>Timer 11</td>
<td>ADV7183A VSYNC. For more information, see “Video Configuration Switch (SW2)” on page 3-10.</td>
</tr>
<tr>
<td>PPI 1 Clock</td>
<td></td>
<td>A choice of ADV7183A output clock, a local 27 MHz oscillator, or an external clock from ADSP-BF53x/BF561 EZ-Extender 1.</td>
</tr>
</tbody>
</table>
System Architecture

Video Input (PPI0)

The PPI0 interface is configured as input and connect to the on-board video decoder device, ADV7183A. The ADV7183A decoder receives three analog video channels on AIN1, AIN4, and AIN5 input. The decoder’s pixel data outputs P15–8 drive the PPI0 inputs 8–0. The decoder’s 27 MHz pixel clock output can be selected to drive any of the PPI clocks, as shown in Table 3-7 on page 3-13.

Synchronization outputs of the decoder, HS/HACTIVE, VS/VACTIVE, and FIELD can connect to the processor’s PPI1 SYNC1, SYNC2, and PF3 flag via the SW2 DIP switch, as described in “Video Configuration Switch (SW2)” on page 3-10.

UART Port

The processor’s Universal Asynchronous Receiver/Transmitter (UART) port connects to the ADM3202 RS232 line driver as well as to the expansion interface. The RS232 line driver is attached to the DB9 male connector, allowing you to interface with a PC or other serial device.

Expansion Interface

The expansion interface consists of the three 90-pin connectors, J3–1. Table 3-3 shows the interfaces each connector provides. For the exact pinout of these connectors, refer to Appendix B, “Schematics” on page B-1. The mechanical dimensions of the connectors can be obtained from Technical or Customer Support.
Limits to the current and to the interface speed must be taken into consideration when you use the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

⚠️ Analog Devices does not support and is not responsible for the effects of additional circuitry.

### JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor’s internal and external memory through a 6-pin interface. The JTAG emulation port of the processor also connects to the USB debugging interface. When an emulator connects to the board at P4, the USB debugging interface is disabled. See “JTAG (P4)” on page 3-20 for more information about the JTAG connector.

To learn more about available emulators, contact Analog Devices (see “Product Information”).

<table>
<thead>
<tr>
<th>Connector</th>
<th>Interfaces</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>5V, GND, Address, Data, PPI0 3–0, PF15–6, PF4</td>
</tr>
<tr>
<td>J2</td>
<td>3.3V, GND, SPI, NMI, PPI0 SYNC3–1, SPORT0, SPORT1, PF15–0, EBU1 control signals</td>
</tr>
<tr>
<td>J3</td>
<td>5V, 3.3V, GND, UART, PPI1 15–0, Reset, Video control signals</td>
</tr>
</tbody>
</table>
Jumper and DIP Switch Settings

This section describes the operation of the jumpers and DIP switches. The jumper and DIP switch locations are shown in Figure 3-2.

Figure 3-2. DIP Switch Locations

Video Configuration Switch (SW2)

The video configuration switch (SW2) controls how some video signals from the ADV7183A video decoder and ADV7179 video encoder are routed to the processor’s PPIs. The switch also determines if the PF2 pin controls the $\sim OE$ signal of the ADV7183A video decoder outputs. Table 3-4 shows which processor’s signals are connected to the encoder and decoder when in the “ON” position.
Table 3-4. Video Configuration Switch (SW2)

<table>
<thead>
<tr>
<th>Switch Position (Default)</th>
<th>Processor Signal</th>
<th>Video Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (OFF)</td>
<td>PPI1 SYNC1</td>
<td>ADV7179</td>
</tr>
<tr>
<td>2 (OFF)</td>
<td>PPI0 SYNC1</td>
<td>ADV7183A</td>
</tr>
<tr>
<td>3 (OFF)</td>
<td>PPI1 SYNC2</td>
<td>ADV7183A</td>
</tr>
<tr>
<td>4 (OFF)</td>
<td>PPI1 SYNC2</td>
<td>ADV7179</td>
</tr>
<tr>
<td>5 (OFF)</td>
<td>PF3 (FIELD)</td>
<td>ADV7183A</td>
</tr>
<tr>
<td>6 (ON)</td>
<td>PF2</td>
<td>ADV7183A</td>
</tr>
</tbody>
</table>

Positions 1 through 5 of SW2 determine how and if the SYNC1, SYNC2, and FIELD control signals of the PPI0 and PPI1 interfaces are routed to the processor’s PPIs. In standard configuration of the encoder and decoder, this is not necessary because the processor is capable of reading the embedded control information, which is in the data stream.

Position 6 of SW2 determines whether PF2 connects to the ~OE signal of the ADV7183A. When the switch is “OFF”, PF2 can be used for other operations, and the decoder output enable is held “HIGH” with a pull-up resistor.

**Boot Mode Switch (SW3)**

The SW3 switch positions 1 and 2 set the ADSP-BF561 processor’s boot mode as described in Table 3-5. Position 3 sets the processor’s PLL on boot. When SW3 position 3 is “ON”, the PLL is in bypass.

Table 3-5. Boot Mode Select Switch (SW3)

<table>
<thead>
<tr>
<th>Position 1 BMODE0</th>
<th>Position 2 BMODE1</th>
<th>Boot Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>ON</td>
<td>Reserved</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>Flash memory</td>
</tr>
</tbody>
</table>
Jumper and DIP Switch Settings

Table 3-6. Push Button Enable Switch (SW4)

<table>
<thead>
<tr>
<th>Switch Position</th>
<th>Default Setting</th>
<th>Pin #</th>
<th>Signal (Side 1)</th>
<th>Pin #</th>
<th>Signal (Side 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ON</td>
<td>1</td>
<td>SW6</td>
<td>12</td>
<td>PF5</td>
</tr>
<tr>
<td>2</td>
<td>ON</td>
<td>2</td>
<td>SW7</td>
<td>11</td>
<td>PF6</td>
</tr>
<tr>
<td>3</td>
<td>ON</td>
<td>3</td>
<td>SW8</td>
<td>10</td>
<td>PF7</td>
</tr>
<tr>
<td>4</td>
<td>ON</td>
<td>4</td>
<td>SW9</td>
<td>9</td>
<td>PF8</td>
</tr>
<tr>
<td>5</td>
<td>OFF</td>
<td>5</td>
<td>TFS0</td>
<td>8</td>
<td>RFS0</td>
</tr>
<tr>
<td>6</td>
<td>OFF</td>
<td>6</td>
<td>RSLCK0</td>
<td>7</td>
<td>TSCLKO</td>
</tr>
</tbody>
</table>

The push button enable switch (SW4) positions 1 through 4 allow to disconnect the drivers associated with the push buttons from the PF pins of the processor. Positions 5 and 6 connect the transmit and receive frame syncs and clocks of SPORT0. This is important when the AD1836A video decoder and the processor are communicating in I²S mode. Table 3-6 shows which PF is driven when the switch is in the “ON” position.
PPI Clock Select Switch (SW5)

The SW5 switch controls a clock selection of PPI interfaces, as described in Table 3-7 and Table 3-8.

Table 3-7. PPICLK1 Clock Source Setup

<table>
<thead>
<tr>
<th>SW5 Position 1</th>
<th>SW5 Position 2</th>
<th>PPICLK1 Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI0_CKSEL0</td>
<td>PPI0_CKSEL1</td>
<td></td>
</tr>
<tr>
<td><strong>ON</strong></td>
<td><strong>ON</strong></td>
<td>27 MHz Oscillator (default)</td>
</tr>
<tr>
<td><strong>OFF</strong></td>
<td><strong>ON</strong></td>
<td>ADV7183 Clock Out</td>
</tr>
<tr>
<td><strong>X</strong></td>
<td><strong>OFF</strong></td>
<td>Expansion Interface</td>
</tr>
</tbody>
</table>

Table 3-8. PPICLK2 Clock Source Setup

<table>
<thead>
<tr>
<th>SW5 Position 3</th>
<th>SW5 Position 4</th>
<th>PPICLK2 Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI1_CKSEL0</td>
<td>PPI1_CKSEL1</td>
<td></td>
</tr>
<tr>
<td><strong>ON</strong></td>
<td><strong>ON</strong></td>
<td>27 MHz Oscillator (default)</td>
</tr>
<tr>
<td><strong>OFF</strong></td>
<td><strong>ON</strong></td>
<td>ADV7183 Clock Out</td>
</tr>
<tr>
<td><strong>X</strong></td>
<td><strong>OFF</strong></td>
<td>Expansion Interface</td>
</tr>
</tbody>
</table>

Test DIP Switches (SW10, SW11)

Two DIP switches (SW10 and SW11) are located on the bottom of the board. The switches are used only for testing and should be in the “OFF” position.
LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 3-3 shows the locations of the LEDs and push buttons on the board.

Figure 3-3. LED and Push Button Locations

Reset Push Button (SW1)

The reset push button resets all of the ICs on the board. One exception is the USB interface chip (U34). The chip is not being reset when the push button is pressed after the USB cable has been plugged in and communication with the PC has been initialized correctly. Once communication is initialized, the only way to reset the USB is by powering down the board.
Programmable Flag Push Buttons (SW9–6)

Four push buttons, SW9–6, are provided for general-purpose user input. The buttons connect to the processor’s programmable flag pins PF8–5. The push buttons are active “HIGH” and, when pressed, send a High (1) to the processor. Refer to “Using LEDs and Push Buttons” on page 2-5 for more information on how to use the PFs when programming the processor. The push button enable switch (SW4) is capable of disconnecting the push buttons from the PF (refer to “Push Button Enable Switch (SW4)” on page 3-12). The programmable flag signals and their corresponding switches are shown in Table 3-9.

Table 3-9. Programmable Flag Switches

<table>
<thead>
<tr>
<th>DSP Programmable Flag Pin</th>
<th>Push Button Reference Designator</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF5</td>
<td>SW6</td>
</tr>
<tr>
<td>PF6</td>
<td>SW7</td>
</tr>
<tr>
<td>PF7</td>
<td>SW8</td>
</tr>
<tr>
<td>PF8</td>
<td>SW9</td>
</tr>
</tbody>
</table>

Power LED (J7)

When J7 is lit (green), it indicates that power is being properly supplied to the board.

Reset LEDs (LED2, LED3)

When LED2 is lit, it indicates that the master reset of all the major ICs is active. When LED3 is lit, the USB interface chip (U34) is being reset. The USB chips only reset on power-up, or if USB communication has not been initialized.
LEDs and Push Buttons

USB Monitor LED (LED4)

The USB monitor LED (LED4) indicates that USB communication has been initialized successfully and you may connect to the processor using a VisualDSP++ EZ-KIT Lite session. This should take approximately 15 seconds. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver (see “Installing EZ-KIT Lite USB Driver” on page 1-7).

User LEDs (LED12–5, LED20–13)

Sixteen LEDs are connected to the ADSP-BF561 processor’s programmable flags. Eight LEDs labeled LED5 through LED12 are controlled by programmable flags PF40 through PF47 (equivalent to PPI0 D15–8). Eight LEDs labeled LED13 through LED20 are controlled by programmable flags PF32 through PF39 (equivalent to PPI1 D15–8). To learn how to use the Flash memory when programming the LEDs, refer to “Using LEDs and Push Buttons” on page 2-5.

Table 3-10. User LEDs

<table>
<thead>
<tr>
<th>LED Reference Designator</th>
<th>Flash Port Name</th>
<th>LED Reference Designator</th>
<th>Flash Port Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED5</td>
<td>PB40</td>
<td>LED13</td>
<td>PB32</td>
</tr>
<tr>
<td>LED6</td>
<td>PB41</td>
<td>LED14</td>
<td>PB33</td>
</tr>
<tr>
<td>LED7</td>
<td>PB42</td>
<td>LED15</td>
<td>PB34</td>
</tr>
<tr>
<td>LED8</td>
<td>PB43</td>
<td>LED16</td>
<td>PB35</td>
</tr>
<tr>
<td>LED9</td>
<td>PB44</td>
<td>LED17</td>
<td>PB36</td>
</tr>
<tr>
<td>LED10</td>
<td>PB45</td>
<td>LED18</td>
<td>PB37</td>
</tr>
<tr>
<td>LED11</td>
<td>PB46</td>
<td>LED19</td>
<td>PB38</td>
</tr>
<tr>
<td>LED12</td>
<td>PB47</td>
<td>LED20</td>
<td>PB39</td>
</tr>
</tbody>
</table>
Connectors

This section describes the connector functionality and provides information about mating connectors. The locations of the connectors are shown in Figure 3-4.

![Figure 3-4. Connector Locations](image)

**Expansion Interface (J1, J2, J3)**

Three board-to-board connector footprints provide signals for most of the processor’s peripheral interfaces. The connectors are located at the bottom of the board. For more information about the expansion interface, see on page 3-8. For the availability and pricing of the J1, J2, and J3 connectors, contact Samtec.
Connectors

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>90 Position 0.05” Spacing, SMT (J1, J2, J3)</td>
<td>Samtec</td>
<td>SFC-145-T2-F-D-A</td>
</tr>
</tbody>
</table>

Mating Connector

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>90 Position 0.05” Spacing (Through Hole)</td>
<td>Samtec</td>
<td>TFM-145-x1 Series</td>
</tr>
<tr>
<td>90 Position 0.05” Spacing (Surface Mount)</td>
<td>Samtec</td>
<td>TFM-145-x2 Series</td>
</tr>
<tr>
<td>90 Position 0.05” Spacing (Low Cost)</td>
<td>Samtec</td>
<td>TFC-145 Series</td>
</tr>
</tbody>
</table>

Audio (J4, J5)

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>2x2 RCA Jacks (J4)</td>
<td>SWITCHCRAFT</td>
<td>PJRAS2X2S01</td>
</tr>
<tr>
<td>3x2 RCA Jacks (J5)</td>
<td>SWITCHCRAFT</td>
<td>PJRAS3X2S01</td>
</tr>
</tbody>
</table>

Mating Connector

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two channel RCA interconnect cable</td>
<td>Monster Cable</td>
<td>BI100-1M</td>
</tr>
</tbody>
</table>

Video (J6)

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>3x2 RCA Jacks (J6)</td>
<td>SWITCHCRAFT</td>
<td>PJRAS3X2S01</td>
</tr>
</tbody>
</table>

Power (J7)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board. The power connector supplies DC power to the board. The following table shows the power connector pinout.
The power connector supplies DC power to the EZ-KIT Lite board. Table 3-11 shows the power supply specifications.

Table 3-11. Power Supply Specification

<table>
<thead>
<tr>
<th>Terminal</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center pin</td>
<td>+7.5 VDC@3Amps</td>
</tr>
<tr>
<td>Outer Ring</td>
<td>GND</td>
</tr>
</tbody>
</table>

**USB (J8)**

The USB connector is a standard Type B USB receptacle.
Connectors

**RS232 (P2)**

The RS232-compatible connector is described in Table 3-12.

Table 3-12. RS232 Connector

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB9, Male, Right Angle (P2)</td>
<td>Digi-Key</td>
<td>A2096-ND</td>
</tr>
<tr>
<td>Mating Assembly</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2m Female to Female cable</td>
<td>Digi-Key</td>
<td>AE1016-ND</td>
</tr>
</tbody>
</table>

**SPORT0 (P3)**

The SPORT0 connector is linked to a 20-pin connector. The connector’s pinout can be found in “Schematics” on page B-1. For pricing and availability of the connectors, contact AMP.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>20-position AMPMODU system 50 receptacle (P3)</td>
<td>AMP</td>
<td>104069-1</td>
</tr>
<tr>
<td>Mating Connectors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20-position ribbon cable connector</td>
<td>AMP</td>
<td>111196-4</td>
</tr>
<tr>
<td>20-position AMPMODU system 20 connector</td>
<td>AMP</td>
<td>2-487937-0</td>
</tr>
<tr>
<td>20-position AMPMODU system 20 connector (w/o lock)</td>
<td>AMP</td>
<td>2-487938-0</td>
</tr>
<tr>
<td>Flexible film contacts (20 per connector)</td>
<td>AMP</td>
<td>487547-1</td>
</tr>
</tbody>
</table>

**JTAG (P4)**

The JTAG header is the connecting point for a JTAG in-circuit emulator
pod. When an emulator is connected to the JTAG header, the USB debug interface is disabled.

- Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

- When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.
## A BILL OF MATERIALS

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Reference Design</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10MHZSMT OSC003 3V</td>
<td>U35</td>
<td>RALTRON</td>
<td>C04310-10.00</td>
</tr>
<tr>
<td>2</td>
<td>74LVC14A SOIC14</td>
<td>U47</td>
<td>TI</td>
<td>74LVC14AD</td>
</tr>
<tr>
<td>3</td>
<td>IDT74FCT3244APY SSOP20</td>
<td>U13, U30</td>
<td>IDT</td>
<td>IDT74FCT3244APY</td>
</tr>
<tr>
<td>4</td>
<td>CY7C64603-128 PQFP128</td>
<td>U45</td>
<td>CYPRESS</td>
<td>CY7C64603-128NC</td>
</tr>
<tr>
<td>5</td>
<td>MMBT4401 SOT-23</td>
<td>Q1</td>
<td>FAIRCHILD</td>
<td>MMBT4401</td>
</tr>
<tr>
<td>6</td>
<td>ADP3331ART SOT23-6</td>
<td>VR7</td>
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<td>R125-130</td>
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<td>CT25-28</td>
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SW11: Video Loopback
For Test Purposes
Default = All Off
Note: Signal Names in brackets refer to ADV7183KST

SW2: Video Sync Signals and Encoder Enable Select
Default = OFF, OFF, OFF, OFF, OFF, ON

ON = PF2 used to enable or disable the encoder digital interface
OFF = Encoder digital interface always disabled

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<td>6</td>
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**ADSP-BF561 EZ-KIT LITE: RESET, PUSH-BUTTON SWITCHES, UART**

**Position**  
1-4 Connects the push buttons to the Programmable Flags of the DSP. Useful if using the PFs for another purpose.

5-6 OFF, OFF = AD1836A -> TDM Mode  
ON, ON = AD1836A -> I2S Mode

**NOTE:** Remove R192 when populating R191 and R184
NOTE: R252 or R253 gets populated
Default is R252 IN and R253 OUT
All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com.
ADSP-BF561 EZ-KIT Lite
Schematic
SW11: Video Loopback
For Test Purposes
Default = All Off

1.3A
PH: 1-800-ANALOGD
Nashua, NH 03063
20 Cotton Road

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD
VIDEO DECODER

Note: Signal Names in brackets refer to ADV7183KST
NOTE: Remove R192 when populating R191 and R184

SW4 PB Enable Switch
Default = ON, ON, ON, OFF, OFF, OFF

Position | Function
--- | ---
1-4 | Connects the push buttons to the Programmable Flags of the DSP
5-6 | OFF, OFF = AD1836A -> TDM Mode
ON, ON = AD1836A -> I2S Mode

PH: 1-800-ANALOGD
Nashua, NH 03063
20 Cotton Road

Approvals | Date | Title
--- | --- | ---
Drawn | JSZ | 10/10/03 | ADSP-BF561 EZ-KIT LITE: USB, RESET, PUSH-BUTTON SWITCHES, UART
Checked | | | Board No. A0185-2003
Engineering | | Date 12-16-2003 11:24 | Sheet 11 of 18

Rev 1.3A
All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com.
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