ADSP-BF535 EZ-KIT Lite®
Evaluation System Manual

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Analog Devices, Inc.
One Technology Way
Norwood, Mass. 02062-9106

ANALOG DEVICES

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The ADSP-BF535 EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the “CE” mark.

The ADSP-BF535 EZ-KIT Lite evaluation system had been appended to the Technical Construction File referenced “DSPTOOLS1” dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body as listed below.

Technical Certificate No: Z600ANA1.007

Issued by: Technology International (Europe) Limited
41 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TZ, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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PREFACE

Thank you for purchasing the ADSP-BF535 EZ-KIT Lite®, Analog Devices (ADI) evaluation system for Blackfin® embedded media processors.

The Blackfin processors are embedded processors that support a Media Instruction Set Computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics towards delivering signal processing performance in a microprocessor-like environment.

The evaluation board is designed to be used in conjunction with the VisualDSP++™ development environment to test the capabilities of the ADSP-BF535 (formerly ADSP-21535) Blackfin processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C and ADSP-BF535 assembly
- Load, run, step, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF535 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF535 processor and the

evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and DSP development tools, go to `http://www.analog.com/dsp/tools/`.

ADSP-BF535 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The VisualDSP++ license provided with this EZ-KIT Lite evaluation system limits the size of a user program to 176 KB of internal memory.

The board's features include:

- Analog Devices ADSP-BF535 processor
  - 300 MHz Core Clock Speed (default)
  - Switch-Configurable Core Clock Speed
  - Switch-Configurable Boot Mode
- USB Debugging Interface

This is not the DSP's USB interface.

- Analog Devices AD1885 48 kHz AC'97 SoundMAX® Codec
  - Jumper-Selectable Line-In or Mic-In 3.5 mm Stereo Jack
  - Line-Out 3.5 mm Stereo Jack
- SDRAM
  - 4 M x 32-bit
- Flash Memory
  - 272 K x 16

- Interface Connectors
  - 14-Pin Emulator Connector for JTAG Interface
  - SPORT0 Connector
  - FlashLINK™ Connector (for Flash memory programming)
  - Expansion Interface Connectors (not populated)
- General-Purpose IO
  - 4 Push Buttons connected to DSP Programmable Flags
  - 1 Push Button connected to DSP Non-maskable Interrupt
  - 4 LEDs connected to DSP Programmable Flags
- Real Time Clock
- Analog Devices ADP3331, ADP3338, ADP3339, and ADP3088 Voltage Regulators

The EZ-KIT Lite board has a Flash memory device that can be used to store user specific boot code. By configuring the boot mode switch (SW1) and by programming the Flash memory, the board can run as a stand-alone unit. For information about using the Flash memory, see "Using Flash Memory" on page 2-5.

SPORT0 is interfaced with an audio codec, allowing you to create audio signal processing applications. SPORT0 is also attached to an off-board connector to allow communication with other serial devices. For information about SPORT0, see "SPORT0 Audio Interface" on page 3-3.

Additionally, the EZ-KIT Lite board provides access to most of the processor's peripheral ports. Access is provided in the form of uninstalled expansion interface connectors. The processor's USB pins are brought to the P3 connector but require additional circuitry to function as a USB port. The PCI bus of the DSP is not available at any connector of the EZ-Kit Lite. For information about the expansion interface, see "Expansion Interface" on page 3-4.

Purpose of This Manual

The *ADSP-BF535 EZ-KIT Lite Evaluation System Manual* provides instructions for using the hardware and installing the software on your PC. This manual provides guidelines for running your own code on the ADSP-BF535 EZ-KIT Lite. The manual also describes the operation and configuration of the evaluation board's components. Finally, a schematic and a bill of materials are provided as a reference for future ADSP-BF535 board designs.

Intended Audience

This manual is a user's guide and reference to the ADSP-BF535 EZ-KIT Lite evaluation system. Programmers who are familiar with the Analog Devices Blackfin processor architecture, operation, and programming are the primary audience for this manual.

Programmers who are unfamiliar with Analog Devices Blackfin processors can use this manual in conjunction with the *ADSP-BF535 DSP Hardware Reference* and the *Blackfin Processor Instruction Set Reference*, which describe the processor architecture and instruction set. Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and the VisualDSP++ user's or getting started guides. For the locations of these documents, refer to "Related Documents".

Manual Contents

The manual consists of:

- Chapter 2, “Getting Started” on page 1-1

  Provides software and hardware installation procedures, PC system requirements, and basic board information.

- Chapter 2, “Using EZ-KIT Lite” on page 2-1

  Provides information on the EZ-KIT Lite from a programmer’s perspective and provides an easy-to-access memory map.

- Chapter 3, “EZ-KIT Lite Hardware Reference” on page 3-1

  Provides information on the hardware aspects of the evaluation system.

- Appendix A, “Bill Of Materials” on page A-1

  Provides a list of components used to manufacture the EZ-KIT Lite board.

- Appendix B, “Schematics” on page B-1

  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.

  This appendix is not part of the online Help. The online Help viewers should go the PDF version of the *ADSP-BF535 EZ-KIT Lite Evaluation System Manual* located in the `Docs\EZ-KIT Lite Manuals` folder on the installation CD to see the schematics.

What's New in This Manual

This is the third revision of the *ADSP-BF535 EZ-KIT Lite Evaluation System Manual*. The manual provides an updated listing of related documents.

Technical or Customer Support

You can reach DSP Tools Support in the following ways.

- Visit the DSP Development Tools website at

  `www.analog.com/technology/dsp/developmentTools/index.html`

- Email questions to

  `dsptools.support@analog.com`

- Phone questions to 1-800-ANALOGD
- Contact your ADI local sales office or authorized distributor
- Send questions by mail to

  ```
  Analog Devices, Inc.
  DSP Division
  One Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA
  ```

Supported Processors

The ADSP-BF535 EZ-KIT Lite evaluation system supports ADSP-BF535 (formerly ADSP-21535) Blackfin Analog Devices embedded processors.

Product Information

You can obtain product information from the Analog Devices website, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at www.analog.com. Our website provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

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If you are already a registered user, just log on. Your user name is your email address.

DSP Product Information

For information on digital signal processors, visit our website at www.analog.com/dsp, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- Email questions or requests for information to `dsp.support@analog.com`
- Fax questions or requests for information to 1-781-461-3010 (North America) or +49 (0) 89 76903-157 (Europe)

Related Documents

For information on product related development software, see the following publications.

Table 1. Related DSP Publications

Title	Description
ADSP-BF535 Embedded Processor Datasheet	General functional description, pin-out, and timing.
ADSP-BF535 Blackfin Processor Hardware Reference	Description of internal processor architecture and all register functions.
Blackfin Processor Instruction Set Reference	Description of all allowed processor assembly instructions.

Table 2. Related VisualDSP++ Publications

Title	Description
VisualDSP++ 3.5 User's Guide for 16-Bit Processors	Detailed description of VisualDSP++ 3.5 features and usage.
VisualDSP++ 3.5 Assembler and Preprocessor Manual for Blackfin Processors	Description of the assembler function and commands for Blackfin processors.
VisualDSP++ 3.5 C/C++ Complier and Library Manual for Blackfin Processors	Description of the complier function and commands for Blackfin processors

Table 2. Related VisualDSP++ Publications (Cont'd)

Title	Description
VisualDSP++ 3.5 Linker & Utilities Manual for 16-Bit Processors	Description of the linker function and commands for 16-bit processors.
VisualDSP++ 3.5 Loader Manual for 16-Bit Processors	Description of the loader/splitter function and commands for 16-bit processors.

The listed documents can be found through online Help or in the `Docs` folder of your VisualDSP++ installation. Most documents are available in printed form.

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, refer to the documentation that accompanies the emulator.

Online Documentation

Your software installation kit includes online Help as part of the Windows® interface. These help files provide information about VisualDSP++ and the ADSP-BF535 EZ-KIT Lite evaluation system.

To view VisualDSP++ Help, click on the Help menu item or go to the Windows task bar and select Start -->Programs -->VisualDSP -->VisualDSP++ Documentation.

To view ADSP-BF535 EZ-KIT Lite Help, which now is a part of the VisualDSP++ Help system, go the Contents tab of the Help window and select Manuals --> ADSP-BF535 EZ-KIT Lite.

For more documentation, please go to
`http://www.analog.com/technology/dsp/library.html`.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at 1-800-ANALOGD (1-800-262-5643) and follow the prompts.

VisualDSP++ Documentation Set

Printed copies of VisualDSP++ manuals may be purchased through Analog Devices Customer Service at 1-781-329-4700; ask for a Customer Service representative. The manuals can be purchased only as a kit. For additional information, call 1-603-883-2430.

If you do not have an account with Analog Devices, you will be referred to Analog Devices distributors. To get information on our distributors, log onto `www.analog.com/salesdir/continent.asp`.

Hardware Manuals

Printed copies of hardware reference and instruction set reference manuals can be ordered through the Literature Center or downloaded from the Analog Devices website. The phone number is 1-800-ANALOGD (1-800-262-5643). The manuals can be ordered by a title or by product number located on the back cover of each manual.

Data Sheets

All data sheets can be downloaded from the Analog Devices website. As a general rule, printed copies of data sheets with a letter suffix (L, M, N, S) can be obtained from the Literature Center at 1-800-ANALOGD (1-800-262-5643) or downloaded from the website. Data sheets without the suffix can be downloaded from the website only—no hard copies are available. You can ask for the data sheet by part name or by product number.

If you want to have a data sheet faxed to you, the phone number for that service is 1-800-446-6212. Follow the prompts and a list of data sheet code numbers will be faxed to you. Call the Literature Center first to find out if requested data sheets are available.

Contacting DSP Publications

Please send your comments and recommendations on how to improve our manuals and online Help. You can contact us at `dsp.techpubs@analog.com`.

Notation Conventions

The following table identifies and describes text conventions used in this manual.

Additional conventions, which apply only to specific chapters, may appear throughout this document.

Example	Description
Close command (File menu) or OK	Text in bold style indicates the location of an item within the VisualDSP++ environment's and boards' menu system and user interface items.
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets separated by vertical bars; read the example as `this` or `that`.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipsis; read the example as an optional comma-separated list of `this`.
`PF9-0`	Registers, connectors, pins, commands, directives, keywords, code examples, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.

Example	Description
 Note:	A note providing information of special interest or identifying a related topic. In the online version of this book, the word Note appears instead of this symbol.
 Caution:	A caution providing information about critical design or programming issues that influence operation of a product. In the online version of this book, the word Caution appears instead of this symbol.

1 GETTING STARTED

This chapter provides the information you need to begin using ADSP-BF535 EZ-KIT Lite evaluation system. For correct operation, install the software and hardware in the order presented in "Installation Tasks" on page 1-3.

The chapter includes the following sections.

- "Contents of EZ-KIT Lite Package" on page 1-1

  Provides a list of the components shipped with this EZ-KIT Lite evaluation system.

- "PC Configuration" on page 1-3

  Describes the minimum requirements for the PC to work with the EZ-KIT Lite evaluation system.

- "Installation Tasks" on page 1-3

  Describes the step-by-step procedures for setting up the hardware and software.

Contents of EZ-KIT Lite Package

Your ADSP-BF535 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF535 EZ-KIT Lite board
- *EZ-KIT Lite Quick Start Guide*

- CD containing:
  - VisualDSP++ for Blackfin processors with a limited license
  - ADSP-BF535 EZ-KIT Lite debug software
  - USB driver files
  - Example programs
  - *ADSP-BF535 EZ-KIT Lite Evaluation System Manual* (this document)
- Installation Quick Reference Card for VisualDSP++
- Universal 7.5V DC power supply
- USB 2.0 type cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

PC Configuration

For correct operation of the VisualDSP++ software and the EZ-KIT Lite, your computer must have the minimum configuration:

Windows 98, Windows 2000, Windows XP
Intel (or comparable) 166 MHz processor
VGA Monitor and color video card
2-button mouse
50 MB free on hard drive
32 MB RAM
Full-speed USB port
CD-ROM Drive

EZ-KIT Lite does not run under Windows 95 or Windows NT.

Installation Tasks

The following task list is provided for the safe and effective use of the ADSP-BF535 EZ-KIT Lite. Follow the instructions in the presented order to ensure correct operation of your software and hardware.

1. VisualDSP++ and EZ-KIT Lite software installation
2. VisualDSP++ license installation
3. EZ-KIT Lite hardware setup
4. EZ-KIT Lite USB driver installation
5. USB driver installation verification
6. VisualDSP++ startup

Installing VisualDSP++ and EZ-KIT Lite Software

This EZ-KIT Lite comes with the latest version of VisualDSP++ 3.5 for 16-bit processors. VisualDSP++ installation includes EZ-KIT Lite installations.

To install VisualDSP++ and EZ-KIT Lite software:

1. Insert the VisualDSP++ installation CD into the CD-ROM drive.
2. If Autoplay is enabled on your PC, you see the Install Shield Wizard Welcome screen. Otherwise, choose Run from the Start menu, and enter `D:\ADI_Setup.exe` in the Open field, where `D` is the name of your local CD-ROM drive.
3. Follow the on-screen instructions to continue installing the software.
4. At the Custom Setup screen, select your EZ-KIT Lite from the list of available systems and choose the installation directory. Click an icon in the Feature Description field to see the selected system's description. When you have finished, click Next.
5. At the Ready to Install screen, click Back to change your install options, click Install to install the software, or click Cancel to exit the install.
6. When the EZ-KIT Lite installs, the Wizard Completed screen appears. Click Finish.

Installing VisualDSP++ License

To install the VisualDSP++ license:

1. Locate the serial number provided on the sticker affixed to the CD sleeve and the registration form.
2. From the Start menu, choose Programs, Analog Devices, VisualDSP++ 3.5 for 16-bit Processors, VisualDSP++ Environment.
3. The information screen asks if you would like to install a license. Click Yes. The About VisualDSP++ screen appears.
4. Select the Licenses tab and click New.
5. In the Install a New License dialog that opens, select Single User.
6. Fill in the tools serial number in the field provided exactly as it appears on your CD sleeve or registration form and click Next. An information window notifies of successful license installation.

Setting Up EZ-KIT Lite Hardware

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF535 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

To connect the EZ-KIT Lite board:

1. Remove the EZ-KIT Lite board from the package. Be careful when handling the board to avoid the discharge of static electricity, which may damage some components.
2. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before continuing.

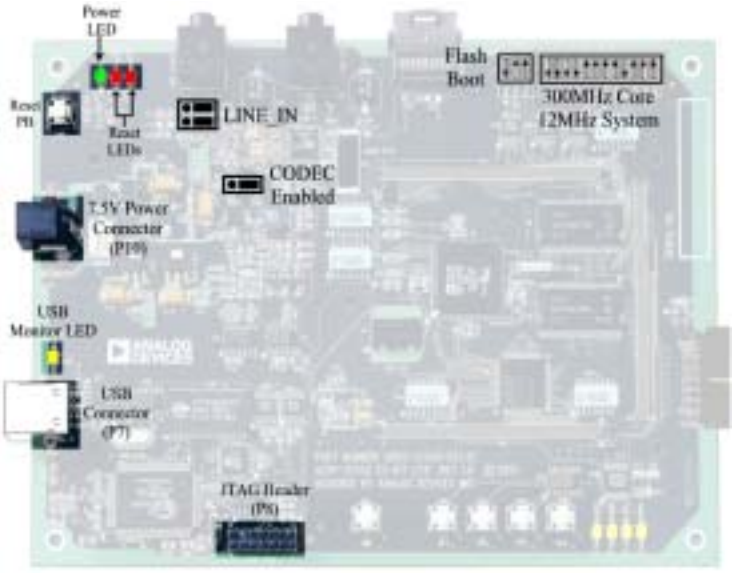


Figure 1-1. EZ-KIT Lite Hardware Setup

3. Plug the provided power supply into P10 on the EZ-KIT Lite board. Visually verify that the green power LED (LED6) is on. Also verify that the two red reset LEDs (LED7 and LED8) go on for a moment and then go off.

4. Connect one end of the USB cable to an available full speed USB port on your PC and the other end to P7 on the ADSP-BF535 EZ-KIT Lite board.

Installing EZ-KIT Lite USB Driver

The EZ-KIT Lite evaluation system installed on Windows 98, Windows 2000, and Windows XP requires one full-speed USB port.

- "Windows 98 USB Driver" on page 1-8 describes the installation on Windows 98.
- "Windows 2000 USB Driver" on page 1-12 describes the installation on Windows 2000.
- "Windows XP USB Driver" on page 1-13 describes the installation on Windows XP.

The USB driver used by the debug agent is not Microsoft certified because it is intended for a development or laboratory environment, not a commercial environment.

Windows 98 USB Driver

Before using the ADSP-BF535 EZ-KIT Lite for the first time, the Windows 98 USB driver must first be installed.

To install the USB driver:

1. Insert the CD into the CD-ROM drive.
   The connection of the device to the USB port activates the Windows 98 Add New Hardware Wizard, as shown in Figure 1-2.

Figure 1-2. Windows 98 – Add New Hardware Wizard

2. Click Next.

3. Select Search for the best driver for your device, as shown in Figure 1-3.

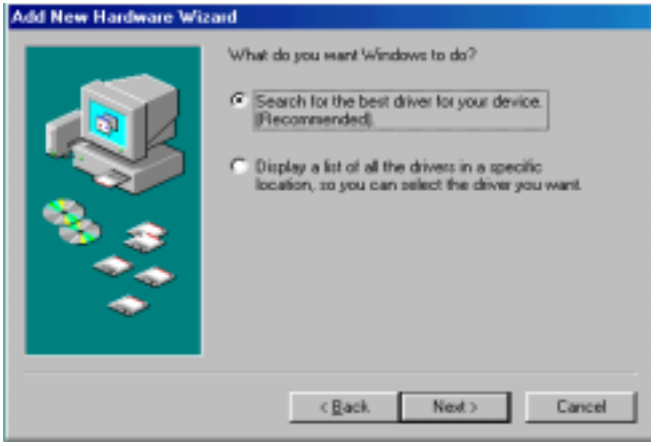


Figure 1-3. Windows 98 – Searching for Driver

4. Click Next.
5. Select CD-ROM drive, as shown in Figure 1-4.

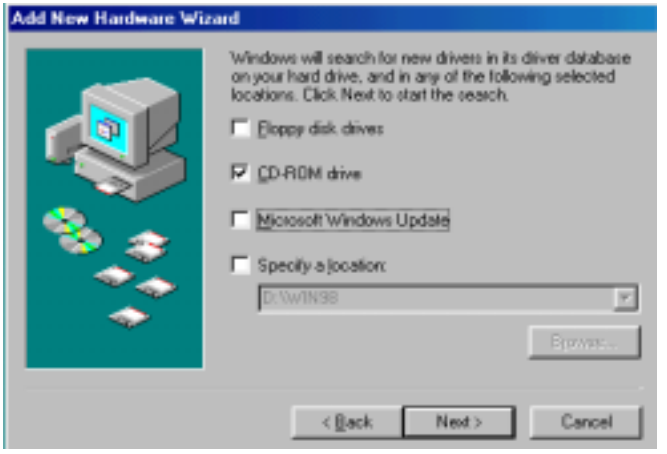


Figure 1-4. Windows 98 – Searching for CD-ROM

6. Click Next.
   Windows 98 locates the `WmUSBEz.inf` file on the installation CD, as shown in Figure 1-5.

Figure 1-5. Windows 98 – Locating Driver

7. Click Next.
   The Coping Files dialog box appears (Figure 1-6).

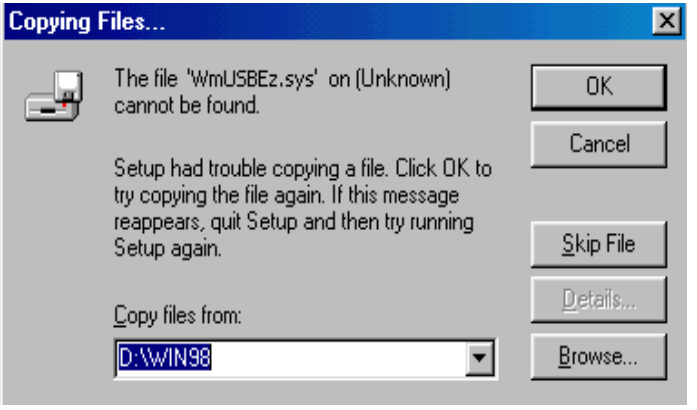


Figure 1-6. Windows 98 – Searching for .SYS File

8. Click Browse.
   The Open dialog box, shown in Figure 1-7, appears on the screen.

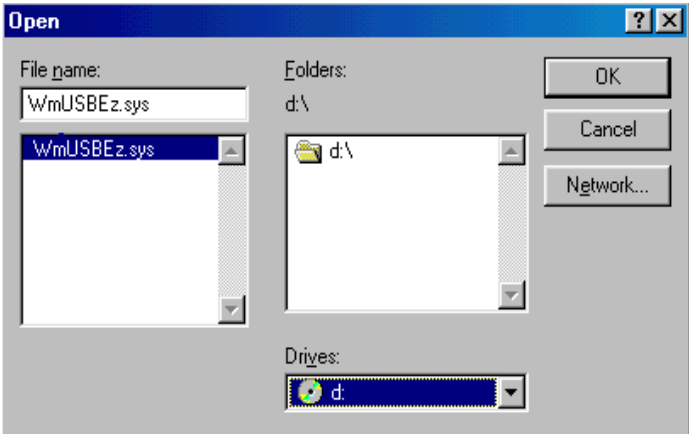


Figure 1-7. Windows 98 – Opening .SYS File

9. In Drives, select your CD-ROM drive.
10. Click OK. The Copying Files dialog box (Figure 1-8) appears.

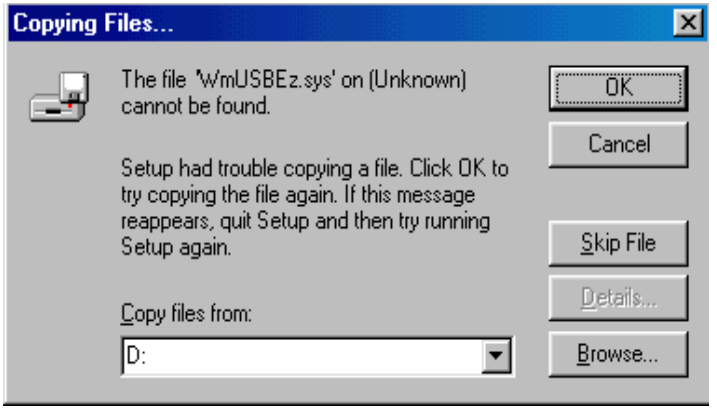


Figure 1-8. Windows 98 – Copying .SYS File

11. Click OK.
    The driver installation is now complete, as shown in Figure 1-9.

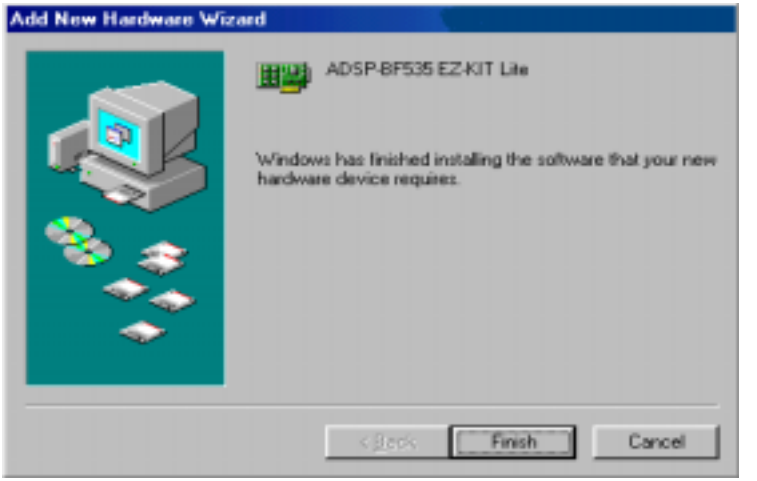


Figure 1-9. Windows 98 – Completing Software Installation

12. Click Finish to exit the wizard.
13. Verify the installation by following the instructions in "Verifying Driver Installation" on page 1-15.

Windows 2000 USB Driver

VisualDSP++ 3.5 installation software pre-installs the necessary drivers for the selected EZ-KIT Lite. The install also upgrades an older driver if such is detected in the system.

Prior to running the VisualDSP++ 3.5 installer, ensure there are no other Hardware Wizard windows running in the background. If there are any wizard windows running, close them before starting the installer.

To install the USB driver:

1. If VisualDSP++ 3.5 is already installed on your system, go to step 2.
   Otherwise, run VisualDSP++ 3.5 installation. Refer to the *Installation Quick Reference Card for VisualDSP++* for a detailed installation description.
   When installing VisualDSP++ 3.5 on Windows 2000, make sure the appropriate EZ-KIT Lite component is selected for the installation.
2. Connect the EZ-KIT Lite device to your PC's USB port. Windows 2000 automatically detects an EZ-KIT device and automatically installs the appropriate driver for the selected device (see step 1).
3. Verify the installation by following the instructions in "Verifying Driver Installation" on page 1-15.

Windows XP USB Driver

VisualDSP++ 3.5 installation software pre-installs the necessary drivers for the selected EZ-KIT Lite. The install also upgrades an older driver if such is detected in the system.

Prior to running the VisualDSP++ 3.5 installer, ensure there are no other Hardware Wizard windows running in the background. If there are any wizard windows running, close them before starting the installer.

To install the USB driver:

1. If VisualDSP++ 3.5 is already installed on your system, go to step 2.
   Otherwise, run VisualDSP++ 3.5 installation. Refer to the *Installation Quick Reference Card for VisualDSP++* for a detailed

installation description.
When installing VisualDSP++ 3.5 on Windows XP, make sure the appropriate EZ-KIT Lite component is selected for the installation.

2. Connect the EZ-KIT Lite device to your PC's USB port.
   By connecting the device to the USB port you activate the Windows XP Found New Hardware Wizard, shown in Figure 1-10.

Figure 1-10. Windows XP – Found New Hardware Wizard

3. Select Install the software automatically (Recommended) and click Next.

When Windows XP completes the driver installation for the selected device (see step 1), a window shown in Figure 1-11 appears on the screen.

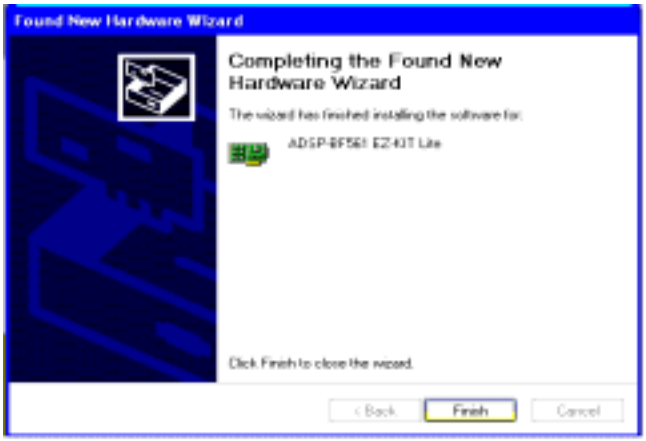


Figure 1-11. Windows XP – Completing Driver Installation

4. Verify the installation by following the instructions in "Verifying Driver Installation".

Verifying Driver Installation

Before you use the EZ-KIT Lite evaluation system, verify that the USB driver software is installed properly:

1. Ensure that the USB cable is connected to the evaluation board and the PC.
2. Verify that the yellow USB monitor LED (LED4) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

3. Verify that the USB driver software is installed properly. Open Windows Device Manager and verify that ADSP-BF535 EZ-KIT Lite shows under ADI Development Tools with no exclamation point, as in Figure 1-12.

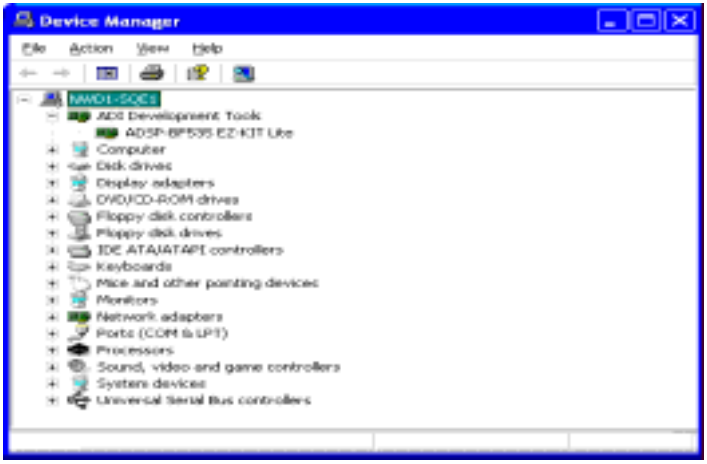


Figure 1-12. Device Manager Window

If using an EZ-KIT Lite on Windows 98, disconnect the USB cable from the board before booting the PC. When Windows 98 is booted and you are logged on, re-connect the USB cable to the board. The operation should continue normally from this point.

Starting VisualDSP++

To set up a session in VisualDSP++.

1. Verify that the yellow USB monitor LED (LED5, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. Hold down the Control (CTRL) key.

3. Select the Start button on the Windows taskbar, then choose Programs-->VisualDSP-->VisualDSP++.
   If you are running VisualDSP++ for the first time, go to step 4. If you already have existing sessions, the Session List dialog box appears on the screen.
4. Click New Session.
5. The New Session dialog box, shown in Figure 1-13, appears on the screen.

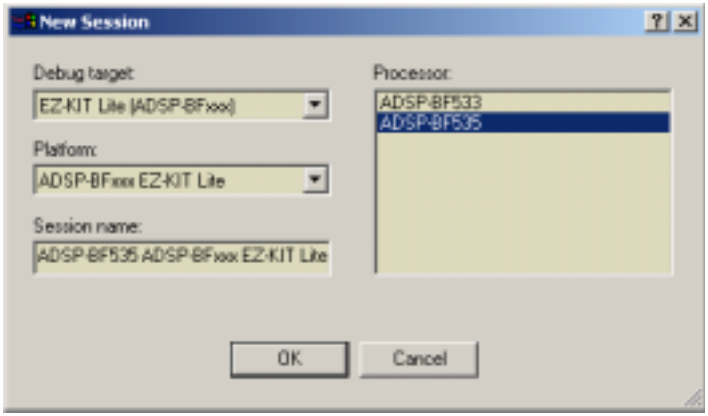


Figure 1-13. New Session Dialog Box

6. In Debug Target, choose EZ-KIT Lite (ADSP-BFxxx).
7. In Processor, choose the appropriate processor, ADSP-BF535.
8. Type a new target name in Session Name or accept the default name.
9. Click OK to return to the Session List. Highlight the new session and click Activate.

2 USING EZ-KIT LITE

This chapter provides specific information to assist you with developing programs for the ADSP-BF535 EZ-KIT Lite evaluation board. This information appears in the following sections.

- "EZ-KIT Lite License Restrictions" on page 2-2

  Describes the restrictions of the VisualDSP++ license shipped with the EZ-KIT Lite.

- "Memory Map" on page 2-3

  Defines the ADSP-BF535 EZ-KIT Lite's memory map.

- "Using SDRAM Interface" on page 2-4·

  Defines the register values to configure the on-board SDRAM.

- "Using Flash Memory" on page 2-5

  Describes how to program and use the on-board Flash memory.

- "Using Programmable Flag Pins" on page 2-6

  Describes the function and use of the programmable flag pins on the EZ-KIT Lite evaluation system.

- "Example Programs" on page 2-8

  Provides information about the example programs included in the ADSP-BF535 EZ-KIT Lite evaluation system.

- "Using Flash Programmer Utility" on page 2-9

Provides information on the Flash Programmer utility included with the EZ-KIT Lite software.

- "Using Background Telemetry Channel" on page 2-9

  Highlights the advantages of the Background Telemetry Channel features of VisualDSP++.

- "Using EZ-KIT Lite VisualDSP++ Interface" on page 2-10

  Describes the trace, performance monitoring, boot loading, context switching, hardware breakpoints, and target options of the EZ-KIT Lite system.

For more detailed information about programming the ADSP-BF535 Blackfin processor, see the documents referred to as "Related Documents".

EZ-KIT Lite License Restrictions

The license shipped with the EZ-KIT Lite imposes the following restrictions.

- The user program is limited to 176 KB of the ADSP-BF535 processor's internal memory space.
- No connections to Simulator or Emulator sessions are allowed.
- Only one EZ-KIT Lite board can be connected to the host PC and debugged at a time.
- The EZ-KIT Lite hardware must be connected and powered up in order to use VisualDSP++ with a kit license.

Memory Map

The ADSP-BF535 processor has internal SRAM that can be used for instruction or data storage. The configuration of internal SRAM is detailed in the *ADSP-BF535 Processor Hardware Reference*.

The ADSP-BF535 EZ-KIT Lite board contains 272K x 16 bits of external Flash memory. This memory is connected to the processor's ~AMS0 memory select pin. The external memory interface is also connected to 4M x 32-bit SDRAM memory. This memory is connected to the ~SMS0 pin.

Table 2-1. EZ-KIT Lite Evaluation Board Memory Map

Start Address		End Address	Content
External Memory	0x0000 0000	0x00FF FFFF	SDRAM Bank 0 (SDRAM) See "Using SDRAM Interface" on page 2-4.
	0x2000 0000	0x2009 FFFF	ASYNC Memory Bank 0 (FLASH) See "Using Flash Memory" on page 2-5.
	All other locations		Not used
Internal Memory	0xF000 0000	0xF003 FFFF	L2 SRAM 256 KB
	0xFF80 0000	0xFF80 3FFF	Data Bank A 16 KB
	0xFF90 0000	0xFF90 3FFF	Data Bank B 16 KB
	0xFFA0 0000	0xFFA0 3FFF	Instruction SRAM 16 KB
	0xFFB0 0000	0xFFB0 0FFF	Scratch Pad SRAM 4 KB
	0xFFC0 0000	0xFFDF FFFF	System MMRs 2 MB
	0xFFE0 0000	0xFFFF FFFF	Core MMRs 2 MB
	All other locations		Reserved

Using SDRAM Interface

In order to use the 4M x 32 bits (16 MB) of SDRAM memory, the three SDRAM control registers must be initialized. Table 2-2 shows the standard configuration for these registers when using the EZ-KIT Lite in the default configuration. These numbers were derived using the M48LC4M16ATG-75 with a system clock frequency of 120 MHz.

Table 2-2. SDRAM Default Settings

Register	Value	Function
EBIU_SDRRC	0x0000074A	RDIV = 1866 clock cycles
EBIU_SDBCTL	0x00000001	Bank 0 enabled Bank 0 size = 16 MB Bank 0 column address width = 8 bits
EBIU_SDGCTL	0x0091998F	32-bit data path External buffering timing disabled t_{WR} = 2 SCLK cycles t_{RCD} = 3 SCLK cycles t_{RP} = 3 SCLK cycles t_{RAS} = 6 SCLK cycles pre-fetch disabled CAS latency = 3 SCLK cycles SCLK1 disabled

If you are in an EZ-KIT Lite session (that is, not using an emulator), the SDRAM registers are configured automatically through the debugger. The debugger uses the values in Table 2-2 whenever Bank 0 is accessed through the debugger (such as viewing memory windows or loading a program). Clearing the appropriate checkbox on the Target Options dialog box, which is accessible through the Settings pull-down menu, disables this feature and allows manual configuration.

An example program is included in the EZ-KIT installation directory to demonstrate how to set up the SDRAM interface.

Using Flash Memory

The DSM2150 Flash/PLD chip provides a total of 272K x 16 bits of external Flash memory, arranged into two independent flash arrays (boot and main). The chip also has a series of configuration registers to control IO and PLD. This chip is initially configured with the memory sectors mapped to the DSP, as shown in Figure 2-1.

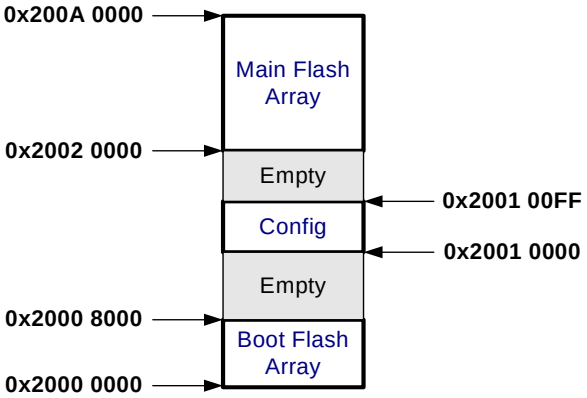


Figure 2-1. Flash Memory Map

Use PSDsoft Express™ to modify the default settings for the Flash memory. The DSM project must be modified and the Flash memory must be reprogrammed using FlashLINK. The default project files can be found in `\…\VisualDSP\Blackfin\EZ-KITs\ADSP-BF535\PSDConfigFiles`. Analog Devices does not provide any support for setting up the DSM2150 with PSDsoft Express or programming it using FlashLINK. E-mail STMicroelectronics at `apps.psd@st.com` for technical assistance.

To program the Flash memory with your boot code, you must first create a loader file from your DSP code. Set up the loader in VisualDSP++, depending on how you plan to boot the Flash memory. The two possibili-

ties are to boot the DSP in 16-bit external execution mode or in 8-bit boot mode. See “Boot Mode Select Switch (SW1)” on page 3-7 for the boot mode settings.

Next, the loader file must be programmed into the Flash memory. This can be done through the DSP using the VisualDSP++ Flash Programmer utility (see “Using Flash Programmer Utility” on page 2-9) or by using the FlashLink programmer.

The DSM2150 can be re-programmed using the FlashLINK JTAG programming cable available from STMicroelectronics (`www.st.com/psd`) for approximately $59. FlashLINK plugs into any PC parallel port. The software development tool, PSDsoft Express, is required to modify the DSM2150 configuration and to operate the FlashLINK cable. PSDsoft Express can be downloaded at no charge from at `www.st.com/psd`.

Using Programmable Flag Pins

The ADSP-BF535 processor has 16 asynchronous Programmable Flag (PF) IO pins. During reset, `PF9-0` function as inputs to the internal PLL of the DSP. They are not valid until 120 uS after reset. Table 2-3 describes how the PFs can be used after reset.

Table 2-3. Programmable Flag Pin Summary

Flag	Connected To	Description
`PF0`	`LED4`	`PF3-0` are connected to the LEDs. These can be used to light an LED when a routine completes.
`PF1`	`LED1`	
`PF2`	`LED2`	
`PF3`	`LED3`	

Table 2-3. Programmable Flag Pin Summary (Cont'd)

Flag	Connected To	Description
PF4	SW4	PF7-4 are connected to the push buttons on the EZ-KIT Lite board and are for user input. Your routine can monitor and execute specific code when a push button is pressed.
PF5	SW5	
PF6	SW6	
PF7	SW7	
PF8		Not used
PF9		Not used
PF10		Not used
PF11		Not used
PF12	PMGMT0	These are used to change the internal voltage of the DSP. Refer to "Power Management" on page 2-7 for more information.
PF13	PMGMT1	
PF14	PMGMT2	
PF15	U7.11	Connected to the reset of the AD1885 codec (U7). This signal must be output as a high (1) to enable the AD1885 codec.

After a DSP reset, all of the PF pins are initialized as inputs. The direction of the PF is configured by the FIO_DIR Memory Mapped Register (MMR). The PFs are set HIGH (1) using the FIO_FLAG_S and cleared (0) using the FIO_FLAG_C MMRs. For more information on configuring the PF pins, see the *ADSP-BF535 Processor Hardware Reference Manual*.

All of the PFs can are brought out to the expansion connector P2. The location of the PF nets can be found in "Schematics" on page B-1.

Power Management

The PF14-12 pins allow you to program the core voltage of the processor. The default core voltage is 1.5V. Table 2-4 gives the value of the core voltage corresponding to the state of the PFs.

Table 2-4. Power Management PF Settings

PF14	PF13	PF12	VDD_INT
0	0	0	0.9V
0	0	1	1.0V
0	1	0	1.1V
0	1	1	1.2V
1	0	0	1.3V
1	0	1	1.4V
1[1]	1[1]	0[1]	1.5V[1]
1	1	1	1.6V

1 Default settings

When lowering the core voltage of the processor, the frequency of the DSP should also be taken into consideration. As you lower the core voltage, the frequency the core is running at must be decreased.

Example Programs

Example programs are provided with the ADSP-BF535 EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in `\…\VisualDSP\Blackfin\EZ-KITs\ADSP-BF535\Examples`. Please refer to the readme file provided with each example for more information.

Using Flash Programmer Utility

The ADSP-BF535 EZ-KIT Lite evaluation system includes a Flash Programmer utility. The utility allows you to program the Flash memory on the EZ-KIT Lite. The Flash Programmer is installed with VisualDSP++. Once the utility is installed, it is accessible from the Tools pull-down menu.

For more information on the Flash Programmer utility, select Start and choose Programs-->VisualDSP-->VisualDSP++ Documentation.

Using Background Telemetry Channel

The ADSP-BF535 USB debug agent supports the Background Telemetry Channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting DSP execution.

The BTC allows the user to view a variable as it is updated or changed, all while the processor continues to execute. For increased performance of the BTC, including faster reading and writing, please check out our latest line of DSP emulators at `www.analog.com/Analog_Root/productPage/productHome/0,2121,EMULATORS,00.html`.

For more information about the Background Telemetry Channel, see the *VisualDSP++ 3.5 User's Guide for 16-Bit Processors* or online Help.

Using EZ-KIT Lite VisualDSP++ Interface

This section provides information on the following parts of the VisualDSP++ graphical user interface:

Trace Window

Choosing the Trace command from the View-->Debug Windows menu opens the Trace window (Figure 2-2).

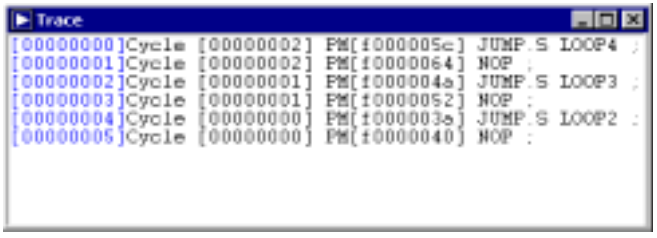


Figure 2-2. Trace Window

The trace buffer stores a history of the last 16 changes in program flow taken by the program sequencer. View the history to recreate the program sequencer's most recent path.

The trace buffer does not track changes in flow caused by zero-overhead loops or while in the reset service routine.

To use the trace buffer, ensure your program leaves the reset service routine.

Enabling Trace Buffer

To view trace history in the Trace window, first, enable the trace buffer (choose Enable Trace from the Tools->Trace menu). On each halt, the Trace window is updated with the changes that occurred since the last halt. Reading the trace buffer destroys the trace buffer's contents and discards the information previously stored before the last run.

Reading Trace Buffer Data

The first column between the square brackets (in blue) indicates the line number in the Trace window.

The second column between square brackets, which comes in vertical pairs, shows the trace number. For each discontinuity, the first (top position) is the source trace, and the second (bottom position) is the destination trace. The third column in between square brackets shows the addresses of the instructions. Each address is followed by the assembly instruction.

The trace grows upward. In Figure 2-2 on page 2-10, trace 0 occurred before trace 1, which occurred before trace 2, and so on.

Performance Monitor

Choosing Performance Monitor from the Settings menu opens the Performance Monitor Control dialog box shown in Figure 2-3 on page 2-12. A description of the dialog box appears in Table 2-5 on page 2-12.

Figure 2-3. Performance Monitor Dialog Box

The performance monitor is a 32-bit counter that allows you to track occurrences of events within the core and use these to analyze system behavior. When the counter reaches zero, it causes an exception or emulation event, as specified by the Type option.

Table 2-5. Performance Monitor Options

Option	Description
Enable	Enables performance monitoring.
Mode	Determines the mode of operation for tracking events: Disabled disables the monitor. User tracks while in user mode. Supervisor tracks while in supervisor mode. Both tracks while in both user mode and supervisor mode.
Type	Determines the type of event occurring on a match: Exception causes an exception to occur. You can install a handler to detect and handle this exception. Emulation halts the DSP.

Table 2-5. Performance Monitor Options (Cont'd)

Option	Description
Event	Specifies the tracked event. Refer to your processor's *Hardware Reference* for details. Events include stalls, cache hits or misses, loop iterations, branches, interrupts, loads, stores, DMA accesses, and so on.
Count	Specifies the count. When the 32-bit counter reaches zero, an exception or emulation event occurs. For example, to halt on the third occurrence of an event, load the count with `0xFFFFFFFE` and set Type to Emulation. The counter counts up and wraps around, causing the processor to halt as desired.

Boot Load

Choosing Boot Load from the Settings menu runs the processor and performs a hard reset on the board. This command saves you from having to shut down VisualDSP++, reset the EZ-KIT Lite board, and bring up VisualDSP++ again when you want to perform a hard reset.

Use this feature when loading debug boot code from an external part or when you want to put the device into a known state.

Context Switching

The ADSP-BF535 EZ-KIT Lite evaluation system uses two methods to obtain and restore the processor's context: by using the `M3` register or by using the stack.

Using M3 Register

Set Use M3 register for context switching option in the Target Options dialog box, as described on page 2-19.

When this option is selected, VisualDSP++ uses the `M3` register for context switches. This renders `M3` unavailable for user code since the register will be corrupted. When cleared, VisualDSP++ uses the address pointed to by the Stack Pointer register (`SP`).

This method is very straightforward. M3 is chosen as the register for temporary storage and is, therefore, corrupted and cannot be employed in user code. Only use this method when there may be a problem using the stack method.

Using Stack Pointer

If the processor is in the reset service routine at startup, it is assumed the Stack Pointer (SP) is not pointing to a valid address. In this case, the SP is initialized to point to a valid address (0xFFB00FFC), and this location is used for temporary storage.

If the processor is not in the reset service routine, it is assumed the user code has already initialized the SP to a valid address, and this location is used for temporary storage. After the initial startup, the SP is assumed valid. User code can change the SP at any time after leaving the reset service routine, and the new value of the SP is used for context switches. In all cases, the stack is pushed and popped and is non-intrusive to the user code.

This method is less intrusive than the M3 method but is also more prone to problems. First, this method requires at least one available location on the stack. It also assumes user code will not point the SP to an invalid memory location during debugging and that, if not in the reset service routine, the SP has been programmed correctly. Additionally, it may be possible that a user program has not yet left the reset service routine, but the SP is already initialized. In this case, at startup, the processor is detected in the reset service routine still and the user's SP value would be overwritten.

Hardware Breakpoints

Choosing Hardware Breakpoints from the Settings menu opens the Hardware Breakpoints dialog box. The Hardware Breakpoints dialog box contains four tabbed pages: Data 0-1, Instruction 0-1, Instruction 2-3, and Instruction 4-5.

Hardware breakpoints allow you to set breaks on instructions or data transfers within a user-defined memory range. The two types of breakpoints are described in "Data Breakpoints" on page 2-15 and "Instruction Breakpoints" on page 2-16.

Global Breakpoint Options

Global breakpoint options apply to all hardware breakpoints regardless of type. These options are listed in Table 2-6.

Table 2-6. Global Breakpoint Options

Option	Description
Enable watchpoint unit	Enables the watchpoint unit.
Enable data AND instruction	Specifies that the processor AND the data and instruction breakpoints to form the composite interrupt. Normally each of the group interrupts are ORed to create a composite interrupt.

Common Breakpoint Attributes

Each tabbed page in the Hardware Breakpoints dialog box has the following common attributes, as described in Table 2-7.

Data Breakpoints

Figure 2-4 on page 2-17 shows the Data 0-1 page of the Hardware Breakpoints dialog box. Two individual data breakpoints can be set. A data breakpoint is triggered by a memory access to a specified address or range. Selecting Enable Range enables the two data breakpoints.

Data Breakpoint Specific Attributes

Data breakpoints have the attributes listed in Table 2-8.

Table 2-7. Common Breakpoint Attributes

Option	Description
Enable	Enables the individual breakpoint. Ensure that Global watchpoint unit is also selected.
Enable Range	Each tab (Data 0-1, Instruction 0-1, Instruction 2-3, and Instruction 4-5) is considered a range. Selecting this option on a particular tabbed page specifies a search range instead of a single address. Select the inclusive or exclusive range radio button as desired, for example: WPIA0 < IA <= WPIA1 causes the DSP to break for an address greater than the instruction breakpoint 0 address AND less than or equal to the instruction breakpoint 1 address. IA <= WPIA0 || IA > WPIA1 causes the DSP to break for an address less than or equal to the instruction breakpoint 0 address OR greater than the instruction breakpoint 1 address.
Address	Each breakpoint has an associated address. For a single address, this is the address searched when Enable Range is selected. This may be the upper or lower bound address.
Skip count	Each individual breakpoint has an associated skip count. When this count is reached, the breakpoint triggers on the next match of this breakpoint. For example, to break on every third match, enter a skip count of 2.

Instruction Breakpoints

Figure 2-5 shows the Instruction 0-1 page of the Hardware Breakpoint dialog box.

Six individual instruction breakpoints can be set. An instruction breakpoint occurs when an instruction is executed or an instruction in a specified range is executed. Three ranges, each with its own page, can be specified. You must select Enable Range to set up an instruction range.

Instruction Breakpoint Specific Attributes

Each instruction breakpoint have a specific attribute, as described in Table 2-9.

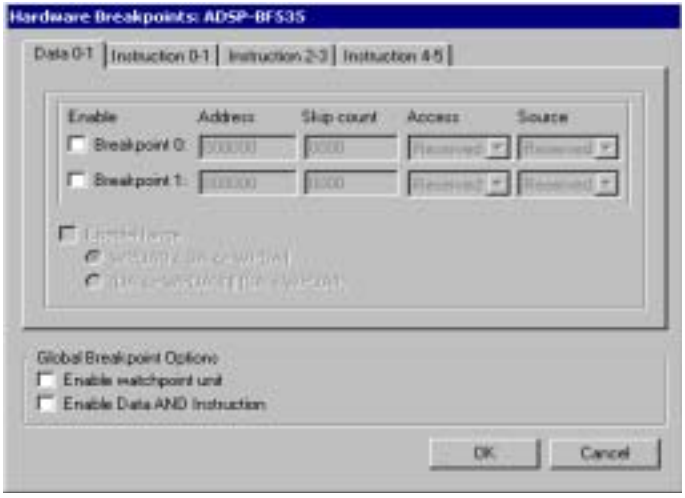


Figure 2-4. Data Breakpoints Dialog Box

Table 2-8. Data Breakpoint Specific Attributes

Attribute	Description
Access	Specifies the type of access: Reserved (reserved). Write triggers the breakpoint on any write to the specified address. Read triggers the breakpoint on any read from the specified address. Both triggers the breakpoint on any write to or read from the specified address.
Source	Specifies the source of access: Reserved (reserved). DAG0 triggers the breakpoint on any access using DAG0 with the specified address. DAG1 triggers the breakpoint on any access using DAG1 with the specified address. Both triggers the breakpoint on any access using DAG0 or DAG1 with the specified address.

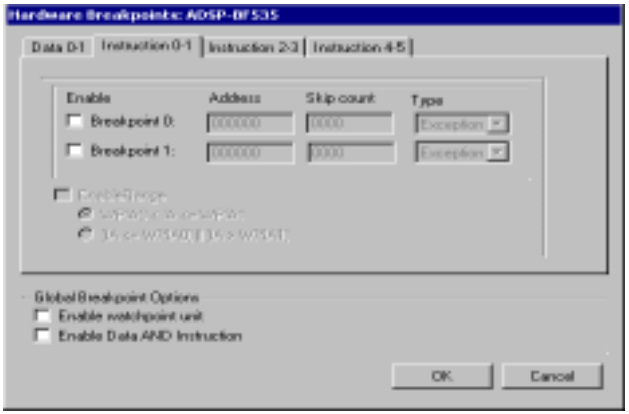


Figure 2-5. Instruction Breakpoints Dialog Box

Table 2-9. Instruction Breakpoint Specific Attribute

Attribute	Description
Type	Determines the type of event that occurs on a match: Exception causes an exception to occur. You can install a handler to detect and handle this exception. Emulation halts the processor.

Hardware Breakpoints Tips and Tricks

Be aware of the following tips and tricks when using hardware breakpoints on Blackfin processors.

Latency

There are no latency cycles for hardware breakpoint matches on the ADSP-BF535 EZ-KIT Lite evaluation system.

Restrictions

When using hardware breakpoints, do not place breaks at any address where a `JUMP`, `CALL`, or `IDLE` instruction is not valid.

Do not attempt to place breaks in the last few instructions of a `DO LOOP` or in the delay slots of a delayed branch. For more information on these illegal locations, see the processor's *Hardware Reference*.

Target Options

Choosing Target Options from the Settings menu opens the Target Options dialog box (Figure 2-6). Use target options to control certain aspects of the processor on the ADSP-BF535 EZ-KIT Lite evaluation system.

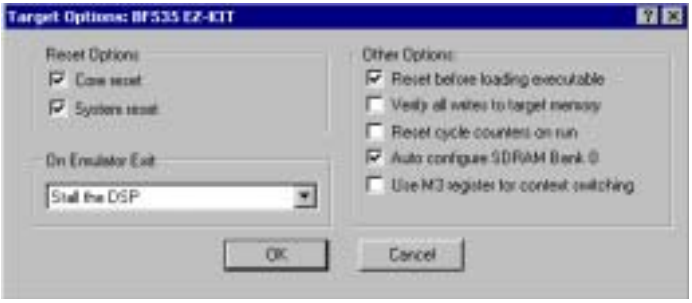


Figure 2-6. Target Options Dialog Box

Reset Options

Reset options control how the processor behaves when a reset occurs. The reset options are described in Table 2-10.

Table 2-10. Reset Options

Option	Description
Core reset	Resets the core when the debugger executes a reset.
System reset	Resets the peripherals when the debugger executes a reset.

On Emulator Exit

This target option controls processor behavior when VisualDSP++ relinquishes DSP control (for example, when exiting VisualDSP++). The option is described in Table 2-11.

Table 2-11. On Emulator Exit Target Options

Option	Description
On Emulator Exit	Determines the state the DSP is left in when the emulator relinquishes control of the DSP. Reset DSP and Run causes the DSP to reset and begin execution from its reset vector location. Run from current PC causes the DSP to begin running from its current location. Stall the DSP resets the DSP and then writes a `JUMP 0` to the first location in internal memory so the DSP is stuck in a tight loop after exiting.

Other Options

Table 2-12 describes other available target options.

Table 2-12. Miscellaneous Target Options

Option	Description
Reset before loading executable	Resets registers before loading a DSP executable. Clear this option when DSP registers must not change to their reset values when a file load occurs.
Verify all writes to target memory	Validates all memory writes to the DSP. After each write, a read is performed and the values are checked for a matching condition. Enable this option during initial program development to locate and fix initial build problems (such as attempting to load data into non-existent memory). Clear this option to increase performance while loading executable files, since VisualDSP++ does not perform the extra reads that are required to verify each write.

Table 2-12. Miscellaneous Target Options (Cont'd)

Option	Description
Reset cycle counters on run	Resets the cycle count registers to zero before a Run command is issued. Select this option to count the number of cycles executed between breakpoints in a program.
Auto configure SDRAM bank 0	VisualDSP++ will auto-configure the necessary registers to communicate with the SDRAM bank 0 memory included on the EZ-KIT Lite evaluation board. Select this option to cause VisualDSP++ to configure bank 0 when it is accessed through VisualDSP++ (for example, when viewing memory windows or loading a program). Clear this option if you want to manually configure memory.
Use M3 register for context switching	Allows VisualDSP++ to use the `M3` register for context switches. This leaves M3 unavailable for user code because it will be corrupted. Clear this option to specify that the `M3` register and VisualDSP++ use the address pointed to by the Stack Pointer register.

Restricted Software Breakpoints

The EZ-KIT Lite development system restricts breakpoint placement when certain conditions are met. That is, under some conditions, breakpoints cannot be placed effectively. Such conditions depend on bus architecture, pipeline depth, and ordering of the EZ-KIT Lite and its target processor.

3 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF535 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 3-2

  Describes the configuration of the ADSP-BF535 (formerly ADSP-21535) processor and explains how the board components interface with the processor.

- "Jumper and DIP Switch Settings" on page 3-5

  Shows the location and describes the function of the configuration jumpers and DIP switches.

- "LEDs and Push Buttons" on page 3-9

  Shows the location and describes the function of the LEDs and push buttons.

- "Connectors" on page 3-12

  Shows the location and gives the part number for all of the connectors on the board. Also, the manufacturer and part number information is given for the mating parts.

- "Specifications" on page 3-15

  Gives the requirements for powering the board.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

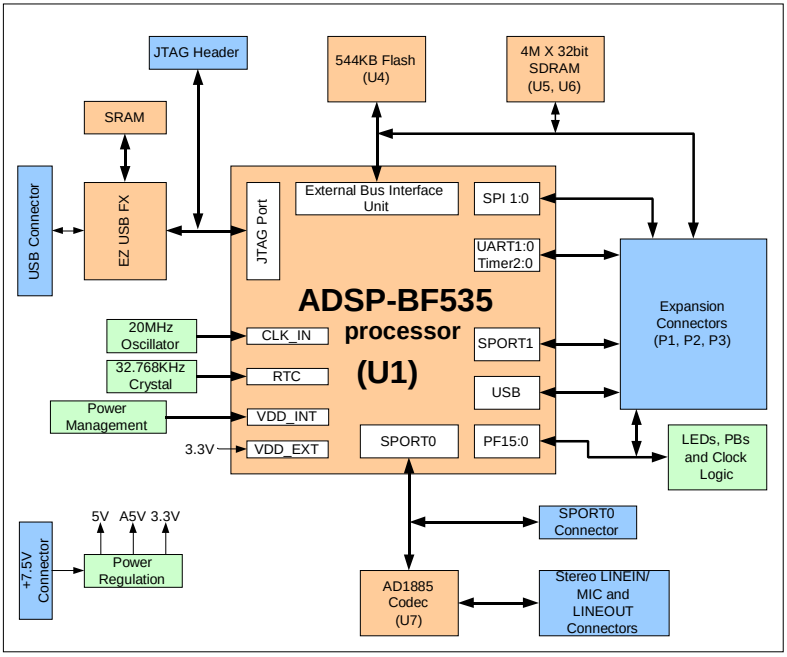


Figure 3-1. System Architecture

The EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-BF535 Blackfin processor. The processor has a default core voltage of 1.5V. Refer to "Power Management" on page 2-7 for more information about changing the core voltage without halting the processor. The voltage of the processor's peripheral interface is 3.3V.

A 20 MHz oscillator supplies the input clock to the processor. The speed at which the core and peripherals operate is determined by the configuration of the multiplier select switch (SW2) at reset. (See "DSP PLL Setup

Switch (SW2)" on page 3-7.) By default, the processor core runs at 300 MHz and the peripheral interface runs at 120 MHz. A 32.768 kHz crystal supplies the Real Time Clock (RTC) inputs of the processor.

The EZ-KIT Lite board can be configured to boot in all of the possible ADSP-BF535 boot modes. For information about configuring the boot mode, see "Boot Mode Select Switch (SW1)" on page 3-7.

External Bus Interface

The External Bus Interface Unit (EBIU) is connected to 4M x 32 bits of SDRAM (16 MB). This memory is connected to the synchronous memory select 0 (~SMS0) pin. Refer to "Using SDRAM Interface" on page 2-4 for information about configuring the SDRAM.

The EBIU is also connected to 272K x 16 bits of Flash memory. This memory is connected to the asynchronous memory select (~AMS0) pin. The processor can use this memory for both booting and storing information during normal operation. Refer to "Using Flash Memory" on page 2-5 for information about using the Flash memory.

All of the address, data, and control signals are available externally via the extender connectors (P3-1). The pin-out of these connectors can be found in "Schematics" on page B-1.

SPORT0 Audio Interface

SPORT0 is connected to the AD1885 SoundMAX codec (U7). Two 3.5mm stereo jacks (P5, P6) allow audio to be input and output. You can supply an audio input to the Codec Microphone Input Channel (MIC1) or to the stereo LINE_IN input channel. The jumper settings of JP1 determine the codec channel driven by the input jack (P5). For information about configuring JP1, see "Audio Input Select Jumper (JP1)" on page 3-5.

SPORT0 is also routed to an off-board connector (P9). When using the off-board connector, the codec must be held in reset, so that it does not drive any of the SPORT0 signals. The codec can be held in reset by driving PF15 low or by setting up JP2 to always hold the codec in reset (see "Audio Codec Disable Jumper (JP2)" on page 3-6). PF15 must be pulled HI (1) for the codec to function.

TCLK0 and RCLK0 pins are shorted together using R114 and R118.

Expansion Interface

The expansion interface consists of the footprints for three connectors. Table 3-1 shows the interfaces each connector provides. For the exact pin-out of these connectors, refer to "Schematics" in Appendix B, Schematics. Analog Devices does not populate these connectors or provide any additional support for this interface. The mechanical locations of these connectors can be found in "Mechanical Dimensions" on page 3-17.

Table 3-1. Connector Interfaces

Connector	Interfaces
P1	5V, GND, Address, Data
P2	3.3V, GND, EBUI control signals, PF15-0, SPI1-0, SPORT1, UART1-0, TMR2-0, NMI
P3	1.5V, GND, Reset, USB, CLKOUT, SLEEP

Limits to the current and to the interface speed must be taken into consideration if you use this interface. The maximum current limit is dependent on the capabilities of the regulator used. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a 6-pin interface. The JTAG emulation port of the DSP is also connected to the USB debugging interface (Note that this is not the processor's USB interface). When an emulator is connected to the board at P8, the USB debugging interface is disabled. See "JTAG (P8)" on page 3-14 for more information about the JTAG connector.

To learn more about available emulators, contact Analog Devices (see "Product Information").

Jumper and DIP Switch Settings

This section describes the function of all the jumpers and DIP switches. The following figure (Figure 3-2 on page 3-6) shows the location of all the jumpers and DIP switches.

Audio Input Select Jumper (JP1)

The audio input jack (P5) can be connected to the MIC1 or the LINEIN input channels of the AD1885 codec (U7). When the JP1 jumpers connect pins 1 and 3 and pins 2 and 4, P3 connects to the mono MIC1 channel. When the jumpers connect pins 3 and 5 and pins 4 and 6, P5 connects to the stereo LINE_IN channel of the AD1885 codec. These jumper settings are illustrated in Figure 3-2 on page 3-6. (The words MIC and LINE are on the board as a reference)

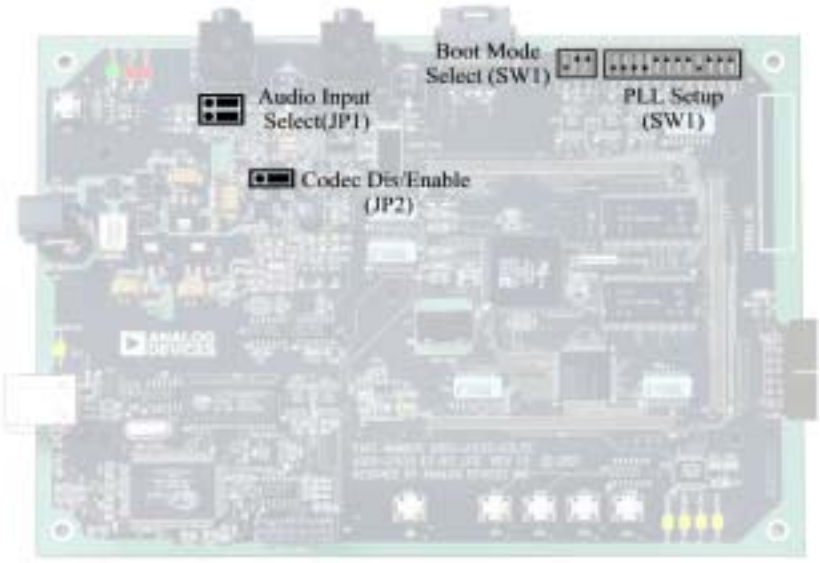
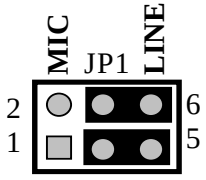
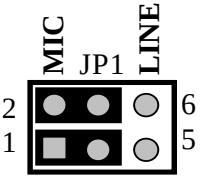


Figure 3-2. Jumper Locations

Table 3-2. Audio Input Jumper Settings (JP1)

Stereo LINE_IN (DEFAULT)	Mono MIC1
	

Audio Codec Disable Jumper (JP2)

Placing a jumper between pins 1 and 2 of JP2 holds the AD1885 in reset, preventing it from driving signals to the serial port. When a jumper is between pins 2 and 3 of JP2, the AD1885 is held in reset until PF15 is set to an output and is asserted. These positions are labeled on the board as DIS and ENA 1885.

Boot Mode Select Switch (SW1)

The boot mode select switch determines how the processor boots. Table 3-3 shows the switch settings for the boot modes.

SPI ROM is not available on the EZ-KIT Lite.

Table 3-3. Boot Mode Select Switch

BMODE0 Pin 1	BMODE1 Pin 2	BMODE2 Pin 3	Description
On	On	On	Execute from 16 bit external memory (no boot).
Off[1]	On[1]	On[1]	Boot from 8-bit EPROM[1]
On	Off	On	Boot from SPI0 ROM (8-bit addresses)
Off	Off	On	Boot from SPI0 ROM (16-bit addresses)
–	–	Off	All others reserved

1 Default settings

DSP PLL Setup Switch (SW2)

The processor's Phase Lock Loop (PLL) multiplies the 20 MHz input clock by a multiplication factor to set the core clock speed of the DSP. Internal to the processor the Programmable Flag pins, PF9-0, are multiplexed with the PLL setup signals, SSEL6-0, DF, and MSEL1-0.

During reset, the function of the pins is to setup the PLL. At this time, the signals are attached to the SW2 switch and determine the core and external clock speeds of the processor. The SW2 switch drives the processor pins during reset and, for approximately 120mS, after reset. Once this time has elapsed, the PFs are no longer connected to the SW2 but are connected to the general-purpose IO (LEDs, push buttons) on the board. This is done with an external 2-to-1 multiplexer and is provided for flexibility when using the EZ-KIT Lite.

The following table shows the switch position that corresponds to a processor pin.

Table 3-4. PLL Setup Switch (SW2) Functions

DSP Pin	Switch Position	DSP Pin	Switch Position
MSEL0	1	MSEL6	7
MSEL1	2	DF	8
MSEL2	3	SSEL0	9
MSEL3	4	SSEL1	10
MSEL4	5	None	11
MSEL5	6	Bypass	12

Figure 3-3 shows the default setting for SW2. This will produce a 300 MHz core clock speed and a 120 MHz peripheral interface speed. For more information about setting up the multiplication factors, refer to the Managing DSP Clocks section of the *ADSP-BF535 Processor Hardware Reference*.

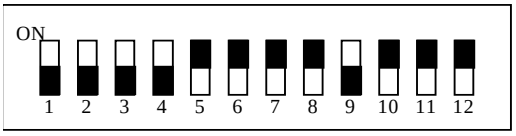


Figure 3-3. Default PLL Setup Switch Settings (SW2)

A switch setting of ON supplies a logic low (0) on the corresponding processor pin.

LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 3-4 shows the locations of the LEDs and push buttons.

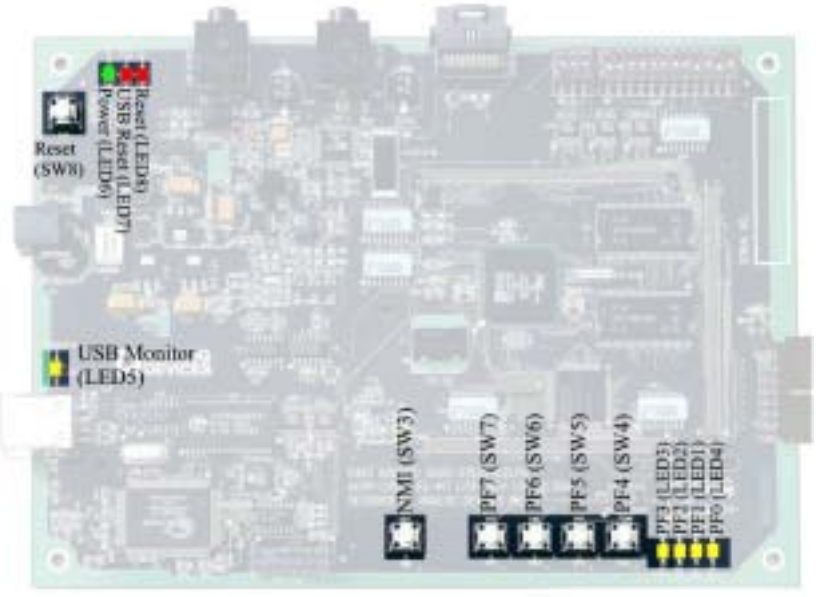


Figure 3-4. LED and Push Button Locations

Programmable Flag LEDs (LED1, LED2, LED3, LED4)

Four LEDs are connected to four of the processor's Programmable Flag (PF) pins, `PF3-0`. These LEDs are active `HIGH` and are lit by an output of "`1`" from the processor. Refer to "Using Programmable Flag Pins" on page 2-6 for more information about using of the PFs when programming the processor.

Table 3-5. Programmable Flag LEDs

LED Reference Designator	DSP Programmable Flag Pin
LED4	PF0
LED1	PF1
LED2	PF2
LED3	PF3

USB Monitor LED (LED5)

The USB Monitor LED (LED5) indicates that USB communication has been initialized successfully and you may connect to the processor using a VisualDSP++ EZ-KIT Lite session. This should take approximately 15 seconds. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver (see “Installing EZ-KIT Lite USB Driver” on page 1-7).

Power LED (LED6)

When LED6 is lit (green), it indicates that power is being properly supplied to the board.

Reset LEDs (LED7, LED8)

When LED8 is lit, it indicates that master reset for all the major ICs is active. When LED7 is lit, the USB interface chip (U11) is being reset. The USB chips only reset on power-up, or if USB communication has not been initialized.

Non-Maskable Interrupt Push Button (SW3)

The SW3 button is connected to the Non-maskable Interrupt (NMI) pin of the processor. When pressed, the processor vectors to the NMI interrupt vector.

Programmable Flag Push Buttons (SW4, SW5, SW6, SW7)

Four push buttons are provided for general-purpose user input. SW7-4 connect to the processor's Programmable Flag (PF) pins, PF7-4. The push buttons are active HIGH and, when pressed, send a High (1) to the processor. Refer to "Using Programmable Flag Pins" on page 2-6 for more information about the use of the PFs when programming the DSP. Table 3-6 shows the PF signal and the switch it is connected to.

Table 3-6. Programmable Flag Switches

Push Button Reference Designator	DSP Programmable Flag Pin
SW4	PF4
SW5	PF5
SW6	PF6
SW7	PF7

Reset Push Button (SW8)

The RESET push button resets all of the ICs on the board. This reset does not affect the USB interface chip (U11) unless communication has not been initialized with a PC. After USB communication has been initialized, the only way to reset the USB is by powering down the board.

Connectors

This section describes the connector functionality and provides information about mating connectors. The locations of the connectors are shown in Figure 3-5 on page 3-10.

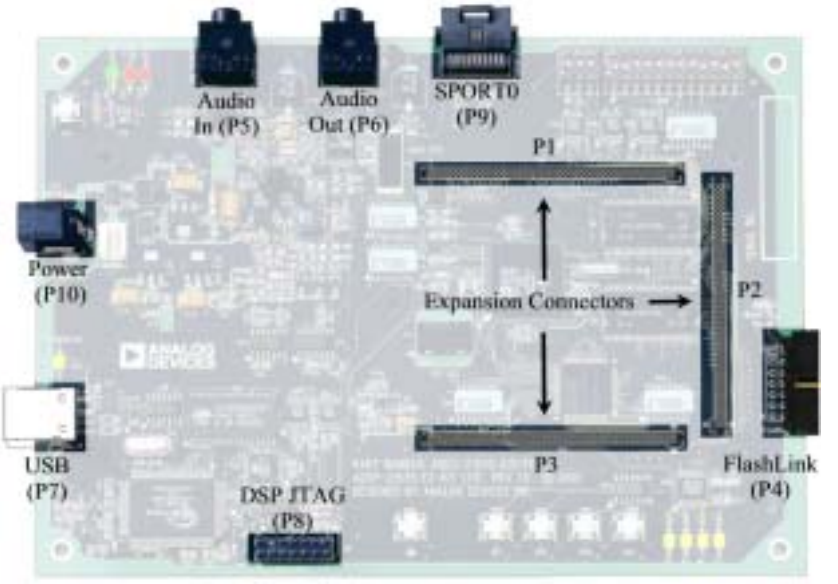


Figure 3-5. Connector Locations

Expansion Interface (P1, P2, P3)

Three board-to-board connector footprints provide signals for most of the DSP peripheral interfaces. Analog Devices does not populate these connectors or provide any additional support for this interface. For more information on the expansion interface, see “Expansion Interface” on page 3-4. Contact Samtec for the availability and pricing of the connectors.

Part Description	Manufacturer	Part Number
90 Position 0.05" Spacing (P1, P2, P3)	Samtec	SFM-145-01-S-D
Mating Connector		
90 Position 0.05" Spacing (Through Hole)	Samtec	TFM-145-x1 Series
90 Position 0.05" Spacing (Surface Mount)	Samtec	TFM-145-x2 Series
90 Position 0.05" Spacing (Low Cost)	Samtec	TFC-145 Series

FlashLINK (P4)

The FlashLINK connector allows you to configure and program the STMicroelectronics DSM2150 flash/PLD chip. See "Using Flash Memory" on page 2-5 for more information about using the FlashLINK connector.

Part Description	Manufacturer	Part Number
Right-angle 7X2 Shrouded 0.1 Spacing	TYCO	2-767004-2
Mating Assembly		
FlashLINK JTAG Programmer	ST Micro	L-101B

Audio (P5, P6)

There are two 3.5 mm stereo audio jacks: one input and one output.

Part Description	Manufacturer	Part Number
3.5 mm stereo jack (P5, P6)	Shogyo	SJ-0359AM-5

Part Description	Manufacturer	Part Number
Mating Cable		
3.5 mm stereo plug to 3.5 mm stereo cable	Radio Shack	42-2387A

USB (P7)

The USB connector is a standard Type B USB receptacle. This connector is used to debug the processor and is not connected to the processor's USB interface.

Part Description	Manufacturer	Part Number
Type B USB receptacle (P7)	Mill-Max	897-30-004-90-000
	Digi-Key	ED90003-ND
Mating Connector		
USB cable (provided with kit)	Assmann	AK672-5
	Digi-Key	AK672-5ND

JTAG (P8)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. When an emulator is connected to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

SPORT0 (P9)

SPORT0 is connected to a 20-pin connector. The pin-out for this connector can be found in "Schematics" on page B-1. Contact AMP for pricing and availability on these connectors.

Part Description	Manufacturer	Part Number
20 position AMPMODU system 50 receptacle (P9)	AMP	104069-1
Mating Connectors		
20 position AMPMODU ribbon cable connector	AMP	111196-4

Power Connector (P10)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm Power Jack (P10)	Switchcraft	RAPC712
	Digi-key	SC1152-ND
Mating Power Supply (shipped with EZ-KIT Lite)		
7.5V Power Supply	GlobTek	TR9CC2000LCP-Y

Specifications

This section provides the requirements for powering the board and the mechanical dimensions of the board.

Power Supply

The power connector supplies DC power to the EZ-KIT Lite board. Table 3-7 shows the power connector pin-out.

Table 3-7. Power Connectors

Terminal	Connection
Center pin	+7.5 VDC@2amps
Outer Ring	GND

Board Current Measurements

The ADSP-BF535 EZ-KIT Lite board provides eight zero-ohm resistors that may be removed to measure current draw. Table 3-8 shows the resistor number, the voltage plane, and a description of each component on the plane.

Table 3-8. Current Measurement Resistors

Resistor	Voltage Plane	Description
R2	VDD_RTC	DSP Real Time Clock Supply
R3	VDD_EXT	DSP External Interface Supply
R6	VDD_INT	DSP Internal Interface Supply
R7	VDD_PCIEXT	DSP PCI Interface Supply
R8	VDD_PLL	DSP Phase Lock Loop Supply
R110	5V	5V Supply
R111	3V	3V supply to all non DSP-related components
R113	3V_DSP	3V to DSP-related components

Mechanical Dimensions

Figure 3-6 shows the location of the mounting holes as well as the PIN1 of each of the expansion connectors.

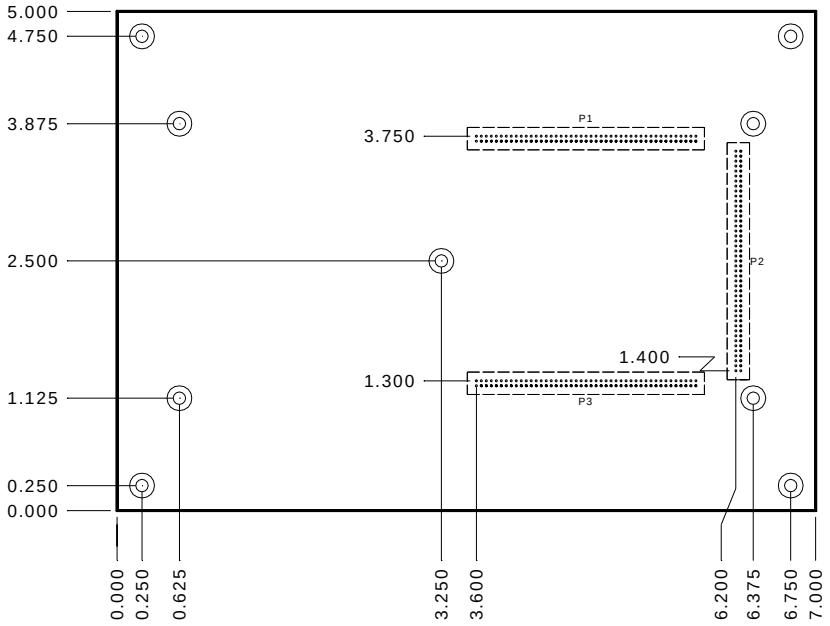


Figure 3-6. Mechanical Drawing

A BILL OF MATERIALS

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
2	3	74LVC14A SOIC14 HEX-INVER-SCHMITT-TRIGGER	U9-10, U19	TI	74LVC14AD
3	1	IDT74FCT3244APY SSOP20 3.3V-OCTAL-BUFFER	U24	IDT	IDT74FCT3244APY
4	1	24.576MHZ SMT OSC005 CRYSTAL	Y2	EPSON	MA505 24.576M-C2
5	1	CY7C64603-128 PQFP128 USB-TX/RX MICROCONTROL-LER	U11	CYPRESS	CY7C64603-128NC
6	1	MMBT4401 SOT-23 NPN TRANSISTOR 200MA	Q1	FAIRCHILD	MMBT4401
7	1	74LVC00AD SOIC14	U13	PHILIPS	74LVC00AD
8	1	24LC00-SN SOIC8 128 BIT SERIAL EEPROM	U25	MICROCHIP	24LC00-SN
9	1	ADP3331ART SOT23-6 ADJ 200MA REGULATOR	VR3	ANALOG DEVICES	ADP3331ART
10	3	BSS123 SOT23D NMOS FET	M1-3	FAIRCHILD	BSS123
11	1	CY7C1019BV33-15VC SOJ32 128K X 8 SRAM	U12	CYPRESS	CY7C1019BV33-12VC
12	1	SN74AHC1G02 SOT23-5 SINGLE-2 INPUT-NOR	U16	TI	SN74AHC1G02DBVR

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
13	1	SN74LV164A SOIC14 8-BIT-PARALLEL-SERIAL	U17	TI	SN74LV164AD
14	1	CY7C4201V-15AC TQFP32 64-BYTE-FIFO	U18	CYPRESS	CY7C4201V-15AC
15	1	12.0MHZ THR OSC006 CRYSTAL	Y3	DIG01	300-6027-ND
16	2	MT48LC4M16 TSOP54 4MX16-SDRAM-133MHZ	U5-6	MICRON	MT48LC4M16A2TG-75
17	1	32.768kHz TH OSC007 CRYSTAL	Y1	ECPLITEK	EC38T
18	1	SN74AHC1G00 SOT23-5 SINGLE-2-INPUT-NAND	U26	TI	SN74AHC1G00DBVR
19	1	21535 BRD DSM2150F5V U4"" BLKFIN160.OBJ SUM 876F5F1	U4	ST MICRO	DSM2150F5V
20	2	1000pF 50V 5% 1206 CERM	C25-26	AVX	12065A102JAT2A
21	2	0.1uF 50V 10% 1206 CERM	C8-9	PHILIPS	12062R104K9BB2
22	1	ADM708SAR SOIC8 VOLTAGE-SUPERVISOR	U23	ANALOG DEVICES	ADM708SAR
23	1	AD1885JST LQFP48 AC97 STEREO CODEC	U7	ANALOG DEVICES	AD1885JST
24	2	ADP3338AKC-33 SOT-223 3.3V-1.0AMP REGULATOR	VR1-2	ANALOG DEVICES	ADP3338AKC-3.3
25	1	ADP3339AKC-5 SOT-223 5V-1.5A REGULATOR	VR4	ANALOG DEVICES	ADP3339AKC-5-REEL
26	1	ADP3088 MSOP8 500MA-BUCK-REGULATOR	VR5	ANALOG DEVICES	ADP3088ARM-REEL
27	1	ADSP-21535PKB-300 PBGA260 308KBYTES-BLACKFIN	U1	ANALOG DEVICES	ADSP-21535PKB-300

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
28	5	RUBBER FEET BLACK	MH1-5	MOUSER	517-SJ-5018BK
29	1	PWR 2.5MM_JACK CON005 RA	P10	SWITCH-CRAFT	SC1152-ND12
30	1	USB 4PIN CON009 USB	P7	MILL-MAX	897-30-004-90-000000
31	1	.05 10X2 CON014 RA	P9	AMP	104069-1
32	6	SPST-MOMENTARY SWT013 6MM	SW3-8	PANASONIC	EVQ-PAD04M
33	1	DIP12 SWT014	SW2	DIGI-KEY	CKN3063-ND
34	1	DIP3 SWT015	SW1	DIGI-KEY	CKN3055-ND
35	1	IDC 7X2 IDC7X2SRDRA RIGHT ANGLE SHROUDED	P4	MOLEX	70247-1401
36	23	0.00 1/8W 5% 1206	R2-3, R6-12, R21, R63-64, R77, R97, R111-118, R127	YAGEO	0.0ECT-ND
37	2	220uF 10V 20% E ELEC	CT7-8	SPRAGUE	293D227X9010E2T
38	5	AMBER-SMT LED001 GULL-WING	LED1-5	PANASONIC	LN1461C-TR
39	2	22pF 50V 5% 805 CERM	C5-C6	AVX	08055A220JAT

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
40	79	0.01uF 100V 10% 805 CERM	C19, C30-92, C94, C96-97, C99-109, C116	AVX	08051C103KAT2A
41	1	0.22uF 25V 10% 805 CERM	C114	AVX	08053C224FAT
42	5	0.1uF 50V 10% 805 CERM	C3, C24, C27-29	AVX	08055C104KAT
43	4	10uF 16V 10% C TANT	CT15-18	SPRAGUE	293D106X9025C2T
44	44	10K 100MW 5% 805	R1, R13-19, R31-32, R37, R44-45, R47-54, R57, R59-61, R66, R68, R78-81	AVX	CR21-103J-T
45	44	10K 100MW 5% 805	R83-84, R87-88, R90-93, R105, R120-122, R125	DALE	CRCW0805-103JRT1
46	4	33 100MW 5% 805	R4-5, R46, R119	AVX	CR21-330JTR
47	5	4.7K 100MW 5% 805	R55-56, R58, R62, R107	AVX	CR21-4701F-T
48	1	1M 100MW 5% 805	R41	AVX	CR21-1004F-T

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
49	1	1.5K 100MW 5% 805	R43	AVX	CR21-1501F-T
50	1	22uF 16V 10% D TANT	CT1	DIG01	PCT3226CT-ND
51	3	2.21K 1/8W 1% 1206	R30, R35, R40	AVX	CR32-2211F-T
52	4	10uF 16V 10% B TANT	CT4, CT19-21	AVX	TAJB106K016R
53	1	1A HSM160J DO-214AA SCHOTTKY	D4	MICRO-SEMI	HSM160J
54	5	100 100MW 5% 805	R67, R82, R85-86, R89	AVX	CR21-101J-T
55	1	1000 100MHZ 1.5A FER002 0.06 CHOKE	FER9	MURATA	PLM250S40T1
56	3	2A S2A_RECT DO-214AA SILICON RECTIFIER	D1-3	GENER-ALSEMI	S2A
57	8	600 100MHZ 500MA 1206 0.70 BEAD	FER1-8	DIGIKEY	240-1019-1-ND
58	1	0.047UF 16V 10% 1206	C10	AVX	12065C473JATME
59	2	270PF 50V 10% 805	C11, C13	KEMET	C1206C271J5GAC210
60	6	1UF 16V 10% 805 X7R	C4, C22, C110-113	MURATA	GRM40X7R105K016AL
61	6	470PF 100V 10% 1206 CERM	C12, C14-16, C20-21	AVX	12061A471JAT2A
62	2	30PF 100V 5% 1206	C17-18	AVX	12061A300JAT2A
63	3	10UF 25V +80-20% 1210 Y5V	C93, C95, C98	MURATA	GRM235Y.5V106Z025

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
64	1	0.47UF 20V 10% A TANT	CT14	KEMET	T491A474K025AS
65	1	16K 1/8W5% 1206	R65	DALE	CRCW1206-163JRT1
66	1	53.6K 1/10W 1% 805	R95	PHILIPS	9C08052A5362FKRT/R
67	1	165K 1/10W 1% 805	R102	PHILIPS	9C08052A1653FKRT/R
68	1	316K 1/10W 1% 805	R103	PHILIPS	9C08052A3163FKRT/R
69	1	332K 1/10W 1% 805	R101	PHILIPS	9C08052A3323FKRT/R
70	1	665K 1/10W 1% 805	R100	PHILIPS	9C08052A6653FKRT/R
71	1	10UH 47+/-20 IND001	L1	TDK	SLF7045T-100M1R1-2
72	1	243.0K 1/10W 1% 805	R106	PHILIPS	9C08052A2433FKRT/R
73	1	1.00M 1/4W 1% 1210	R108	PANASONIC ECG	ERJ-14NF1004U
74	3	10K 31MW 5% RNET8	RN6-8	CTS	746X101103J
75	2	39PF 50V 5% 805 NPO	C1-C2	PANASONIC	ECJ-2VC1H390J
76	5	10K 100MW 2% RNET16 BUSSED	RN1-5	CTS	767-161-103G
77	1	1K 1/8W 5% 1206	R38	AVX	CR32-102J-T
78	6	10K 1/8W 5% 1206	R23-27, R33	DALE	CRCW1206-1002FRT1
79	1	100K 1/8W 5% 1206	R109	DALE	CR1206-1003FTR1
80	1	20.0K 1/8W 1% 1206	R104	DALE	CRCW1206-2002FRT1
81	3	22 1/8W 5% 1206	R36, R39, R126	DALE	CR1206-22R0JTR
82	7	270 1/8W 5% 1206	R69-73, R75-76	AVX	CR32-271J-T
83	4	4.7K 1/8W 5% 1206	R20, R22, R28-29	AVX	CR32-472J-T

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
84	1	680 1/8W 5% 1206	R74	AVX	CR32-681J-T
85	1	20MHZ 1/2 OSC001	U2	ECLIPTEK	EC1100HS-20.000MHZ
86	2	RED-SMT LED001 GULL-WING	LED7-8	PANASONIC	LN1261C
87	1	GREEN-SMT LED001 GULL-WING	LED6	PANASONIC	LN1361C
88	5	1uF 25V 20% A TANT -55+125	CT9-13	PANASONIC	ECS-T1EY105R
89	5	QS3257Q QSOP16 QUICKSWITCH-257	U14-15, U20-22	ANALOG DEVICES	ADG774ABRQ
90	1	IDC 3X1 IDC3X1	JP2	BERG	54101-T08-03
91	1	IDC 3X2 IDC3X2	JP1	BERG	54102-T08-03
92	1	IDC 7X2 IDC7X2	P8	BERG	54102-T08-07
93	3	IDC 2PIN_JUMPER 0.1	SJ1-3	MOLEX	15-38-1024
94	1	2.5A RESETABLE FUS001	F1	RAYCHEM CORP.	SMD250-2
95	2	3.5MM STEREO_JACK CON001	P5-6	A/D ELEC-TONICS	ST-323-5

ADSP-BF535 EZ-KIT LITE

Approvals	Date
Drawn	
Checked	
Engineering	

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20 Cotton Road
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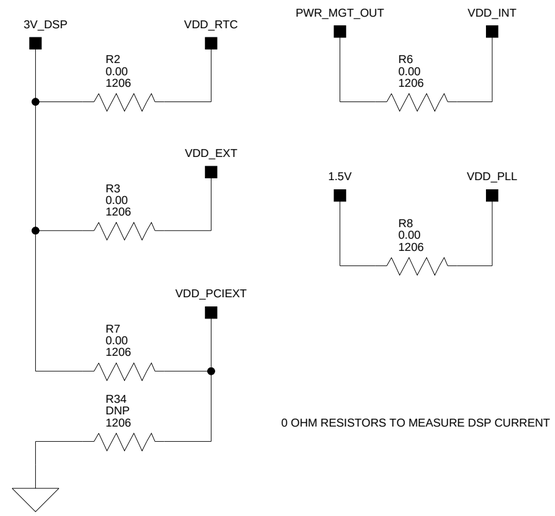
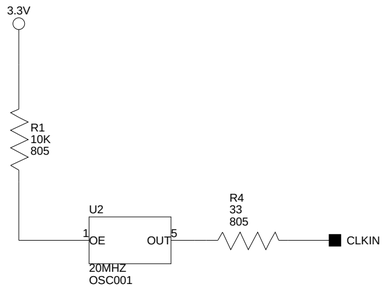
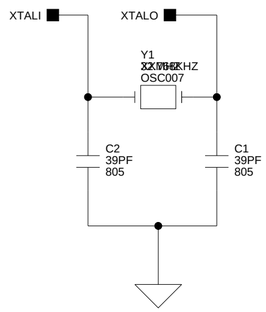
Title	ADSP-BF535 EZ-KIT LITE - TITLE		
Size C	Board No. A0162-2000		Rev 1.6
Date 3-12-2003_15:48		Sheet 1 of 12	

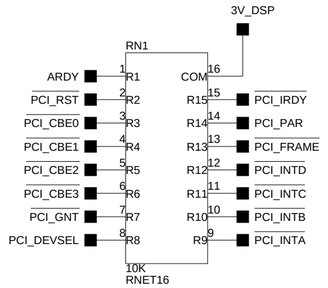


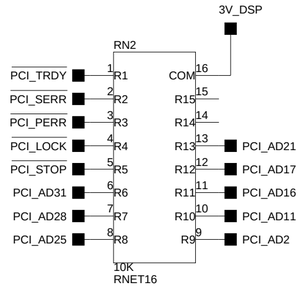
0 OHM RESISTORS TO MEASURE DSP CURRENT

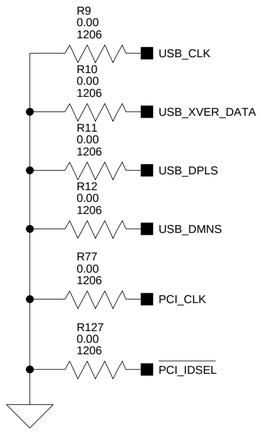


FOR RTC









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Approvals	Date
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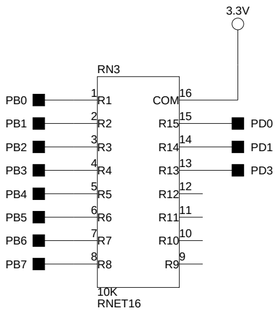
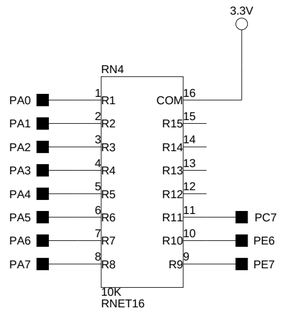
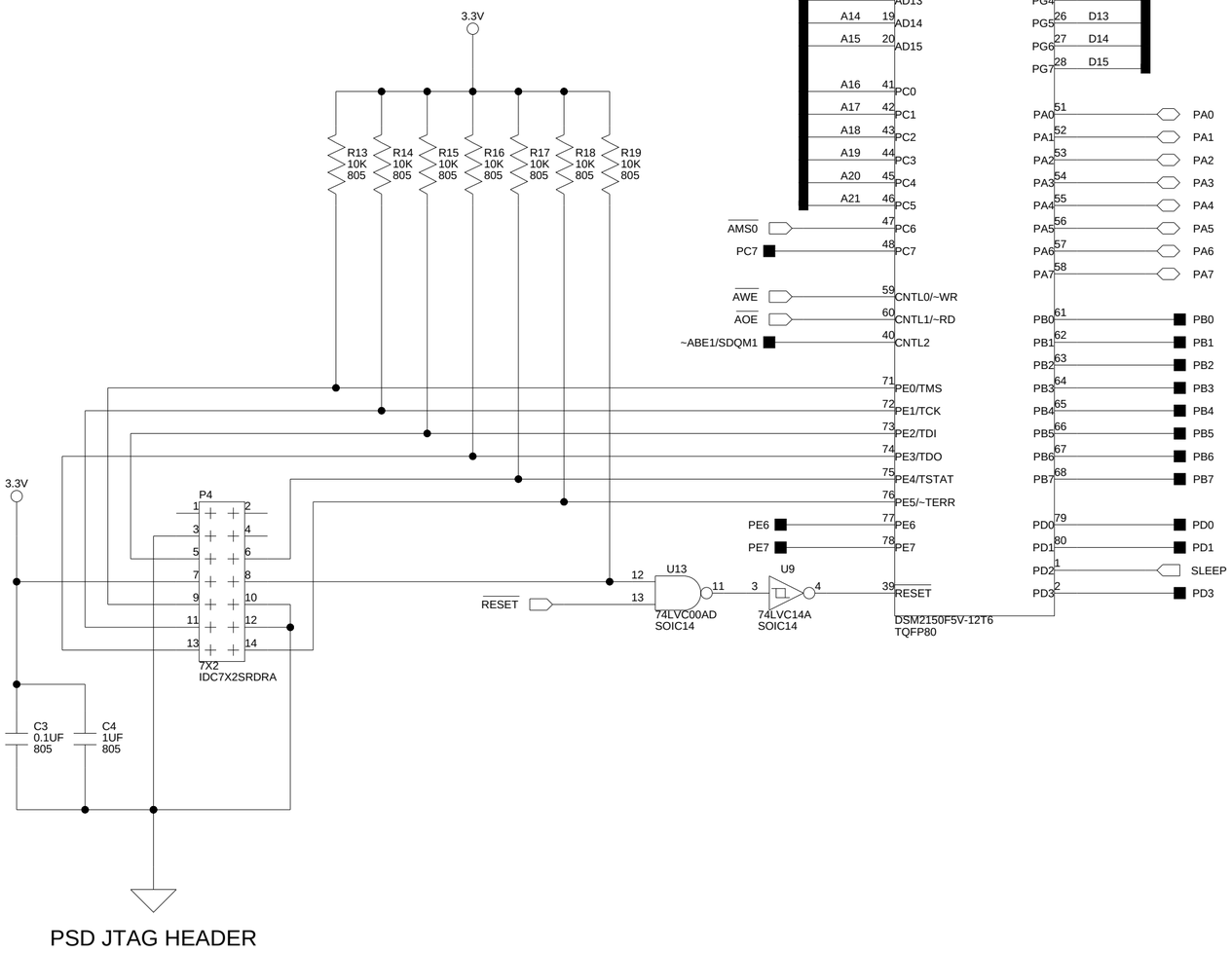
Title: ADSP-BF535 EZ-KIT LITE - DSP

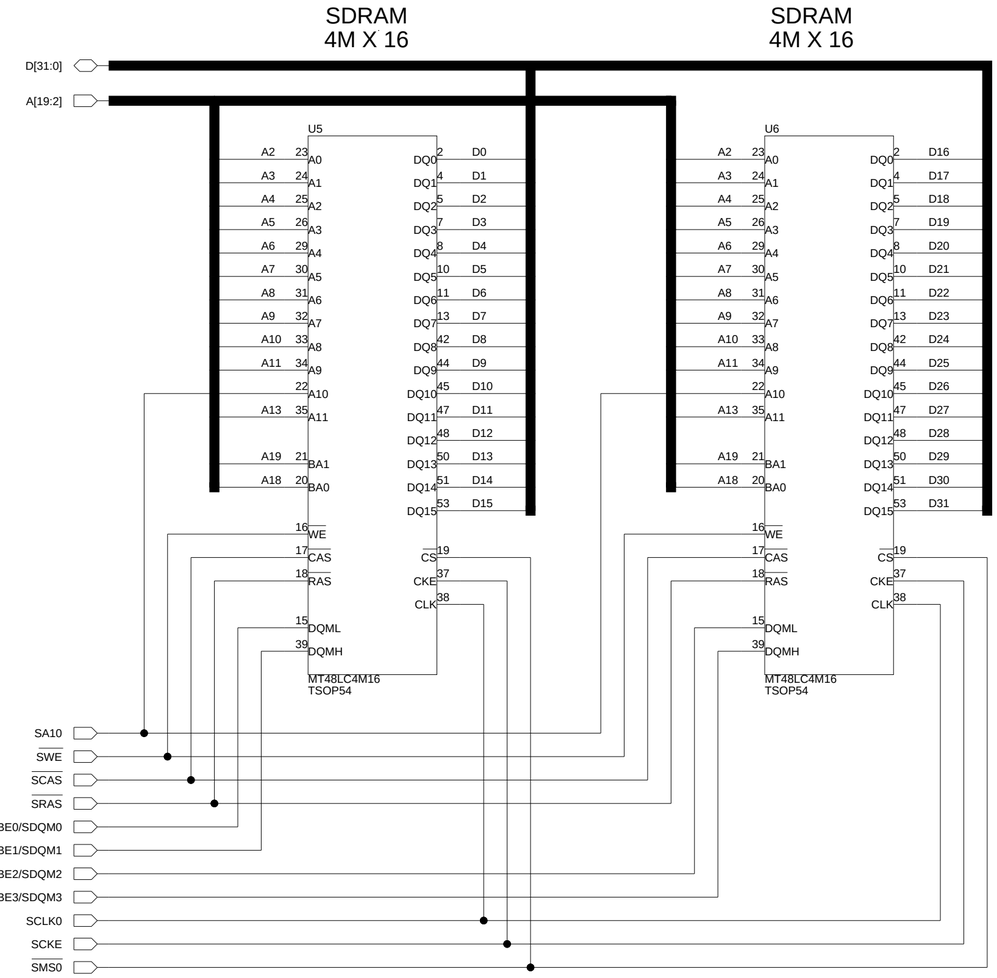
Size	Board No.	Rev
C	A0162-2000	1.6

Date: 3-25-2003_9:50 Sheet 2 of 12









Approvals	Date
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Checked	
Engineering	

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Title: ADSP-BF535 EZ-KIT LITE - DSP MEMORY

Size	Board No.	Rev
C	A0162-2000	1.6

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AUDIO CODEC
AD1885

SJ2
SHORTING JUMPER
DEFAULT=4 & 6

SJ1
SHORTING JUMPER
DEFAULT=3 & 5

JP1 SETTINGS

	SJ1	SJ2	INPUT SOURCE
*	1 & 3	2 & 4	MIC IN
	3 & 5	4 & 6	LINE IN

* Denotes Default Setting

LINE IN/MIC
P5
CON001
HEAD PHONE OUT
P6
CON001

JP1
FER1 600 1206
FER2 600 1206
FER3 600 1206
FER4 600 1206
D5 VC0805 40A 805
D6 VC0805 40A 805
D7 VC0805 40A 805
D8 VC0805 40A 805
C15 470PF 1206
C14 470PF 1206
C12 470PF 1206
C16 470PF 1206
R29 4.7K 1206
R22 4.7K 1206
R28 4.7K 1206
R20 4.7K 1206
R27 10K 1206
R33 10K 1206
C112 1UF 805
C113 1UF 805
POPULATE TO COMPLY WITH PC99
R21 0.00 1206
ALT_VAL=1K
C7 0.01UF 1206 DNP
C114 0.22UF 805
R30 2.21K 1206
CT4 10UF B
CT7 220UF E
CT8 220UF E
C8 0.1UF 1206
C11 270PF 805
C13 270PF 805
C110 1UF 805
C111 1UF 805
C10 0.047UF 1206
C9 0.1UF 1206
TP1
TP2
TP3
AGND
SHGND
A5V
3.3V

U7
AD1885JST LQFP48

	Analog Signals	Digital Signals
25	AVDD1	
38	AVDD2	
43	AVDD3	
26	AVSS1	
40	AVSS2	
44	AVSS3	
27	VREF	
28	VREFOUT	
30	AFILT2	
29	AFILT1	
32	FILT_L	
31	FILT_R	
33	RX3D	
34	CX3D	
22	MIC2	
21	MIC1	
24	LINE_IN_R	
23	LINE_IN_L	
36	LINE_OUT_R	
35	LINE_OUT_L	
37	MONO_OUT	
41	HP_OUT_R	
39	HP_OUT_L	
1		VDD1
9		VDD2
4		VSS1
7		VSS2
2		XTAL_IN
3		XTL_OUT
8		SDATA_IN
5		SDATA_OUT
6		BIT_CLK
10		SYNC
11		RESET
46		ID1
45		ID0
48		JS1
47		JS0
12		PC_BEEP
13		PHONE_IN
14		AUX_L
15		AUX_R
16		VIDEO_L
17		VIDEO_R
18		CD_L
20		CD_R
19		CD_GND_REF

Y2 24.576MHZ OSC005
C6 22PF 805
C5 22PF 805
R114 0.00 1206
R118 0.00 1206
DR0
DT0
TCLK0
RFS0
RCLK0
R26 10K 1206
R25 10K 1206
R23 10K 1206
R24 10K 1206

JP2: 1885 DISABLE

	1 & 2	DISABLE AD1885
*	2 & 3	NORMAL OPERATION

* DENOTES DEFAULT SETTING

JP2
IDC3X1
SJ3
SHORTING JUMPER
DEFAULT=1 & 2
PF15
R32 10K 805
R31 10K 805
W1 COPPER
R112 0.00 1206
DNP

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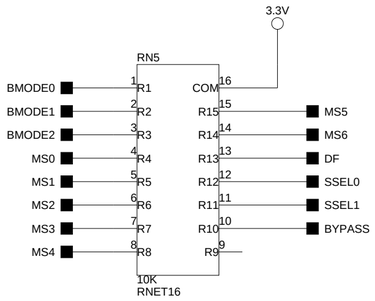
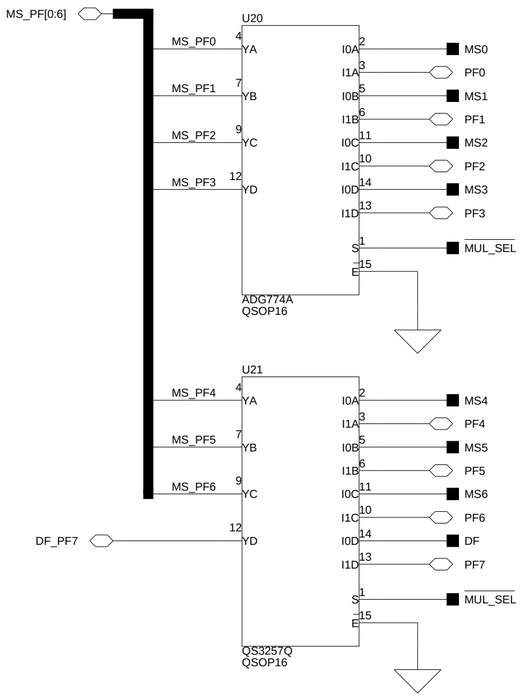
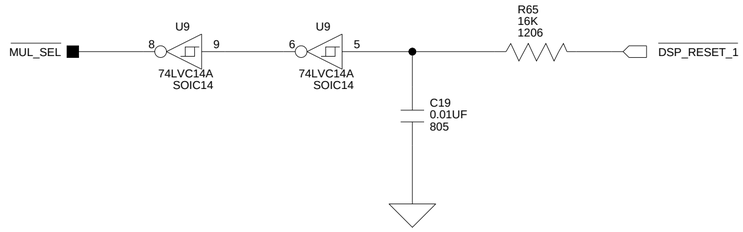
Title: ADSP-BF535 EZ-KIT LITE - AUDIO CODEC

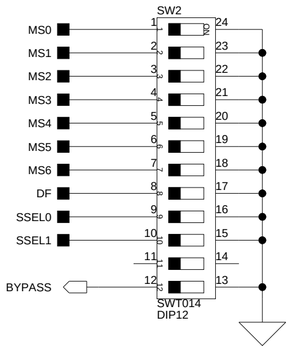
Size	Board No.	Rev
C	A0162-2000	1.6

Date: 3-21-2003_12:05 Sheet 4 of 12







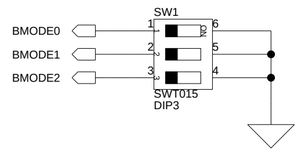


SW2: CLOCK MULTIPLIER SELECT SWITCH

1	2	3	4	5	6	7	8	9	10	11	12
OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	ON	ON

DEFAULT SETTINGS:
Internal Clock - 15:1 - 300MHZ
External Clock - 2.5:1 - 120MHZ

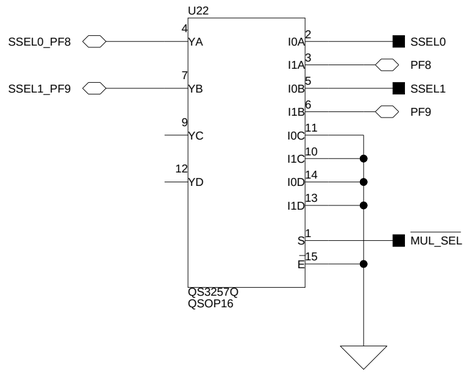
REFER TO DSP HARDWARE REFERENCE FOR DETAILED SETTING INFOMATION

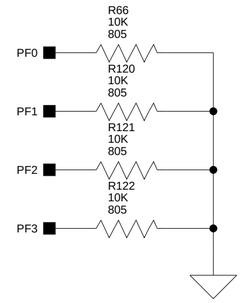


SW1 SETTINGS: BOOT MODE SELECTION

	BMODE2	BMODE1	BMODE0	BOOT MODE
*	ON	ON	ON	EXECUTE 16-BIT EXTERNAL
	ON	ON	OFF	8-BITS ROM
	ON	OFF	ON	SPI0 ROM (8-BIT ADDRESS)
	ON	OFF	OFF	SPI0 ROM (16-BIT ADDRESS)
	OFF	-	-	ALL OTHERS RESERVED

* = DEFAULT





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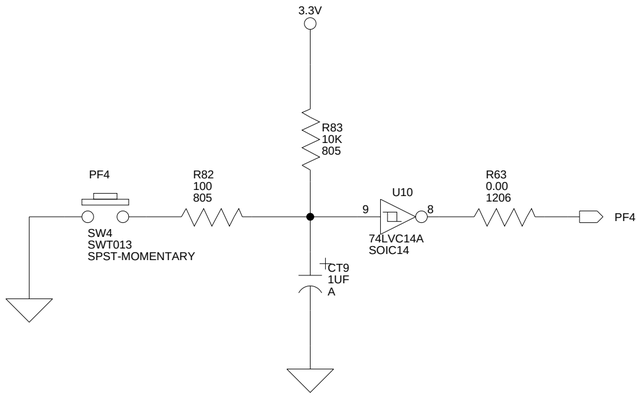
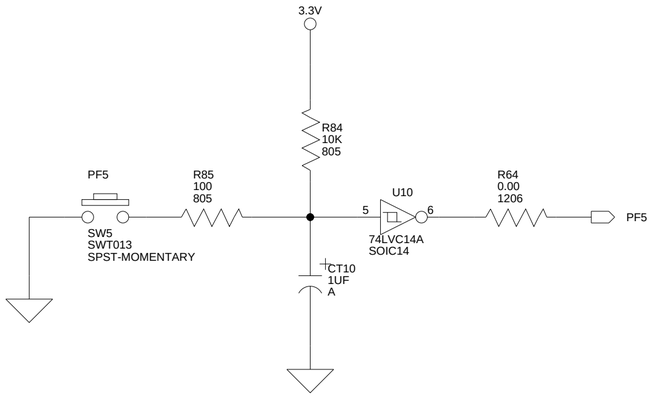
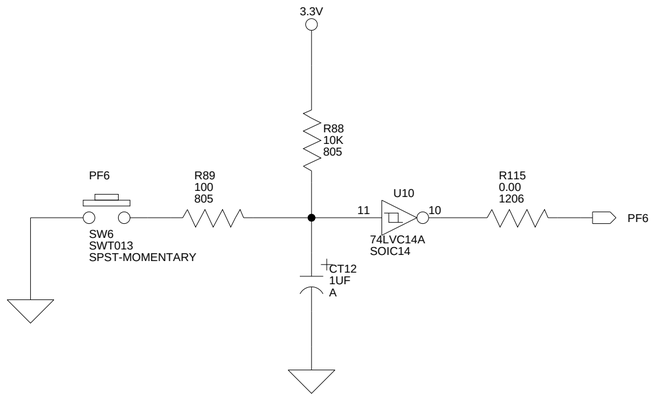
Title: ADSP-BF535 EZ-KIT LITE - CONFIG

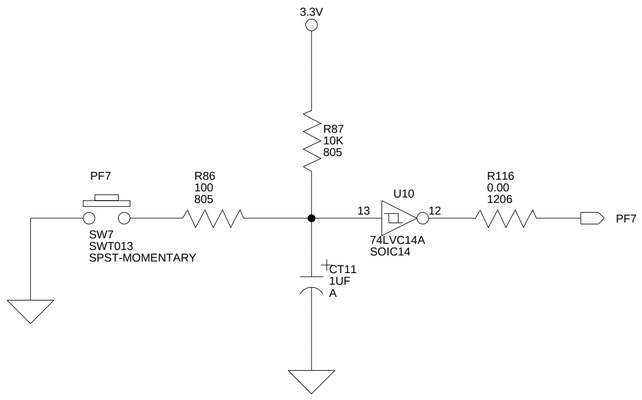
Size	Board No.	Rev
C	A0162-2000	1.6

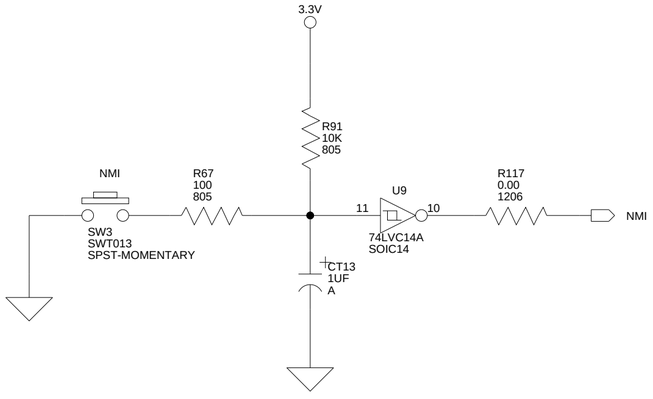
Date: 3-12-2003_15:48 Sheet 5 of 12

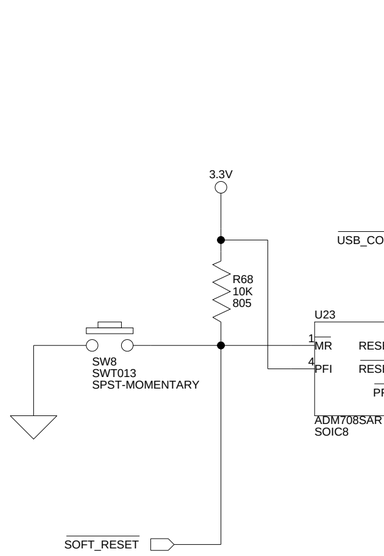


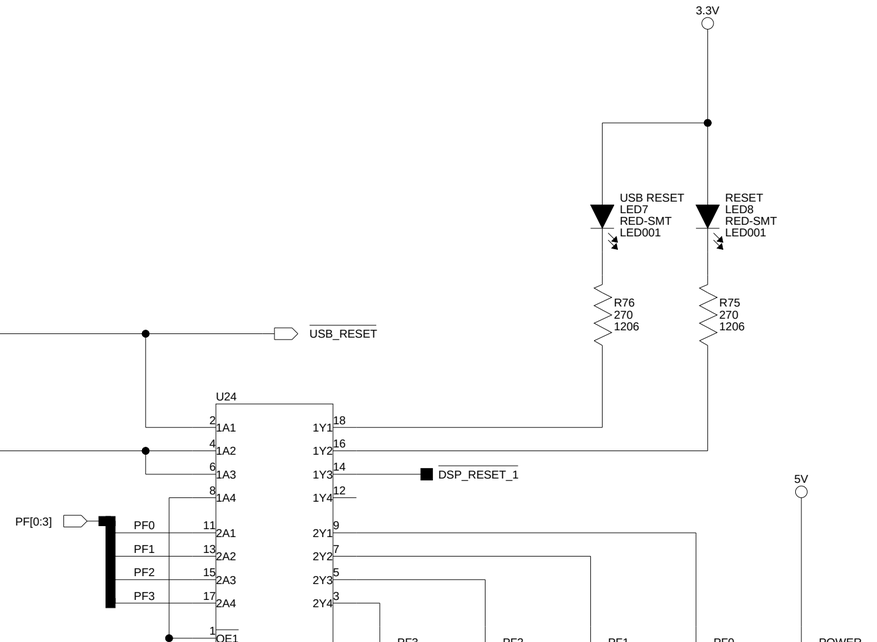


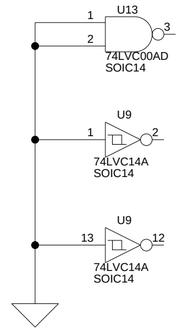


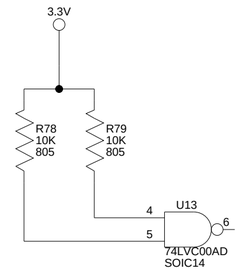


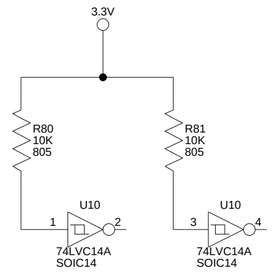












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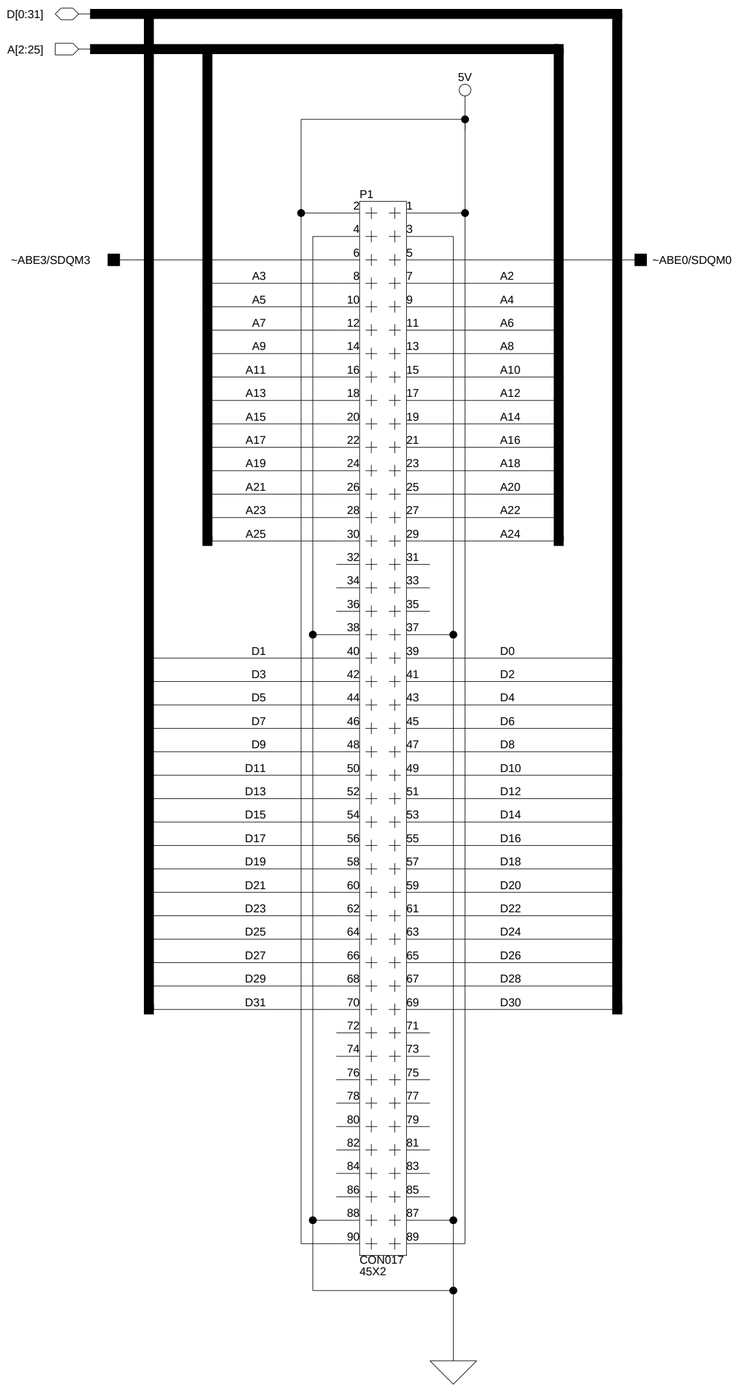
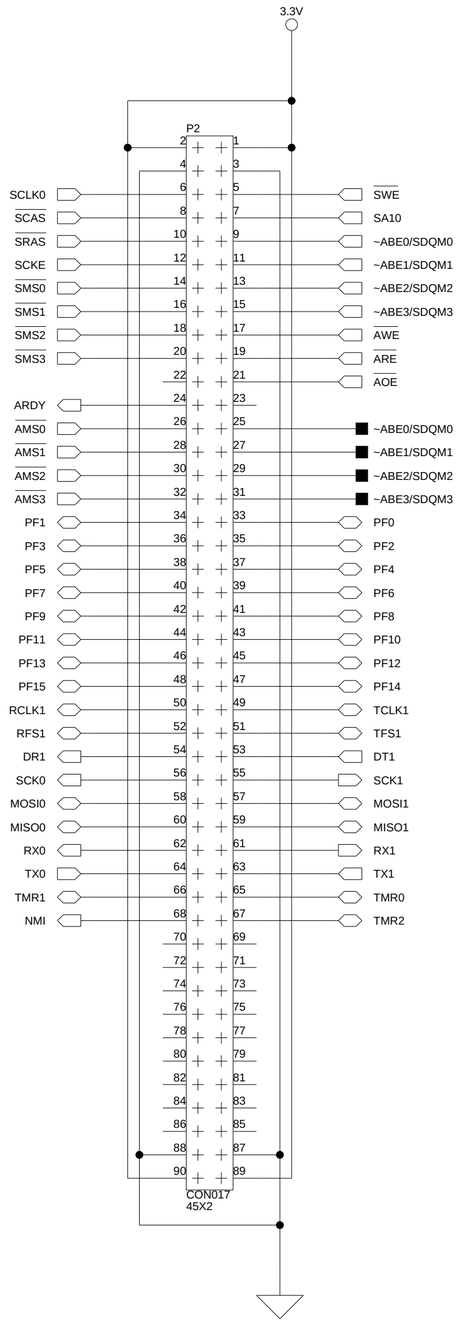
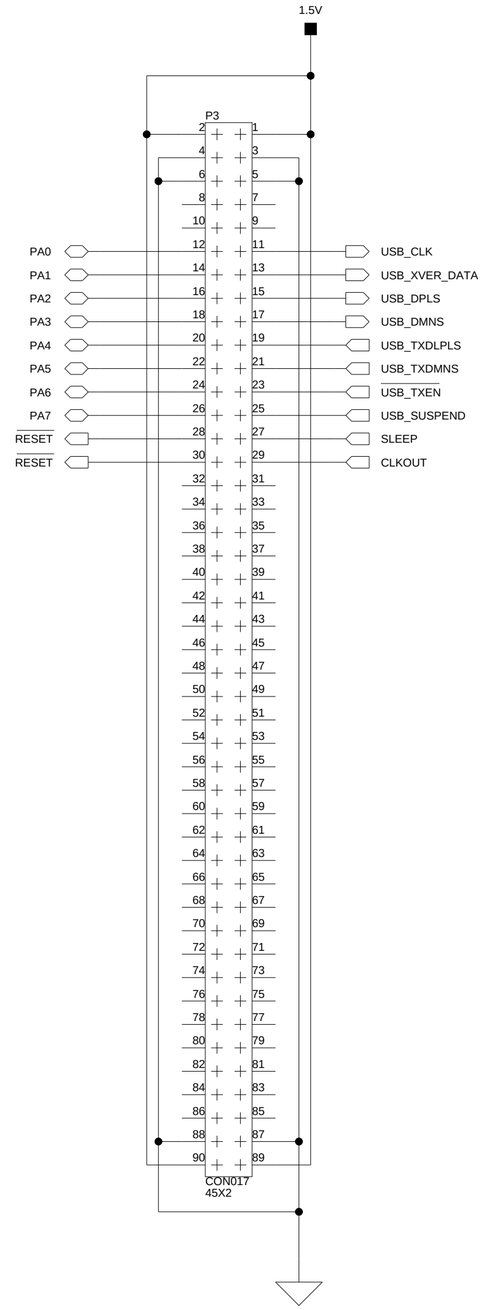
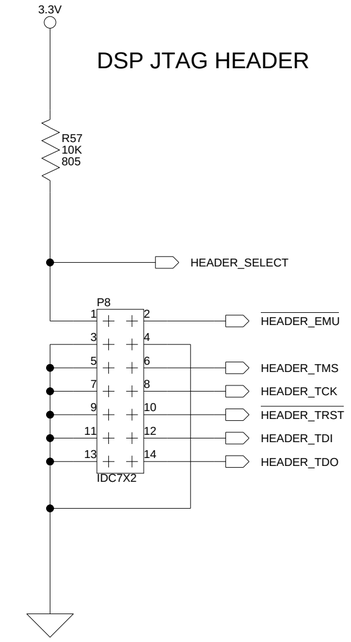
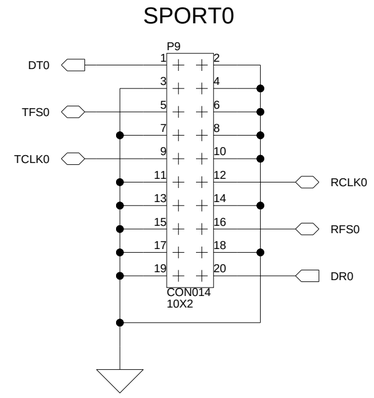
Title	ADSP-BF535 EZ-KIT LITE - RESET/PB/LED		
Size C	Board No. A0162-2000		Rev 1.6
Date 3-13-2003_19:50		Sheet 6 of 12	











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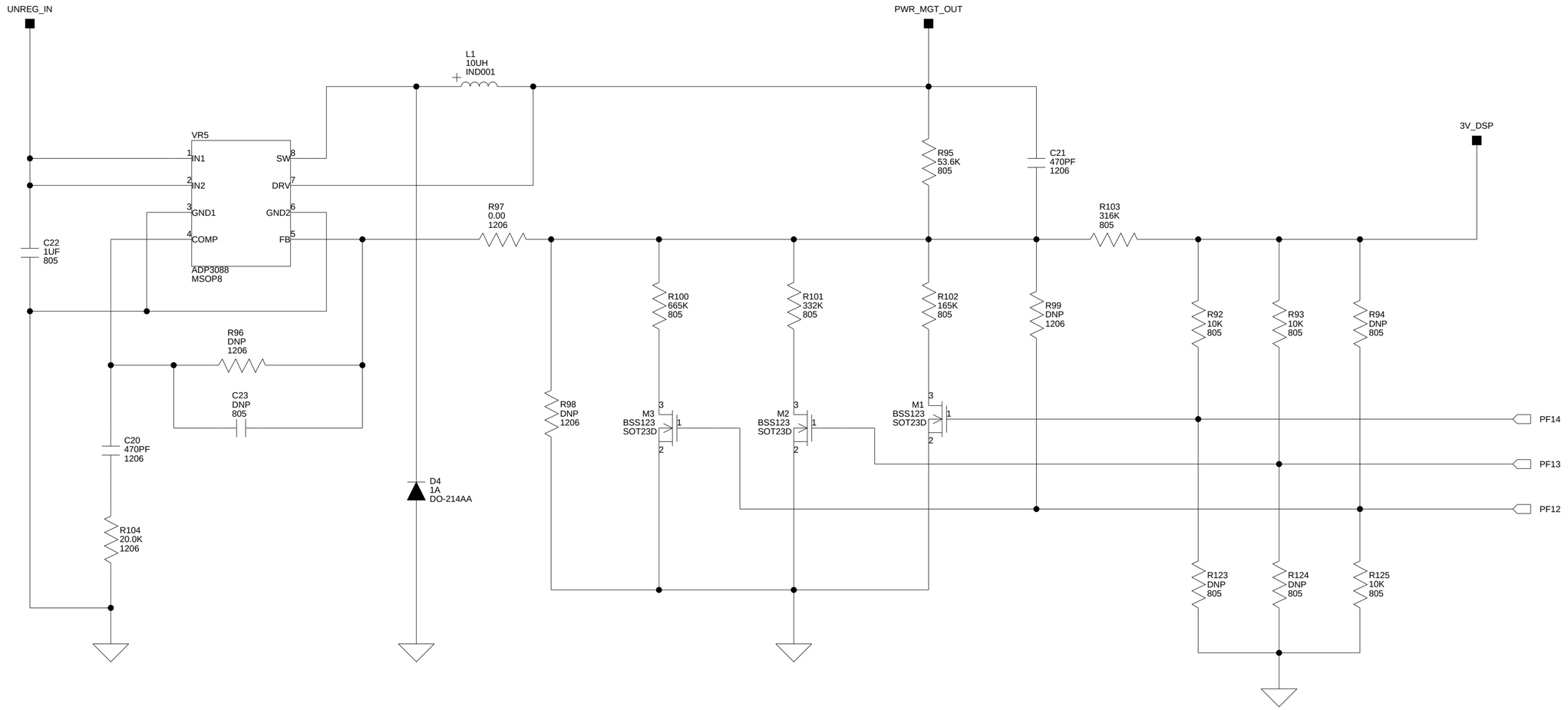
Title	ADSP-BF535 EZ-KIT LITE - CONNECTORS		
Size C	Board No. A0162-2000		Rev 1.6
Date 3-13-2003_19:50		Sheet 7 of 12	

PF14	PF13	PF12	VDD_INT	
1	1	1	1.6V	
1	1	0	1.5V	*
1	0	1	1.4V	
1	0	0	1.3V	
0	1	1	1.2V	
0	1	0	1.1V	
0	0	1	1.0V	
0	0	0	0.9V	

* = DEFAULT
WAIT 100uS FOR VOLTAGE TO SETTLE
AFTER CHANGING PF11-9



Approvals	Date
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ANALOG DEVICES
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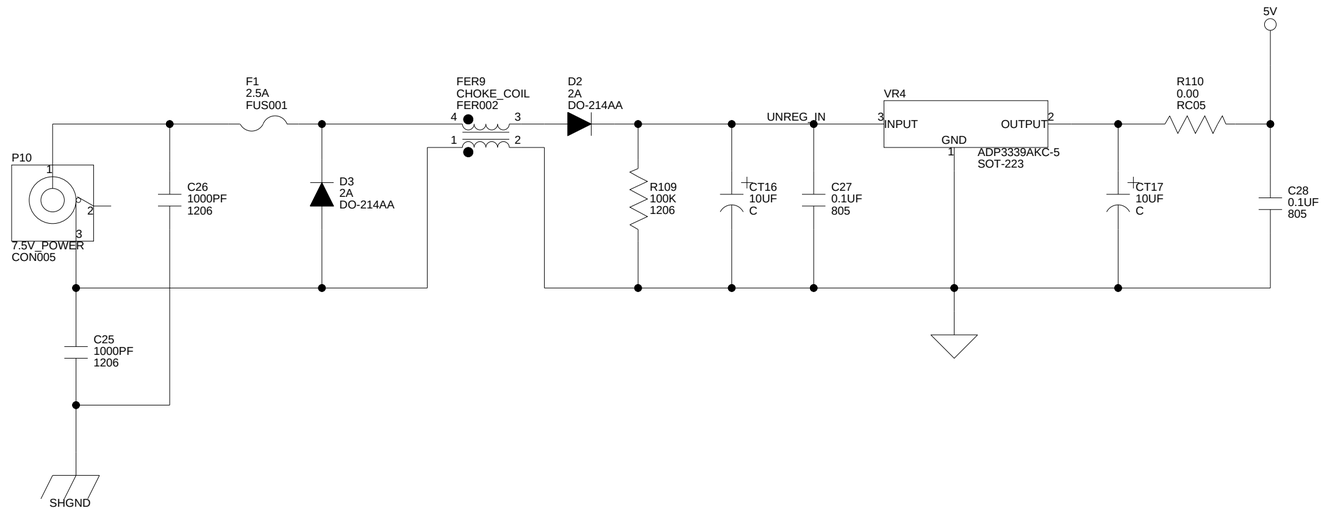
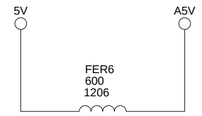
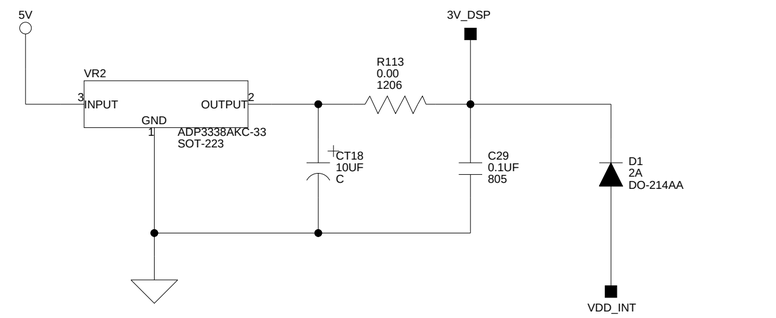
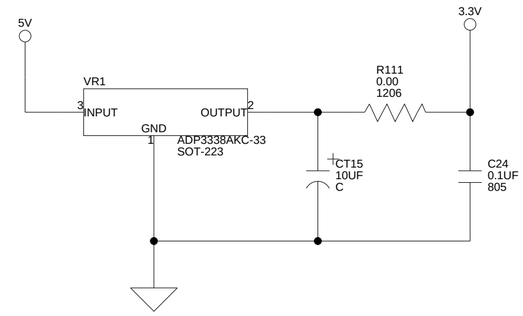
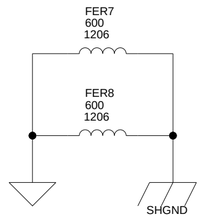
Title	ADSP-BF535 EZ-KIT LITE - POWER 1		
Size C	Board No. A0162-2000		Rev 1.6
Date 3-12-2003_15:48		Sheet 8 of 12	

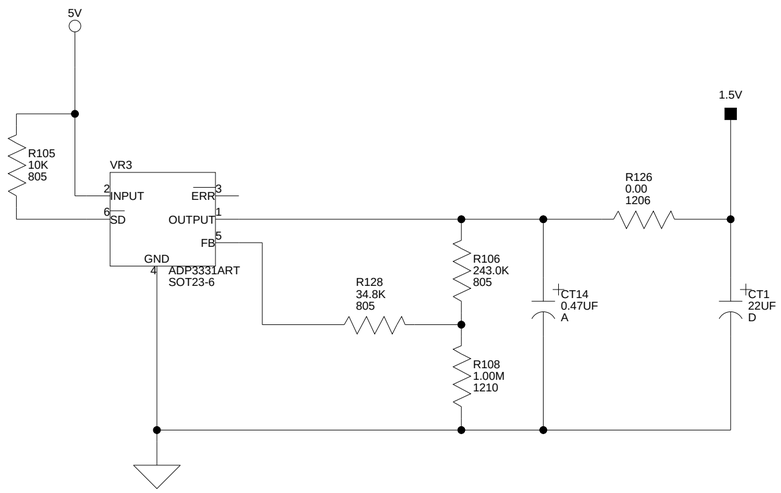


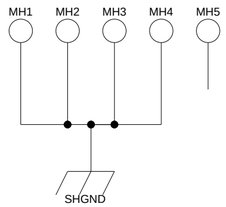












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Title: ADSP-BF535 EZ-KIT LITE - POWER 2		
Size: C	Board No.: A0162-2000	Rev: 1.6
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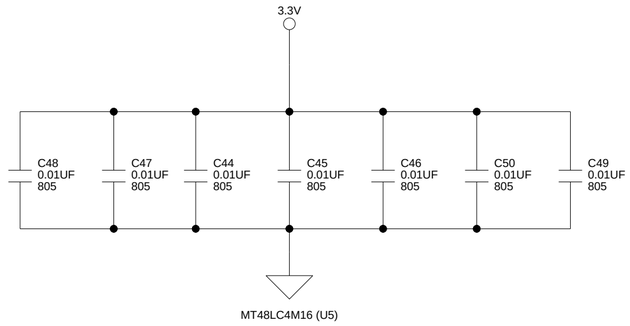

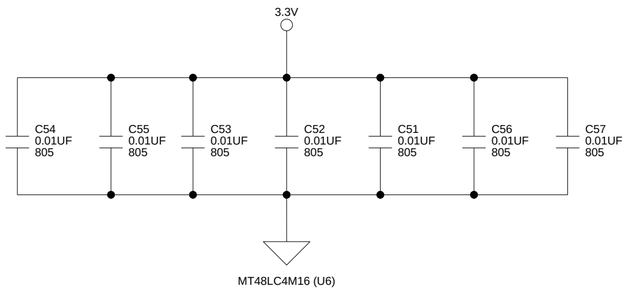

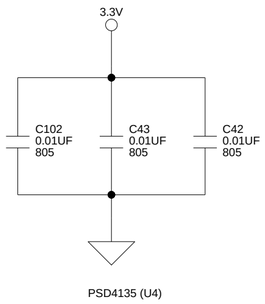

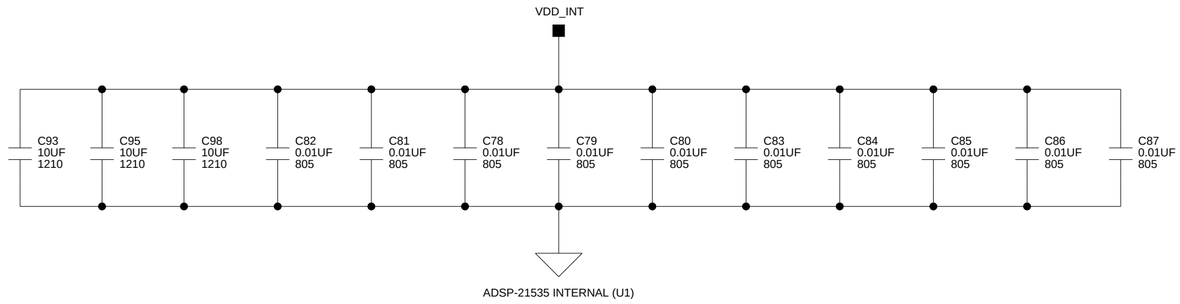

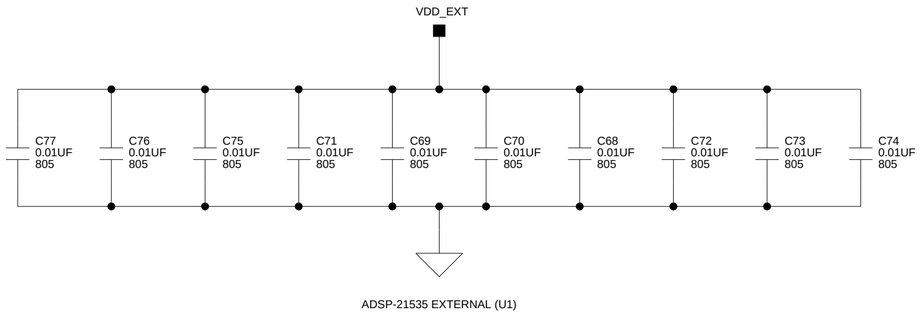

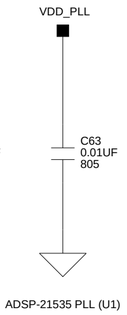

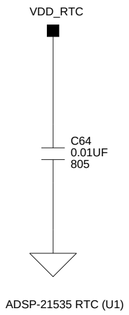

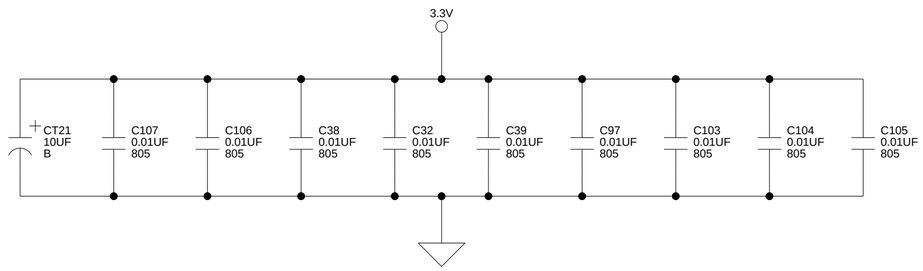

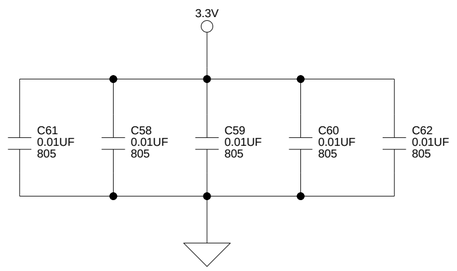

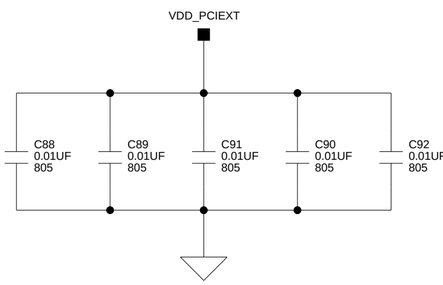

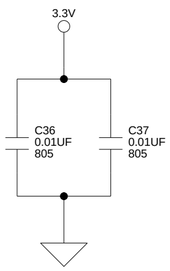

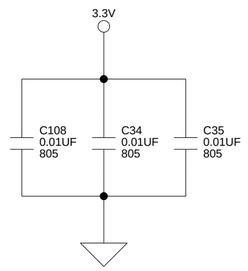

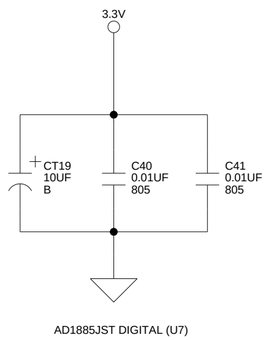

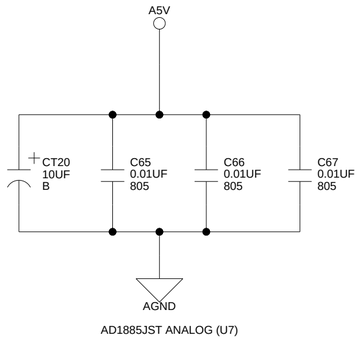

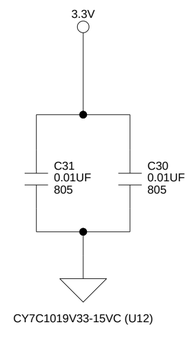

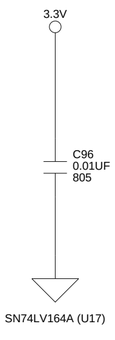

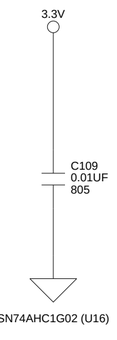

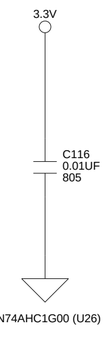

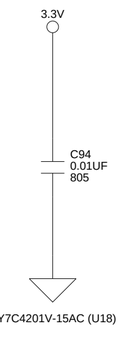

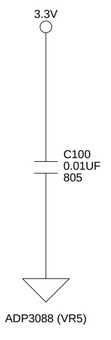

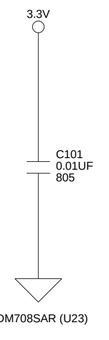

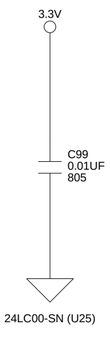

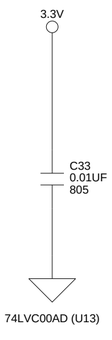

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Title	ADSP-BF535 EZ-KIT LITE - BYPASS CAPS		
Size C	Board No. A0162-2000		Rev 1.6
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All USB interface circuitry is considered proprietary
and has been omitted from this schematic

When designing your JTAG interface please refer to
the Engineer to Engineer Note EE-68 which can be found at
http://www.analog.com

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Size	Board No.	Rev
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