ABOUT ADSP-CM402F/CM403F/CM407F/CM408F/CM409F SILICON ANOMALIES

These anomalies represent the currently known differences between revisions of the ADSP-CM402F/CM403F/CM407F/CM408F/CM409F product(s) and the functionality specified in the ADSP-CM402F/CM403F/CM407F/CM408F/CM409F data sheet(s) and the Hardware Reference book(s).

PRODUCT REVISIONS

A product revision letter with the form "-x" is branded on all parts. The implementation field bits <31:28> of the JTAG0_IDCODE register can be used to differentiate the revisions as shown below.

<table>
<thead>
<tr>
<th>Product REVISION</th>
<th>JTAG0_IDCODE&lt;31:28&gt;</th>
<th>Analog Front End (AFE) ID*</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>0x2</td>
<td>0x3</td>
</tr>
<tr>
<td>D</td>
<td>0x1</td>
<td>0x3</td>
</tr>
<tr>
<td>0.0</td>
<td>0x0</td>
<td>0x0</td>
</tr>
</tbody>
</table>

* = The adi_adcc_ReadAFEID API software driver can be used to read Analog Front End ID

ANOMALY LIST REVISION HISTORY

The following revision history lists the anomaly list revisions and major changes for each anomaly list revision.

<table>
<thead>
<tr>
<th>Date</th>
<th>Anomaly List Revision</th>
<th>Data Sheet Revision</th>
<th>Additions and Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>05/19/2015</td>
<td>F</td>
<td>PrG</td>
<td>Added Anomalies: 17000029, 17000030, 17000031</td>
</tr>
<tr>
<td>04/02/2015</td>
<td>E</td>
<td>PrG</td>
<td>Added Anomalies: 17000027, 17000028</td>
</tr>
<tr>
<td>12/15/2014</td>
<td>D</td>
<td>PrF</td>
<td>Added Anomalies: 17000025</td>
</tr>
<tr>
<td>10/7/2014</td>
<td>C</td>
<td>PrF</td>
<td>Added Anomalies: 17000004, 17000013, 17000014, 17000015, 17000016, 17000019, 17000020, 17000021, 17000022, 17000023, 17000024</td>
</tr>
<tr>
<td>08/26/2014</td>
<td>B</td>
<td>PrF</td>
<td>Added Anomalies: 17000004, 17000013, 17000014, 17000015, 17000016, 17000019, 17000020, 17000021, 17000022, 17000023, 17000024</td>
</tr>
<tr>
<td>09/17/2013</td>
<td>A</td>
<td>PrE</td>
<td>Initial Version</td>
</tr>
</tbody>
</table>
# SUMMARY OF SILICON ANOMALIES

The following table provides a summary of ADSP-CM402F/CM403F/CM407F/CM408F/CM409F anomalies and the applicable product revision(s) for each anomaly.

<table>
<thead>
<tr>
<th>No.</th>
<th>ID</th>
<th>Description</th>
<th>0.0</th>
<th>D</th>
<th>H</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>17000002</td>
<td>Minimum operating clock frequency of ADC is 44MHz</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>2</td>
<td>17000003</td>
<td>After emulation event, PWM outputs resume without clearing PWM_STAT.EMU bit</td>
<td>x</td>
<td>x</td>
<td>.</td>
</tr>
<tr>
<td>3</td>
<td>17000004</td>
<td>Capture Timer is not implemented</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>4</td>
<td>17000005</td>
<td>EMUID registers are not functional</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>5</td>
<td>17000006</td>
<td>Cache Pre-fetching is not functional</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>6</td>
<td>17000008</td>
<td>Oscillator Watchdog is not functional</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>7</td>
<td>17000009</td>
<td>Security feature is not implemented</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>8</td>
<td>17000010</td>
<td>ADC loopback via DAC is not implemented</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>9</td>
<td>17000011</td>
<td>Restriction in using Ethernet MAC and SMC simultaneously</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>10</td>
<td>17000013</td>
<td>The setup time of USB0_ID signal deviates from the specification of all other system inputs</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>11</td>
<td>17000014</td>
<td>Unexpected multiple DMA parity error</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>12</td>
<td>17000015</td>
<td>ADCC collision status is indicated for only one ADC in simultaneous sampling mode</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>13</td>
<td>17000016</td>
<td>SPI data pins are driven high in open drain mode</td>
<td>x</td>
<td>x</td>
<td>.</td>
</tr>
<tr>
<td>14</td>
<td>17000019</td>
<td>SPI1 master boot fails when invoked via ROM API</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>15</td>
<td>17000020</td>
<td>The debug reset module is not implemented in accordance with standard ARM tools</td>
<td>x</td>
<td>x</td>
<td>.</td>
</tr>
<tr>
<td>16</td>
<td>17000021</td>
<td>The software selection of SPI Slave Enable Signal does not drive to the programmed value in the Slave Select Register</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>17</td>
<td>17000022</td>
<td>SPI Transmit Collision Error may occasionally be missed</td>
<td>x</td>
<td>x</td>
<td>.</td>
</tr>
<tr>
<td>18</td>
<td>17000023</td>
<td>Offset Error and Gain Error of the ADCs deviate from the specification</td>
<td>x</td>
<td>x</td>
<td>.</td>
</tr>
<tr>
<td>19</td>
<td>17000024</td>
<td>SPORT0 A and TIMERO signals do not appear on Port E and Port D respectively</td>
<td>x</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>20</td>
<td>17000025</td>
<td>TIMER_DATA_ILAT bit is set in EXTCLK mode when TIMER_TMRn_CNT rolls over to 1</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>21</td>
<td>17000026</td>
<td>Analog Front End control bits are not initialized</td>
<td>.</td>
<td>x</td>
<td>.</td>
</tr>
<tr>
<td>22</td>
<td>17000027</td>
<td>RCU0_SRRQSTAT register is not affected by TRU’s System Reset Request</td>
<td>.</td>
<td>.</td>
<td>x</td>
</tr>
<tr>
<td>23</td>
<td>17000028</td>
<td>ECC Logic in Analog Front End Does Not Trigger a Fault</td>
<td>.</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>24</td>
<td>17000029</td>
<td>SPI data pins are internally pulled high in open drain mode</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>25</td>
<td>17000030</td>
<td>System DMAs do not halt in emulation mode</td>
<td>x</td>
<td>x</td>
<td>.</td>
</tr>
<tr>
<td>26</td>
<td>17000031</td>
<td>SPORT May Drive Data Pins During Inactive Channels in Multichannel Mode</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

Key: x = anomaly exists in revision  
    . = Not applicable
DETAILED LIST OF SILICON ANOMALIES

The following list details all known silicon anomalies for the ADSP-CM402F/CM403F/CM407F/CM408F/CM409F including a description, workaround, and identification of applicable product revisions.

1. **17000002 - Minimum operating clock frequency of ADC is 44MHz:**

   **DESCRIPTION:**
   The ADC clock frequency is calculated as:
   \[ \text{ADC Clock} = \frac{\text{SYSCLK}}{(\text{ADCC_TC0.CKDIV} + 1)} \]
   
   Due to the internal timing constraints in the Analog subsystem, the minimum ADC clock frequency is limited to 44MHz.

   **WORKAROUND:**
   None. User has to configure the ADC clock between 44MHz to 50MHz.

   **APPLIES TO REVISION(S):**
   0.0

2. **17000003 - After emulation event, PWM outputs resume without clearing PWM_STAT.EMU bit:**

   **DESCRIPTION:**
   When an Emulation event occurs with PWM_CTL.EMURUN bit cleared, the PWM timers are stopped internally and the PWM outputs are tripped (i.e., outputs are shutoff). When emulation event is de-asserted the PWM outputs should remain tripped until the PWM_STAT.EMU status bit is cleared.
   
   Due to this anomaly, PWM timers and outputs resume normal operation even without clearing the PWM_STAT.EMU bit.

   **WORKAROUND:**
   None.

   **APPLIES TO REVISION(S):**
   0.0, D

3. **17000004 - Capture Timer is not implemented:**

   **DESCRIPTION:**
   The Capture Timer can be configured to capture the total ON time of input signal between two pulses of trigger.
   
   This feature is not implemented. Hence, the Capture Timer signals do not appear on PORT B.

   **WORKAROUND:**
   None

   **APPLIES TO REVISION(S):**
   0.0, D
4. **17000005 - EMUID registers are not functional:**

**DESCRIPTION:**
The EMUID0_ADIID register located at 0x40002020 is used by debugger to confirm that the device they are connected to via Serial Wire is an implementation of the Cortex from ADI.

The EMUID0_CHIPID register located at 0x40002024 is unique to the implementation of the Cortex-M series.

These registers are not functional and cannot be accessed.

**WORKAROUND:**
None.

**APPLIES TO REVISION(S):**
0.0

5. **17000006 - Cache Pre-fetching is not functional:**

**DESCRIPTION:**
The prefetch unit inside the cache controller is not functional. Programming M4P_CACHE_CFG.PF field has no impact on the performance. Therefore, merging of contiguous addresses may not happen in memory-mapped mode at the SPI0 and SPI2 controllers.

Due to this limitation, the maximum bandwidth with the internal SPI flash is limited to under 35MBPS.

**WORKAROUND:**
None.

**APPLIES TO REVISION(S):**
0.0, D
6. 17000008 - Oscillator Watchdog is not functional:

DESCRIPTION:
The fault output of the Oscillator Watchdog module is not deterministic. The OSCW.EVT interrupt should not be enabled until CGU.OSCWDCTL.FAULTEN is cleared. The SYS_FAULT signal is unreliable until CGU.OSCWDCTL.FAULTEN and the SEC external fault condition are cleared.

WORKAROUND:
There is no workaround to restore proper oscillator monitoring. User code should disable the oscillator watchdog and clear potential fault code as early as possible in the application code, preferably in the reset vector.

The following code is included as part of the startup.c provided with the ADSP-CM40x Enablement Software.

```c
__disable_irq();
pADI_SEC0->FCTL &= ~BITM_SEC_FCTL_EN;
pADI_SEC0->FCTL &= ~(BITM_SEC_FCTL_FIEN | BITM_SEC_FCTL_FOEN);
pADI_CGU0->OSCWDCTL &= ~BITM_CGU_OSCWDCTL_FAULTEN;
__ISB();
if (((pADI_SEC0->FSTAT & BITM_SEC_FSTAT_ACT) >> BITP_SEC_FSTAT_ACT) &
    ((pADI_SEC0->FEND & BITM_SEC_FSID_FEXT) >> BITP_SEC_FSID_FEXT))
{
    pADI_SEC0->FEND = BITM_SEC_FEND_FEXT;
}
pADI_SEC0->FCTL |= (BITM_SEC_FCTL_FOEN | BITM_SEC_FCTL_FIEN);
pADI_SEC0->FCTL |= BITM_SEC_FCTL_EN;
__enable_irq();
```

APPLIES TO REVISION(S):
0.0

7. 17000009 - Security feature is not implemented:

DESCRIPTION:
The processor provides a mechanism to block the accesses in secure mode.

This feature is not implemented.

WORKAROUND:
None

APPLIES TO REVISION(S):
0.0, D
8. 17000010 - ADC loopback via DAC is not implemented:

**DESCRIPTION:**
For the functional self-check of the converters, the ADC can be looped back via DAC at the last channel of ADC by specifying the ADC channel ID as 0xC (ADSP-CM402F, ADSP-CM403F and ADSP-CM409F processors) and 0x8 (ADSP-CM407F and ADSP-CM408F processors) in the Event Control register.

This feature is not implemented on ADSP-CM407F and ADSP-CM408F processors.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0

9. 17000011 - Restriction in using Ethernet MAC and SMC simultaneously:

**DESCRIPTION:**
The Ethernet data pins ETH0_TXD0 and ETH0_TXD1 are multiplexed with the SMC byte enable signals SMC0_ABE0 and SMC0_ABE1 respectively. Due to this conflict, 8-bit SMC write accesses are not possible when using Ethernet MAC. This does not impose a restriction to use the SMC for 16-bit accesses.

**Note:** From revision D onwards Ethernet data pins and SMC byte enable signals are not multiplexed, thus can be used simultaneously.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0

10. 17000013 - The setup time of USB0_ID signal deviates from the specification of all other system inputs:

**DESCRIPTION:**
The tSSYS (System Inputs Setup Before TCK High) timing parameter for USB0_ID signal is 30ns as opposed to 12ns applicable for all system inputs. The USB0_ID pin is statically controlled (Host mode: Connect to GND; Device mode: Left floating), the long setup requirement will not have any implications.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0, D, H

11. 17000014 - Unexpected multiple DMA parity error:

**DESCRIPTION:**
DMA should be ideally blocked when parity error occurs. However, parity error doesn't prevent the DMA from reading the memory content. If DMA tries to access a memory location when parity error has occurred, the core indicates a status of multiple parity error.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0, D, H
12. 17000015 - ADCC collision status is indicated for only one ADC in simultaneous sampling mode:

**DESCRIPTION:**
In case of simultaneous sampling, if one event undergoes collision (indicating the event will be delayed), its paired event would also be delayed and ideally the collision status should be reflected for both the paired events.

However the status of collision is reflected only for the event which underwent collision, and not for both the ADC events when all the below conditions are true:

1. TIMER1 initiates a pair of simultaneous sampling events
2. TIMER0 event comes at the same time as that of that of the paired events
3. ADCs are not performing any sampling
4. Pending FIFO is empty

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0, D, H

13. 17000016 - SPI data pins are driven high in open drain mode:

**DESCRIPTION:**
SPI in open drain mode tri-states the output when data driven is logic high. But due to a race condition, the data pins will drive logic high for a small duration.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0, D

14. 17000019 - SPI1 master boot fails when invoked via ROM API:

**DESCRIPTION:**
The SPI1 Master boot can be invoked via ROM API. The Pin Mux is incorrectly configured in the Boot ROM which leads to boot failure.

**WORKAROUND:**
Set the `BCMD_NOCFG` in the dBootCommand parameter to instruct the Boot ROM not to use the default settings. Configure the pin mux to select the SPI1 signals before invoking the ROM API.

**APPLIES TO REVISION(S):**
0.0

15. 17000020 - The debug reset module is not implemented in accordance with standard ARM tools:

**DESCRIPTION:**
When the emulator is connected to the processor, it issues a reset and thus leads to the execution of the code in the flash (eg: if BMODE = 1). Thus, the peripherals may not be at their default state when emulator is connected which can affect the external peripherals in the system.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0, D
16. 17000021 - The software selection of SPI Slave Enable Signal does not drive to the programmed value in the Slave Select Register:

DESCRIPTION:
The SPI Slave Enable signal can be selected via software by setting to the required value in the Slave Select Register. However, this value doesn't get driven on the SPI Slave Enable Signal.

WORKAROUND:
Perform two back to back writes to the Slave Select Register in order to drive the signal to the required level.

APPLIES TO REVISION(S):
0.0, D, H

17. 17000022 - SPI Transmit Collision Error may occasionally be missed:

DESCRIPTION:
SPI Transmit Collision Error is signalled when loading data to the transmit shift register happens near the first transmitting edge of SPI_CLK. This error is signalled only in slave mode. But due to incorrect timing of the first drive edge signal, it can occasionally cause a Transmit Collision Error to be unreported in the SPI_STAT register.

WORKAROUND:
None

APPLIES TO REVISION(S):
0.0, D

18. 17000023 - Offset Error and Gain Error of the ADCs deviate from the specification:

DESCRIPTION:
The two 16-bit ADCs have a higher than specified Offset Error and Gain Error. An Offset Error of up to -5mV (typical) and a Gain Error of +30mV (typical) has been measured. This will be different for each part and each ADC. There is no reduction in the ADC input signal range (0V - 2.5V) due to these errors. The user has to do a one-time measurement of these errors and include a correction factor in their software.

A pictorial description of the Errors is shown below.

WORKAROUND:
None

APPLIES TO REVISION(S):
0.0, D
19. 17000024 - SPORT0 A and TIMER0 signals do not appear on Port E and Port D respectively:

**DESCRIPTION:**
SPORT0 A signals do not appear on Port E and TIMER0 signals do not appear on Port D. Refer to the datasheet for signal multiplexing scheme.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0

20. 17000025 - TIMER_DATA_ILAT bit is set in EXTCLK mode when TIMER_TMRn_CNT rolls over to 1:

**DESCRIPTION:**
When TIMER is configured in External Clock mode, after the TIMER_TMRn_CNT register reaches the value programmed in the TIMER_TMRn_PER register, the corresponding TIMER_DATA_ILAT bit should be set along with a trigger / interrupt being generated. However, TIMER_DATA_ILAT bit will be set after the TIMER_TMRn_CNT register rolls over to 1.

Consider TIMER_TMRn_PER register to be configured to a value n. After the TIMER has started, the first interrupt/ trigger will occur after the TIMER receives n+1 edges externally and the subsequent ones after every n edges.

**WORKAROUND:**
For interrupts/ triggers to occur at every n edges of the external clock the TIMER_TMRn_PER register should be configured to n-1 for the initial event and to n for subsequent ones.

Pseudo code:

```
TIMER_TMRn_PER = n-1;  // Configure PERIOD register with n-1
TIMER_RUN_SET = 1;     // Run the timer
TIMER_TMRn_PER = n;    // Configure PERIOD register with n
```

**APPLIES TO REVISION(S):**
0.0, D, H

21. 17000026 - Analog Front End control bits are not initialized:

**DESCRIPTION:**
There are certain Analog Front End control bits that are not properly initialized.

**WORKAROUND:**
The adi_adcc_OpenDevice API software driver will properly initialize the Analog Front End (AFE) control registers. It is required to use this driver with ADI_WA_17_0026=1 included in the defined symbols section of the preprocessor settings for proper operation of the AFE.

**APPLIES TO REVISION(S):**
D

22. 17000027 - RCU0_SRRQSTAT register is not affected by TRU's System Reset Request:

**DESCRIPTION:**
The RCU system reset request status register (RCU0_SRRQSTAT) contains status bits indicating which system reset request input triggered the System Reset. These bits are set by the assertion of the corresponding System Reset Request input.

In case, if this System Reset Request input is active only for 1 SCLK period, then corresponding status bits may not get set. This can happen mainly if the System Reset Request input comes from Trigger Routing Unit (TRU) of the processor.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
H
23. 17000028 - ECC Logic in Analog Front End Does Not Trigger a Fault:

**DESCRIPTION:**
The hardware trigger of a FAULT is not implemented for Analog Front End Non-Volatile Configuration ECC errors.

**WORKAROUND:**
The following code checks the Analog Front End Non-Volatile Configuration ECC status:

```c
*pREG_ADCC0_CTL = 0x0000;
while(*pREG_ADCC0_CFG & 0x01);
*((volatile uint32_t *) 0x40027010) = (uint32_t) (0x1e7b1c96);
*((volatile uint32_t *) 0x40027010) = (uint32_t) (0xdff0c3b2);
*((volatile uint32_t *) 0x40027010);
*pREG_ADCC0_CTL  = (uint32_t) 0x00000001;
*((volatile uint32_t *) 0x4000E404) = (uint32_t) (0x08000000);
while (((*(volatile uint32_t *) 0x4000E404 & 0x00000001) != 1));
while (((*(volatile uint32_t *) 0x4000E404 & 0x00000001) != 0));
int CFG_Reg = *((volatile uint32_t *) 0x4000E404) >> 1) & 0xFFFFFFFF;
if(CFG_Reg & 0x007F)
{
    "ECC error is detected, generate Fault"
}
*((volatile uint32_t *) 0x40027010) = (uint32_t) 0x00000000;
*((volatile uint32_t *) 0x40027010) = (uint32_t) 0x00000000;
*pREG_ADCC0_CTL  = 0x00;
while(*pREG_ADCC0_CFG & 0x01);
```

The above code must be run after Analog Front End initialization in order to trigger a FAULT if an ECC error has been detected.

**APPLIES TO REVISION(S):**
D, H

24. 17000029 - SPI data pins are internally pulled high in open drain mode:

**DESCRIPTION:**
SPI in open drain mode tri-states the output pins when data driven is logic high. But due to internal pull-up resistors, the data pins will be pulled high.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0, D, H

25. 17000030 - System DMAs do not halt in emulation mode:

**DESCRIPTION:**
The System DMAs continue to run even when the processor is halted via emulator.

**WORKAROUND:**
None

**APPLIES TO REVISION(S):**
0.0, D
26. 17000031 - SPORT May Drive Data Pins During Inactive Channels in Multichannel Mode:

DESCRIPTION:
When a SPORT is operating in multichannel mode, the transmitter tri-states the data pins during the inactive channels. When SPMUX functionality is enabled, under specific conditions, one SPORT half may continue to drive on the inactive channels. This happens when all the below conditions are true.

1. SPORT half “X” is configured as transmitter (SPORT_CTL_x.SPTRAN = 1)
2. Imports Frame sync internally from the pairing half SPORT (SPORT_CTL2_x.FSMUXSEL = 1).
3. Multichannel Frame Delay is zero (SPORT_MCTL_x.MFD = 0)
4. Window Offset is zero (SPORT_MCTL_x.OFFSET = 0)
5. Channel-0 of multichannel frame is enabled for transmission (SPORT_CS0_x.CH0 = 1)
6. Frame sync is active low (SPORT_xCTL.LFS = 1)
7. Frame Sync edge Detect bit is 0 (SPORT_CTL_x.FSED = 0)

If any of these conditions is false, this anomaly does not occur.

When this exact configuration is used, after completion of all the active channels, the SPORT half transmitter drives the first bit of next word to be transmitted once the number of channels specified in WSIZE expires. Therefore the SPORT half may drive on inactive channels which can cause contention when other transmitters configured to drive on these inactive channels.

WORKAROUND:
Set the Frame Sync edge Detect bit (SPORT_CTL_x.FSED = 1) if SPORT is configured with above mentioned settings

APPLIES TO REVISION(S):
0.0, D, H