

## ADSP-2185M Anomaly List for Revision 2.1

The list below represents the known anomalies and workarounds for the ADSP-2185M. This silicon revision of a particular device can be found on the chip, as shown below:

ADSP-2185Mxxx -xxx xyzzzzzz-2.1 wwyy	Part Number/Package Speed Grade Lot Number and <b>Silicon Revision</b> Date Code (week/year)
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The Table below shows which ADSP-2185M's have each anomaly. The left hand side of the table lists the type of anomaly and the numbers on the top of the table refer to the particular revision of the silicon. Any box that has an 'x' contained in it has that anomaly. For a complete description of the anomaly, please refer to the subsequent page.

	2.0	2.1
1. Wait stated writes to external memory from group IV registers	X	X
2. Speed path with decoding a group IV register write instruction	X	
3. When the PDForce bit in SPORT1 Autobuffer Control Register (0x3FEF) is set, it remains HIGH after powerdown	X	
4. Latch-up Spec. This device can only sink a maximum of 70mA.	X	

### Anomaly #1

If you are executing the instruction:

```
<reg> = DM(<addr>);
```

from external program memory (PMOVLAY=1 or 2), there will be a one cycle latency after the instruction finishes executing until the value in <reg> will be valid. This means that your code must wait one cycle after this instruction executes before the <reg> register can be safely tested or operated on.

The affected group IV registers for this anomaly are listed below:

ASTAT, MSTAT, SSTAT, IMASK, ICNTL, CNTR

### Workarounds:

There are two potential workarounds for this anomaly:

1. If possible, place all Data Memory loads of the group IV register in internal memory.
2. If Data Memory loads of the group IV register must lie in external memory, make the next instruction a NOP.

This anomaly is unaffected by the number of waitstates used to access external program memory.

#### Anomaly #2

When writing certain values to a group IV register, the instruction is slow being decoded. The result is that the device will execute a push on the PC Stack. This limits the operating voltage, for 75MHz operation to 2.55V-2.65V across the commercial temperature range(0C – 70C).

#### Anomaly #3

When coming out of powerdown the PDForce bit does not get cleared. This will **not** force another powerdown, and can be ignored. If another powerdown needs to be forced, you must set the PDForce bit again. This anomaly only applies to systems entering powerdown by writing the power-down force bit. When exiting power down the PDForce bit does not get cleared. This will **not** force another power down, and can be ignored or manually cleared. You will not encounter any problems if you never read and write back the SPORT1 Autobuffer Control Register. If you are writing back to the SPORT1 Autobuffer Control Register, make sure that that the power-down force bit is always manually written to zero.