DEMO MANUAL DC1746A

LTM2881:
Isolated RS485/RS422
µModule Transceiver + Power

DESCRIPTION

Demonstration circuit 1746A is an isolated RS485/RS422 µModule® transceiver + power featuring the LTM®2881. The demo circuit is a 2500V RMS galvanically isolated RS485/RS422 transceiver interface. The demo circuit features an EMI optimized circuit configuration and printed circuit board layout. All components are integrated into the µModule transceiver. The demo circuit operates from a single external supply on VCC. The part generates the output voltage VCC2 and communicates all necessary signaling across the isolation barrier using LTC’s isolator µModule technology.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Input Supply Range</td>
<td>LTM2881-5</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LTM2881-3</td>
<td>3.0</td>
<td>3</td>
<td>3.6</td>
</tr>
<tr>
<td>VCC2</td>
<td>Output Voltage</td>
<td>ILOAD = 0mA to 100mA, DE = 0V</td>
<td>4.7</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>fMAX</td>
<td>Maximum Data rate</td>
<td>SLO = VCC2</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VORM</td>
<td>Maximum Working Insulation Voltage</td>
<td>GND to GND2</td>
<td>560</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Common Mode Transient Immunity</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

OPERATING PRINCIPLES

The LTM2881 contains an isolated DC/DC converter, delivering power to VCC2 at 5V from the input supply, VCC. Isolation is maintained by the separation of GND and GND2 where significant operating voltages and transients can exist without affecting the operation of the LTM2881. The logic side ON pin enables or shuts down the LTM2881. RS485/RS422 signaling is controlled by the logic inputs DE, DI, TE and RE. Connection to the transceiver pins (A, B, Y and Z) allows full- or half-duplex operation on the isolated side of the demo circuit. A full-/half-duplex switch is included on the demo circuit to ease setting the system configuration. The SLO pin configures the slew rate of the driver output pins Y and Z. Data is transmitted out the driver pins Y and Z from the input DI with DE set on. Data is received through the difference in A and B to the output RO with RE set on.

The demo circuit has been designed and optimized for low RF emissions. To this end some features of the LTM2881 are not available for evaluation on the demo circuit. The logic supply voltage, VL, is tied to VCC on the demo circuit. All control signals are selectable by jumper programming only, including ON, RE, DE, TE and SLO. The spare logic channel DIN to DOUT is not available.
EMI mitigation techniques used include the following:

1. Four layer PCB, allowing for isolated side to logic side ‘bridge’ capacitor. The bridge capacitor is formed between an inner layer of floating copper which overlaps the logic side and isolated side ground planes. This structure creates two series capacitors, each with approximately 0.008” of insulation, supporting the full dielectric withstand rating of 2500V\(_{\text{RMS}}\). The bridge capacitor provides a low impedance return path for injected currents due to parasitic capacitances of the LTM2881’s signal and power isolating elements.

2. Discrete bridge capacitors (C3, C4) mounted between GND2 and GND. The discrete capacitors provide additional attenuation at frequencies below 400MHz. Capacitors are safety rated type Y2, manufactured by Murata, part # GA342QR7GF471KW01L.

3. Board/ground plane size has been minimized. This reduces the dipole antenna formed between the logic side and isolated side ground planes.

4. Top signal routing and ground floods have been optimized to reduce signal loops, minimizing differential mode radiation.

5. Common mode filtering is integrated into the input pin header and output DB9 connector. Filtering helps to reduce emissions caused by conducted noise and minimizes the effects of cabling to common mode emissions.

6. A combination of low ESL and high ESR decoupling is used. A low ESL ceramic capacitor is located close to the module minimizing high frequency noise conduction. High ESR tantalum capacitors are included to minimize board resonances and prevent voltage spikes due to hot plugging of the input supply voltage.

EMI performance is shown in Figure 1, measured using a gigahertz transverse electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, “Testing and Measurement Techniques—Emission and Immunity Testing in Transverse Electromagnetic Waveguides”.

![Figure 1. DC1746A Radiated Emissions](image-url)
QUICK START PROCEDURE

Demonstration circuit 1746A is easy to set up and evaluate the performance of the LTM2881. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below.

NOTE: When measuring the input or output voltage ripple or high speed signals, care must be taken to avoid a long ground lead on the oscilloscope probe.

1. Install jumpers in following positions: (all are default except JP5 and SW1)
   JP1 ON
   JP2 ON
   JP3 ON
   JP4 ON
   JP5 OFF
   SW1 HALF DUPLEX

2. With power off, connect the input power supply to V_{CC} and GND on pin header J1.

3. Turn on the power at the input.
   NOTE: Make sure that the input voltage does not exceed 6V.

4. Check for the proper output voltage. V_{CC2} = 5V, this can be measured between probe points V2 and C.

5. Once the proper output voltage is established, connect a function generator to pin DI and set to square wave with a low of 0V, high = V_{CC}. Set frequency to 10MHz (20Mbps). Enable output of function generator.

6. Connect oscilloscope to pin RO and observe 10MHz waveform. This demonstration shows data that is transmitted from DI, loops back through half-duplex connection, and out of RO.

Figure 2. Demo Board Setup
## PCB Layout

### Layer 1. Top Layer

### Layer 2. Ground Plane

### Layer 3. Signal Layer

### Layer 4. Bottom Layer

## Parts List

<table>
<thead>
<tr>
<th>ITEM</th>
<th>QTY</th>
<th>REFERENCE</th>
<th>PART DESCRIPTION</th>
<th>MANUFACTURER/PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Required Circuit Components</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>U1</td>
<td>I.C., LTM2881CY-3</td>
<td>LINEAR LTM2881CY-3#PBF</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>U1</td>
<td>I.C., LTM2881CY-5</td>
<td>LINEAR LTM2881CY-5#PBF</td>
</tr>
<tr>
<td><strong>Hardware/Components (For Demo Board Only)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>C1, C5</td>
<td>CAP, TANT 10μF 10V 20% TAJA</td>
<td>AVX TAJA106M010RNJ</td>
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<tr>
<td>3</td>
<td>1</td>
<td>C2</td>
<td>CAP, CER 1μF 10V 20% 0508</td>
<td>MURATA LLL219R71A105MA01L</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>C3, C4</td>
<td>CAP, CER 470pF 250VAC 10% 1808</td>
<td>MURATA GA342QR7GF471K01L</td>
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<tr>
<td>5</td>
<td>1</td>
<td>J1</td>
<td>0.1” DOUBLE ROW HEADER, 5 × 2 PIN</td>
<td>SAMTEC TSW-105-22-G-D</td>
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<tr>
<td>6</td>
<td>1</td>
<td>J1</td>
<td>0.1” FERRITE PLATE, 5 × 2 HOLE</td>
<td>FAIR RITE 2644247101</td>
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<tr>
<td>7</td>
<td>1</td>
<td>J2</td>
<td>CON, FILTERED, DSUB 9-PIN</td>
<td>KOBICOMN 152-3609</td>
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<tr>
<td>8</td>
<td>5</td>
<td>JP1-5</td>
<td>2mm SINGLE ROW HEADER, 3-PIN</td>
<td>SAMTEC TMM-103-02-L-S</td>
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<tr>
<td>9</td>
<td>5</td>
<td>JP1-5</td>
<td>SHUNT</td>
<td>SAMTEC 2SN-BK-G</td>
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<tr>
<td>10</td>
<td>1</td>
<td>SW1</td>
<td>SWITCH, DPDT, SMD</td>
<td>COPAL CAS-220TA</td>
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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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