

**LTC3634**
**15V Dual 3A Monolithic Step-Down  
 Regulator Board for DDR Power**
**DESCRIPTION**

Demonstration circuit DC1708A is a dual-output regulator focused specifically for DDR memory power applications. It is built based on the LTC<sup>®</sup>3634, a high voltage dual-channel, controlled on-time monolithic synchronous buck regulator. The DC1708A has an input voltage range of 3.6V to 15V. The output voltage of the first channel,  $V_{DDQ}$ , of the DC1708A has three fixed voltage settings: 1.5V, 1.8V and 2.5V, and is capable of delivering up to 3A of output current. The second channel,  $V_{TT}$ , is set to regulate to half the voltage on the VDDQIN pin, which can be either the channel 1 output or an external reference voltage. It can source or sink a maximum of 3A of output current. The LTC3634 also provides a 10mA buffered output of half  $V_{DDQIN} - V_{TTR}$ , which is used to provide the reference voltage needed for DDR applications. With the use of a timing resistor, the DC1708A can have its operating frequency programmed from 500kHz to 4MHz. Additionally the DC1708A can be easily synchronized to an external clock, due to an internal phase-locked loop, within this same frequency range. The DC1708A  $V_{DDQ}$  output can

operate in either Burst Mode<sup>®</sup> operation or forced continuous mode. In Burst Mode operation, which is the preferred mode of low load current operation, the DC supply current is typically only 1.3mA (both channels) at no load (sleep mode), and less than 15 $\mu$ A in shutdown. In Burst Mode operation or continuous mode operation, the DC1708A is a very efficient circuit at high load currents: over 80% for either channel. The LTC3634 is also capable of 90° or 180° out-of-phase operation, and can allow its output to track an external voltage, either coincidentally or ratiometrically. The LTC3634 comes in a 28-pin QFN package, featuring an exposed pad on the bottom-side of the IC for better thermal performance. All of these features make the DC1708A an ideal circuit for powering DDR memory applications.

**Design files for this circuit board are available at**  
<http://www.linear.com/demo>

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**PERFORMANCE SUMMARY** ( $T_A = 25^\circ\text{C}$ )

PARAMETER	CONDITIONS	TYPICAL VALUE
Minimum Input Voltage		3.6V
Maximum Input Voltage		15V
Output Voltage $V_{OUT1} - V_{DDQ}$	$V_{IN} = 3.6\text{V to } 15\text{V}, I_{OUT1} = 0\text{A to } 3\text{A}$	1.5V $\pm 2\%$ 1.8V $\pm 2\%$ 2.5V $\pm 2\%$
Typical Output Ripple $V_{DDQ}$	$V_{IN} = 12\text{V}, I_{OUT1} = 3\text{A}$ (20MHz BW)	< 20mV <sub>p-p</sub>
Output Voltage $V_{OUT2} - V_{TT}$	$V_{IN} = 3.6\text{V to } 15\text{V}, I_{OUT2} = 0\text{A to } \pm 3\text{A}$	
	$V_{OUT1} = 1.5\text{V}$	0.75V $\pm 3\%$
	$V_{OUT1} = 1.8\text{V}$	0.9V $\pm 3\%$
	$V_{OUT1} = 2.5\text{V}$	1.25V $\pm 3\%$
Typical Output Ripple $V_{TT}$	$V_{IN} = 12\text{V}, I_{OUT2} = \pm 3\text{A}$ (20MHz BW)	< 20mV <sub>p-p</sub>
Nominal Switching Frequencies	$R_T = 324\text{k}$	1MHz
Burst Mode Operation-to-CCM Transition	Channel 1: $V_{IN} = 12\text{V}, V_{OUT1} = 1.8\text{V}, f_{SW} = 1\text{MHz}$	$I_{OUT1} \sim 1.6\text{A}$
INTV <sub>CC</sub>		3.3V
V <sub>TTR</sub>	$V_{DDQIN} = 2.5\text{V}$	1.25V

## QUICK START PROCEDURE

The DC1708A is easy to set up to evaluate the performance of the LTC3634. For a proper measurement equipment configuration, set up the circuit according to the diagram in Figure 1.

**NOTE:** When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the  $V_{IN}$  or  $V_{OUT}$  and GND terminals. See the proper scope probe technique in Figure 2.

Please follow the procedure outlined below for proper operation.

1. Connect the input power supply to the  $V_{IN}$  and GND terminals. Connect the loads between the  $V_{OUT}$  and GND terminals. Refer to Figure 1 for the proper measurement equipment setup.

Before proceeding to operation, insert jumper shunts XJP1 and XJP2 into the OFF positions of headers JP1 and JP2, shunt XJP3 into the forced continuous mode (FCM) position of MODE header JP3, shunt XJP4 into the 180° (out-of-phase) position of PHASE header JP4, shunt XJP5 into the soft-start position of TRACK/SS header JP5, and shunt XJP6 into the  $V_{OUT1}$  voltage options of choice of header JP6: 1.2V, 1.5V or 1.8V.

2. Apply 5V at  $V_{IN}$ . Measure both  $V_{OUTs}$ . Both should read 0V. If desired, one can measure the shutdown supply current at this point. The supply current should approximately 15 $\mu$ A in shutdown.
3. Turn on  $V_{OUT1}$ ,  $V_{DDQ}$ , and  $V_{OUT2}$ ,  $V_{TT}$ , by shifting shunts XJP1 and XJP2 from the OFF positions to the ON positions. Both output voltages should be within a tolerance of  $\pm 1\%$ .
4. Vary the input voltage from 3.6V to 15V, the channel 1 load current from 0A to 3A, and the channel 2 load current from 0A to  $\pm 3A$  (the  $V_{TT}$  channel sinks as well as sources current. An easy way to test this capability is shown in the test setup diagram. Connect a variable

resistor from  $V_{IN}$  to  $V_{OUT}$ , along with an amp meter. The current will be  $V_{IN}$  minus  $V_{OUT}$  divided by the variable resistor value).  $V_{DDQ}$  output voltage tolerance should be within  $\pm 2\%$ , whereas the output voltage tolerance of  $V_{TT}$  should be within  $\pm 3\%$ .

5. Set the load current of both outputs to 3A and the input voltage to 12V, then measure each output ripple voltage (refer to Figure 2 for the proper measurement technique). Each should measure less than 20mVAC. Also, observe the voltage waveform at either switch node (Pins 23 and 24 for channel 1, and Pins 13 and 14 for channel 2) of each regulator. Both switch node waveforms should be rectangular in shape, and 180° out-of-phase with each other. The switching frequencies should be between 800kHz and 1.2MHz ( $T = 1.25\mu$ s and 0.833 $\mu$ s).
6. With the board under proper operation, observe the load regulation, efficiency, 90° out-of-phase operation (by changing jumper XJP4 to the 90° position), or Burst Mode operation (by changing jumper XJP3 to the Burst Mode position).
7. *Optional:* Moving the 0 $\Omega$  resistor at  $R_{VDDQ}$ , inserting it into  $R_{DDQIN}$ , and applying a voltage to turret VDDQIN allows the channel 2 output voltage ( $V_{TT}$ ) to be adjusted to one-half the voltage at VDDQIN.

When finished, insert shunts XJP1 and XJP2 to the off position(s) and disconnect the power.

**Warning** - If the power for the demo board is carried in long leads, the input voltage at the part could “ring”, which could affect the operation of the circuit or even exceed the maximum voltage rating of the IC. To eliminate the ringing, a small tantalum capacitor (for instance, the AVX part TAJW335M035R) is inserted on the pads between the input power and return terminals on the bottom of the demo board. The (greater) ESR of the tantalum capacitor will dampen the (possible) ringing voltage due to the use of long input leads. On a normal, typical PCB with short traces, this capacitor is not needed.

**QUICK START PROCEDURE**

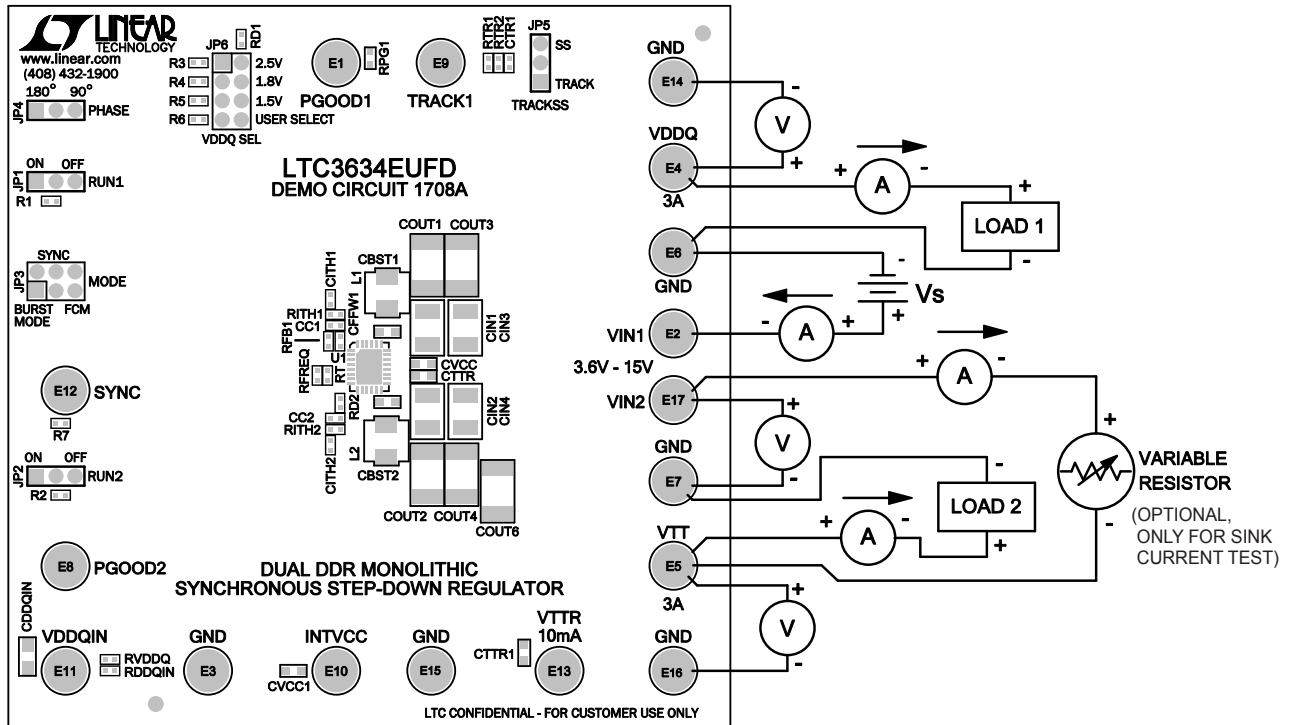


Figure 1. Proper Measurement Equipment Setup

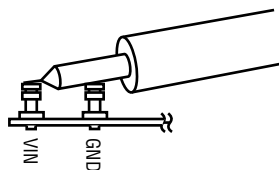


Figure 2. Measuring Input or Output Ripple

# DEMO MANUAL DC1708A

## QUICK START PROCEDURE

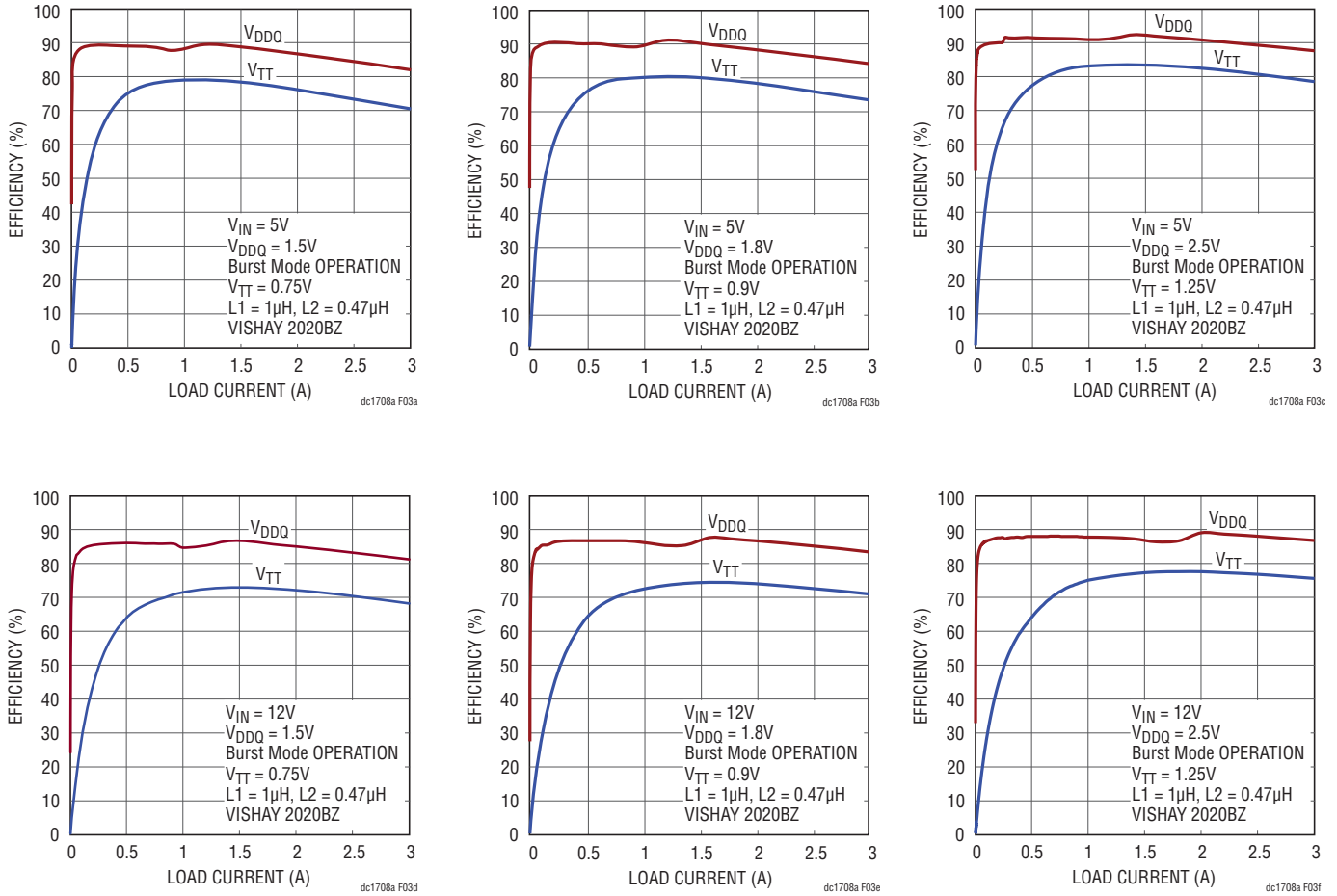


Figure 3. LTC3634 DC1708A Efficiency

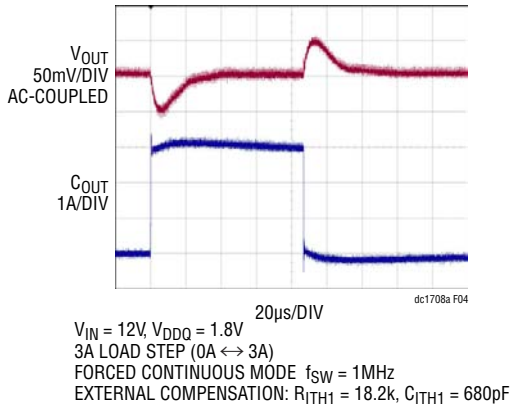


Figure 4.  $V_{DDQ}$  Load Step Response

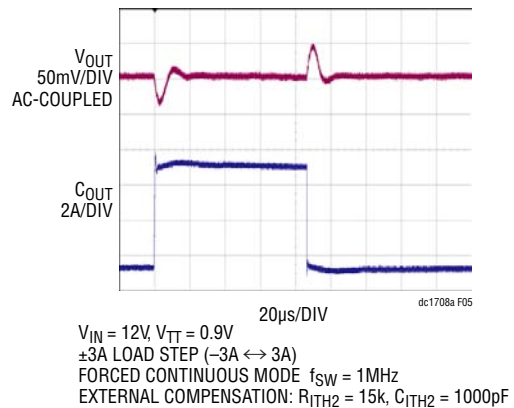
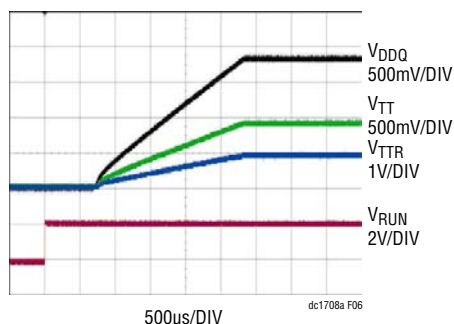


Figure 5.  $V_{TT}$  Load Step Response

## QUICK START PROCEDURE



$V_{IN} = 12V$ ,  $V_{DDQ} = 1.8V$ ,  $V_{TT} = 0.9V$ , 3A LOAD (EACH)  
 $V_{TTR} = 0.9V$ , 10mA  
 FORCED CONTINUOUS MODE  $f_{SW} = 1MHz$   
 $C_{SS} = 4700pF$

Figure 6. LTC3634 DC1708A Start-Up with Soft Start

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
<b>Required Circuit Components</b>				
1	2	$C_{BST1}$ , $C_{BST2}$	CAP, 0603, 0.1µF, 10%, 50V, X7R	NIC, NMC0603X7R104K50TRPF
2	1	$C_{FFW1}$	CAP, 0402, 10pF, 5%, 25V, NPO	NIC, NMC0402NPO100J25TRPF
3	2	$C_{IN1}$ , $C_{IN2}$	CAP, 1210, 47µF, 20%, 16V, X5R	Taiyo Yuden EMK325BJ476MM-T
4	1	$C_{ITH1}$	CAP, 0402, 680pF, 5%, 25V, X7R	AVX, 04023C681JAT2A
5	1	$C_{ITH2}$	CAP, 0402, 1000pF, 10%, 25V, X7R	AVX, 04023C102KAT2A
6	5	$C_{OUT1}$ to $C_{OUT4}$ , $C_{OUT6}$	CAP, 1812, 100µF, 20%, 6.3V, X5R	TDK C4532X5R0J107M
7	1	$C_{TTR}$	CAP, 0603, 10nF, 10%, 16V, X7R	AVX, 0603YC103KAT2A
8	1	$C_{VCC}$	CAP, 0603, 1µF, 10%, 16V, X5R	NIC, NMC0603X5R105K16TRPF
9	1	L1	IND, 1µH	Vishay, IHLP2020BZER1R0M01
10	1	L2	IND, 0.47µH	Vishay, IHLP2020BZERR47M01
11	1	$R_{FB1}$	RES, 0402, 34.8kΩ, 1%, 1/16W	NIC, NRC04F3482TRF
12	1	$R_{ITH1}$	RES, 0402, 18.2kΩ, 1%, 1/16W	Vishay, CRCW040218K2FKED
13	1	$R_{ITH2}$	RES, 0402, 15kΩ, 1%, 1/16W	Vishay, CRCW040215K0FKED
14	1	$R_T$	RES, 0402, 324kΩ, 1%, 1/16W	NIC, NRC04F3243TRF
15	1	$R_{VDDQ}$	RES, 0402, 0Ω, JUMPER	NIC, NRC04Z0TRF
16	1	R3	RES, 0402, 11kΩ, 1%, 1/16W	NIC, NRC04F1102TRF
17	1	U1	IC, Monolithic Synchronous Step-Down Regulator	Linear Technology Corporation, LTC3634EUF
<b>Additional Demo Board Circuit Components</b>				
1	0	CC1, CC2 (Option)	CAP, 0402, 10pF, 5%, 25V, NPO	NIC, NMC0402NPO100J25TRPF
2	0	$C_{DDQIN}$ (Option)	CAP, 0805, 10µF, 10%, 6.3V, X5R	NIC, NMC0805X5R106K6.3TRPLP3KF

# DEMO MANUAL DC1708A

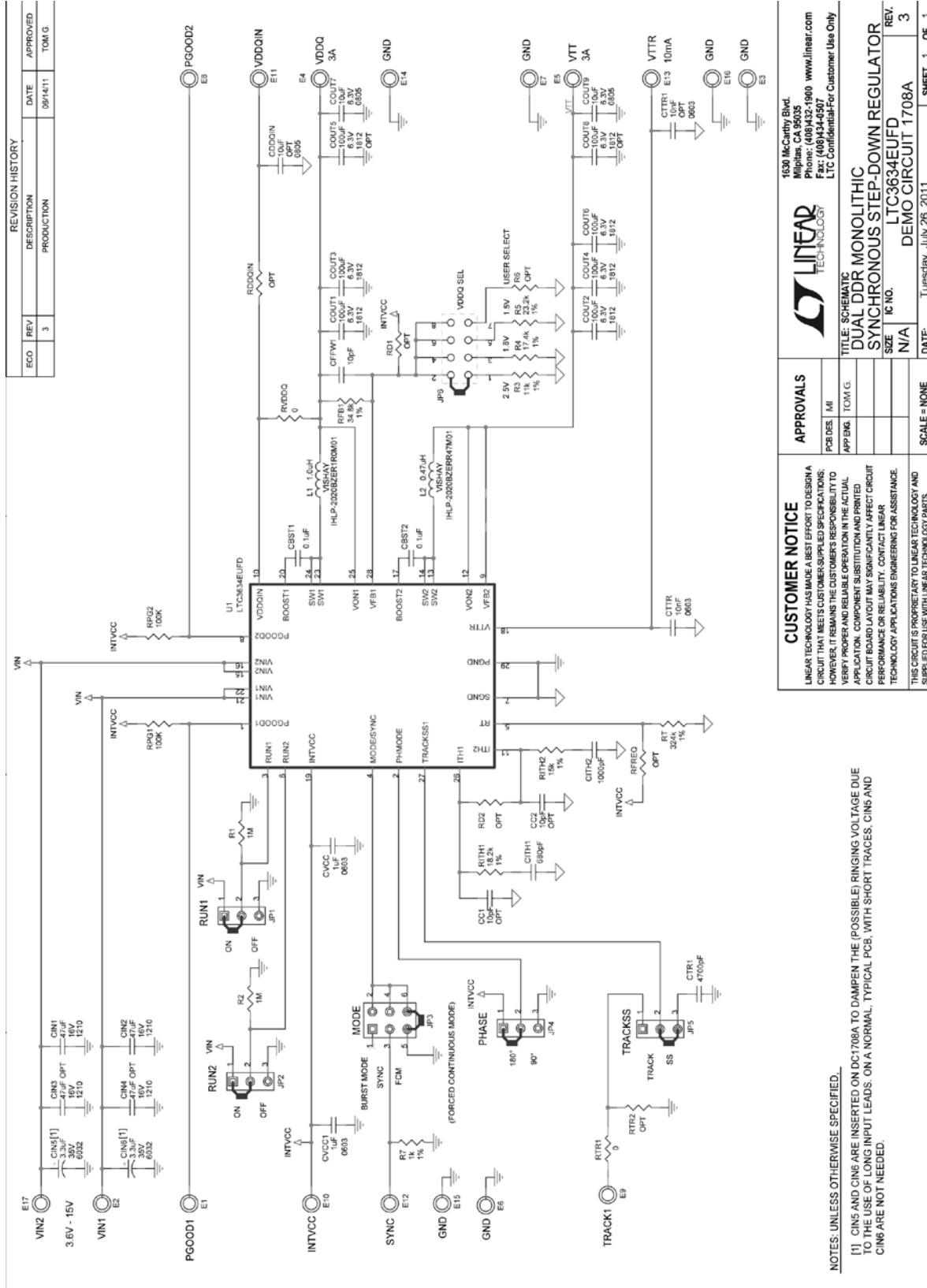
## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
3	0	C <sub>IN3</sub> , C <sub>IN4</sub> (Option)	CAP, 1210, 47μF, 20%, 16V, X5R	Taiyo Yuden, EMK325BJ476MM-T
4	2	C <sub>IN5</sub> , C <sub>IN6</sub>	CAP, TANT., 6032 3.3μF, 20%, 35V,	AVX, TAJW335M035R
5	0	C <sub>OUT5</sub> , C <sub>OUT8</sub> (Option)	CAP, 1812, 100μF, 20%, 6.3V, X5R	TDK, C4532X5R0J107M (Option)
6	2	C <sub>OUT7</sub> , C <sub>OUT9</sub>	CAP, 0805, 10μF, 10%, 6.3V, X5R	NIC, NMC0805X5R106K6.3TRPLP3KF
7	1	C <sub>TR1</sub>	CAP, 0402, 4700pF, 10%, 50V, X7R	TDK, C1005X7R1H472K
8	0	C <sub>TR1</sub>	CAP, 0603, 10nF, 10%, 16V, X7R	AVX, 0603YC103KAT2A (Option)
9	1	C <sub>VCC1</sub>	CAP, 0603, 1μF, 10%, 16V, X5R	NIC, NMC0603X5R105K16TRPF
10	0	R <sub>D1</sub> , R <sub>TR2</sub> , R <sub>D2</sub> , R <sub>6</sub> , R <sub>FREQ</sub> , R <sub>DDQIN</sub> (Option)	RES, 0402	Option
11	2	R <sub>PG1</sub> , R <sub>PG2</sub>	RES, 0402, 100kΩ, 5%, 1/16W	NIC, NRC04J104TRF
12	1	R <sub>TR1</sub>	RES, 0402, 0Ω, Jumper	NIC, NRC04Z0TRF
13	2	R <sub>1</sub> , R <sub>2</sub>	RES, 0402, 1MΩ, 5%, 1/16W	NIC, NRC04J105TRF
14	1	R <sub>4</sub>	RES, 0402, 17.4kΩ, 1%, 1/16W	NIC, NRC04F1742TRF
15	1	R <sub>5</sub>	RES, 0402, 23.2kΩ, 1%, 1/16W	NIC, NRC04F2322TRF
16	1	R <sub>7</sub>	RES, 0402, 1kΩ, 1%, 1/16W	NIC, NRC04F1001TRF
17	1	R <sub>8</sub>	RES, 0603, 0Ω, Jumper	NIC, NRC06Z0TRF

### Hardware: For Demo Board Only

1	17	E1 to E17	Turret	Mill-Max, 2501-2-00-80-00-00-07-0
2	4	JP1, JP2, JP4, JP5	Header, 3-Pin, 2mm	Samtec, TMM-103-02-L-S
3	1	JP3	Header, 3-Pin, DBL ROW 2mm	Samtec, TMM-103-02-L-D
4	1	JP6	Header, 4-Pin, DBL ROW 2mm	Samtec, TMM-104-02-L-D
5	6	JP1 to JP6	Shunt, 2mm	Samtec, 2SN-BK-G

**SCHEMATIC DIAGRAM**



REVISION HISTORY			
ECO	REV	DESCRIPTION	DATE
	3	PRODUCTION	08/14/11
			TOM.G

APPROVALS	
DESIGN	MI
APP'G	TOM.G

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TITLE: SCHEMATIC	
DUAL DDR MONOLITHIC SYNCHRONOUS STEP-DOWN REGULATOR	
SIZE	IC NO.
N/A	LTC3634EUFD
REV.	DEMO CIRCUIT 1708A
3	

DATE:	SHEET	OF
Tuesday, July 26, 2011	1	1

NOTES: UNLESS OTHERWISE SPECIFIED,  
 [1] C1N5 AND C1N6 ARE INSERTED ON DC1708A TO DAMPEN THE (POSSIBLE) RINGING VOLTAGE DUE TO THE USE OF LONG INPUT LEADS. ON A NORMAL PCB, WITH SHORT TRACKS, C1N5 AND C1N6 ARE NOT NEEDED.

Figure 7. Circuit Schematic



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# DEMO MANUAL DC1708A

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dc1708af



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