DESCRIPTION

Demonstration circuit 1524A-A is a high linearity direct quadrature modulator featuring the LTC®5588-1.

The LTC5588-1 is a direct conversion I/Q modulator designed for high performance wireless applications. It allows direct modulation of an RF signal using differential baseband I and Q signals. It supports LTE, GSM, EDGE, TD-SCDMA, CDMA, CDMA2000, W-CDMA, Wi-Max and other communication standards. It can also be configured as an image reject upconverting mixer, by applying 90° phase-shifted signals to the I and Q inputs.

The LTC5588-1 accepts externally applied balanced I and Q baseband input signals with a common-mode voltage level of 0.5V. These voltage signals are converted to currents and translated to RF frequency by means of double-balanced upconverting mixers. The mixer outputs are combined to single-ended through an on-chip RF output balun, which also transforms the output impedance to 50Ω for a wide RF frequency range. A single-ended or differential LO input signal drives a precision quadrature phase shifter followed by LO buffers, which in-turn drive the upconverting mixers.

The LTC5588-1 offers exceptional linearity performance. An external voltage can be applied to the LINOPT pin to further improve its output 3rd-order intercept. The LTC5588-1’s supply voltage range is 3.15V to 3.45V, and consumes about 303mA current.

Demonstration circuit 1524A-A is designed for evaluating the LTC5588-1 IC at RF frequencies from 700MHz to 5GHz. With a few component changes, it can be easily optimized for evaluations at lower or higher frequencies. Refer to “Application Note” section and the LTC5588-1 data sheet for details.

Table files for this circuit board are available. Call the LTC factory.

Table 1. Typical Demo Circuit Performance Summary

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>TYPICAL PERFORMANCE</th>
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</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td>3.15V to 3.45V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>I&lt;sub&gt;CC1&lt;/sub&gt;+I&lt;sub&gt;CC2&lt;/sub&gt;, EN = High</td>
<td>303mA</td>
</tr>
<tr>
<td>Sleep Current</td>
<td>I&lt;sub&gt;CC1&lt;/sub&gt;+I&lt;sub&gt;CC2&lt;/sub&gt;, EN = 0V</td>
<td>33µA</td>
</tr>
<tr>
<td>Baseband Bandwidth</td>
<td>-1dB Bandwidth, R&lt;sub&gt;SOURCE&lt;/sub&gt; = 25Ω, Single-ended</td>
<td>430MHz</td>
</tr>
<tr>
<td>Baseband Input Current</td>
<td>Single-Ended</td>
<td>-136µA</td>
</tr>
<tr>
<td>Baseband Input Resistance</td>
<td>Single-Ended</td>
<td>-3kΩ</td>
</tr>
<tr>
<td>Baseband DC Common-Mode Voltage</td>
<td>Externally Applied</td>
<td>0.5V</td>
</tr>
<tr>
<td>Baseband Amplitude Swing</td>
<td>No Hard Clipping, Single-Ended</td>
<td>0.86V&lt;sub&gt;p.p&lt;/sub&gt;</td>
</tr>
<tr>
<td>LO Match Frequency Range</td>
<td>Standard Demo Board, S&lt;sub&gt;11&lt;/sub&gt; &lt; -10dB</td>
<td>600MHz to 6000MHz</td>
</tr>
<tr>
<td>RF Match Frequency Range</td>
<td>Standard Demo Board, S&lt;sub&gt;22&lt;/sub&gt; &lt; -10dB</td>
<td>700MHz to 5000MHz</td>
</tr>
</tbody>
</table>

Table 1. Typical Demo Circuit Performance Summary

TA = 25°C; V<sub>CC</sub> = 3.3V, EN = 3.3V; BBPI, BBMI, BBPO, BBMO common-mode DC Voltage V<sub>CMBB</sub> = 0.5VDC, I and Q baseband input signal = 100kHz CW, 1V<sub>P-P(DIFF)</sub> each (two-tone I and Q baseband input signal are at 4.5MHz and 5.5MHz), I and Q 90° shifted, lower side-band selection; P<sub>LOM</sub> = 0dBm; f<sub>RF</sub> = f<sub>LO</sub> - f<sub>BB</sub>, unless otherwise noted.

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T<sub>A</sub> = 25°C; V<sub>CC</sub> = 3.3V, EN = 3.3V; BBPI, BBMI, BBPQ, BBMQ common-mode DC Voltage V<sub>CMBB</sub> = 0.5V<sub>DC</sub>; I and Q baseband input signal = 100kHz CW, 1Vp-p(DIFF) each (two-tone I and Q baseband input signal are at 4.5MHz and 5.5MHz), I and Q 90° shifted, lower side-band selection; P<sub>LOM</sub> = 0dBm; f<sub>RF</sub> = f<sub>LO</sub> – f<sub>BB</sub>: LINOPT pin floating unless otherwise noted.

<table>
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</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>f&lt;sub&gt;LO&lt;/sub&gt; = 900MHz</td>
<td>f&lt;sub&gt;LO&lt;/sub&gt; = 1900MHz</td>
</tr>
<tr>
<td>Conversion Voltage Gain</td>
<td>20 • Log (V&lt;sub&gt;RF(OUT)(50Ω)&lt;/sub&gt; / V&lt;sub&gt;IN(DIFF)(I OR Q)&lt;/sub&gt;)</td>
<td>0dB</td>
</tr>
<tr>
<td>Absolute Output Power</td>
<td>1Vp-p(DIFF) CW Signal, I and Q</td>
<td>4.0dBm</td>
</tr>
<tr>
<td>Output 1dB Compression</td>
<td>LINOPT pin floating</td>
<td>12.1dBm</td>
</tr>
<tr>
<td>Output 2nd Order Intercept</td>
<td>IM2 is Measured at f&lt;sub&gt;LO&lt;/sub&gt; – 10MHz</td>
<td>73.6dBm</td>
</tr>
<tr>
<td>Output 3rd Order Intercept</td>
<td>IM3 is Measured at f&lt;sub&gt;LO&lt;/sub&gt; – 3.5MHz and f&lt;sub&gt;LO&lt;/sub&gt; – 6.5MHz</td>
<td>31.3dBm</td>
</tr>
<tr>
<td>RF Output Noise Floor</td>
<td>LINOPT pin voltage optimized for best OIP3</td>
<td>35.1dBm</td>
</tr>
<tr>
<td>Image Rejection</td>
<td>No Baseband AC Input Signal (6MHz offset)</td>
<td>-161.6dBm/Hz</td>
</tr>
<tr>
<td>LO Feedthrough</td>
<td>Without nulling (unadjusted)</td>
<td>-45.5dBc</td>
</tr>
<tr>
<td></td>
<td>Without nulling (unadjusted)</td>
<td>-43.1dBm</td>
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</table>
**APPLICATION NOTE**

**ABSOLUTE MAXIMUM RATINGS**

**NOTE:** Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

- **Supply Voltage** ..................................... 3.8V
- **Common Mode Level of BBPI, BBMI and BBPO, BBMQ** ..................................... 0.55V
- **Voltage on Any Pin** ...................... -0.3V to VCC + 0.3V
- **T_JMAX** ................................................... 150°C
- **Operating Temperature Range** ............. -40°C to 85°C
- **Storage Temperature Range** .............. -65°C to 150 °C

**POWER SUPPLY CONSIDERATION**

In demonstration circuit 1524A-A (see Figure 3 for schematic), resistors R1 and R2 reduce the charging current in the power supply bypass capacitors C1 and C2 and reduce supply ringing during a fast power ramp-up in case an inductive cable is connected to the VCC and GND. While the LTC5588-1 IC is enabled, the voltage drop across R1 and R2 is approximately 0.15V. The supply voltages applied directly to the chip can be monitored by measuring at the test points TP1 and TP2. If the power supply used ramps up slower than 7V/µs and limits its output overshoot to below 3.8V, R1 and R2 can be omitted.

**ENABLE INTERFACE**

The EN input in demonstration circuit 1524A-A controls the operation of the LTC5588-1 IC. When a voltage of 2V or higher is applied, the IC is turned on. When the input voltage falls below 1V, the IC is turned off and enters sleep mode. If the EN input is not connected, the LTC5588-1’s 100kΩ on-chip pull-up resistor assures the IC is enabled. The voltage applied to the EN input must never exceed VCC by more than 0.3V. Surpassing this limit may cause permanent damage to the IC.

**BASEBAND INPUT INTERFACE**

Demonstration circuit 1524A-A has two channels of high impedance differential inputs to which external I and Q baseband signals can be applied. BBPI and BBMI are the differential I-channel baseband inputs. BBPO and BBMQ are the differential Q-channel baseband inputs.

Because the LTC5588-1 baseband inputs’ single-ended impedance is -3k each, it is important to keep the source resistance low enough such that the parallel value remains positive for the entire baseband frequency range.

A common-mode voltage of 0.5V (maximum 0.55V) must be externally applied to the baseband inputs for proper operation. In any case, the baseband inputs must NOT be left floating to avoid damages to the LTC5588-1 IC.

**LO INPUT INTERFACE**

The standard demonstration circuit 1524A-A can accept either single-ended or differential LO inputs. If single-ended LO input is used, the LO signal should be applied to the LOM port, and the LOP port should be terminated in 50Ω for best image rejection performance. In most cases, single-ended LO drive should be sufficient. However, the LOP and LOM inputs can also be driven differentially when an exceptionally low large-signal output noise floor is required.

Demonstration circuit 1524A-A’s LO inputs are optimized for 600MHz to 6GHz operations with better than 10dB input return loss. At lower LO frequencies, the image rejection and the large-signal noise performance can be improved with higher LO drive levels. However, if the single-ended drive level causes internal clipping, the LO leakage degrades. Using a balun such as the Anaren B031QJ50100A00 increases the LO drive level without internal clipping and provides a relatively broadband LO port impedance match. The balun (U2) can be installed by removing the DC blocking capacitors C5 and C6. However, for this particular balun, an external DC block is required.

Refer to the LTC5588-1 datasheet for more information and impedance data.
RF OUTPUT INTERFACE
Demonstration circuit 1524A-A's RF output is single-ended and is 50Ω matched across a wide RF frequency range from 700MHz to 5GHz with better than 10dB return loss using C7=6.8pF and C8=0.2pF. For 240MHz operation, C7=4.7nH and C8=10pF is recommended. For 450MHz, C7=2.7nH and C8=10pF is recommended. The frequency of the best match is purposefully set lower than the band center frequency to compensate for the gain roll-off of the on-chip RF output balun at lower frequencies. Refer to the LTC5588-1 datasheet for more information and impedance data.

LINEARITY OPTIMIZATION
The LTC5588-1 features a LINOPT input pin for optimizing the linearity of the RF circuitry. The nominal DC bias voltage of the LINOPT pin is 2.56V, and the typical adjustment range is from 2V to VCC+0.3V. The LINOPT pin's input impedance is about 150Ω while the IC is enabled. The LINOPT voltage for optimum linearity is a function of LO frequency, temperature, supply voltage, baseband frequency, high-side or low-side LO injection, process, signal bandwidth, and RF output level.

TEST EQUIPMENT AND SETUP
The LTC5588-1 is a high linearity direct quadrature modulator IC with very high output 2nd and 3rd order intercepts. Accuracy of its performance measurement is highly dependent on equipment setup and measurement technique. Then following precautions are recommended:

1. Use high performance signal generators with fully configurable differential I and Q outputs, such as the Rohde & Schwarz SMJ100A vector signal generator or equivalent.

2. The third harmonic content of the LO can degrade image rejection severely. It should be kept at least 6dB lower than the desired image rejection. Although the second harmonic content of the LO is less damaging, it can still be significant, and should be kept as low as possible.

3. Cables connecting the baseband signal source to the demonstration circuit baseband inputs should provide a well-defined match for the entire baseband frequency range up to 500MHz. Therefore, short, high quality coaxial cables are recommended.

4. If possible, use small attenuator pads with good VSWR on the demonstration circuit LO input and RF output ports to improve source and load match to reduce reflections, which may degrade measurement accuracy.

5. Use narrow resolution bandwidth (RBW) and engage video averaging on the spectrum analyzer to lower the displayed average noise level (DANL) in order to improve sensitivity and to increase dynamic range. However, the trade off is increased sweep time.

6. Spectrum analyzers can produce significant internal distortion products if they are overdriven. Generally, spectrum analyzers are designed to operate at their best with about -30dBm to -40dBm at their input filter or preselector. Sufficient spectrum analyzer input attenuation should be used to avoid saturating the instrument, but too much attenuation reduces sensitivity and dynamic range.

7. Before taking measurements, the system performance should be evaluated to ensure that: 1) clean input signal can be produce, 2) the LO harmonics are minimized, 3) the spectrum analyzer's internal distortion is minimized, 4) the spectrum analyzer has enough dynamic range and sensitivity, and 5) the system is accurately calibrated for power and frequency.
QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1524A-A
200MHz TO 6000MHz QUADRATURE MODULATOR WITH ULTRAHIGH OIP3

QUICK START PROCEDURE

Demonstration circuit 1524A-A is easy to set up to evaluate the performance of the LTC5588-1. Refer to Figure 1 and Figure 2 for proper measurement equipment connections and follow the procedure below:

NOTE: Care should be taken to never exceed absolute maximum input ratings. Observe standard ESD precautions and avoid static discharge.

TURNING ON THE DEMONSTRATION CIRCUIT
1. Remove the demonstration circuit from its protective packaging in an ESD-safe working area.
2. Turn off DC power supply. Turn off baseband and LO signal sources outputs.
3. With the power supply and the signal sources turned off, connect the four baseband inputs: BBPI, BBMI, BBPQ, and BBMQ.
4. Turn on baseband signal source DC bias, and slowly increase the DC common-mode voltage (V_CMBB) to 0.5V. Do not exceed 0.55V.
5. Connect DC power supply, and slowly increase supply voltage to 3.45V. Using a voltmeter, verify the voltages at the LTC5588-1 V_CC pins 18 (TP2) and 24 (TP1) are 3.3V. Adjust if necessary. Do not exceed 3.8V at pins 18 and 24.
6. Apply 3.3V to demonstration circuit 1524A-A’s enable control (EN). The enable voltage must never exceed the LTC5588-1’s Vcc supply voltage (TP1 and TP2) by 0.3V or drop below -0.3V.
7. Verify the total V_CC supply current is approximately 303mA. The demonstration circuit is now turned on and is ready for measurements.
8. The turn off procedure is the reverse of the turn on procedure. Make sure V_CC is removed before V_CMBB.

RETURN LOSS MEASUREMENTS (FIGURE 1)
1. Turn on the demonstration circuit by following the procedures above.
2. Configure the Network Analyzer for return loss measurement, set appropriate frequency range, and set the test signal to 0dBm.
3. Calibrate the Network Analyzer.
4. Connect a 50Ω termination to the LOP input.
5. Connect the Network Analyzer test-set cable to the LOM input, and measure single-ended LO input return loss.
6. Connect the Network Analyzer test-set cable to the RF output, and measure RF output return loss.

VOLTAGE CONVERSION GAIN, OUTPUT 1dB COMPRESSION, IMAGE REJECTION, AND LO FEEDTHROUGH MEASUREMENTS (FIGURE 2)
1. Turn on the demonstration circuit by following the procedures above.
2. Connect the RF output to the Spectrum Analyzer.
3. Connect a 50Ω termination to the LOP input.
4. Connect the LO source to LOM input and apply a 1900MHz, 0dBm, CW signal.
5. Set the baseband signal source to provide a 100kHz, 1V_P-P(DIFF) baseband input signal. The I- and the Q-channels should be 90° shifted and set for lower side-band selection.
6. Measure the modulator RF output on the Spectrum Analyzer at 1899.9MHz.
7. Calculate Conversion Voltage Gain:

\[
G_V = 20 \cdot \log \left( \frac{V_{RF(OUT)}(50\Omega)}{V_{IN(DIFF)}(I \text{ OR } Q)} \right)
\]
8. Measure Output 1dB Compression point by increasing input signal level until the Conversion Voltage Gain degrades by 1dB.
9. Measure Image Rejection at 1900.1MHz.
10. Measure LO Feedthrough at 1900MHz.
QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1524A-A
200MHz TO 6000MHz QUADRATURE MODULATOR WITH ULTRAHIGH OIP3

OUTPUT 2ND ORDER AND 3RD ORDER INTERCEPT MEASUREMENTS (FIGURE 2)

1. Set the baseband signal source to provide a two-tone baseband input signal at 4.5MHz and 5.5MHz with 1V_p-p(diff) each tone. The I- and the Q-channels should be 90° shifted and set for lower side-band selection.

2. Measure the modulator RF output on the Spectrum Analyzer:
   a. The two-tone RF output signals are located at 1894.5MHz and 1895.5MHz.
   b. The 2nd order intermodulation product is located at 1890MHz.
   c. The 3rd order intermodulation products are located at 1893.5MHz and 1896.5MHz.

3. Calculate the Output 2nd and 3rd Order Intercepts:
   \[ OIP2 = 2 \cdot P_{OUT} - P_{IM2} \]
   \[ OIP3 = \frac{(3 \cdot P_{OUT} - P_{IM3})}{2} \]
   Where \( P_{OUT} \) is the lowest power level of the two RF output signals at either 1894.5MHz or 1895.5MHz, \( P_{IM2} \) is the 2nd order intermodulation product level at 1890MHz, and \( P_{IM3} \) is the largest 3rd order intermodulation product level at either 1893.5MHz or 1896.5MHz. All units are in dBm.

   Alternatively, the output intercept can be calculated using the power difference between the desired output signal and the intermodulation products:
   \[ OIP2 = \Delta_{IM2} + P_{OUT} \]
   \[ OIP3 = \frac{\Delta_{IM3}}{2} + P_{OUT} \]
   Where \( \Delta_{IM(2\ OR\ 3)} = P_{OUT} - P_{IM(2\ OR\ 3)} \).

USING LINEARITY OPTIMIZATION

1. Apply a 2.5V DC voltage to demonstration circuit 1524A-A’s linearity optimization control input (LINOPT).

2. Measure Output 3rd Order Intercept by following the procedures above.

3. Adjust LINOPT voltage and re-measure OIP3 until desired performance is achieved. The LINOPT adjustment range is 2V to Vcc+0.3V. The LINOPT voltage must not exceed the LTC5588-1’s Vcc supply voltage (TP1 and TP2) by 0.3V or drop below -0.3V.

4. To disable linearity optimization, disconnect LINOPT, and leave it floating.
Figure 1. Proper Equipment Setup for Return Loss Measurements
Figure 2. Proper Equipment Setup for RF Performance Measurements
Figure 3. Demonstration Circuit Schematic