

LTM9011-14, LTM9010-14,
 LTM9009-14, LTM9008-14, LTM9007-14,
 LTM9006-14: 14-Bit, 125/105/80/
 65/40/25MSPS Octal ADC Family

DESCRIPTION

DC1884 supports the LTM[®]9011 high speed, octal ADC family.

The versions of the 1884A demo board are listed in Table 1. Depending on the required resolution and sample rate, the DC1884 is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input

frequencies from 1MHz to 70MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at <http://www.linear.com/demo/DC1884A>

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Table 1. DC1884 Variants

DC1884 VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1884A-A	LTM9011-14	14-Bit	125MSPS	1MHz to 70MHz
1884A-B	LTM9010-14	14-Bit	105MSPS	1MHz to 70MHz
1884A-C	LTM9009-14	14-Bit	80MSPS	1MHz to 70MHz
1884A-D	LTM9008-14	14-Bit	65MSPS	1MHz to 70MHz
1884A-E	LTM9007-14	14-Bit	40MSPS	1MHz to 70MHz
1884A-F	LTM9006-14	14-Bit	25MSPS	1MHz to 70MHz

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage – DC1884A	Depending on Sampling Rate and the A/D Converter Provided, This Supply Must Provide Up to 700mA	Optimized for 3.5V [3.3V to 6V Minimum/Maximum]
Analog Input Range	Depending on SENSE Pin Voltage	1V _{p-p} to 2V _{p-p}
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode)	350mV/1.25V Common Mode
	Minimum Logic Levels (100Ω Load, 3.5mA Mode)	247mV/1.25V Common Mode
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Encode Clock Level	Single-Ended Encode Mode (ENC ⁻ Tied to GND)	0V to 3.6V
Encode Clock Level	Differential Encode Mode (ENC ⁻ Not Tied to GND)	0.2V to 3.6V
Resolution	See Table 1	
Input Frequency Range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

DC1884 is easy to set up to evaluate the performance of the LTM9011 family of A/D converters. For proper measurement equipment setup, refer to Figure 1 and follow the procedure explained in the following sections.

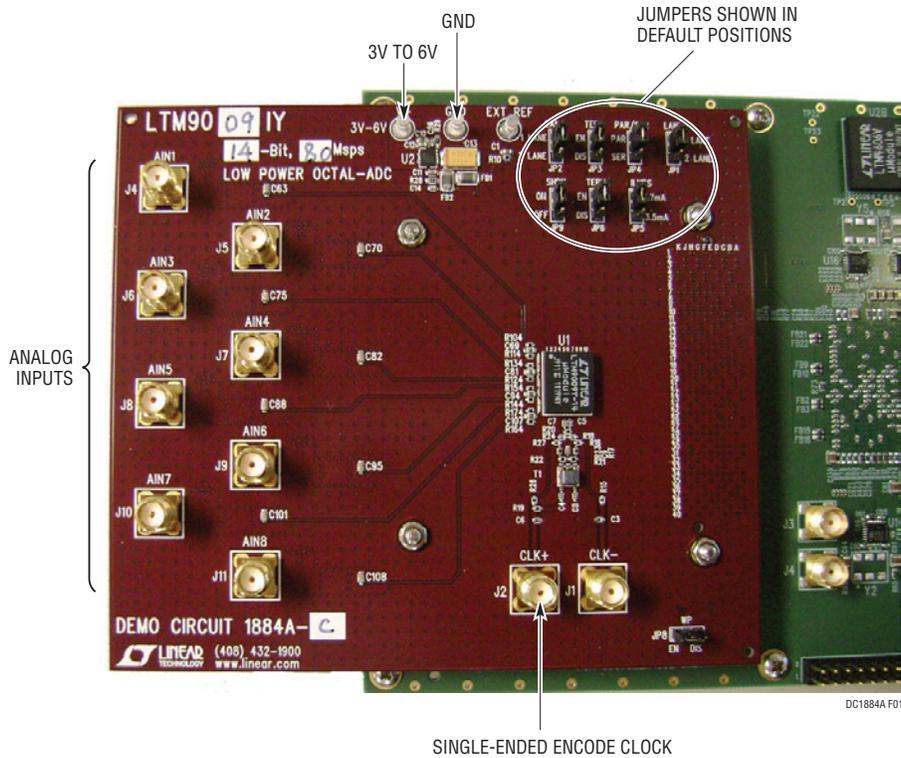


Figure 1. Test Setup of DC1884

QUICK START PROCEDURE

Setup

If a DC1371 data acquisition and collection system was supplied with the DC1884, follow the DC1371 Quick Start Guide to install the required software and to connect the DC1371 to the DC1884 and to a PC.

DC1884 Board Jumpers

The DC1884 board should have the following jumper settings as default positions (as per Figure 1):

JP14: PAR/SER: Selects Parallel or Serial Programming Mode. (Default: Serial)

Optional Jumpers AJ3 and J6: Term: Enables/Disables Optional Output Termination. (Default: Removed)

JP5: I_{LVDS}: Selects Either 1.75mA or 3.5mA of Output Current for the LVDS Drivers. (Default: Removed)

JP1 and JP2: Lane: Selects Either 1-Lane or 2-Lane Output Modes (Default: Removed)

Note: The DC1371 does not support 1-Lane operation.

JP9: SHDN: Enables and Disables the LTM9011. (Default: Removed)

JP8: WP: Enable/Disables Write Protect for the EEPROM. (Default: Removed)

Note: Optional jumper should be left open to ensure proper serial configuration.

Applying Power and Signals to the DC1884

The DC1371 is used to acquire data from the DC1884. The DC1371 must first be connected to a powered USB port and have 5V applied power before applying 3.5V across the pins marked V⁺ and “GND” on the DC1884. DC1884 requires 3.5V for proper operation.

The DC1884 demonstration circuit requires up to 700mA depending on the sampling rate and the A/D converter supplied.

The DC1884 should not be removed or connected to the DC1371 while power is applied.

Analog Input Network

For optimal distortion and noise performance, the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 70MHz, refer to the LTM9011 data sheet for a proper input network.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a gallium arsenide gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and high IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demonstration circuit.

Encode Clock

Note: Apply an encode clock to the SMA connector on the DC1884 demonstration circuit board marked “J2 CLK⁺.” As a default, the DC1884 is populated to have a single-ended input.

For the best noise performance, the ENCODE input must be driven with a very low jitter, square wave source. The amplitude should be large, up to 3V_{P-P} or 13dBm. When using a sinusoidal signal generator, a squaring circuit can be used. Linear Technology also provides demo board DC1075A that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTM9011.

QUICK START PROCEDURE

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1884 a bandpass filter used for the clock should be used prior to the DC1075A. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used for both the clock input and the analog input.

Digital Outputs

Data outputs, data clock, and frame clock signals are available on J1 of the DC1884. This connector follows the VITA-57/FMC standard, but all signals should be verified when using an FMC carrier card other than the DC1371.

Software

The DC1371 is controlled by the PScope system software that can be downloaded from the Linear Technology website at <http://www.linear.com/software/>.

To start the data collection software, “PScope.exe,” which is installed by default to \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu, and browse to the PScope directory and select “PScope.”

If the DC1884 is properly connected to the DC1371, PScope should automatically detect the DC1884 and configure itself accordingly.

If everything is hooked up properly and a powered and suitable convert clock is present, clicking the “Collect” button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371 Quick Start Guide, and in the online help feature within the PScope program itself.

Serial Programming

PScope has the ability to program the DC1884 serially through the DC1371. There are several options available in the LTM9011 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the “Set Demo Bd Options” icon on the PScope toolbar (Figure 2).

This will bring up the menu shown in Figure 3.

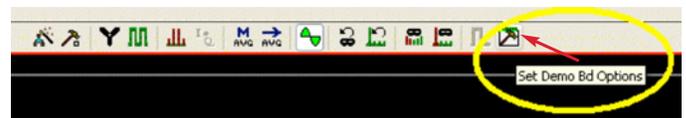


Figure 2. PScope Toolbar

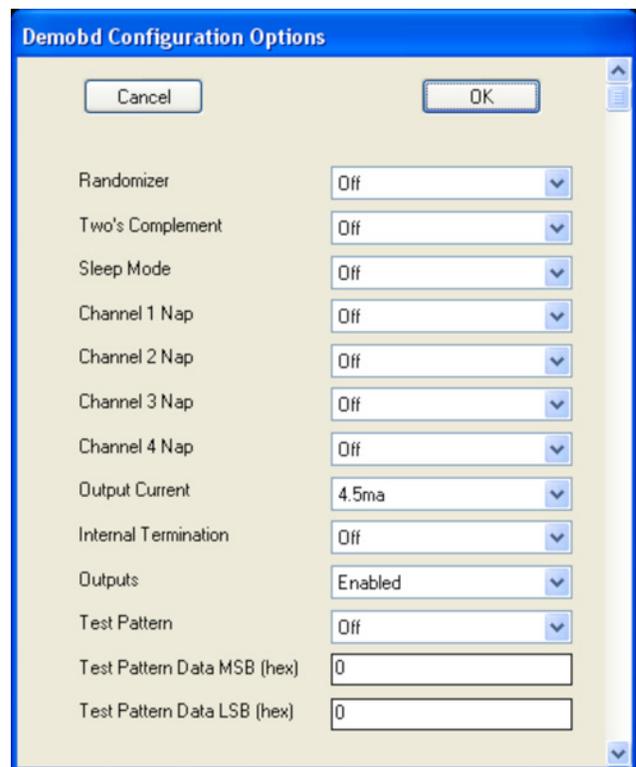


Figure 3. Demo Board Configuration Options

QUICK START PROCEDURE

This menu allows any of the options available for the LTM9011 family to be programmed serially. The LTM9011 family has the following options:

Randomizer: Enables Data Output Randomizer.

- Off (Default): Disables data output randomizer.
- On: Enables data output randomizer.

Two's Complement: Enables Two's Complement Mode.

- Off (Default): Selects offset binary mode.
- On: Selects two's complement mode.

Sleep Mode: Selects Between Normal Operation and Sleep Mode.

- Off (Default): Entire ADC is powered and active.
- On: The entire ADC is powered down.

Channel 1 Nap: Selects Between Normal Operation and Putting Channel 1 in Nap Mode.

- Off (Default): Channel 1 is active.
- On: Channel 1 is in nap mode.

Channel 2 Nap: Selects Between Normal Operation and Putting Channel 2 in Nap Mode.

- Off (Default): Channel 2 is active.
- On: Channel 2 is in nap mode.

Channel 3 Nap: Selects Between Normal Operation and Putting Channel 3 in Nap Mode.

- Off (Default): Channel 3 is active.
- On: Channel 3 is in nap mode.

Channel 4 Nap: Selects Between Normal Operation and Putting Channel 4 in Nap Mode.

- Off (Default): Channel 4 is active.
- On: Channel 4 is in nap mode.

Output Current: Selects the LVDS Output Drive Current.

- 1.75mA (Default): LVDS output driver current.
- 2.1mA: LVDS output driver current.
- 2.5mA: LVDS output driver current.
- 3.0mA: LVDS output driver current.
- 3.5mA: LVDS output driver current.
- 4.0mA: LVDS output driver current.
- 4.5mA: LVDS output driver current.

Internal Termination: Enables LVDS Internal Termination.

- Off (Default): Disables internal termination.
- On: Enables internal termination.

Outputs: Enables Digital Outputs.

- Enabled (Default): Enables digital outputs.
- Disabled: Disables digital outputs.

Test Pattern: Selects Digital Output Test Patterns. The desired test pattern can be entered into the text boxes provided.

- Off (Default): ADC input data is displayed.
- On: Test pattern is displayed.

Once the desired settings are selected, click "OK" and PScope will automatically update the register of the device on the DC1884 demo board.

DEMO MANUAL DC1884A

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