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Regulatory Compliance

The ADSP-21369 EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-21369 EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 2004/108/EC and therefore carries the “CE” mark.

The ADSP-21369 EZ-KIT Lite has been appended to Analog Devices, Inc. EMC Technical File (EMC TF) referenced DSPTOOLS1, issue 2 dated June 4, 2008 and was declared CE compliant by an appointed Notified Body (No.0673) as listed below.

Notified Body Statement of Compliance: Z600ANA1.025 dated December 19, 2005

Issued by: Technology International (Europe) Limited
60 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TY, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.
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Thank you for purchasing the ADSP-21369 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for SHARC® processors.

SHARC processors are based on a 32-bit super Harvard architecture that includes a unique memory architecture comprised of two large on-chip, dual-ported SRAM blocks coupled with a sophisticated I/O processor, which gives a SHARC processor the bandwidth for sustained high-speed computations. SHARC processors represents today’s de facto standard for floating-point processing, targeted toward premium audio applications.

The evaluation system is designed to be used in conjunction with the VisualDSP++® development environment to test capabilities of the ADSP-21369 SHARC processors. The VisualDSP++ development environment aides advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-21369 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-21369 processor from a personal computer (PC) is achieved through a USB port or an external JTAG emulator. The USB interface provides unrestricted access to the ADSP-21369 processor and
evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools/.

The ADSP-21369 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. For details about evaluation license restrictions after the 90 days, refer to “Evaluation License Restrictions” on page 1-7 and the VisualDSP++ Installation Quick Reference Card.

The ADSP-21369 EZ-KIT Lite provides example programs to demonstrate the product capabilities.

**Product Overview**

The board features:

- Analog Devices ADSP-21369 SHARC processor
  - 256-pin SBGA package
  - 400 MHz core clock speed
- Synchronous dynamic random access memory (SDRAM)
  - 1M x 32-bit x 4 banks
- Synchronous random access memory (SRAM)
  - 512 Kbit x 8-bit
- Flash memory
  - 1M x 8-bit
• Serial peripheral interface (SPI) flash memory
  ✓ 2 Mbit
• Analog audio interface
  ✓ AD1835A codec
  ✓ 4 x 2 RCA phono jack for 4 channels of stereo output
  ✓ 2 x 1 RCA phono jack for 1 channel of stereo input
  ✓ 3.5 mm headphone jack for 1 channel stereo output
• Digital audio interface
  ✓ RCA phono jack output
  ✓ RCA phono jack input
• Universal asynchronous receiver/transmitter (UART)
  ✓ ADM3202 RS-232 driver/receiver
  ✓ DB9 female connector
• National Instruments Educational Laboratory Virtual Instrumentation Suite (ELVIS) Interface
  ✓ LabVIEW™-based virtual instruments
  ✓ Multifunction data acquisition device
  ✓ Bench-top workstation and prototype board
• LEDs
  ✓ Eleven LEDs: one power (green), one board reset (red), one USB monitor (amber), and eight general-purpose (amber)
Product Overview

- Push buttons
  - Five push buttons: one reset, two connected to DAI, and two connected to the FLAG pins of the processor
- Expansion interface (Type A)
  - Parallel port, FLAG pins, DPI, DAI
- Other features
  - JTAG ICE 14-pin header
  - Test points for processor current measurement
  - DPI header
  - DAI header

The EZ-KIT Lite board has a total of 1 MB of parallel flash memory and 2 Mbit of SPI flash memory. Flash memories can store user-specific boot code and allow the board to run as a stand-alone unit. For more information, see “External Memory” on page 1-7 and “Boot Mode and Clock Ratio Select Switch (SW2)” on page 2-10. The board also has 512 KB of SRAM and 16 MB of SDRAM, which can be used at runtime.

The DAI port of the processor is connected to the AD1835A audio codec, Sony/Philips Digital Interface (S/PDIF), and an external phase lock loop (PLL). The DAI interface facilitates development of digital and analog audio signal-processing applications. See “Analog Audio” on page 1-10 and “S/PDIF Coax Connectors (J7 and J8)” on page 2-24 for more information.

The DPI port of the processor is connected to the UART and SPI interfaces. The UART interface can connect to a standard RS-232 connector, while the SPI connects to 2 Mbit of serial flash memory.
Additionally, the EZ-KIT Lite board provides access to all of the processor’s peripheral ports. Access is provided in the form of a three-connector expansion interface. See “Expansion Interface” on page 2-7 for details.

**Purpose of This Manual**

The *ADSP-21369 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-21369 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided for reference.

The product software component is detailed in the *VisualDSP++ Installation Quick Reference Card*.

**Intended Audience**

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts (such as the *ADSP-2136x SHARC Processor Programming Reference* and *ADSP-21368 SHARC Processor Hardware Reference*) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and user’s or getting started guides. For the locations of these documents, see “Related Documents”.
Manual Contents

The manual consists of:

- Chapter 1, “Using ADSP-21369 EZ-KIT Lite” on page 1-1
  Describes EZ-KIT Lite operation from a programmer’s perspective and provides an easy-to-access memory map.

- Chapter 2, “ADSP-21369 EZ-KIT Lite Hardware Reference” on page 2-1
  Provides information on the EZ-KIT Lite hardware components

- Appendix A, “ADSP-21369 EZ-KIT Lite Bill Of Materials” on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.

- Appendix B, “ADSP-21369 EZ-KIT Lite Schematic” on page B-1
  Provides the resources to allow board-level debugging or to use as a reference guide. Appendix B is part of the online Help.

What’s New in This Manual

The ADSP-21369 EZ-KIT Lite Evaluation System Manual has been updated to reflect the latest board revision. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.
Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:


- E-mail tools questions to processor.tools.support@analog.com

- E-mail processor questions to processor.support@analog.com (World wide support)
  processor.europe@analog.com (Europe support)
  processor.china@analog.com (China support)

- Phone questions to 1-800-ANALOGD

- Contact your Analog Devices, Inc. local sales office or authorized distributor

- Send questions by mail to:
  Analog Devices, Inc.
  One Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

The ADSP-21369 EZ-KIT Lite evaluation system supports Analog Devices ADSP-21369 SHARC processors.
Product Information

Product Information

Product information can be obtained from the Analog Devices Web site, VisualDSP++ online Help system, and a technical library CD.

Analog Devices Web Site


To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Visit MyAnalog.com to sign up. If you are a registered user, just log on. Your user name is your e-mail address.
VisualDSP++ Online Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, Dinkum Abridged C++ library, and FLEXnet License Tools software documentation. You can search easily across the entire VisualDSP++ documentation set for any topic of interest.

For easy printing, supplementary Portable Documentation Format (.pdf) files for all manuals are provided on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

<table>
<thead>
<tr>
<th>File</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>.chm</td>
<td>Help system files and manuals in Microsoft help format</td>
</tr>
<tr>
<td>.htm or .html</td>
<td>Dinkum Abridged C++ library and FLEXnet License Tools software documentation. Viewing and printing the .html files requires a browser, such as Internet Explorer 6.0 (or higher).</td>
</tr>
<tr>
<td>.pdf</td>
<td>VisualDSP++ and processor manuals in PDF format. Viewing and printing the .pdf files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).</td>
</tr>
</tbody>
</table>

Technical Library CD

The technical library CD contains seminar materials, product highlights, a selection guide, and documentation files of processor manuals, VisualDSP++ software manuals, and hardware tools manuals for the following processor families: Blackfin, SHARC, TigerSHARC, ADSP-218x, and ADSP-219x.

To order the technical library CD, go to http://www.analog.comprocessors/technical_library, navigate to the manuals page for your processor, click the request CD check mark, and fill out the order form.
Related Documents

Data sheets, which can be downloaded from the Analog Devices Web site, change rapidly, and therefore are not included on the technical library CD. Technical manuals change periodically. Check the Web site for the latest manual revisions and associated documentation errata.

Related Documents

For information on product related development software and hardware, see these publications:

Table 1. Related Processor Publications

<table>
<thead>
<tr>
<th>Title</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADSP-21367/ADSP-21368/ADSP-21369 SHARC Processors Data Sheet</td>
<td>General functional description, pinout, and timing of the processor</td>
</tr>
<tr>
<td>ADSP-21368 SHARC Processor Hardware Reference (Includes ADSP-21367, ADSP-21368, ADSP-21369, ADSP-21371, ADSP-21375)</td>
<td>Description of the internal processor architecture, registers, and all peripheral functions</td>
</tr>
<tr>
<td>ADSP-2136x SHARC Processor Programming Reference</td>
<td>Description of all allowed processor assembly instructions</td>
</tr>
</tbody>
</table>

Table 2. Related VisualDSP++ Publications

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>VisualDSP++ Assembler and Preprocessor Manual</td>
<td>Description of the assembler function and commands</td>
</tr>
<tr>
<td>VisualDSP++ C/C++ Compiler Manual for SHARC Processors</td>
<td>Description of the compiler function and commands for SHARC processors</td>
</tr>
<tr>
<td>VisualDSP++ Run-Time Library Manual for SHARC Processors</td>
<td>Description of the run-time library functions for SHARC processors</td>
</tr>
</tbody>
</table>
Text conventions used in this manual are identified and described as follows.

<table>
<thead>
<tr>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Close command (File menu)</td>
<td>Titles in reference sections indicate the location of an item within the VisualDSP++ environment’s menu system (for example, the Close command appears on the File menu).</td>
</tr>
<tr>
<td>{this</td>
<td>that}</td>
</tr>
<tr>
<td>[this</td>
<td>that]</td>
</tr>
<tr>
<td>[this,...]</td>
<td>Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of this.</td>
</tr>
<tr>
<td>.SECTION</td>
<td>Commands, directives, keywords, and feature names are in text with letter gothic font.</td>
</tr>
<tr>
<td>filename</td>
<td>Non-keyword placeholders appear in text with italic style format.</td>
</tr>
</tbody>
</table>
### Notation Conventions

<table>
<thead>
<tr>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
</table>
| ![Note](https://example.com/note.png) | **Note:** For correct operation, ...  
A Note provides supplementary information on a related topic. In the online version of this book, the word *Note* appears instead of this symbol. |
| ![Caution](https://example.com/caution.png) | **Caution:** Incorrect device operation may result if ...  
Caution: Device damage may result if ...  
A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word *Caution* appears instead of this symbol. |
| ![Warning](https://example.com/warning.png) | **Warning:** Injury to device users may result if ...  
A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word *Warning* appears instead of this symbol. |
1 USING ADSP-21369 EZ-KIT LITE

This chapter provides information to assist you with development of programs for the ADSP-21369 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- “Package Contents” on page 1-2
  Lists the items contained in your EZ-KIT Lite package.

- “Default Configuration” on page 1-3
  Shows the default configuration of the EZ-KIT Lite board.

- “Installation and Session Startup” on page 1-5
  Instructs how to start a new or open an existing EZ-KIT Lite session using VisualDSP++.

- “Evaluation License Restrictions” on page 1-7
  Describes the VisualDSP++ license restrictions; the Visual DSP++ licence is shipped with the EZ-KIT Lite.

- “External Memory” on page 1-7
  Describes the memory map of the EZ-KIT Lite; describes how to access external memory.

- “ELVIS Interface” on page 1-9
  Describes the on-board National Instruments Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) interface.

- “Analog Audio” on page 1-10
  Describes how to set up and communicate with the on-board audio codec.
**Package Contents**

- “LEDs and Push Buttons” on page 1-12
  Describes the board’s general-purpose I/O pins and buttons.

- “Example Programs” on page 1-13
  Provides information about example programs included in the evaluation system.

- “Background Telemetry Channel” on page 1-13
  Highlights the advantages of the Background Telemetry Channel feature of VisualDSP++.

- “Reference Design Information” on page 1-14
  Highlights the available technical resources for the design, layout, fabrication, and assembly of the EZ-KIT Lite.

For information on the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online Help.

For detailed information on how to program the ADSP-21369 SHARC processor, refer to the documents referenced in “Related Documents”.

**Package Contents**

Your ADSP-21369 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-21369 EZ-KIT Lite board
- *VisualDSP++ Installation Quick Reference Card*
- CD containing:
  - VisualDSP++ software
  - ADSP-21369 EZ-KIT Lite debug software
  - USB driver files
Using ADSP-21369 EZ-KIT Lite

- Example programs
- *ADSP-21369 EZ-KIT Lite Evaluation System Manual* (this document)

- Universal 7V DC power supply
- USB 2.0 cable
- 3.5 mm stereo headphones
- 6-foot RCA audio cable
- 6-foot 3.5 mm/RCA x 2 Y-cable

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-21369 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components.
To connect the EZ-KIT Lite board:

1. Remove the EZ-KIT Lite board from the package. Be careful when handling the board to avoid the discharge of static electricity, which may damage some components.

2. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before continuing.

Figure 1-1. EZ-KIT Lite Hardware Setup
3. Plug the provided power supply into J4 on the EZ-KIT Lite board. Visually verify that the green power LED (LED9) is on. Also verify that the red reset LED (LED10) goes on for a moment and then goes off, and, finally, LED1 through LED8 are sequentially blinking.

4. Connect one end of the USB cable to an available full speed USB port on your PC and the other end to ZJ1 on the ADSP-21369 EZ-KIT Lite board.

### Installation and Session Startup

For correct operation, install the software and hardware in the order presented in the *VisualDSP++ Installation Quick Reference Card*.

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the Start -> Programs menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the Ctrl key while starting VisualDSP++. Do not release the Ctrl key until the Session Wizard appears on the screen. Go to step 4.
Installation and Session Startup

3. To connect to a new EZ-KIT Lite session, start Session Wizard by selecting one of the following.
   - From the Session menu, New Session.
   - From the Session menu, Session List. Then click New Session from the Session List dialog box.
   - From the Session menu, Connect to Target.

4. The Select Processor page of the wizard appears on the screen. Ensure SHARC is selected in Processor family. In Choose a target processor, select ADSP-21369. Click Next.

5. The Select Connection Type page of the wizard appears on the screen. Select EZ-KIT Lite and click Next.

6. The Select Platform page of the wizard appears on the screen. Ensure that the selected platform is ADSP-21369 EZ-KIT Lite via Debug Agent. Specify your own Session name for your session or accept the default name.

   The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and open a new session.

   Click Next.

7. The Finish page of the wizard appears on the screen. The page displays your selections. Check the selections. If you are not satisfied, click Back to make changes; otherwise, click Finish. VisualDSP++
Using ADSP-21369 EZ-KIT Lite

creates the new session and connects to the EZ-KIT Lite. Once connected, the main window’s title is changed to include the session name set in step 6.

To disconnect from a session, click the disconnect button or select Session—>Disconnect from Target.

To delete a session, select Session —> Session List. Select the session name from the list and click Delete. Click OK.

Evaluation License Restrictions

The ADSP-21369 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

1. VisualDSP++ allows a connection to the ADSP-21369 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.

2. The linker restricts a user program to 7281 words of memory for code space with no restrictions for data space.

Refer to the VisualDSP++ Installation Quick Reference Card for details.

External Memory

The EZ-KIT Lite contains four types of memory: parallel flash (1 MB), SPI flash (2 Mbit), SRAM (512 Kbit), and SDRAM (128 Mbit). Flash memories can store user-specific boot code and allow the board to run as a stand-alone unit. For more information on how to select a boot device for the processor, see “Boot Mode and Clock Ratio Select Switch (SW2)” on page 2-10.
Table 1-1 provides start and end addresses of the on-board external memories.

Table 1-1. EZ-KIT Lite Evaluation Board External Memory

<table>
<thead>
<tr>
<th>Start Address</th>
<th>End Address</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0020 0000</td>
<td>0x0027 FFFF</td>
<td>SRAM memory (~MS0)</td>
</tr>
<tr>
<td>0x0400 0000</td>
<td>0x040F FFFF</td>
<td>Flash memory (~MS1)</td>
</tr>
<tr>
<td>0x0800 0000</td>
<td>0x083F 0000</td>
<td>SDRAM memory (~MS2)</td>
</tr>
<tr>
<td>0x0C00 0000</td>
<td>0x0CFF FFFF</td>
<td>Unused chip select (~MS3) for non-SDRAM addresses</td>
</tr>
<tr>
<td>0x0C00 0000</td>
<td>0x0FFF FFFF</td>
<td>Unused chip select (~MS3) for SDRAM addresses</td>
</tr>
</tbody>
</table>

Parallel flash memory, SDRAM, and SRAM are connected to the external memory of the processor. To access SRAM and flash memories, use memory addressing via the respective memory bank or use the DMA controller.

SDRAM memory is connected to the SDRAM controller of the processor. A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory accesses. Care must be taken when configuring the SDRAM control registers. For more information regarding the setup of the SDRAM controller, refer to the *ADSP-21368 SHARC Processor Hardware Reference* (includes ADSP-21369).

An example program is included in the EZ-KIT Lite installation directory to demonstrate the controller setup.

SPI flash memory is connected to the SPI port of the processor; SPI flash designates:

- DPI pin 5 (DPI5) as a chip select
- DPI pin 3 (DPI3) as the SPI clock
- DPI pin 1 (DPI1) as the MOSI
- DPI pin 2 (DPI2) as the MISO
By default, the DPI is set up for the SPI flash, and any required changes to the SPI flash can be made by modifying the DPI of the processor. An example program is included in the EZ-KIT Lite installation directory to demonstrate the SPI flash memory reads and writes.

Asynchronous SRAM memory and parallel flash memory are connected to the asynchronous memory controller of the processor. Each of their respective memory banks can be programmed independently with different timing parameters. For more information on changing wait states to speed up or slow down the asynchronous controller and other setup information, refer to the ADSP-21368 SHARC Processor Hardware Reference (includes ADSP-21369).

Example programs are included in the EZ-KIT Lite installation directory to demonstrate flash memory reads and writes.

**ELVIS Interface**

The ADSP-21369 EZ-KIT Lite board contains the National Instruments Educational Laboratory Virtual Instrumentation Suite interface. The interface features the DC voltage and current measurement modules, oscilloscope and bode analyzer modules, function generator, arbitrary waveform generator, and digital I/O.

The ELVIS interface is a LabVIEW-based design and prototype environment for university science and engineering laboratories. The ELVIS interface consists of LabVIEW-based virtual instruments, a multifunction data acquisition (DAQ) device, and a custom-designed bench-top workstation and prototype board. This combination provides a ready-to-use suite of instruments found in most educational laboratories. Because the interface is based on LabVIEW and provides complete data acquisition and prototyping capabilities, the system is ideal for academic coursework that range from lower-division classes to advanced project-based curriculums.
Analog Audio

For more information on ELVIS and example demonstration programs, visit National Instruments Web site at www.ni.com.

Analog Audio

The AD1835A device is a high-performance, single-chip codec featuring four stereo digital-to-analog converters (DACs) for audio output and one stereo analog-to-digital converters (ADCs) for audio input. The codec can input and output data with a sample rate of up to 96 kHz on all channels. A 192 kHz sample rate can be used with one of the DAC channels.

The processor is interfaced with the AD1835A codec via the DAI port. The DAI pins can be configured to transfer serial data from the codec in either time-division multiplexed (TDM) or 2-wire interface mode (TWI). For more information on the AD1835A connection to the DAI, see “DAI Interface” on page 2-4.

The master input clock (MCLK) for the AD1835A codec can be generated by the on-board 12.288 MHz oscillator or supplied by one of the DAI pins of the processor. Using a DAI pin to generate the MCLK, as opposed to the on-board oscillator, allows synchronization of multiple devices in the system. This is done on the EZ-KIT Lite when data is coming from the Sony/Philips Digital Interface (S/PDIF) receiver and being output through the codec. The S/PDIF MCLK is routed to the AD1835A’s MCLK in the processor’s signal routing unit (SRU). It is possible to disable the on-board audio oscillator from driving the audio codec and the processor’s input pin. For instructions on how to configure the clock, refer to “Codec Setup Switch (SW3)” on page 2-11.

The AD1835A codec can be configured as a master or a slave, depending on the DIP switch settings. In master mode, the codec drives the serial port clock and frame sync signals to the processor. In slave mode, the processor must generate and drive all of the serial port clock and frame sync signals. For more information, refer to “Codec Setup Switch (SW3)” on page 2-11.
The internal configuration registers of the codec are configured using the SPI port of the processor. The DPI pin 4 (DPI4 register) is used as the select for the device. For information on how to configure the multichannel codec, refer to the product datasheet at http://www.analog.com/en/prod/0,2877,AD1835A,00.html.

The RCA connector (J10) is used to input analog audio. When using an electret microphone on this connector, configure switch SW4 according to the instructions in “Electret Microphone Select Switch (SW4)” on page 2-12. The four output channels connect to the RCA connector (J5). Channel 4 of the codec connects to the headphone jack (J9). For more information, see “Connectors” on page 2-21.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to configure and use the board’s analog audio interface.
The EZ-KIT Lite has eight general-purpose user LEDs and four general-purpose push buttons.

Two general-purpose push buttons are attached to the FLAG pins of the processor, while the other two are attached to the DAI pins. All of the push buttons are connected to the processor through a DIP switch (SW7). The DIP switch can disconnect the processor pins connected to the push buttons. See “Push Button Enable Switch (SW7)” on page 2-13 for instructions on how to disable a push button from driving its corresponding processor pin.

The state of the push buttons connected to the FLAG pins can be determined by reading the FLAG register. The push buttons connected to the DAI pins must be configured as interrupts. It is necessary to set up an interrupt routine to determine each pin’s state. Table 1-2 shows the push button and processor connections. Refer to the related example program shipped with the EZ-KIT Lite for more information.

Table 1-2. Push Button Connections

<table>
<thead>
<tr>
<th>Push Button Label</th>
<th>Push Button Reference Designator</th>
<th>Processor Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB1</td>
<td>SW8</td>
<td>FLAG1/~IRQ1</td>
</tr>
<tr>
<td>PB2</td>
<td>SW11</td>
<td>FLAG0/~IRQ0</td>
</tr>
<tr>
<td>PB3</td>
<td>SW10</td>
<td>DAI19</td>
</tr>
<tr>
<td>PB4</td>
<td>SW9</td>
<td>DAI20</td>
</tr>
</tbody>
</table>

Table 1-3 summarizes the LED connections to the processor. To use the LEDs connected to the DAI or DPI pins, configure the respective registers of the processor. For more information, refer to the ADSP-21368 SHARC Processor Hardware Reference (includes ADSP-21369).
An example program is included in the EZ-KIT Lite installation directory to demonstrate functionality of the LEDs and push buttons.

### Example Programs

Example programs are provided with the ADSP-21369 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are installed with the VisualDSP++ software and can be found in the `<install_path>\213xx\Examples\ADSP-21369 EZ-KIT Lite` directory. Refer to a readme file provided with each example for more information.

### Background Telemetry Channel

The ADSP-21369 USB debug agent supports the background telemetry channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting processor execution.

#### Table 1-3. LED Connections

<table>
<thead>
<tr>
<th>LED Reference Designator</th>
<th>Processor Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED1</td>
<td>DPI6</td>
</tr>
<tr>
<td>LED2</td>
<td>DPI7</td>
</tr>
<tr>
<td>LED3</td>
<td>DPI8</td>
</tr>
<tr>
<td>LED4</td>
<td>DPI13</td>
</tr>
<tr>
<td>LED5</td>
<td>DPI14</td>
</tr>
<tr>
<td>LED6</td>
<td>DAI15</td>
</tr>
<tr>
<td>LED7</td>
<td>DAI16</td>
</tr>
<tr>
<td>LED8</td>
<td>FLAG3/~MS3/~IRQ3</td>
</tr>
</tbody>
</table>
Reference Design Information

The BTC allows the user to view a variable as it is updated or changed, all while the processor continues to execute. For increased performance of the BTC, including faster reading and writing, please check our latest line of SHARC processor emulators at http://www.analog.com/proces-sors/sharc/evaluationDevelopment/crosscore/index.html. For more information about the background telemetry channel, see the VisualDSP++ User’s Guide or online Help.

Reference Design Information

A reference design info package is available for download on the Analog Devices Web site. The package provides information on the design, layout, fabrication, and assembly of the EZ-KIT Lite and EZ-Board products.

The information can be found at:
This chapter describes the hardware design of the ADSP-21369 EZ-KIT Lite board.

The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-21369 board configuration and explains how the board components interface with the processor.

- "Switches" on page 2-9
  Shows the locations and describes the on-board switches.

- "LEDs and Push Buttons" on page 2-15
  Shows the locations and describes the on-board LEDs and push buttons.

- "Jumpers" on page 2-18
  Shows the locations and describes the on-board configuration jumpers.

- "Connectors" on page 2-21
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.
This section describes the processor’s configuration on the EZ-KIT Lite board (Figure 2-1).

Figure 2-1. System Architecture Block Diagram

The EZ-KIT Lite is designed to demonstrate the ADSP-21369 processor capabilities. The processor core is powered at 1.3V, and the I/O is powered at 3.3V.
The **CLKIN** pin of the processor connects to a 24.576 MHz oscillator. The core frequency of the processor is derived by multiplying the frequency at the **CLKIN** pin by a value determined by the state of the processor pins **CLKCFG1** and **CLKCFG0**. The value at these pins is determined by the state of switch **SW2** state (see “Boot Mode and Clock Ratio Select Switch (SW2)” on page 2-10). By default, the EZ-KIT Lite provides a core frequency of 393.216 MHz. It is possible to change the speed of the processor by changing the value of the **PMCTL** register.

The **SW2** switch also configures the boot mode of the processor. The EZ-KIT Lite is capable of EPROM/flash boot and SPI boot. By default, the EZ-KIT Lite boots from flash memory. For details, see “Boot Mode and Clock Ratio Select Switch (SW2)” on page 2-10.

## External Port

The external port of the ADSP-21369 processor consists of a 24-bit address bus, 32-bit data memory bus, and control lines. The control lines are used to select, read, and write to external memory devices.

The external port connects to an 8-bit parallel flash memory, an 8-bit SRAM memory, and a 32-bit SDRAM memory. See “External Memory” on page 1-7 for more information about accessing flash memory and SDRAM memory.

All of the external port signals are available externally via the expansion interface connectors (**J1—3**). The pinout of the connectors can be found in “ADSP-21369 EZ-KIT Lite Schematic” on page B-1.
System Architecture

DAI Interface

The digital application interface (DAI) pins are connected to the signal routing unit (SRU) of the processor. The SRU is a flexible routing system, providing a large system of signal flows within the processor. In general, the SRU allows to route the DAI pins to different internal peripherals in various combinations.

The DAI pins are connected to the AD1835A audio codec, a 26-pin header, two RCA connectors, audio oscillator output, an external phase lock loop (PLL) circuit, two LEDs, and two push buttons. Figure 2-2 illustrates the EZ-KIT Lite’s connections to the DAI.

![Figure 2-2. DAI Connections Block Diagram](image-url)
To use the DAI for a different purpose, disable any signal driving the DAI pin with a switch (see “Codec Setup Switch (SW3)” on page 2-11). In addition, SW3 enables flexible routing of the 12.288 MHz audio oscillator’s output signal. By default, the SW3 signal is used as the master clock (MCLK) for the AD1835A codec.

All of the DAI signals are available externally via the expansion interface connectors (J1–3) and 0.1” spaced header (P4). The pinout of the connectors can be found in “ADSP-21369 EZ-KIT Lite Schematic” on page B-1.

**DPI Interface**

The digital peripheral interface (DPI) pins are connected to a second signal routing unit of the processor (SRU2). The SRU2 unit, similar to the SRU, is a flexible routing system, providing a large system of signal flows within the processor. In general, the SRU2 can route the DPI pins to different internal peripherals in various combinations.

![DPI Connections Block Diagram](image-url)
The DPI pins are connected to the SPI flash memory, SPI of the AD1835A codec, a UART, a 20-pin header, and five LEDs. Figure 2-3 illustrates the EZ-KIT Lite’s connections to the DPI.

To use the DPI for a different purpose, disable any signal driving a DPI pin with a switch (see “UART Enable Switch (SW5)” on page 2-12). Any DPI pin connected to a LED can be used without having to disconnect the pin. You can, however, see the respective LED turn **ON** and **OFF** when the signal is used elsewhere on the board.

All of the DPI signals are available externally via the expansion interface connectors (J1–3) and 0.1” spaced header (P3). The pinout of the connectors can be found in “ADSP-21369 EZ-KIT Lite Schematic” on page B-1.

**FLAG Pins**

The processor has four general-purpose I/O flag pins. Table 2-1 describes the flag pin connections.

Table 2-1. I/O FLAG Pins

<table>
<thead>
<tr>
<th>Processor FLAG Pin</th>
<th>EZ-KIT Lite Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLAG0</td>
<td>Push button (SW2) input</td>
</tr>
<tr>
<td>FLAG1</td>
<td>Push button (SW2) input</td>
</tr>
<tr>
<td>FLAG2</td>
<td>SDRAM chip select</td>
</tr>
<tr>
<td>FLAG3</td>
<td>LED8</td>
</tr>
</tbody>
</table>

For information on how to disable a push button from driving its corresponding flag pin, see “Push Button Enable Switch (SW7)” on page 2-13.

The FLAG signals are available externally via the expansion interface connectors (J1–3). The pinout of the connectors can be found in “ADSP-21369 EZ-KIT Lite Schematic” on page B-1.
External PLL

The ADSP-21369 EZ-KIT Lite contains an external phase lock loop to help generate a faster and more stable master input clock, MCLK. The PLL uses DAI pin 3 as an input clock from the ADSP-21369 processor. The new clock generated by PLL connects to the processor via DAI pin 2.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to configure and use the board’s external PLL.

Expansion Interface

The expansion interface consists of three 90-pin connectors. Table 2-2 shows the interfaces each connector provides. For the exact pinout of the connectors, refer to “ADSP-21369 EZ-KIT Lite Schematic” on page B-1. The mechanical dimensions of the connectors can be obtained from Technical or Customer Support.

Table 2-2. Expansion Interface Connectors

<table>
<thead>
<tr>
<th>Connector</th>
<th>Interfaces</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>5V, ADDR23–0, DATA31–0</td>
</tr>
<tr>
<td>J2</td>
<td>3.3V, FLAG3–0, DAIP20–1, DPI14–1, SDRAM control signals</td>
</tr>
<tr>
<td>J3</td>
<td>5V, 3.3V, reset, parallel port control signals</td>
</tr>
</tbody>
</table>

Limits to the current and interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry also can add extra loading to signals, decreasing their maximum effective speed.

⚠️ Analog Devices does not support and is not responsible for the effects of additional circuitry.
System Architecture

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the internal and external memory of the processor through a 6-pin interface. The JTAG emulation port of the processor also connects to the USB debugging interface. When an emulator connects to the board at ZP4, the USB debugging interface is disabled. This is not a standard connection of the JTAG interface.

For information about the standard connection of the interface, see EE-68 published on the Analog Devices Web site. For more information about the JTAG connector, see “JTAG Header (ZP4)” on page 2-25. To learn more about available SHARC emulators, go to Analog Devices Web site: http://www.analog.com/processors/sharc/evaluationDevelopment/crosscore/index.html.
Switches

This section describes operation of the on-board switches. The switch locations and default settings are shown in Figure 2-4.

Figure 2-4. Switch Locations and Default Settings
Switches

Boot Mode and Clock Ratio Select Switch (SW2)

The SW2 switch sets the boot mode and clock multiplier ratio of the processor. Table 2-3 shows how to set up the boot mode using SW2 positions 1 and 2. By default, the EZ-KIT Lite boots in external port mode from flash memory.

Table 2-3. Boot Mode Configuration Switch (SW2)

<table>
<thead>
<tr>
<th>BOOTCFG0 Pin (Position 1)</th>
<th>BOOTCFG1 Pin (Position 2)</th>
<th>Boot Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>ON</td>
<td>SPI slave boot</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>Parallel flash boot (default)</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>SPI master boot</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Table 2-4 shows how to set up the clock multiply ratio using SW2 positions 3 and 4. By default, the processor increases the clock multiply ratio by sixteen, setting the core clock to 393.216 MHz.

Table 2-4. Core Clock Rate Configuration

<table>
<thead>
<tr>
<th>CLKCFG0 (Position 3)</th>
<th>CLKCFG1 (Position 4)</th>
<th>Core to CLKin Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>ON</td>
<td>6:1</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>16:1 (default)</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>32:1</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

The core clock frequency can be increased or decreased via software by writing to the PMCTL register. For more information on changing the core clock frequency and other setup information, refer to the ADSP-21368 SHARC Processor Hardware Reference (includes ADSP-21369).
Codec Setup Switch (SW3)

The codec setup switch (SW3) can be used to change the routing of some signals going to the AD1835A codec and to set up the communication protocol of the codec.

SW3 positions 1 and 2 determine the clock routing for the audio oscillator to the codec and to the processor. Figure 2-5 illustrates how the switch positions 1 and 2 connect on the board. In the default position, route the DAI_P17 pin to DAI_P6 (in software) to clock the AD1835A codec.

SW3 position 3 determines if the AD1835A device is a master or a slave. If the AD1835A is a master, the device’s serial interface generates the frame sync and clock signals necessary to transfer data. When the device is a slave, the processor must generate the frame sync and clock signals. By default, position 3 is ON, and the AD1835A codec generates the control signals.

SW3 position 4 disconnects the AD1835A codec’s ADC_DATA pin from the DAI. This is useful when the DAI is connected to another device.
Switches

Electret Microphone Select Switch (SW4)

To connect an electret microphone to audio input, place all positions of SW4 ON. The default switch position is all OFF. When SW4 is all ON, a DC offset of 2.5V is added to the signal, and gain of the input amplifiers is changed from 1x to 10x.

UART Enable Switch (SW5)

The UART enable switch (SW5) disconnects the UART signals from the DPI pins of the processor. When SW5 is OFF, its associated DPI signal (see Table 2-5) can be used on the expansion interface.

Table 2-5. UART Enable Switch (SW5)

<table>
<thead>
<tr>
<th>Switch Position</th>
<th>EZ-KIT Lite Signal</th>
<th>Processor Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (OFF)</td>
<td>CTS</td>
<td>DPI12</td>
</tr>
<tr>
<td>2 (ON)</td>
<td>RX</td>
<td>DPI10</td>
</tr>
<tr>
<td>3 (OFF)</td>
<td>RTS</td>
<td>DPI11</td>
</tr>
<tr>
<td>4 (ON)</td>
<td>T2IN tied to R2OUT</td>
<td>N/A</td>
</tr>
</tbody>
</table>

1 Bold typeface denotes the default setting.

Loopback Test Switches (SW6 and SW14)

The loopback test switch (SW6) is located at the top left side of the board. The second loopback test switch, SW14, is located at the top right side of the board. These switches are used for testing only; all switch positions should remain OFF.
Push Button Enable Switch (SW7)

The push button enable switch (SW7) disconnects the push buttons from the respective processor pins. This allows the signals to be used elsewhere on the board. Table 2-6 shows switch SW7 connections. By default, all positions of SW7 are ON, and the push buttons function as designed.

Table 2-6. Push Button Enable Switch (SW7)

<table>
<thead>
<tr>
<th>Switch Position</th>
<th>Push Button Label</th>
<th>Push Button Reference Designator</th>
<th>Processor Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PB1</td>
<td>SW8</td>
<td>FLAG1/~IRQ</td>
</tr>
<tr>
<td>2</td>
<td>PB2</td>
<td>SW11</td>
<td>FLAG0/~IRQ0</td>
</tr>
<tr>
<td>3</td>
<td>PB3</td>
<td>SW10</td>
<td>DAI19</td>
</tr>
<tr>
<td>4</td>
<td>PB4</td>
<td>SW9</td>
<td>DAI120</td>
</tr>
</tbody>
</table>

SPI Disable Switch (SW15)

The SPI interface switch (SW15) disables the SPI chip select lines connected to SPI flash memory and AD1835A audio codec. The switch allows you to re-use the same pins on the SPI interface and expansion interface. By default, SW15 positions 1–3 are ON and position 4 is OFF unless any of the SPI interface signals are used on the expansion connector or via an EZ-Extender®.

ELVIS Oscilloscope Configuration Switch (SW1)

The oscilloscope configuration switch (SW1) determines which audio circuit signals connect to channels A and B of the oscilloscope. The switch is used only when the board is connected to the Educational Laboratory Virtual Instrumentation Suite (ELVIS) station (see “ELVIS Interface” on page 1-9). Each channel must have only one signal selected at a time, as described in Table 2-7.
Switches

Table 2-7. Oscilloscope Configuration Switch (SW1)

<table>
<thead>
<tr>
<th>Channel</th>
<th>Switch Position</th>
<th>Audio Circuit Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1 (OFF)</td>
<td>AMP_LEFT_IN</td>
</tr>
<tr>
<td>A</td>
<td>2 (OFF)</td>
<td>AMP_RIGHT_IN</td>
</tr>
<tr>
<td>A</td>
<td>3 (OFF)</td>
<td>LEFT_OUT</td>
</tr>
<tr>
<td>A</td>
<td>4 (OFF)</td>
<td>RIGHT_OUT</td>
</tr>
<tr>
<td>B</td>
<td>5 (OFF)</td>
<td>AMP_LEFT_IN</td>
</tr>
<tr>
<td>B</td>
<td>6 (OFF)</td>
<td>AMP_RIGHT_IN</td>
</tr>
<tr>
<td>B</td>
<td>7 (OFF)</td>
<td>LEFT_OUT</td>
</tr>
<tr>
<td>B</td>
<td>8 (OFF)</td>
<td>RIGHT_OUT</td>
</tr>
</tbody>
</table>

1  Bold typeface denotes the default settings.

ELVIS Function Generator Configuration Switch (SW13)

The function generator configuration switch (SW13) controls which signals connect to the left and right input signals of the audio interface. The SW13 switch is used only when the board is connected to the ELVIS station (see “ELVIS Interface” on page 1-9). Each channel must have only one signal selected at a time, as described in Table 2-8.

Table 2-8. ELVIS Function Generator Configuration Switch (SW13)

<table>
<thead>
<tr>
<th>Channel</th>
<th>Switch Position</th>
<th>Audio Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMP_LEFT_IN</td>
<td>1 (ON)</td>
<td>LEFT_IN</td>
</tr>
<tr>
<td>AMP_RIGHT_IN</td>
<td>2 (ON)</td>
<td>RIGHT_IN</td>
</tr>
<tr>
<td>AMP_LEFT_IN</td>
<td>3 (OFF)</td>
<td>DAC0</td>
</tr>
<tr>
<td>AMP_RIGHT_IN</td>
<td>4 (OFF)</td>
<td>DAC1</td>
</tr>
</tbody>
</table>
LEDs and Push Buttons

This section describes the on-board LEDs and push buttons. The LED and push button locations are shown in Figure 2-6.

Table 2-8. ELVIS Function Generator Configuration Switch (SW13)

<table>
<thead>
<tr>
<th>Channel</th>
<th>Switch Position</th>
<th>Audio Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMP_LEFT_IN</td>
<td>5 (OFF)</td>
<td>FUNCTION_OUT</td>
</tr>
<tr>
<td>AMP_RIGHT_IN</td>
<td>6 (OFF)</td>
<td>FUNCTION_OUT</td>
</tr>
</tbody>
</table>

1 Bold typeface denotes the default settings.

Figure 2-6. LED and Push Button Locations
LEDs and Push Buttons

**General Purpose LEDs (LED1-8)**

There are eight general-purpose LEDs on the board. Five LEDs are connected to the DPI interface, two LEDs are connected to the DAI interface, and one LED is connected to FLAG3 of the processor. “LEDs and Push Buttons” on page 1-12 summarizes the LED connections. To use an LED connected to the DAI or DPI, program its respective register on the processor. For more information on how to program the registers, refer to the ADSP-21368 SHARC Processor Hardware Reference (includes ADSP-21369).

**Power LED (LED9)**

When LED9 is lit (green), it indicates that power is being supplied to the board properly.

**Reset LEDs (LED10)**

When LED10 is lit (red), a master reset of all the major ICs is active.

**USB Monitor LED (ZLED3)**

The USB monitor LED (ZLED3) indicates that USB communication has been initialized successfully, and you can connect to the processor using a VisualDSP++ EZ-KIT Lite session. Once the USB cable is plugged into the board, it takes approximately 15 seconds for the USB monitor LED to light. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver (see the VisualDSP++ Installation Quick Reference Card).

When VisualDSP++ is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.
Push Buttons (SW8–11)

Four push buttons (SW8–11) are provided for general-purpose user input. Two push buttons are connected to the FLAG pins of the processor, while the other two are connected to the DAI of the processor. The push buttons are active high and, when pressed, send a high (1) to the processor. Refer to “LEDs and Push Buttons” on page 1-12 for more information. The push button enable switch (SW7) is capable of disconnecting the push buttons from the corresponding processor pins. Refer to “Push Button Enable Switch (SW7)” on page 2-13 for more information.

The push buttons and corresponding processor signals are summarized in Table 2-9.

Table 2-9. Push Button Connections

<table>
<thead>
<tr>
<th>Push Button Label</th>
<th>Push Button Reference Designator</th>
<th>Processor Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB1</td>
<td>SW8</td>
<td>FLAG1/~IRQ1</td>
</tr>
<tr>
<td>PB2</td>
<td>SW11</td>
<td>FLAG0/~IRQ0</td>
</tr>
<tr>
<td>PB3</td>
<td>SW10</td>
<td>DAI19</td>
</tr>
<tr>
<td>PB4</td>
<td>SW9</td>
<td>DAI20</td>
</tr>
</tbody>
</table>

Board Reset Push Button (SW12)

The RESET push button (SW12) resets all of the ICs on the board. The only exception is the USB interface chip (U4). The chip is not reset when the push button is pressed after the USB cable has been plugged in and communication initialized correctly with the PC. After USB communication has been initialized, the only way to reset the USB is by powering down the board.
Jumpers

This section describes functionality of the configuration jumpers. The jumper locations are shown in Figure 2-7.

Figure 2-7. Jumper Locations
VCO Select Jumper (JP1)

The voltage-controlled oscillator (VCO) select jumper (JP1) configures the frequency selection of the on-board external PLL (U39). When JP1 is installed, the VCO output frequency is multiplied by a factor of 1.0. Conversely, when uninstalled, the VCO output frequency is multiplied by a factor of 0.5 or divided in half. The jumper settings are shown in Table 2-10.

Table 2-10. VCO Select Jumper (JP1)

<table>
<thead>
<tr>
<th>JP1 Setting</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>VCO output frequency x ½ (default)</td>
</tr>
<tr>
<td>ON</td>
<td>VCO output frequency x 1.0</td>
</tr>
</tbody>
</table>

ELVIS Select Jumper (JP2)

The ELVIS select jumper (JP2) configures the EZ-KIT Lite’s connection to an ELVIS station (see “ELVIS Interface” on page 1-9). When JP2 is installed, the connections to the push buttons and LED are re-directed to the ELVIS station instead of the processor. The jumper settings are shown in Table 2-11.

Table 2-11. ELVIS Select Jumper (JP2)

<table>
<thead>
<tr>
<th>JP2 Setting</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>Not connected to an ELVIS station (default)</td>
</tr>
<tr>
<td>ON</td>
<td>Connected to an ELVIS station</td>
</tr>
</tbody>
</table>
Jumpers

**ELVIS Voltage Selection Jumper (JP3)**

The ELVIS voltage selection jumper (JP3) is used to select the power source for the EZ-KIT Lite. In a standard mode of operation, the board receives its power from an external power supply. When JP3 is installed, the board is powered from an ELVIS station, and no external power supply is required. The jumper settings are shown in Table 2-12.

Table 2-12. ELVIS Voltage Selection Jumper (JP3)

<table>
<thead>
<tr>
<th>JP3 Setting</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>Powered from an external power supply (default)</td>
</tr>
<tr>
<td>ON</td>
<td>Powered from an ELVIS station</td>
</tr>
</tbody>
</table>

⚠️ The external power supply must be disconnected from the board when JP3 is installed to avoid potential damage to the EZ-KIT Lite board and ELVIS unit.

**ELVIS Programmable Flag Jumper (JP4)**

The ELVIS programmable flag jumper (JP4) connects the ADSP-21369 processor’s DA14 pin to the ELVIS trigger pin. When JP4 is installed, DA14 connects to the ELVIS TRIG1_2 pin directly. Conversely, when JP4 is uninstalled, DA1P4 is disconnected and can be used for another non-ELVIS operation. The jumper settings are shown in Table 2-13.

Table 2-13. ELVIS Select Jumper (JP4)

<table>
<thead>
<tr>
<th>JP4 Setting</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>DA14 disconnected from the ELVIS TRIG pin (default)</td>
</tr>
<tr>
<td>ON</td>
<td>DA14 connected to the ELVIS TRIG pin</td>
</tr>
</tbody>
</table>
Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-8.

Figure 2-8. Connector Locations
Connectors

Expansion Interface Connectors (J1-3)

Three board-to-board connectors (J1–3) provide signals for most peripheral interfaces of the processor. The connectors are located at the bottom of the board. For more information about the expansion interface, see “Expansion Interface” on page 2-7. For the connectors availability and pricing, contact Samtec.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>90-position 0.05” spacing, SMT</td>
<td>SAMTEC</td>
<td>SFC-145-T2-F-D-A</td>
</tr>
</tbody>
</table>

Mating Connectors

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>90-position 0.05” spacing (through hole)</td>
<td>SAMTEC</td>
<td>TFM-145-x1 series</td>
</tr>
<tr>
<td>90-position 0.05” spacing (surface mount)</td>
<td>SAMTEC</td>
<td>TFM-145-x2 series</td>
</tr>
<tr>
<td>90-position 0.05” spacing (low cost)</td>
<td>SAMTEC</td>
<td>TFC-145 series</td>
</tr>
</tbody>
</table>
Audio In RCA Connector (J10)

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two-channel right angle RCA jack</td>
<td>SWITCHCRAFT</td>
<td>PJRAS1X2S02</td>
</tr>
<tr>
<td>Mating Cable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Two-channel RCA interconnect cable</td>
<td>MONSTER CABLE</td>
<td>BI100-1M</td>
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</tbody>
</table>

Audio Out RCA Connector (J5)

<table>
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<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Four-channel right angle RCA jack</td>
<td>SWITCHCRAFT</td>
<td>PJRAS4X2U01</td>
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<tr>
<td>Mating Cable</td>
<td></td>
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</tr>
<tr>
<td>Two-channel RCA interconnect cable</td>
<td>MONSTER CABLE</td>
<td>BI100-1M</td>
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</tbody>
</table>

Headphone Out Jack (J9)

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
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<tr>
<td>3.5 mm stereo jack</td>
<td>A/D ELECTRONICS</td>
<td>ST-323-5</td>
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</table>

Power Jack (J4)

The power connector (J4) provides all of the power necessary to operate the EZ-KIT Lite board.

<table>
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<th>Part Description</th>
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<th>Part Number</th>
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<tbody>
<tr>
<td>2.5 mm power jack</td>
<td>SWITCHCRAFT</td>
<td>RAPC712X-ND</td>
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<tr>
<td></td>
<td>DIGI-KEY</td>
<td></td>
</tr>
<tr>
<td>Mating Power Supply (shipped with EZ-KIT Lite)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7V power supply</td>
<td>CUI INC.</td>
<td>DMS070214-P6P-SZ</td>
</tr>
</tbody>
</table>
Connectors

The power connector supplies DC power to the EZ-KIT Lite board. Table 2-14 shows the power supply specifications.

Table 2-14. Power Supply Specifications

<table>
<thead>
<tr>
<th>Terminal</th>
<th>Connection</th>
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<tr>
<td>Center pin</td>
<td>+7 <a href="mailto:VDC@2.14A">VDC@2.14A</a></td>
</tr>
<tr>
<td>Outer ring</td>
<td>GND</td>
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</tbody>
</table>

RS-232 Connector (J6)

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB9, female, right angle</td>
<td>AMP/TYCO</td>
<td>5745781-4</td>
</tr>
<tr>
<td>Mating Cable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cable DB9M to DB9F 6 feet</td>
<td>DIGI-KEY</td>
<td>45-0308-0000-ND</td>
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</tbody>
</table>

S/PDIF Coax Connectors (J7 and J8)

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<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
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</thead>
<tbody>
<tr>
<td>Coaxial</td>
<td>SWITCHCRAFT</td>
<td>PJRAN1X1U01</td>
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<tr>
<td>Mating Cable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Two-channel RCA interconnect cable</td>
<td>MONSTER CABLE</td>
<td>BI100-1M</td>
</tr>
</tbody>
</table>

DPI Header (P3)

The DPI connector (P3) provides access to all of the DPI signals in the form of a .1” spacing header. When using the header to access the DPI pins of the processor, ensure that signals, which normally drive the DPI pins, are disabled. For more information, see “DPI Interface” on page 2-5.
DAI Header (P4)

The DAI connector (P4) provides access to all of the DAI signals in the form of a .1” spacing header. When using the header to access the DAI pins of the processor, ensure that signals, which normally drive the DAI pins, are disabled. Refer to “Codec Setup Switch (SW3)” on page 2-11 for more information on how to disable signals already being driven from elsewhere on the EZ-KIT Lite.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>20-pin IDC header</td>
<td>FCI</td>
<td>68737-420HLF</td>
</tr>
</tbody>
</table>

JTAG Header (ZP4)

The JTAG header (ZP4) is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

- Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.
- When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>26-pin IDC header</td>
<td>BERG</td>
<td>4102-T08-13LF</td>
</tr>
<tr>
<td>14-pin IDC header</td>
<td>FCI</td>
<td>68737-414HLF</td>
</tr>
</tbody>
</table>
Connectors
### ADSP-21369 EZ-KIT Lite Bill of Materials

The bill of materials corresponds to “ADSP-21369 EZ-KIT Lite Schematic” on page B-1.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Qty.</th>
<th>Description</th>
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<th>Manufacturer</th>
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<td>TI</td>
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<td></td>
<td>SOIC14</td>
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<tr>
<td>2</td>
<td>1</td>
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<td>U37</td>
<td>IDT</td>
<td>IDT74FCT3244APYG</td>
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<td>APY SSOP20</td>
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<td>3</td>
<td>1</td>
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<td>U1</td>
<td>EPSON</td>
<td>SG-8002CA MP</td>
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<td>VR1</td>
<td>LINEAR TECH</td>
<td>LT1765ES8#PBF</td>
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<td>U36</td>
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<td>SN74LVC1G08</td>
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A-4 ADSP-21369 EZ-KIT Lite Evaluation System Manual
## ADSP-21369 EZ-KIT Lite Bill Of Materials

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<td>311-24.9KHRTR-ND</td>
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<td>47UF 6.3V 10% B</td>
<td>CT5</td>
<td>NIC COMPONENTS</td>
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<td>R13</td>
<td>SEI</td>
<td>CSF 1/2 0.05 1%R</td>
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<td>C100,C224</td>
<td>AVX</td>
<td>1210YD106KAT2A</td>
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<td>RED LED001</td>
<td>LED10</td>
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<td>C213-214</td>
<td>AVX</td>
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<td>R16</td>
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<td>L3</td>
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<td>Reference Designator</td>
<td>Manufacturer</td>
<td>Part Number</td>
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<td>D5</td>
<td>VISHAY</td>
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<td>D3,D6-7,D13-14</td>
<td>ON SEMI</td>
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<td>D9-11</td>
<td>VISHAY</td>
<td>GSOT05-GS08</td>
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<td>GSOT03-GS08</td>
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<td>D8</td>
<td>VISHAY</td>
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<td>0.03 1/2W 1% 1206</td>
<td>R199,R201</td>
<td>SEI</td>
<td>CSF 1/2 0.03 1%R</td>
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</table>
ADSP-21369 EZ-KIT Lite
Schematic
When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com
The requirement is specified in SDRAM device specific and the DQM signals are either tied to GND or 3.3V.
WHEN USING AN ELECTRET MICROPHONE
PLACE ALL SWITCHES IN ON POSITION

INPUTS

ADC RIGHT
ADC LEFT

HEADPHONE OUT
DAC4

ELECTRET MICROPHONE ENABLE SWITCH
(DEFAULT = ALL OFF)

VREF_MIC_R
VREF_MIC_L
AIN_LEFT
AIN_RIGHT

AUDIO_VREF_ADC

R106
R105
301.0
0603

R109
237.0
0603

R104
R103
R102
11.0K
0603

R116
750.0K
0603

R119
49.9K
0603

R118
5.76K
0603

R117
5.76K
0603

R112
5.49K
0603

R114
5.49K
0603

R115
750.0K
0603

R121
49.9K
0603

R113
5.49K
0603

R111
5.76K
0603

R108
237.0
0603

R107
0
0402

R101
2.05K
0402

R100
2.05K
0402

R120
49.9K
0603

R110
2.05K
0402

R122
237.0
0603

R123
0
0603

C148
680PF
0603

C149
680PF
0603

C147
0603

C160
680PF
0603

C161
0603

C155
100PF
0603

C157
1000PF
0603

C156
0603

C164
1000PF
0603

C165
1000PF
0603

C166
0603

C167
100PF
0603

R127
0
0402

R128
301.0
0603

R129
301.0
0603

R130
600
FER3
600

R131
600
FER4
600

R132
5.76K
0603

R134
11.0K
0603

C159
120PF
0603

C150
0603

C152
0.22UF
0805

C153
0.22UF
0805

C151
10UF
0805

R153
100
0402

R154
1K
0402

R155
1K
0402

R156
1K
0402

R157
1K
0402

R158
1K
0402

R159
1K
0402

C158
680PF
0603

C159
680PF
0603

U14
SOIC8
AD8606ARZ

U13
SOIC8
AD8606ARZ

U15
SOIC8
AD8606ARZ

U19
SOIC8
AD8532ARZ

Title
ADSP-21369 EZ-KIT Lite
AUDIO IN & HEADPHONE OUT

Date
5-28-2009, 15:27

Rev
2.2

Page
1 of 4

Analog Devices
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Board No.
A0196-2005

Sheet
8
NOTE:
R143 needs to be replaced with 0.1 OHM resistor, if this circuit is to work for ELVIS power measurements.

DSP CORE CURRENT

DSP IO CURRENT

ELVIS CONNECTOR

ELVIS INTERFACE

ADSP-21369 EZ-KIT Lite
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