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Related to the previous article is the question this article will answer: how is inductor current measured? Switched-mode power supplies commonly use inductors for temporarily storing energy. In the evaluation of these power supplies, it is often useful to measure the inductor current to gain a complete picture of the voltage conversion circuit.
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Get Up and Running with LTspice

LTspice® is used to draft, probe, and analyze the performance of circuit designs. The platform includes a schematic editor and waveform trace viewer that are simple to use once you learn some basic commands. This article will get you up to speed on creating simulations with this efficient tool.

Rarely Asked Questions—Issue 172: Manipulating MCU SPI Interface to Access a Nonstandard SPI ADC

Many current precision ADCs have an SPI or another serial interface to communicate with controllers including MCUs, DSPs, or FPGAs. However, some new ADCs have a serial peripheral interface and use a nonstandard 3-wire or 4-wire SPI as a slave to achieve faster throughput. This article explains how to design a microcontroller SPI for ADC configuration and code reading.

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Bernhard became editor of Analog Dialogue in March 2017. He has been with Analog Devices for over 30 years, starting at the ADI Munich office in Germany. In his current role as the chief technical editor, he is responsible for the worldwide technical article program within Analog Devices.

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Analog Dialogue

Analog Dialogue is a technical magazine created and published by Analog Devices. It provides in-depth design related information on products, applications, technology, software, and system solutions for analog, digital, and mixed-signal processing. Published continuously for over 50 years—starting in 1967—it is produced as a monthly online edition and as a printable quarterly journal featuring article collections. For history buffs, the Analog Dialogue archive includes all issues, starting with Volume 1, Number 1, and four special anniversary editions. To access articles, the archive, the journal, design resources, and to subscribe, visit the Analog Dialogue home page, analogdialogue.com.
Isolated sigma-delta (∑-Δ)-based analog-to-digital converters (ADCs) have become the preferred method for phase current measurement in high performance motor and servo drives. The converters have deservedly earned a reputation for robust galvanic isolation and excellent measurement performance. With every new generation of ADCs, the performance is increased even further, but to fully utilize the potential of the latest ADCs, the rest of the motor drive needs to be designed accordingly.

This article is Part 1 in a series of two. Part 1 discusses demodulation of sigma-delta coded data using sinc filters in a motor control application. It then takes a close look at different approaches for sinc filter and control algorithm synchronization. Part 2 of the series proposes a new sinc filter structure that improves measurement performance in motor control applications. This is followed by a discussion on implementation of sinc filters with HDL code for optimum performance, and, finally, measurement results from an FPGA-based 3-phase servo drive are presented.

Introduction

Motor drive manufacturers continue to improve the performance and robustness of their products. Some of the improvements have been realized through more advanced control algorithms and higher computational power. Other improvements have been accomplished by minimizing nonideal effects in the feedback circuits such as latency, skewing, and temperature drift.1

When it comes to feedback for the motor control algorithm, the most critical part is phase current measurement. As control performance increases, the system becomes more and more sensitive to nonideal effects such as timing accuracy, offset/gain errors, and synchronization of multiple feedback channels. Over the years, semiconductor companies have focused on reducing these nonideal effects in the feedback signal chain, and that trend is likely to continue. The ADuM7701 is one example of the latest generation of isolated sigma-delta ADCs optimized for phase current measurement. While the performance of the ADC is important, there is a high risk of introducing nonideal effects into the rest of the feedback path as well. This article goes beyond the ADC and primarily discusses the remaining part of the feedback path. While the main focus is on motor control applications, this article applies to any system that requires tight synchronization of sigma-delta ADCs.

The typical signal chain, when using a sigma-delta ADC, is shown in Figure 1. An analog input voltage is created by letting the phase current pass through a resistive shunt. The sigma-delta ADC converts the analog signal into a 1-bit data stream and provides galvanic isolation so everything that follows the ADC is isolated from the motor phase potential. Following the converter is demodulation in the form of a filter. The filter converts the 1-bit signal into a multibit (M-bit) signal and brings the data update rate down through the process of decimation. While the decimation in the filter lowers the data rate, it is typically still too high to match the update rate of the control algorithm. To solve this problem, a final downsampling stage is added.

Throughout this article, it is assumed that the filter and decimation stages are implemented in an FPGA and that the filter is a third-order sinc filter (sinc3).
Sigma-delta ADCs and sinc filters are criticized for being difficult to control in the time domain and for their lack of a defined sampling instant. When compared to a conventional ADC with a dedicated sample-and-hold circuit, there is some reason for concern. However, there are ways to work around this. As will be shown in this section, it is crucial to synchronize the sinc filter to the rest of the system and to sample the phase current at the right instant. If this is not done correctly, the resulting measurement will suffer from significant distortion.

The output from a sinc filter is not a representation of what the input to the sigma-delta ADC is at that instant. Rather, the output is a weighted average of what the input was during a windowed period in the past. This behavior is due to the filter’s impulse response. Figure 2a shows the impulse response of a sinc3 with a decimation rate of 5. The figure shows how the filter output is a weighted sum of the input sequence that gives more weight to samples at the center and less weight to samples at the beginning/end.

Before proceeding, a few basic definitions are needed. The sigma-delta ADC clock, also called the modulator clock, is referred to as \( f_{\text{mod}} \). The decimation rate (DR) determines the decimation frequency \( f_{\text{dec}} \) and is linked to \( f_{\text{mod}} \), as shown in Equation 1:

\[
DR = \frac{f_{\text{mod}}}{f_{\text{dec}}} \quad (1)
\]

The right side of Figure 2 shows the effect the impulse response has on the filter’s step response. As the step is applied, the filter output is unaffected, and it takes 3 full decimation cycles before the filter reaches steady state. Based on this, some important properties of a sinc3 filter can be stated:

- The group delay is 1.5 decimation cycles long
- The settling time is 3 decimation cycles long

These properties are important when it comes to synchronizing the filter to the control system and they will be utilized throughout the article.

Before discussing sinc filter synchronization, the characteristics of the input signal must be defined. This in turn will define to what the filter must be synchronized.

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Before discussing sinc filter synchronization, the characteristics of the input signal must be defined. This in turn will define to what the filter must be synchronized.
Figure 4. Measuring phase current at the beginning and center points of a PWM period attenuates the current ripple.

Figure 5 shows the result of what happens when this kind of sampling is applied to the waveform appearing in Figure 3. The right side shows a close-up of the actual phase current and the sampled current. Note how the sample-and-hold process completely removes the ripple.

A per-unit representation of the sampled current is used where 0 A is mapped to 0.5 and the full scale is 8 A. This scaling is chosen for easier comparison to the sigma-delta measurements that follow. The result shown in Figure 5 is the ideal scenario, with only the fundamental component left after sampling. As such, these data can be considered the benchmark to which the sigma-delta measurements will be compared.

Sigma-Delta Measurement and Aliasing

With the ideal sample-and-hold ADC, it is possible to extract the fundamental component because of tight control of the sampling instant. However, sigma-delta conversion is a continuous sampling process and the ripple component will inevitably be part of the measurement.

With sigma-delta conversion, there is a close link between the decimation rate and signal-to-noise ratio (SNR). The higher the decimation rate, the more effective number of bits (ENOB) of the output. The downside is, as the decimation rate increases, the group delay also increases so the designer must compromise between signal resolution and delay in the feedback chain. As a general rule, the delay must be kept small compared to the control cycle period. For motor control, typical decimation rates fall in the range of 128 to 256, which provides a good compromise between SNR and group delay.

For data sheet specifications, a decimation rate of 256 is commonly used. For example, ADuM7701 has an ENOB of 14 bits, at a decimation rate of 256. With such a high ENOB number, a very clean measurement is to be expected. To verify this, suppose the phase current shown in Figure 3 is measured with a sigma-delta ADC clocked at 20 MHz and that the data stream is demodulated by a sinc3 using a decimation rate of 256. The result is shown in Figure 6a.
The fundamental component of the phase current is obvious, but the measured signal is very noisy when compared to the ideal sampling shown in Figure 5a. So while the ADC and sinc filter by themselves provide impressive ENOB numbers, the quality of the feedback signal is quite poor. The reason for this can be seen in Figure 6b, which shows a close-up of the sinc filter output and the actual phase current. Notice how the 10 kHz switching component of the phase current is phase shifted but hardly attenuated by the sinc filter. Now, suppose the motor control algorithm is executed once per PWM period and that the latest sinc filter output is read at the beginning of the period. Effectively, the sinc filter output is downsampled to match the update rate of the control algorithm. The downsampling and resulting signal is shown as the sampled sinc output in Figure 6b. Figure 7a shows the result of a full fundamental period that is filtered and sampled at the PWM rate. It is clear the phase current measurement is highly distorted and would lead to poor control performance. Increased torque ripple and a need to reduce the bandwidth of the current control loop should be expected. If the measurement in Figure 7a is subtracted from the ideal measurement (Figure 5a), the error is obtained (see Figure 7b). The error is approximately 7% of the full-scale signal, which is very far from matching the expected 14 ENOB.

This sigma-delta measurement and aliasing scenario demonstrates a very common operating mode of sigma-delta-based current measurement and how it has led designers to conclude that sigma-delta ADCs are unsuited for motor drives. However, the example does not demonstrate the poor performance of the ADC itself. Rather, it demonstrates poor performance of the remaining signal chain because it is not properly set up for phase current measurement.

The ADC samples the input signal at several megahertz (typically 10 MHz to 20 MHz), and, with a decimation rate of 256, the sinc filter effectively removes the modulation noise. With such a high sampling rate, the ripple component of the phase current is present in the filter output, and that can become a problem in the downsampling stage of the signal chain (see Figure 1). If the ripple component is not sufficiently attenuated, and the motor control algorithm consumes current feedback at the PWM rate, the result is aliasing due to downsampling.

To avoid aliasing, the signal must be free of energy above half the sampling frequency, as per standard sampling theory. If the sigma-delta ADC output is downsampled to 10 kHz, any noise at 5 kHz or higher would fold into the measurement. As shown, there was plenty of 10 kHz switching noise left in the signal after the sinc filter. One option to attenuate the 10 kHz noise is to increase the decimation rate, but doing so would result in an unacceptably long group delay. A different approach is needed.

Improving Measurement Through Synchronization

The main problem with the antialiasing approach discussed in the previous section is illustrated in Figure 8. The output from the sinc filter is read at some instant uncorrelated to the switching component of the phase current. When the output is read, the filter delivers a weighted average of the input signal according to the impulse response. Sometimes this weighted average spans the low point of the switching waveform and sometimes it spans the highpoint. As a result, the signal used as feedback contains significant noise with frequencies from 0 Hz to half the PWM frequency.

A sigma-delta ADC samples continuously and the sinc filter outputs multiple measurements per PWM cycle (typically 10 to 20). Since each measurement spans 3 decimation cycles, the impulse responses overlap. For simplification, only three of these measurement/impulse responses are shown in Figure 8.
The source of the problem is that the impulse response is not locked to the switching component of current, which in turn is locked to PWM. The solution is to select the decimation rate so that there is a fixed integer number of decimation cycles per PWM period. For example, with a PWM frequency of 10 kHz, a modulator clock of 20 MHz, and a decimation rate of 200, there are exactly 10 decimation cycles per PWM period. With a fixed number of decimation cycles per PWM period, the impulse response is locked to PWM at all times and the measurement used for feedback is captured at the same point within the PWM cycle. The measurement of the phase current in this synchronization scheme is shown in Figure 9a.

It is clear that synchronizing the impulse response to PWM has had a positive effect. The noise has been eliminated and, at first glance, the result seems similar to the ideal measurement in Figure 5a. However, when the sigma-delta measurement is subtracted from the ideal measurement, the result is the error signal in Figure 9b. The error magnitude is similar to the one shown in Figure 7b, but the frequency spectrum has changed. Now the error is a first-order harmonic that is equivalent to a gain error. The reason for this error pattern is illustrated in Figure 10.

To get rid of the first-order harmonic measurement error, the impulse response must always be centered around the beginning or around the center of a PWM period where the phase current is exactly at its average value. Figure 11 shows the impulse response centered at the beginning of a switching period. Around this point the switching waveform is symmetrical, so by having an equal number of measurement points on either side, the ripple component averages out to zero around this point.

With the impulse response locked and centered around the instant of average current, the resulting measurement is shown in Figure 12a and the measurement error is shown in Figure 12b. As the ideally sampled measurement, the signal is free of both white noise and gain error.

The presented results show that the quality of a sigma-delta measurement relies on much more than just the decimation rate. The common belief that increasing the decimation rate will result in higher ENOB is only true in the absence of aliasing. Controlling the filter update rate and phase with respect to the input signal is much more important than the decimation rate. As an example, compare Figure 7, which was based on a decimation rate of 256, and Figure 12, which was based on a decimation rate of 200. Lowering the decimation rate improved the measurement significantly.
Summary of Part 1
In summary, the conditions for an optimized sigma-delta-based phase current measurement are:

- The impulse response of a third-order sinc filter is 3 decimation cycles long, meaning it takes 3 decimation cycles for data to propagate through the filter.
- The impulse response of the filter must be centered around the instant of average current.
- 1.5 decimation cycles of the impulse response must be located before the instant of average current and 1.5 decimation cycles of the impulse response must be located after the instant of average current.
- The sinc filter generates multiple outputs during a PWM period, but only one of these outputs is used. The rest are ignored.

This concludes Part 1 of this article series. Part 2 will move on to propose a new sinc filter structure that is particularly suited for motor control applications and discuss how to best implement sinc filters on an FPGA. To verify the ideas discussed in the article series, Part 2 also presents several measurements performed on an FPGA-based, 3-phase servo drive.

References

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A Direct Method of Measuring Op Amp Input Differential Capacitance

Glen Brisebois, Product Applications Engineer
and Arthur Alfred Roxas, Product Applications Engineer

Introduction
Input capacitance can be a key specification for high impedance and high frequency operational amplifier (op amp) applications. Notably, when photodiode junction capacitance is small, the op amp input capacitance can dominate noise and bandwidth issues. The op amp input capacitance and the feedback resistor create a pole in the amplifier’s response, impacting stability and increasing the noise gain at higher frequencies. As a result, stability and phase margin could degrade and output noise could increase. In fact, some previous CDM (capacitance—difference mode) measurement techniques were based on high impedance inverting circuits and stability analysis, as well as noise analysis. These techniques can be quite tedious.

In a feedback amplifier such as an op amp, total effective input capacitance is comprised of CDM in parallel with the negative input common-mode capacitance, or CCM–, to ground. One of the reasons CDM is difficult to measure is that the op amp’s main task is keeping the two inputs from separating. Compared to the difficulty of CDM measurement, measuring positive input common-mode capacitance, CCM+, to ground directly is relatively easy. By putting a large series resistance in the noninverting pin of the op amp and applying a sine wave or noise source, the –3 dB frequency response due to the op amp input capacitance is measured using a network analyzer or a spectrum analyzer. CDM and CCM+ are assumed to be identical, especially for voltage feedback amplifiers. However, measuring CDM has been more elusive through the years; various techniques used were dissatisfying due to the inherent nature of an op amp to force its inputs to be equal, bootstrapping the CDM. When the inputs are forced apart and current is measured, the output tries to counter. Traditional methods of probing CDM are indirect, relying on phase margin degradation and being complicated by other capacitances such as CCM– in parallel.

It is desired that the op amp under test be truly operational and functioning, as it normally would be under closed-loop conditions, just as customers use them. One possibility suggested was to split the inputs and let the output clip, but depending on the op amp topology, this could render internal circuitry nonoperational, so the measured capacitance may not reflect actual operational capacitance. In this approach, the inputs are not split too much to avoid nonlinearities in the input stage as well as excessive output swing or clipping. This article will present a simple and direct method of measuring CDM.

![Figure 1. Direct measurement of CDM impedance in LTspice. Plot V(r)/I(R1) to get the impedance. In this case, at 1 MHz, Z is 19.89437 kΩ (10(85.97/20)) at –89.996°, which is exactly 8 pF using C = 1/(2π × Z × Freq).](image-url)
A New Way to Measure $C_{COM}$

The authors decided to simply use a gain of 1 buffer circuit and excite the output and inverting input with a current source. The output and inverting input will move only as much as the op amp allows. At low frequencies, the output will move very little, so the current through $C_{CM}$ would be small. And at too high frequencies, the test may not be valid, nor the results useful. But at medium frequencies, where the gain-bandwidth of the op amp is falling but still not too low, the output motion could be adequate to provide enough voltage excitation and a measurable current through $C_{CM}$.

The practically unlimited noise floor of LTspice® enabled a simple test simulation, shown in Figure 1. After seeing the technique work rather exactly in LTspice, the question became “will I have adequate SNR in the real world to make a good measurement?”

The angle is almost equal to $-90^\circ$, which indicates that the impedance is capacitive. The 2 pF common-mode capacitances did not corrupt the measurement because $C_{CM}$ is not in the path and $1/(2 \times \pi \times \text{Freq} \times C_{CM}) >> 1 \Omega$.

Challenges: Finding the Right Equipment and Actual Test Setup

Looking at Figure 1, the 2 kΩ is put in series at the op amp output to transform the excitation from a voltage source to a current source. This will allow a small voltage in node “r,” which should be not too far from the voltage that will be seen in the noninverting pin of the op amp and will cause small current to flow in between the inputs for the $C_{CM}$ to be measured. Now, of course, the output voltage is small, being buffered by the device under test (DUT), and also the current in $C_{CM}$ is very small (57 nA in the simulation), so measuring it using a 1 Ω resistor would be difficult on the bench. LTspice.ac tran simulations do not have resistor noise, but a 1 Ω resistor in the real world has 130 pA/$\sqrt{\text{Hz}}$ and would render only 57 nV of signal from our anticipated 57 nA of capacitor current. Further simulations showed that replacing R1 with 50 Ω or 1 kΩ would not result in too much lost current into $C_{CM}$ at frequencies within the bandwidth of interest. For a better current measurement technique than a simple resistor, a transimpedance amplifier (TIA) could be used instead to replace R1. The TIA input would be connected to the noninverting pin of the op amp where the current is desired while fixing the voltage at virtual ground to preclude current in $C_{CM}$. It turns out that this is exactly how four-port impedance analyzers such as the Keysight/Agilent HP4192A are implemented. The HP4192A can measure impedance over frequencies from 5 Hz to 13 MHz. Some of the newer pieces of equipment in the market that use the same impedance measurement technique are the E4990A impedance analyzer with 10 Hz to 120 MHz range and precision LCR meters like Keysight E4980A with 20 Hz to 2 MHz range.

Looking at the test circuit in Figure 2 below, the noninverting pin of the op amp is in virtual ground due to the TIA inside the impedance analyzer. Because of this, $C_{CM}$ would not affect the measurement since both of its terminals will be seen to be at ground potential. The small current developed across the $C_{CM}$ of the DUT will flow through the feedback resistor $R_r$ of the TIA, which is then measured with the internal voltage meter.

Figure 3. Direct $C_{CM}$ measurement method test setup.

Figure 4 shows the exact test setup used to achieve a very minimal parasitic capacitance contribution to $C_{CM}$ from the board and wiring. Any general-purpose board can be used for slow op amps while high speed op amps demand stricter PCB board layout. The vertical grounded copper board dividers are placed to make sure to prevent the input and output from seeing additional field paths in parallel with the DUT $C_{CM}$.

Results and Discussions

First, the board is tested without the DUT to measure its board capacitance. The board shown in Figure 4 was measured at 16 fF of DUT-less capacitance. This is a relatively small capacitance that can be neglected, as $C_{CM}$ values are typically expected in hundreds to thousands of femtofarads.

Most JFET and CMOS input op amps were measurable using this new $C_{CM}$ measurement technique. As an example, to illustrate this method, an LT1792 low noise precision JFET op amp was measured. The table below lists the impedance ($Z$), phase angle ($\theta$), reactance $X_S$, and the calculated $C_{CM}$ across a range of frequencies. Impedance exhibits a purely capacitive nature when the phase angle is $-90^\circ$.
A test was also done to measure $C_{DM}$ on a different supply voltage. The dependence of $C_{DM}$ on supplies and common-mode voltage may vary across different op amps; different topologies and transistor types are expected to result in different junction parasitics to high and low supplies. Table 2 shows the results for the ±5 V supply still with the LT1792. The average measured $C_{DM}$ is 9.2 pF, which is relatively close to the result of 10 pF with ±15 V supply. Thus, it could be concluded that LT1792 $C_{DM}$ does not change significantly by changing the supply voltage. This is in stark contrast to its $C_{CM}$ which varies considerably with supply voltage.

### Table 1. LT1792 Impedance Measurement Across Frequencies at ±15 V Supply

<table>
<thead>
<tr>
<th>Frequency</th>
<th>$Z$ (kΩ)</th>
<th>$\theta$</th>
<th>$X_c$ (kΩ)</th>
<th>$C_{DM}$ = $1/(2 \times \pi \times X_c \times \text{Freq})$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 kHz</td>
<td>33</td>
<td>–89°</td>
<td>–32.9</td>
<td>9.7</td>
</tr>
<tr>
<td>600 kHz</td>
<td>27</td>
<td>–90°</td>
<td>–26.9</td>
<td>9.8</td>
</tr>
<tr>
<td>700 kHz</td>
<td>22.6</td>
<td>–90°</td>
<td>–22.6</td>
<td>10</td>
</tr>
<tr>
<td>800 kHz</td>
<td>19.65</td>
<td>–90°</td>
<td>–19.7</td>
<td>10.1</td>
</tr>
<tr>
<td>900 kHz</td>
<td>17.4</td>
<td>–90°</td>
<td>–17.4</td>
<td>10.2</td>
</tr>
<tr>
<td>1 MHz</td>
<td>15.64</td>
<td>–89.9°</td>
<td>–15.6</td>
<td>10.2</td>
</tr>
<tr>
<td>2 MHz</td>
<td>7.76</td>
<td>–89.8°</td>
<td>–7.76</td>
<td>10.25</td>
</tr>
<tr>
<td>3 MHz</td>
<td>5.1</td>
<td>–90°</td>
<td>–5.1</td>
<td>10.4</td>
</tr>
<tr>
<td>4 MHz</td>
<td>3.74</td>
<td>–90°</td>
<td>–3.74</td>
<td>10.6</td>
</tr>
<tr>
<td>5 MHz</td>
<td>2.92</td>
<td>–90°</td>
<td>–2.92</td>
<td>10.9</td>
</tr>
</tbody>
</table>

Table 1 above gives results measured in the frequency range of 500 kHz to 5 MHz. The phase in this frequency range is close to being purely capacitive with a phase of –89° to –90°. Also, the reactance $X_c$ dominates the total input impedance such that $Z = X_c$. The averaged computed $C_{DM}$ is around 10.2 pF. Maximum frequency of measurement is 5 MHz because this part bandwidth is up to 5.6 MHz only. Results at lower frequencies became incoherent, presumably because of switching artifacts in the source or the input pins.

The output of the op amp should also be checked at each step frequency to make sure that it is not being overdriven by the signal coming out from the impedance analyzer. The amplitude of this signal from HP4192A can be adjusted from 0.1 V to 1.1 V, just enough to create a wiggle in the output of the op amp and move the voltage level a little in the inverting input pin. Figure 5 shows a 28 mV peak-to-peak undistorted signal (green signal) at the output of the op amp at frequency equals 800 kHz. The yellow signal oscillating output port of the analyzer. It is arbitrarily decided not to allow distortion in the output, out of fairness, both to the DUT and to the HP4192A. The output voltage reduced by op amp action, while $X_c$ also becomes a higher impedance at low frequency.

### Table 2. LT1792 Impedance Measurement Across Frequencies at ±5 V Supply

<table>
<thead>
<tr>
<th>Frequency</th>
<th>$Z$ (kΩ)</th>
<th>$\theta$</th>
<th>$X_c$ (kΩ)</th>
<th>$C_{DM}$ = $1/(2 \times \pi \times X_c \times \text{Freq})$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 kHz</td>
<td>37</td>
<td>–90°</td>
<td>–37</td>
<td>8.6</td>
</tr>
<tr>
<td>600 kHz</td>
<td>30</td>
<td>–91°</td>
<td>–30</td>
<td>8.8</td>
</tr>
<tr>
<td>700 kHz</td>
<td>25.3</td>
<td>–91°</td>
<td>–25.2</td>
<td>9</td>
</tr>
<tr>
<td>800 kHz</td>
<td>22</td>
<td>–91°</td>
<td>–22</td>
<td>9</td>
</tr>
<tr>
<td>900 kHz</td>
<td>19.5</td>
<td>–91°</td>
<td>–19.5</td>
<td>9</td>
</tr>
<tr>
<td>1 MHz</td>
<td>17.5</td>
<td>–91°</td>
<td>–17.5</td>
<td>9.1</td>
</tr>
<tr>
<td>2 MHz</td>
<td>8.62</td>
<td>–92°</td>
<td>–8.62</td>
<td>9.2</td>
</tr>
<tr>
<td>3 MHz</td>
<td>5.6</td>
<td>–93°</td>
<td>–5.6</td>
<td>9.5</td>
</tr>
<tr>
<td>4 MHz</td>
<td>4.07</td>
<td>–94°</td>
<td>–4.07</td>
<td>9.8</td>
</tr>
<tr>
<td>5 MHz</td>
<td>3.14</td>
<td>–94°</td>
<td>–3.14</td>
<td>10.1</td>
</tr>
</tbody>
</table>

Meanwhile, bipolar input op amps are almost as straightforward compared to their FET counterparts. However, their high input bias current and current noise will be noticed, as these are in parallel with the $C_{DM}$ current. Added to that is the intrinsic differential resistance $R_{DM}$ inherent in bipolar differential pair inputs, also in parallel with $C_{DM}$. Using ADA4004, a low noise precision amplifier as a sample, Table 3 shows the impedance measurements. Obviously, the phase does not indicate a purely capacitive behavior, as it is far from –90°. Although, the 4 MHz, 5 MHz, and 10 MHz frequencies are quite close, a parallel equivalent impedance RC model would fit this case, to be able to extract the $C_{DM}$ out of the other resistances. Therefore, parallel conductance $G_c$, susceptance $B_c$, and the calculated $C_{DM}$ across a range of frequencies are shown in Table 3, wherein $C_r$ is assumed to be equal to $C_{DM}$.

### Table 3. ADA4004 Impedance Measurement Across Frequencies at ±15 V Supply

<table>
<thead>
<tr>
<th>Frequency</th>
<th>$Z$ (kΩ)</th>
<th>$\theta$</th>
<th>$G_c$ (µs)</th>
<th>$B_c$ (µs)</th>
<th>$C_{DM} = C_{DM} = 1/(2 \times \pi \times X_c \times \text{Freq})$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 kHz</td>
<td>29.4</td>
<td>–36°</td>
<td>27.5</td>
<td>20</td>
<td>6.4</td>
</tr>
<tr>
<td>600 kHz</td>
<td>27.2</td>
<td>–41°</td>
<td>27.6</td>
<td>24.1</td>
<td>6.4</td>
</tr>
<tr>
<td>700 kHz</td>
<td>25.3</td>
<td>–45.4°</td>
<td>27.6</td>
<td>28</td>
<td>6.4</td>
</tr>
<tr>
<td>800 kHz</td>
<td>23.5</td>
<td>–49°</td>
<td>27.9</td>
<td>32</td>
<td>6.4</td>
</tr>
<tr>
<td>900 kHz</td>
<td>22</td>
<td>–52°</td>
<td>28</td>
<td>35.7</td>
<td>6.3</td>
</tr>
<tr>
<td>1 MHz</td>
<td>20.7</td>
<td>–54.3°</td>
<td>28.1</td>
<td>39.3</td>
<td>6.3</td>
</tr>
<tr>
<td>2 MHz</td>
<td>12</td>
<td>–72.6°</td>
<td>24.9</td>
<td>79.4</td>
<td>6.3</td>
</tr>
<tr>
<td>3 MHz</td>
<td>7.8</td>
<td>–79.2°</td>
<td>24</td>
<td>126</td>
<td>6.7</td>
</tr>
<tr>
<td>4 MHz</td>
<td>5.8</td>
<td>–81.8°</td>
<td>24.5</td>
<td>171</td>
<td>6.8</td>
</tr>
<tr>
<td>5 MHz</td>
<td>4.7</td>
<td>–83.5°</td>
<td>24.2</td>
<td>212.7</td>
<td>6.8</td>
</tr>
<tr>
<td>10 MHz</td>
<td>2.5</td>
<td>–86°</td>
<td>28</td>
<td>319.5</td>
<td>6.3</td>
</tr>
</tbody>
</table>

Based on the results in Table 3, ADA4004 $C_{DM}$ can be estimated to be around 6.4 pF. The results also imply that across the frequency range presented in Table 3, $C_{DM}$ has some substantial parallel conductance $G_c$ and is not a purely capacitive $C_{DM}$. The measurement is revealing the approximate 40 kΩ (1/25 µs) of real input differential resistance in this bipolar op amp.

Additional note: attempts were made at measuring other types of op amps such as zero-drift op amps (LT2080) and high speed bipolar op amps (LT6200). Results were incoherent, presumably because of switching artifacts in the zero-drift op amp and excessive current noise in the high speed bipolar op amp.
Conclusion

$C_{\text{in}}$ is not a difficult measurement. One caveat is that the HP4192A reports an impedance in magnitude and angle. The capacitance reading assumes a simple series of RCs or parallel RCs, whereas op amp input impedance can be much more complicated. The capacitance reading should not necessarily just be taken at face value. Each op amp is also a unique case of its own. The frequency range wherein a capacitive reactance dominates the input impedance may vary from design to design. The input stage design, devices and processes used, Miller effects, and packaging could all contribute to the totality of the differential input impedance and its measurement. A JFET input op amp and a bipolar input op amp were measured, revealing both $C_{\text{in}}$ and in the case of the bipolar input op amp, $R_{\text{in}}$ results.

References


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High Power Density in a Small Form Factor

Steve Knoth, Senior Product Marketing Manager

Background
Sophisticated high power density digital integrated circuits (ICs), such as graphics processor units (GPUs) and field programmable gate arrays (FPGAs), can be found in a broad range of feature-rich electronic environments, including:

- Automotive
- Medical
- Telecom
- Datacom
- Industrial
- Communications
- Gaming
- Consumer audio/video

With this level of market penetration, it is no surprise that the global demand for high current, low voltage digital ICs is exploding. The current global market is assessed at more than US $1.8B, and this is expected to rise annually by 10.87% to reach US $3.7B over the 2018 to 2025 period. As one of the biggest slices of this market, FPGAs account for a projected US $1.53B by the end of 2025. The rest of the digital IC market is represented by GPUs, microcontrollers and microprocessors, programmable logic devices (PLDs), digital signal processors (DSPs), and application-specific integrated circuits (ASICs).

High power density digital ICs have penetrated virtually every embedded system. FPGAs enable cutting-edge applications in the market segments previously listed. For example, in automotive applications, advanced driver assistance systems (ADAS) and collision avoidance systems prevent catastrophe due to human error. Likewise, government-mandated safety features such as antilock brake systems, stability control, and electronically controlled independent suspension systems require FPGAs to function.

In consumer electronics, the demand for Internet of Things (IoT) functionality, sophisticated graphic engine functionality, and machine-to-machine (M2M) functionality call for advanced digital ICs. Massive data storage and cloud computing centers and expansive networks of optical networking modules drive the need for FPGAs and digital ICs.

These digital ICs are powerful, yet temperamental, especially regarding power requirements. Traditionally, efficient switching regulator controllers that drive high power MOSFETs have been used to power FPGAs and ASICs, but these controller-based power schemes have potential noise interference issues, relatively slow transient response, and layout limitations. In recent years, small and quiet low dropout (LDO) regulators that minimize heat have been used as an alternative, but not without their own set of limitations. Recent power conversion innovations have introduced high power monolithic switching regulators that are able to efficiently power digital ICs with low noise and high efficiency while minimizing space requirements.

Switching Regulators vs. Charge Pumps vs. LDO Regulators

Low voltage, high current step-down conversion and regulation can be achieved via a variety of methods, each with its own performance and design trade-offs. Switching regulator controllers feature high efficiency at high load currents over a wide range of voltages, but they require several external components such as inductors, capacitors, and FETs to operate; and they can be a source of high and low frequency noise. Inductorless charge pumps (or switched capacitor voltage converters) can also be used to produce low voltages, but are limited in output current capability, suffer from poor transient performance, and require several external components. For these reasons, charge pumps are not commonly found in digital IC power applications. Linear regulators—especially LDO regulators—are simple in that they only require two external capacitors to operate. However, they may be power limited depending on the size of the input-to-output voltage differential across the IC and how much current is demanded by the load, plus the thermal resistance characteristics of the package. This certainly limits their ability to power digital ICs.

Monolithic Buck Converter Design Challenges

Moore’s law has proven to be visionary and valid since its debut in 1965. Wafer fabrication technology line widths are continually being reduced, pushing digital IC voltages lower. Smaller geometry processes allow higher integration of more power-hungry features in the end product. For example, modern computer servers and optical communication routing systems demand higher bandwidth to process more computing data and internet traffic; these systems also generate a lot of heat, and therefore highly efficient...
ICs are required. Cars have more on-board electronics for entertainment, navigation, self-driving features, and even engine control. As a result, there is an increase in both the system’s current consumption and the associated total power required. Therefore, state-of-the-art packaging and innovative, internal power-stage design are required to drive the heat out of the power IC while delivering unprecedented power.

High power supply rejection ratio (PSRR) and low output voltage noise, or ripple, are important considerations. A device with high supply rejection can filter and reject noise at the input, resulting in a clean and stable output. Furthermore, power solutions with low output voltage noise across a wide bandwidth or low output ripple are desirable—modern digital systems have several rails where noise sensitivity is a major design consideration. As speed requirements for high end FPGAs increase, supply noise tolerance decreases in order to minimize bit errors. Noise-induced digital faults drastically reduce the effective data throughput speeds for these high speed PLDs. Input supply noise at high current is one of the more demanding specifications placed on power supplies.

Higher transceiver speeds—in FPGAs, for example—dictate high current levels due to high power consumption from fine geometry circuit switching. These ICs are fast. They may cycle load current from near-zero to several amps within tens to hundreds of nanoseconds, requiring a regulator with ultrafast transient response.

With board area reserved for the power regulators ever-decreasing, many system designers turn to monolithic switching regulators operating at fast switching frequencies to reduce the size of external components and total solution size—accepting the trade-off of some efficiency loss due to switching losses at higher frequencies. This trade-off is eliminated by a new generation of monolithic switching regulators. These new regulators feature synchronous operation with integrated high-side and low-side switches, allowing for tight control of switch gate voltages, greatly reducing dead time, and resulting in higher efficiencies even at high frequencies.

One of the biggest challenges with high current monolithic switchers is their ability to dissipate heat that results from power loss in the IC. This challenge can be met by using multiple power and ground pins, plus thermally enhanced laminate-based packages with copper (Cu) pillars where the heat can be easily transferred from the IC into the board. The large copper planes on the board connected to these power pins allow for the heat to spread more evenly.

**New Family of Silent Switcher Buck Converters**

It’s clear that buck converter solutions for high performance digital ICs must have the following attributes:

- Fast switching frequency to minimize the size of external components
- Zero dead-time design to maximize efficiency at high frequency
- Monolithic chip on-board power device for smaller solution size
- Multiphase operation enables parallel operation for high output currents and reduced ripple
- Low EMI to meet low system noise requirements
- Synchronous operation for high efficiency and minimal power loss
- Easy design simplifies design cycle, qualification, and testing
- Very low output ripple
- Fast transient response time
- Operation over a wide input/output voltage range
- High output current capability
- Excellent thermal performance
- Compact footprint

These features can be found in Analog Devices’ Power by Linear™ LTC3xx family of monolithic high, medium, and low current buck regulators. The highest current member is the LTC3310S, a 5 V, 10 A, high power density, low EMI, Silent Switcher® 2, monolithic, synchronous buck converter in a 9 mm² package (power density = 1.11 A/mm²). The device’s fixed frequency peak current-mode architecture is ideal for applications that demand fast transient response. The LTC3310S uses the Silent Switcher 2 architecture with integrated hot loop bypass capacitors to deliver a highly efficient, small footprint solution at frequencies up to 5 MHz with excellent EMI performance. Multiphase operation enables direct paralleling of up to four devices for higher current up to 40 A.

The LTC3310S’ 2.25 V to 5.5 V input range supports a wide variety of applications, including most intermediate bus voltages. Integrated low on-resistance MOSFETs deliver continuous load currents as high as 10 A with minimal thermal derating. Output voltages ranging from 0.5 V to V IN are ideal for point-of-load applications such as high current, low voltage DSP/FPGA/GPU/ASIC designs. Other key applications include optical networking, telecom/datacom, automotive systems, distributed power architectures, or any medium-to-high power density systems. Figure 1 shows the simplicity of a typical design, while Figure 2 shows how easy it is to produce a 4-phase, 40 A configuration.

![Figure 1. LTC3310S typical application.](image-url)
The LTC3310S’ low 35 ns minimum on-time enables a large step-down ratio at high frequency, and 100% duty-cycle operation delivers low dropout performance when the input and output voltages are close in value. The operating frequency can be synchronized to an external clock. The LTC3310S total reference voltage accuracy is better than ±1% over the –40°C to +125°C operating junction temperature range. Additional features include a power good signal when the output is in regulation, precision enable threshold, output overvoltage protection, thermal shutdown, die temperature monitor, programmable soft start, tracking, clock synchronization, mode selection, and output short-circuit protection.

The LTC3310S is available in a thermally enhanced 18-lead, 3 mm × 3 mm × 0.94 mm LQFN package. The E- and I-grades are specified from the –40°C to +125°C operating junction temperature range, while the J- and H-grades are specified from the –40°C to +150°C operating junction temperature range.

High Efficiency, Low EMI, and Fast Transient Response

Silent Switcher buck regulator designs offer high efficiency at high switching frequencies (>2 MHz) with ultralow electromagnetic interference (EMI) emissions, offering very compact and quiet step-down solutions. The Silent Switcher family uses special design and packaging techniques to enable >92% efficiency at 2 MHz while easily passing the CISPR 25 Class 5 peak EMI limits. The next-generation Silent Switcher 2 technology internal construction uses copper pillars in lieu of bond wires, adds internal bypass capacitors, and an integrated substrate ground plane to further improve EMI, which is not sensitive to PCB layout, simplifying designs and reducing performance risks.
The “S” in the LTC3310S part number indicates its second-generation Silent Switcher technology. The IC has integrated $V_{IN}$ ceramic capacitors to keep all fast ac current loops small, improving the EMI performance. This technology allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI performance (see Figure 3, Figure 4, and Figure 5). Furthermore, it allows for faster, cleaner, low overshoot switching edges, greatly improving efficiency at high switching frequencies. The graph in Figure 6 shows the LTC3310S’s high efficiency performance.

The LTC3310S’s fixed frequency peak current-mode architecture eases compensation and allows the IC to rapidly respond to transient steps. External compensation components allow the control loop to be optimized for the highest bandwidth and fastest transient response.

6 A, 4 A, and 3 A Silent Switcher Bucks in a 2 mm × 2 mm Package

For increased power density, first-generation Silent Switcher architecture is a good solution. Silent Switcher topology is like Silent Switcher 2 topology except the $V_{IN}$ bypass capacitors are external instead of within the plastic encapsulation flip-chip laminate style package. For full Silent Switcher, low EMI performance, external $V_{IN}$ bypass capacitors are placed symmetrically, external to the package. This split cap, symmetrical arrangement minimizes the effective hot loop area, thereby reducing EMI and allowing for a smaller package footprint size.

LTC3309A, LTC3308A, and LTC3307A are 5 V input regulators that can support 6 A, 4 A, and 3 A, respectively, for high power density, low EMI monolithic synchronous buck conversion. They all operate at up to 3 MHz in a 4 mm$^2$ footprint package (LTC3309A power density = 1.5 A/mm$^2$).
Figure 7 shows a typical LTC3309A application. The fixed frequency peak current-mode architecture is ideal for fast transient response, including fast transient response during Burst Mode® operation (see Figure 8). The LTC3309A features Silent Switcher architecture, utilizing external hot loop bypass capacitors. This design enables highly efficient, small footprint solutions at high operating frequencies with excellent EMI performance.

The family’s 2.25 V to 5.5 V input voltage range supports a wide variety of applications, including most intermediate bus voltages, and is compatible with lithium- and nickel-based battery types. Integrated low on-resistance MOSFETs deliver continuous load currents as high as 6 A. Output voltages, ranging from 0.5 V to VIN, are ideal for point-of-load applications such as high current/low voltage DSP/GPU/ASIC reference designs. Other key applications include telecom/datacom and automotive systems, distributed power architectures, and general-purpose power systems.

The LTC3309A, LTC3308A, and LTC3307A operate in forced continuous or pulse skip modes for low noise, or low ripple, low Iq Burst Mode operation for high efficiency at light loads, ideal for battery-powered systems. Low 22 ns minimum on-time enables high step-down ratios even as the power supply operates at high frequency, and 100% duty cycle operation delivers low dropout performance when input and output voltages are the same. The operating frequency can be synchronized to an external clock. The total reference voltage accuracy is better than ±1% over the −55°C to +150°C operating junction temperature range. The device safely tolerates inductor saturation in overload. Additional features include a power good signal when the output is in regulation, internal soft start, precision enable threshold, output overvoltage and short-circuit protection, thermal shutdown, and clock synchronization.

The LTC3309A, LTC3308A, and LTC3307A are all pin-compatible devices available in a thermally enhanced, compact, and low profile 12-lead, 2 mm × 2 mm × 0.74 mm LQFN package. The E- and I-grades are specified from a −40°C to +125°C operating junction temperature range. The J- and H-grades are specified from a −40°C to +150°C operating junction temperature range, and the MP-grade is specified from a −55°C to +150°C operating junction temperature range.

Table 1 compares the features of the members of the LTC33xx Silent Switcher and Silent Switcher 2 family.

### Table 1. Fault Mode and Supported Range

<table>
<thead>
<tr>
<th>Vendor</th>
<th>ADI</th>
<th>ADI</th>
<th>ADI</th>
<th>ADI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part #</td>
<td>LTC3307A</td>
<td>LTC3308A</td>
<td>LTC3309A</td>
<td>LTC3310S</td>
</tr>
<tr>
<td>Topology</td>
<td>Single synchronous monolithic, Silent Switcher</td>
<td>Single synchronous monolithic, Silent Switcher</td>
<td>Single synchronous monolithic, Silent Switcher</td>
<td>Single synchronous monolithic, Silent Switcher 2</td>
</tr>
<tr>
<td>VIN Range</td>
<td>2.25 V to 5.5 V</td>
<td>2.25 V to 5.5 V</td>
<td>2.25 V to 5.5 V</td>
<td>2.25 V to 5.5 V</td>
</tr>
<tr>
<td>VOUT Range</td>
<td>0.5 V to VIN</td>
<td>0.5 V to VIN</td>
<td>0.5 V to VIN</td>
<td>0.5 V to VIN</td>
</tr>
<tr>
<td>Output Current</td>
<td>3 A</td>
<td>4 A</td>
<td>6 A</td>
<td>10 A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>92% (3.3 VIN/1.2 VOUT/2 A)</td>
<td>92% (3.3 VIN/1.2 VOUT/2 A)</td>
<td>92% (3.3 VIN/1.2 VOUT/2 A)</td>
<td>92% (3.3 VIN/1.2 VOUT/3 A)</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>1 MHz to 3 MHz</td>
<td>1 MHz to 3 MHz</td>
<td>1 MHz to 3 MHz</td>
<td>500 kHz to 5 MHz</td>
</tr>
<tr>
<td>Control Mode</td>
<td>Constant-frequency, peak current mode</td>
<td>Constant-frequency, peak current mode</td>
<td>Constant-frequency, peak current mode</td>
<td>Constant-frequency, peak current mode</td>
</tr>
<tr>
<td>VREF Accuracy Room/Temp</td>
<td>±0.2%/±1%</td>
<td>±0.2%/±1%</td>
<td>±0.2%/±1%</td>
<td>±1%</td>
</tr>
<tr>
<td>Current Limit Accuracy</td>
<td>±15%</td>
<td>±15%</td>
<td>±15%</td>
<td>±9%</td>
</tr>
<tr>
<td>Minimum On-Time</td>
<td>22 ns</td>
<td>22 ns</td>
<td>22 ns</td>
<td>35 ns</td>
</tr>
<tr>
<td>Directly Parallelable x Phase?</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes, 4 phase</td>
</tr>
<tr>
<td>Iq Supply Burst Mode/Non-Burst</td>
<td>40 µA BM/1.3 mA</td>
<td>40 µA BM/1.3 mA</td>
<td>40 µA BM/1.3 mA</td>
<td>1.3 mA</td>
</tr>
<tr>
<td>Package Theta JA</td>
<td>51°C/W</td>
<td>51°C/W</td>
<td>51°C/W</td>
<td>40°C/W</td>
</tr>
<tr>
<td>Solution Size</td>
<td>−20 mm²</td>
<td>−20 mm²</td>
<td>−20 mm²</td>
<td>47 mm²</td>
</tr>
<tr>
<td>Package</td>
<td>2 mm × 2 mm × 0.74 mm, 12-lead LQFN</td>
<td>2 mm × 2 mm × 0.74 mm, 12-lead LQFN</td>
<td>2 mm × 2 mm × 0.74 mm, 12-lead LQFN</td>
<td>3 mm × 3 mm × 0.94 mm, 18-lead LQFN</td>
</tr>
</tbody>
</table>
Conclusion

The trend in high performance digital ICs—such as GPUs, FPGAs, and microprocessors—is rapidly raising current demands coupled with dropping operating voltages, a result of shrinking line width wafer fabrication technologies. Current and voltage demands are only part of the power supply picture. Digital IC advancements come with a host of other requirements, including fast transient response, low EMI, low noise/ripple, and efficient operation to minimize heat.

Traditionally, digital ICs has been powered by LDO regulators or inductor-based switching regulator controllers with off-board power devices. With increased power supply performance and space requirements, in many cases these traditional approaches are not up to the task. ADI’s new generation of monolithic power supplies are up to the task, including the LTC3310S, LTC3309A, LTC3308A, and LTC3307A, which support 10 A, 6 A, 4 A, and 3 A, respectively. These high power density Silent Switcher and Silent Switcher 2 buck regulators are housed in thermally efficient, compact flip-chip laminate packages, and have a variety of feature sets to satisfy the requirements of a wide range of digital IC power problems.

About the Author

Steve Knoth is a senior product marketing manager in Analog Devices’ Power Group. He is responsible for all power management integrated circuit (PMIC) products, low dropout (LDO) regulators, battery chargers, charge pumps, charge pump-based LED drivers, supercapacitor chargers, and low voltage monolithic switching regulators. Prior to rejoining Analog Devices in 2004, Steve held various marketing and product engineering positions since 1990 at Micro Power Systems, Analog Devices, and Micrel Semiconductor. He earned his bachelor’s degree in electrical engineering in 1988 and a master’s degree in physics in 1995, both from San Jose State University. Steve also received an M.B.A. in technology management from the University of Phoenix in 2000. In addition to enjoying time with his kids, Steve is an avid music lover and can be found tinkering with pinball and arcade games or muscle cars, and buying, selling, and collecting vintage toys, movie, sports, and automotive memorabilia. He can be reached at steve.knoth@analog.com.
RAQ Issue 170: Inductor Current Measurement in Switched Power Supplies

Frederik Dostal, Field Applications Engineer

Question:
How do you measure inductor current?

Answer:
Switched-mode power supplies commonly use inductors for temporarily storing energy. In the evaluation of these power supplies, it is often useful to measure the inductor current to gain a complete picture of the voltage conversion circuit. But what is the best way to measure the inductor currents?

Figure 1 shows a suggested setup for such a measurement using the example of a typical step-down converter (buck topology). A small auxiliary cable is inserted in series with the inductor. It is used to attach a current probe and display the inductor current with an oscilloscope. It is recommended that measurements be made on the side of the inductor where the voltage is stable. Most switching regulator topologies use the inductor in such a way that the voltage on one side is switched between two extreme values but remains relatively stable on the other side. With the buck converter shown in Figure 1, the voltage at the switching node—that is, the left side of inductor L—switches between the input voltage and the ground voltage at the speed of the switching edges. On the right side of the inductor is the output voltage, which is usually relatively steady. To reduce the interference due to capacitive coupling (electric field coupling), the current measurement loop should be placed on the quiet side of the inductor, as shown in Figure 1.

Figure 1. Schematic illustrating measurement of the inductor current in a switched-mode power supply.

Figure 2 shows the practical setup for this measurement. The inductor is lifted and obliquely soldered back with one of the two terminals on the board. The alternate terminal is connected to the board with the auxiliary wire. This conversion can be accomplished quite easily. Desoldering with hot air is a proven method for detaching the inductor. Many SMD rework stations offer hot air with an adjustable temperature.

Figure 2. Practical setup for inductor current measurement.
Current probes are offered by manufacturers of oscilloscopes. Unfortunately, they are usually quite expensive—thus the question continually arises as to whether the inductor current could also be measured by means of a shunt resistor. This is possible in principle. However, this measurement has the disadvantage that the switching noise generated in a switched-mode power supply can easily couple into a voltage measurement via a shunt resistor. Thus, especially at the points of interest, when the inductor current changes direction, the measurement results would not be a true representation of the behavior of the inductor current.

Figure 3 shows the measurement of the inductor current (in blue) for a switched-mode power supply sensed with a current probe compatible with the oscilloscope used. In addition to the measurement shown in blue, a purple marking was added, indicating how the current flow through the inductor would look when the inductor starts to saturate excessively toward the peak currents. This happens when an inductor is selected that does not have enough current rating for a given application. One of the main reasons for measuring inductor current in a switched-mode power supply is so that one can recognize whether the inductor was properly selected or whether inductor saturation will occur in operation or during a fault condition.

Measurement with a shunt resistor instead of a current clamp would show strongly coupled noise, especially at the peak currents, making it difficult for inductor saturation to be detected.

Sensing of the coil current is very useful in the evaluation of a power supply and can easily be accomplished with suitable equipment.

**About the Author**

Frederik Dostal studied microelectronics at the University of Erlangen in Germany. Starting work in the power management business in 2001, he has been active in various applications positions including four years in Phoenix, Arizona, working on switch-mode power supplies. He joined Analog Devices in 2009 and works as a field applications engineer for power management at Analog Devices in München. He can be reached at frederik.dostal@analog.com.
Dual AMR Motor Position Sensor for Safety Critical Applications

Enda Nicholl, Strategic Marketing Manager

Abstract

This article provides insight into the trends in automotive electrification as we move toward partial and full autonomous driving and, in particular, the changes required to make electrical power steering (EPS) and electrical braking systems meet the necessary safety standards to ensure the safe and reliable control of driverless vehicles.

Analog Devices, Inc. (ADI) is a provider of magnetoresistive (MR) position sensor products and shunt-based current sense amplifier products enabling high performance commutation and safe operation of brushless motors used in EPS and electrical braking systems.

Introduction

The increased emphasis to improve vehicle safety in recent years has resulted in the welcome advancement and introduction of active advanced driver assistance systems (ADASs) to complement the traditional passive systems reliant on airbag deployment for driver and passenger safety. These emerging systems are intended to initially aid—but longer term replace—the driver's vehicle maneuver decision making in safety critical situations. These technology advancements are also leading the way to the transition to semi- and fully autonomous driving. Replacing the driver's decision making with electronic control units (ECUs) and replacing the steering and brake maneuvering of the vehicle with actuators is shifting responsibility away from the driver to the sensors, the ECUs, and the electrical actuators. This trend is leading to the development of more reliable, intelligent, higher performance, and redundant electrical actuator solutions that need to comply with the ISO 26262 functional safety standard. This is a risk-based safety standard, where the risk of hazardous operational situations is qualitatively assessed, and safety measures are designed into the components and system to avoid or control systematic failures and to detect or control random hardware failures or mitigate their effects. These actuator systems generally use brushless dc (BLDC) motor drives, and as these systems are safety critical, the designers must design the solution hardware and software such that the system complies with the highest automotive safety integrity level (ASIL) D.

BLDC Motor Commutation and Control

Brushless dc motors, as the name suggests, have no brush contacts, and motor position sensors (MPSs) are needed to measure the relative position between the stator and rotor to ensure the correct stator coil energizing sequence. This is particularly critical at startup when there is no back EMF available and it is impossible for the microcontroller to determine the relative rotor and stator positions.

Traditionally, block commutation (see Figure 1a), which is comprised of three Hall switches, has been used to indicate the rotor position in BLDC motors. The demands to improve performance and, in particular, reduce noise, vibration, and harshness (NVH) and improve running efficiency of BLDC motor drives (including EPS systems) is resulting in a move away from block commutation to sine commutation control. The Hall switches can be replaced with an MR angle sensor positioned in front of a dipole magnet mounted onto the end of the motor shaft (see Figure 1b). It is also typical for the MPS to be mounted onto the ECU assembly and for the ECU to be integrated into the motor casing and positioned at the end of the motor shaft.

![Figure 1. (a) BLDC block commutation control and (b) BLDC sine commutation control.](image-url)
ISO 26262 was introduced in 2011 as a safety standard to address the possible hazards caused by electrical safety-related system failures and has subsequently been replaced with a 2018 edition.

A safety and risk analysis must be carried out on the system to determine the ASIL of the system. The ASIL rating is established by reviewing the system’s potential hazards during operation in terms of severity, exposure, and controllability (see Figure 2).

For example, if we do a risk and hazard analysis on an EPS system, it will be concluded that severe events such as steering blocking and self-steering land in the ASIL D category because of the severity, controllability, and exposure of these events. Similarly, for upcoming electrical braking systems, the same logic applies to the severity of uncontrollable events such as brake blocking or self-braking.

Following on with the EPS or braking system examples, the ASIL D system rating can be achieved through subsystem decomposition as shown below in Figure 3a, Figure 3b, and Figure 3c.

It is not required that each system component be developed to ASIL D standards and processes to enable ASIL D system compliance; however, the overall system must fulfill the requirements when viewed at system level and can incorporate QM, ASIL A, B, C, or D level subcomponents as part of the system.

The system decomposition should also ensure a sufficient independence and take into account the possibility of dependent or common cause failures.

### Functional Safety for Safety Critical Applications

**[Example EPS]**

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The system decomposition should also ensure a sufficient independence and take into account the possibility of dependent or common cause failures.
The motor shaft position (MSP) angle combined with phase current measurement information is used for the commutation and control of the EPS motor drive. The basic typical EPS motor control loop is as outlined in Figure 5. The torque assistance level required varies depending on the driving conditions and is determined by the wheel speed sensors and the torque sensor, which measures the torque applied to the steering wheel by the driver or by the motor actuator in driverless cars. The microcontroller then uses the MSP data in combination with the phase current data to control the current loads supplied to the motor that provide the needed assistance.

**EPS Motor Position and Phase Current Sensors**

An MPS sensor fault or failure could potentially cause or contribute to a severe system failure such as steering lock or self-steering, and for that reason the MPS is a critical component in the EPS system. It is therefore essential that the system has comprehensive diagnostic coverage of sensor faults and redundancy built in to ensure continued functionality in the event of an MPS sensor error or fault and ensure severe system failures cannot occur, or in the event an error does occur, that the system fails in a safe manner.

Current sense amplifiers are typically used for the indirect precision measurement of the motor load and normally applied to two of the three motor phases, thus enabling additional diagnostic information that can be used as part of the overall system safety case.

In addition, high precision motor position and phase current measurements allow for improvements in the EPS motor control performance that—at a system level—result in a very efficient, quiet, and smooth steering feel, improving the overall driver experience, and are therefore critical components in the system.

**Functional Safety in EPS Motor Control**

Different approaches can be taken to achieve an ASIL D compliance in an EPS or other safety critical motor control application. The following example explains a dual anisotropic magnetoresistive (AMR) motor position sensor combined with the current sense amplifiers from ADI could be integrated into such a system and provide the required level of performance and redundancy needed to achieve ISO 26262 ASIL D compliance at a system level.

In the block diagram outlined in Figure 6, the dual AMR sensor is complemented with an additional sensor based on an alternate technology (for example, Hall, GMR, or TMR). The dual AMR sensor is used as the primary (high precision) sensing channel, and the secondary alternate sensor technology channel serves three purposes:

- Enable the provision of a 2-out-of-3 (2oo3) comparison to validate if there is a fault with one of the sensor channels when combined with other system inputs.
- Provide position feedback in the unlikely event that both AMR channels fail.
- Provide the 360˚ quadrant information to the microcontroller needed for motor commutation in the event the motor has an uneven number of poles.

The precision angle measurement will continue to be provided by both channels of the dual AMR sensor. Additional system diagnostics such as motor load and shaft position can be indirectly inferred in a dynamic state (back EMF) from the precise phase current sense amplifier.

If we look at all the possible sensor failure modes in this sensor architecture example, there should always be two position sensor inputs available for a plausibility check. Even in the unlikely and extreme case of both AMR channels failing simultaneously due to a common cause failure, it is still possible to use the degraded position sense information from the auxiliary sensor channel and cross check this with the back EMF information from the current sensors in the dynamic state and ensure continued basic system functionality.

This system-level diagnostics capability would then ensure that a severe failure mode could not occur and that the system fulfills ISO 26262 ASIL D compliance. The system could then be safely powered down, or moved to limp home mode, and returned to the dealer for repair.

**Summary**

The introduction of ADASs to improve automotive safety, combined with the emergence of fully and semi-autonomous vehicles, is driving the demand for more reliable, intelligent, higher performance, and redundant electrical actuator solutions that comply with the ISO 26262 functional safety standard. Analog Devices has motor shaft position and phase current sensing products available that not only meet the improved performance demands for smooth and efficient motor control, but also provide the redundancy needed to achieve high ASIL requirements in these safety critical applications such as EPS or braking systems.

The ADA4571-2 dual AMR sensor from ADI is designed for such safety critical applications that require redundant and independent sensing channels. This is a 2-channel AMR sensor with integrated signal conditioning amplifiers and ADC drivers. The product incorporates two AMR (Sensitec AA745) sensors combined with two amplifier signal conditioning ASICs. The sensor provides very low angular error signals typically in the 0.1˚ range, with negligible hysteresis, high bandwidth, low latency, and good linearity. These attributes enable the reduction of torque ripple and audible noise for the smooth and efficient control of BLDC motors. In addition, the AMR sensor has no upper magnetic window limitation as it operates in saturation >30 mT, and operating the sensor with a high magnetic field makes the solution very robust to stray magnetic fields present in harsh environments.
The AD8410 current sense amplifier from ADI performs bidirectional current measurements across a shunt resistor in EPS and other BLDC motor control systems. This is a high voltage, high resolution, and high bandwidth current-shunt amplifier designed to operate in harsh environments where precision measurement is needed to provide the required diagnostic in safety critical applications and enable the reduction of torque ripple and audible noise for the smooth and efficient control of BLDC motors such as EPS or braking, and improve the overall driver experience.

References

About the Author
Enda Nicholl is a strategic marketing manager in the Vehicle Electrification Business Unit at Analog Devices based in the ERDC (European Research & Development Centre) in Limerick, Ireland. Enda holds an O.N.C., an H.N.D., and a B.Sc. degree in mechanical engineering from the University of Abertay and has 25 years of experience in the field of automotive sensors, working in applications engineering, strategic marketing, and business development. Thirteen of those years have been with Analog Devices in the Automotive Business Unit. He can be reached at enda.nicholl@analog.com.
Part 2: Optimized Sigma-Delta Modulated Current Measurement for Motor Control

Jens Sorensen, System Applications Engineer, Shane O’Meara, System Applications Engineer, and Dara O’Sullivan, System Applications Manager

This is Part 2 in a two-part series. Part 1 discussed demodulation of sigma-delta (Σ-Δ) coded data using sinc filters in a motor control application. The importance of synchronizing the sinc filter’s impulse response to pulse-width modulation (PWM) was illustrated and strategies for synchronization were proposed; however, the synchronization schemes made it difficult to configure the system properly.

Here in Part 2 of the series, a new sinc filter structure optimized for synchronization is proposed. The filter improves measurement performance in applications that require tight timing control of the feedback chain. Part 2 then moves on to discuss the implementation of sinc filters using HDL code and how to optimize the filters for FPGA implementation. Finally, measurement performed on an FPGA-based 3-phase servo drive are presented.

Sinc Filters Optimized for Synchronization

As discussed in Part 1, an alias-free sigma-delta measurement is possible through the correct alignment of the sinc filter impulse response to PWM. While the method is straightforward, it is difficult—and in many cases impossible—to find a system configuration that gives the desired result. To illustrate this, assume the sinc filter and the PWM block shares a common system clock source that runs at \( f_{sys} \). The modulator clock, \( f_{mclk} \), is then determined by Equation 1.

\[
f_{mclk} = \frac{f_{sys}}{D_{mclk}} \quad (1)
\]

Where \( D_{mclk} \) is the clock divider for the modulator clock. Similarly, the PWM frequency, \( f_{pwm} \), is determined by Equation 2.

\[
f_{pwm} = \frac{f_{sys}}{D_{pwm}} \quad (2)
\]

Where \( D_{pwm} \) is the clock divider determining the PWM frequency. Finally, the decimation rate (data rate) from the sinc filter is given by Equation 3.

\[
f_{dec} = \frac{f_{mclk}}{D_{dec}} = \frac{f_{sys}}{D_{mclk} \times D_{dec}} \quad (3)
\]

Where \( D_{dec} \) is the clock divider for the decimated clock. To avoid drift between the impulse response and the PWM cycle, there must be an integer number of decimation cycles within a PWM cycle:

\[
\frac{f_{dec}}{f_{pwm}} = N \quad (4)
\]

Where \( N \) is an integer. By combining Equation 2, Equation 3, and Equation 4:

\[
\frac{D_{pwm}}{D_{mclk} \times D_{dec}} = N \quad (5)
\]

Clearly, only a limited selection of clock scalers, \( D_x \), satisfy Equation 5. Furthermore, most often there are tight restrictions on how the clock scalers can be selected. For example, a system may be required to run at a certain PWM frequency (for example, 10 kHz) or use a certain modulator clock (for example, 20 MHz). Another complication is the limited number of options when it comes to selecting the modulator clock. For example, if \( f_{sys} \) is 100 MHz, the only reasonable choices for \( D_{mclk} \) falls in a limited range of integers of 5 to 10 (20 MHz down to 10 MHz).

Given all these restrictions, it is very difficult—if not impossible—to find clock scalers that give the desired alignment between impulse response and PWM. What typically happens is the user is forced to select clock scalers that satisfy Equation 5 rather than selecting clock scalers that result in the desired PWM frequency, modulator clock, and signal-to-noise ratio (SNR).

Also, if one of the frequencies changes over time, it becomes impossible to find a valid configuration. This is quite common in multiaxis systems where a single motion controller synchronizes multiple motor controllers in a network.

While the alignment scheme gives excellent measurement performance, it can prove to be impractical. In the following section, a new type of sinc filter is presented. The filter offers optimum measurement performance and at the same time allows the user to select all clock dividers independently.
Flushing Sinc Filter

A traditional third-order sinc filter is shown in Figure 1. The filter generates the modulator clock to the ADC by scaling the system clock and, in return, the ADC generates a 1-bit data stream to the filter. The filter function itself consists of three cascaded integrators, \(1/(1 - z^{-1})\), clocked at the same rate as the modulator and three cascaded differentiators, \(1 - z^{-1}\), clocked at the decimated clock.

The sinc filter and ADC are operated by continuously applying a clock to both. As a result, the filter outputs data continuously at a fixed rate determined by the decimated clock. The data rate from the filter is typically lower than the update rate of the motor control algorithm, so a number of the filter outputs are rejected. Only when the impulse response is centered around the ideal measurement is the output captured and used as feedback.

With space vector modulation, the phase current only assumes its average value two times per PWM period. Following this, there are only two possible alias-free sinc data output per PWM cycle, so there is no need to let the filter run continuously. It is actually sufficient to only enable the measurement when the feedback is needed and then disable the measurement at all other times. In other words, the measurement operates in an on-off mode, not unlike a conventional ADC.

A problem with the on-off mode of operation is that the modulator and filter clocks are derived from the same system clock. That means both the filter and the ADC operate in an on-off mode, which is not recommended because it will result in reduced performance. The reason is that the modulator in the ADC is a higher order system with a certain settling time and damping. So, when first applying a clock to the ADC, the modulator needs to settle before the output bit-stream can be trusted. To solve these problems, a new filter structure is proposed (see Figure 2).

As the standard sinc filter, the core consists of three cascaded integrators and three cascaded differentiators. However, the filter has several features that allow for new operating modes. Firstly, the filter has a new clock generator function that separates the modulator clock from the integrator clock. That makes it possible to continuously clock the ADC, but only enables the integrator clock when obtaining a measurement. Secondly, the filter has a new filter control function. With reference to a synchronization pulse, the control block handles all timing and triggering needed to operate the filter. The primary function of the filter controller is flushing the filter, which involves initializing all filter states, and timers filter ahead of starting a new measurement, as well as enable/disable the integrator clock at the right instances. Finally, the filter has a new buffer and interrupt control unit, which sorts through the output data and captures the correct measurement. The buffer and interrupt unit also notifies the motor control application by interrupting when a new measurement is ready to be consumed. The timing diagram in Figure 3 shows how the filter operates.

To start a measurement a synchronization pulse (sync pulse) is applied to the filter controller. Typically, this pulse indicates the start of a new PWM cycle. The sync pulse starts a timer, which is configured to expire exactly 1.5 decimation cycles before the desired measurement point. At this point, the integrator clock and decimated clock are enabled and the filtering process begins. After 3 decimation cycles (the settling time of a third-order sinc filter), the buffer and interrupt controller captures the data output and asserts the interrupt. In Figure 3, notice how the measurement is centered around the sync pulse. The sequence repeats itself at the next sync pulse, but the modulator clock remains on once the filter has been started.

![Figure 1. Traditional third-order sinc filter.](image1)

![Figure 2. Sinc filter designed for on-off operation and flush of all states.](image2)

![Figure 3. Timing diagram of sinc filter operating in an on-off mode.](image3)
The proposed sinc filter solves the problem of synchronization of a conventional sinc filter. The filter and its operating mode do not make any assumptions about the PWM frequency, the modulator clock, or the decimation rate. It works equally well with all system configurations and even if the PWM frequency varies over time. Since the filter is effectively reset for every measurement, it is also insensitive to drift between the clocks.

HDL Implementation of Sinc Filters

The authors have found that several of the publicly available sinc filter HDL examples have shortcomings that negatively affects filter performance or leads to unexpected behavior. This section will discuss some of the implementation issues and how to design HDL code for optimum performance on an FPGA.

Integrators

In its purest form a sinc3 filter consists of three cascaded integrators and three cascaded differentiators, see Figure 1. First, consider a pure integrator in the z-domain:

$$\frac{y(z)}{u(z)} = \frac{1}{1-z^{-1}} \quad (6)$$

Where u is the input and y is the output. The integrator has the difference equation:

$$y[n] = u[n] + y[n-1] \quad (7)$$

This first order equation is equivalent to an accumulator, which lends itself very well to implementation in clocked logic such as an FPGA. A common implementation approach is a D-type flip-flop accumulator as shown in Figure 4.

If the three integrators are implemented with the D-type flip-flop accumulator in Figure 4, the result is as shown in Figure 5.

Since this is a clocked circuit, it will take several clocks for a change of the input to affect the output. This becomes even clearer when examining the difference equations for the cascade accumulators (see Equation 10).

$$\begin{align*}
y_1[n] &= u[n] + y_1[n-1] \\
y_2[n] &= y_1[n-1] + y_2[n-1] = u[n-1] + y_1[n-2] + y_2[n-1] \\
\end{align*} \quad (10)$$

This difference equation is quite unlike the one for the pure integrators (see Equation 9). With the accumulators, it takes two clocks before an input affects the output, whereas with pure integrators, the input affects the output immediately. To illustrate this, Figure 6 shows the step response of Equation 9 and Equation 10, respectively, when a unit step is applied at sample number 5. As suspected, the accumulators are delayed by two samples compared to the integrators.

![Figure 4. Implementation of an accumulator with a D-type flip-flop.](image1)

This circuit can be implemented on an FPGA with only few logic gates. Now, when cascading three pure integrators, the transfer function in the z-domain is defined by Equation 8.

$$\frac{y(z)}{u(z)} = \left( \frac{1}{1-z^{-1}} \right)^3 = \frac{1}{1-3z^{-1} + 3z^{-2} - z^{-3}} \quad (8)$$

The difference equation for the three cascaded integrators is shown in Equation 9:

$$y[n] = u[n] + 3y[n-1] - 3y[n-2] + y[n-3] \quad (9)$$

Notice how the input at sample n affects the output at sample n.

![Figure 5. Three cascaded accumulators implemented with D-type flip-flops.](image2)
To get the ideal sinc3 response, a direct implementation of the difference from Equation 9 is proposed. The result is shown in Figure 7. Note how the block diagram consists of two parts: a clocked logic part (the flip-flops) and a combinatorial part (the summations). This realization requires more gates, but it has the desired filter performance and delay.

Differentiators

Similar to the integrators, many of the publicly available sinc filter examples implement the differentiator stage incorrectly, which results in reduced filter performances and unexpected delay. This section discusses the differentiator stage and makes recommendations on how to implement an FPGA for optimum performance. First, consider a pure differentiator in the z-domain in Equation 11 and the corresponding difference in Equation 12.

\[
\frac{y(z)}{u(z)} = 1 - z^{-1} \tag{11}
\]

\[
y[n] = u[n] - u[n - 1] \tag{12}
\]

To realize a differentiator on an FPGA a D-type flip-flop is most commonly used, see Figure 8.

A common way to implement the three D-type flip-flop differentiators is illustrated with the following HDL code snippet. Here, pseudo-Verilog is used, but the principle applies to other languages, too.

```verilog
always @(posedge clock)
begin
    y1[n] <= u[n] - u[n-1];
    y2[n] <= y1[n] - y1[n-1];
    y3[n] <= y2[n] - y2[n-1];
    u[n-1] <= u[n];
    y1[n-1] <= y1[n];
    y2[n-1] <= y2[n];
end
```

As with any clocked assignment, all the right-hand side statements are evaluated first and assigned to the left-hand side. Everything is clocked and all assignments are updated in parallel. This is a problem because the output terms \(y[n]\) relies on the delayed terms \(u[n-1]\) and \(y[n-1]\) being updated first. As a result, the previous Verilog snippet implements to logic, as shown in Figure 10.

Due to the clocked assignments, the delay of the differentiators is six clocks rather than the expected three clocks. Since the differentiators are clocked with the decimated clock, this effectively doubles the filter’s group delay and settling time. However, it also affects the filter’s attenuation and the frequency response is not that of an ideal third-order sinc. The implementation in Figure 10 is often seen in published sinc filter examples, but it is highly recommended to choose an approach that mimics an ideal differentiator stage.

The previous Verilog code snippet can be separated into two parts: a combinatorial part that calculates the current outputs and a clocked logic part that updates delayed states. This separation makes it possible to move the combinatorial part outside the always clocked block as shown in the code snippet shown in Figure 11.

```verilog
    u[n-1] <= u[n];
    y1[n-1] <= y1[n];
    y2[n-1] <= y2[n];
end
assign y1[n] = u[n] - u[n-1];
```

Figure 9. Three differentiators implemented as clocked logic.

Figure 10. Differentiators implemented with clocked assignments.
With the combinatorial assignments, there is no additional delay associated with the calculation of $y$, and the total delay is brought down from six clocks to the ideal three clocks. The block diagram for the recommended implementation of the differentiators is shown in Figure 12.

By combining the proposed implementation of the cascaded integrators and differentiators, the sinc filter gets ideal characteristics in terms of attenuation and delay. All sigma-delta-based measurements will benefit from the optimized filter implementation, but especially the flushing sinc that relies on knowing the exact filter delay.

Measurements
The proposed sigma-delta measurement system has been implemented and tested together with a servo motor controller based on a Xilinx® Zynq™-7020 SoC. The system consists of a 60 V, 3-phase permanent magnet servo motor (Kinco SMH40S) and a 3-phase switching voltage source inverter. The SoC runs a field-oriented motor control algorithm, as well as software for capturing measurement data in real time.

For phase current measurement, the system has two isolated sigma-delta ADCs (ADuM7701) followed by two third-order sinc filters. The sinc filters are implemented using the design recommendation discussed in this article, including the flushing sinc mode of operation. For comparison, measurement results for both the traditional, continuously operating filter and the flushing filter will be presented.

While the control system has closed loop field-oriented control, all measurements are performed with the open-loop control. A closed current loop is sensitive to measurement noise and the noise will couple through the current loop. By operating in open-loop, any effects from the current controllers are eliminated, which makes it possible to compare results directly.

Except for mode configuration and alignment to PWM, the measurements were done with the identical configurations including the decimation rate, which was set to 125. Any difference in the measurement results can therefore be contributed to the effect of aligning the sinc3 impulse response correctly to PWM or not. The control algorithm is executed at 10 kHz and the modulator clock is 12.5 MHz.

Unaligned Impulse Response with Continuous Sinc Filter Operation
In the first example (see Figure 13a), the impulse response is uncorrelated to the PWM waveform. Figure 13b shows two phase current measurements when the motor is stopped but the power inverter is switching, with a duty cycle of 50% on all phases. In this operating mode, the measurement shows the noise level of the measurement. Figure 13b shows the phase currents when the motor is running open-loop at 600 rpm. The motor has four pole pairs, so the electrical period is 25 ms. Both plots show significant noise that would severely affect the performance of any closed-loop current controller. The noise level is unrelated to the magnitude of the fundamental phase current, so the noise is relatively worse at light load. The noise in this example is due to an unaligned sinc filter impulse response and it would have little or no increase to the decimation rate (attenuation) of the sinc filter.

Figure 12. Implementation of three cascaded differentiators using a mix of clocked logic and combinatorial logic.

Figure 13. Continuous operating mode with the sinc filter impulse response unaligned to PWM.
Aligned Impulse Response with Continuous Sinc Filter Operation

Figure 14 shows measurement results when there is an integer number of decimation cycles per PWM period and the impulse response is aligned with the ideal measurement point. The results in Figure 14 are directly comparable with the results in Figure 13.

When comparing Figure 13 and Figure 14, the filters are using the same decimation rate, but the noise level has been reduced significantly. The examples illustrate how important system configuration and synchronization are to fully utilize the performance of a sigma-delta-based signal chain.

Flushing Sinc Filter

While the results for the continuously operating sinc filter in Figure 14 were satisfactory, the filter still has difficulty in finding a configuration that enables synchronization. While it is possible to synchronize a continuously operating sinc filter to PWM, it is often not practical. That problem is solved with the flushing sinc filter.

Figure 15 shows measurement results for a flushing sinc filter. The filter is configured to only run for 3 decimation cycles around the ideal measurement point. Performance is, as expected, similar to the continuously operating filter in Figure 14.

For comparison, the flushing filter uses the exact same configuration as the continuously operating filter. The difference is that the continuously operating filter must use this configuration or performance will deteriorate, as illustrated by the results in Figure 13. The flushing filter, on the other hand, will maintain its optimal performance with any possible system configuration.

The magnitude of the noise with the unaligned, continuously operating sinc filter (Figure 13a) is approximately 120 counts out of a 16-bit signal. That corresponds to a loss of approximately the lower 7 bits due to noise. The noise level of the flushing sinc filter (Figure 15a) is approximately 5 counts out of a 16-bit signal, corresponding to losing less than 3 bits due to noise.
Summary

Sigma-delta-based phase current measurement is widely used in motor drives, but getting optimum performance requires correct configuration of the whole system. This article discussed the sources that can lead to poor performance and how to correctly set up a system.

Configuring a system for optimum current feedback performance can be challenging and, in some cases, impossible. To solve this, a new type of sinc filter was proposed. The filter operates in an on-off mode and guarantees optimum performance with any system configuration.

Implementing a sinc filter on an FPGA requires development of HDL code. The article discussed several implementation techniques that lowers delay in the filter and increases attenuation.

Finally, the article presented several measurement results that illustrated the importance of synchronization, as well as performance, of the flushing sinc filter.

References


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Single IC Can Produce Isolated or Nonisolated ±12 V Outputs from 30 V to 400 V Input

Zhijun (George) Qian, Senior Engineer
and William Xiong, Applications Engineer

Electric vehicles, large-scale battery storage stacks, home automation, industrial, and telecom power all require converting high voltages to ±12 V, where dual polarity rails are required for powering amplifiers, sensors, data converters, and industrial process controllers. One challenge in all of these systems is creating a compact, efficient dual polarity regulator that can operate over a temperature range of –40°C to +125°C—especially important in automotive and other high ambient temperature applications.

Linear regulators are well understood and typically top the list of candidates for bipolar supplies, but are not suitable in the high input voltage, low output voltage applications previously mentioned, mainly due to heat dissipation in the linear regulator at high step-down ratios. Furthermore, a dual polarity solution requires at least two integrated circuits (ICs): one positive output linear regulator and a negative converter. A better solution would use a single switching regulator that produces both outputs from a relatively high input, at good efficiency and regulation, while fitting tight spaces and reducing cost.

This article presents two elegant circuits that generate ±12 V outputs from a wide 30 V to 400 V input voltage range, both using a single high voltage LT8315 converter. One circuit is an isolated flyback topology; the other is based on a nonisolated buck topology. The LT8315 itself is a high voltage monolithic converter with integrated 630 V/300 mA MOSFET, control circuitry, and high voltage start-up circuit, inside a thermally enhanced 20-lead TSSOP package.

Isolated Dual Polarity Flyback Regulator with No Optocoupler

Flyback converters are widely used in multi-output applications to provide galvanic isolation, improve safety, and enhance noise immunity. Outputs can be positive or negative, depending on which side of the output is grounded. Traditionally, the output voltage regulation is achieved using optocouplers to transfer information from the secondary-side reference circuitry to the primary side. The problem is that optocouplers add significant complexity and degrade reliability due to propagation delay, aging, and gain variation, etc. Typically, the one output connected to the feedback pin of the IC dominates the regulation loop, while other outputs are loosely controlled through the transformer windings, resulting in poor regulation of those outputs.

The LT8315 requires no optocoupler and samples the reflected, isolated output voltage from a tertiary winding on the power transformer. Also, the output voltage is sensed when the secondary current is almost zero to achieve excellent load regulation. In a dual output design, this unique sensing scheme allows each output to be closely regulated—both outputs can dominate the regulation. As a result, a typical ±5% load regulation is easily achieved.

The LT8315 solution shown in Figure 1 operates under quasi-resonant boundary conduction mode. The primary MOSFET has a minimum turn-on loss because the MOSFET turns on when the switch node rings to its valley. There is no diode reverse recovery loss on the secondary side. A 3 kV reinforced insulation transformer is the only component across the isolation barrier, enhancing system reliability and meeting stringent high voltage power isolation requirements. Figure 2 shows the full load efficiency curve under different input voltages. This flyback converter achieves 85.3% peak efficiency when the input is 70 V and both load currents are 50 mA.

Figure 1 shows the complete schematic of a flyback converter with a wide input range from 30 V to 400 V. It outputs ±12 V and maintains tight regulation with load currents from 5 mA to 50 mA. This flyback converter has 85.3% peak efficiency, as shown in Figure 2.
Figure 1. A complete ±12 V/50 mA isolated flyback converter for a wide input range, 30 V to 400 V.

Figure 2. Full load efficiency vs. input voltage for the flyback converter in Figure 1.

Figure 3. Schematic of a nonisolated dual inductor buck converter using a single LT8315 IC; 30 V to 400 V input to ±12 V outputs at 30 mA each.
Nonisolated Dual Polarity Buck Regulator with Two Inductors

The LT8315’s high voltage input ability can be applied in nonisolated solutions by using off-the-shelf inductors. A buck regulator with dual inductors, requiring only a few components, is shown in Figure 3. This converter accepts an extremely wide-ranging input—30 V to 400 V—and produces ±12 V/30 mA outputs. This circuit can achieve efficiency as high as 87% at full load for both outputs with a 30 V input.

In this topology, LT8315’s GND pad is intentionally ungrounded and connected as the common switch node for driving both outputs. For PCB layout, LT8315’s GND pad’s size should be constrained within the exposed pad area to reduce electromagnetic interference to other components because the GND trace is a relatively noisy switch node in this topology. Diode D2 and two 1% resistors at the FB pin form the feedback path regulating the positive output voltage. D2 is necessary to prevent the FB pin discharging whenever the MOSFET conducts. The resistive voltage divider does not need to take into account the forward voltage drop of D2 because the forward voltage of D2 and D3 are equal and cancel; therefore, the feedback network tracks and closely regulates the positive output voltage.

The negative rail comprises a low voltage coupling capacitor C_LF, a second inductor L2, a catch diode D4, and the negative output capacitor C_O2. According to the inductor volt-second balance for the circuit loop of C_LF-L1-C_O2-L2, the average voltage across L1 and L2 is zero, so the coupling capacitor C_LF’s voltage is equal to the positive output voltage. C_O2 charges up L2 during the on-time of the MOSFET, while D4 provides a path for the L2 discharge during the MOSFET off-time. The negative output voltage is indirectly regulated based on the voltage of C_LF remaining constant and equal to the positive output voltage. As shown in the regulation curve of Figure 4, the negative supply maintains ±5% regulation for a load range of 3 mA to 30 mA at various input voltages, when the positive load is at a full 30 mA.

Figure 4. Negative 12 V load regulation curves at various input voltages for the dual inductor buck converter in Figure 3.

Conclusion

This article presents two dual polarity converter solutions for a wide 30 V to 400 V input range: one isolated, the other nonisolated. The LT8315 is used in both, due to its high voltage integrated MOSFET, no optocoupler feedback loop, and internal high voltage startup circuit. Other features include low ripple Burst Mode operation, soft start, programmable current limit, undervoltage lockout, temperature compensation, and low quiescent current. LT8315’s high level of integration simplifies the design of high voltage input and dual polarity output circuits for a wide variety of applications.

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RAQ Issue 171: “If It Isn’t Broken, Don’t Fix It.” Adjusting the Gain of a Fixed-Gain Difference Amplifier

Rusty Juszkiewicz, Product Engineer

Question:
Is it possible to increase the gain of a fixed-gain difference amplifier?

Answer:
Yes, by adding more resistors.

Classic 4-resistor difference amplifiers solve many difficult measurement problems. However, there are always applications that require more flexibility beyond what these amplifiers offer. Since the matching of resistors in a difference amplifier directly affects the gain error and common-mode rejection ratio (CMRR), implementing these resistors on a single die enables top performance. However, relying on only internal resistors for setting gain removes users’ flexibility to choose their desired gain outside the manufacturer design choices.

When using a fixed-gain amplifier in a signal chain, if more gain is required, typically another amplifier stage is added to achieve the desired overall gain. Although this approach works well, it can increase overall complexity, required board space, noise, cost, etc. Alternatively, there is another way of increasing the system gain without the second gain stage. Providing a positive feedback path by adding a few resistors to the fixed-gain amplifier will reduce the overall negative feedback, and therefore result in a higher overall gain.

In a typical negative feedback configuration, the portion of the output that is fed back to the inverting input is known as $\beta$, with the gain of the circuit being $1/\beta$. With $\beta = 1$, the entire output signal is returned to the inverting input and a unity-gain buffer is realized. With a lower value for $\beta$, a higher gain is achieved.

In order to increase the gain, $\beta$ must be reduced. This can be done by increasing the ratio of $R_2/R_1$. However, there is no way to lower the feedback to the inverting input for a fixed-gain difference amplifier since this would require either a larger feedback resistor or a smaller input resistor. By providing feedback from the output to the reference pin of a difference amplifier, and therefore to the noninverting input, the gain of the previously fixed-gain amplifier can now be increased. The resulting combined $\beta (\beta_c)$ for the op amp is the difference between $\beta-$ and $\beta+$, which will determine the new gain and bandwidth. Please note that $\beta+$ is providing positive feedback, therefore care should be taken to ensure the net feedback remains negative ($\beta- > \beta+$).

Figure 1. Negative feedback: noninverting op amp configuration.

Figure 2. Combined beta.
In order to adjust the circuit gain using $\beta_+$, the first step is to calculate $\beta_-$ (which is $\beta$ for the initial circuit). Note that the attenuation term $G_{\text{attn}}$ is the ratio of the signal from the positive input of the difference amplifier to the noninverting input of the op amp.

\[
G_0 = G_{\text{attn}} \times \text{Noise Gain}
\]
\[
\text{Noise Gain} = 1/\beta-
\]
\[
\beta_- = G_{\text{attn}}/G_0
\]

Once the desired gain is chosen, the required $\beta$ and therefore $\beta_+$ can be determined. Since the fixed-gain amplifier will have a known gain, the calculation of $\beta$ is straightforward.

\[
\beta_c = G_{\text{attn}}/G_1
\]
\[
\beta_c = \beta_- - \beta_+
\]
\[
\beta_+ = G_{\text{attn}}(1/G_0 - 1/G_1)
\]

The quantity $\beta_+$ is exactly the portion of the output signal that is returned to the noninverting input of the op amp. Keep in mind that since the feedback through $\beta_+$ will go to the reference pin, the signal will go through two resistor dividers (see Figure 3), both of which need to be accounted for in order to achieve the correct $\beta_+$.

One key feature of a difference amplifier is the CMRR. Matched resistor ratios on the positive and negative networks are crucial to a good CMRR, therefore a resistor (R5) should also be added in series with the positive input resistor to balance the added resistance on the reference pin.

In order to determine the required values of resistors R3 and R4, a Thévenin equivalent circuit can be used to simplify the analysis.

As mentioned above, in order to maintain a good CMRR, R5 must be added. The value of R5 is determined by the parallel combination of R3 and R4 ratioed by the same factor as the resistors in the input attenuator. Since the ratio of $R1/R2 = (1/G_{\text{attn}}) - 1$, R1 and R5 can be replaced with ratioed R2 and R3||R4, respectively.

\[
\frac{1}{G_{\text{attn}}} - 1 = \alpha
\]

As mentioned earlier, the gain from $V_{\text{OUT}}$ to $A_{\text{in+}}$ of the simplified circuit must be equal to $1/\beta+$.

\[
V_{\text{Th}} \times \alpha/\alpha + 1 = V_{A_{\text{in+}}}
\]

since

\[
V_{A_{\text{in+}}}/V_{\text{OUT}} = \beta_+
\]

where

\[
\beta_+ = G_{\text{attn}}(1/G_0 - 1/G_1)
\]
\[
R_4/(R_3 + R_4) = (1/\alpha) \times (1/G_0 - 1/G_1)
\]
Since R3 and R4 load the op amp, care should be taken not to select values that are too small. Once a desired load \((R3 + R4)\) is chosen, the values of R3 and R4 can be easily calculated from Equation 4. Once R3 and R4 are determined, R5 can then be calculated from \(R3||R4 \times \beta\).

Since this technique relies on a ratio of resistors, there is a lot of flexibility. There is a trade-off between noise and power consumption, and the resistance values should be large enough to prevent overloading the op amp. Also, since R5 is ratioed from R3 and R4, the same type of resistor should be used to maintain good performance over temperature. If R3, R4, and R5 drift together, then the ratio will be maintained and there will be minimal, if any, thermal drift due to these resistors. Since the noise gain of the op amp will increase, the resulting bandwidth will be reduced by the ratio of the \(\beta c/\beta\) following the gain-bandwidth product.

One great application for this technique is with the AD8479, which is a unity-gain, high common-mode difference amplifier. The AD8479 is capable of measuring a differential signal in the presence of ±600 V common mode and it has a fixed-gain of unity. Some applications require gain greater than unity and the previously described technique is a perfect fit. Another commonly desired gain for current-sense applications is 10, therefore let \(G1 = 10\).

Since the AD8479 attenuates the common-mode signal down, then gains the differential signal up to get a system gain of unity, this needs to be considered during the implementation of the gain adjustment.

\[ G0 = 1 \]  
(5)

Since the gain from the positive reference is 60, and the gain from the positive input is 1, the noise gain of the circuit is 61. Also, since the overall gain is unity, \(G_{\text{attn}}\) must therefore be 1/noise gain:

\[ G_{\text{attn}} = 1/61 \]
\[ \beta_\text{c} = 1/61 \]
\[ \beta = 1/610 \]  
(6)

Using Equation 6, R3 and R4 can be easily calculated:

\[ R4/(R3 + R4) = (1/60) \times (1/61 - 1/10) = 1/600 \times (1 - 1/10) = 9/600 \]  
(7)

The gain for the AD8479 is specified with a 2 kΩ load, therefore this is the target for R3 + R4.

Let \(R3 + R4 = 2000, R4 = 30, R3 = 1970, R5 = 1773\)

(8)

In order to build this circuit using standard resistor values, parallel resistors need to be used to achieve a more accurate ratio than single standard resistors will allow.

Let \(R3 = 2050, R4 = (32.4 \parallel 866), \text{ and } R5 = (1910 \parallel 54900)\)

(9)

As you can see from Figure 7, the resulting output (blue) is 10× the input (yellow) as expected.

The nominal bandwidth for the gain of 10 circuit is expected to be 1/10th of the typical AD8479 bandwidth since \(\beta c/\beta\approx 1/10\) and the actual measured –3 dB frequency was 48 kHz.
Figure 9 shows that the resulting pulse response and signature are as expected. The slew rate matches the standard AD8479 slew rate and the settling is longer due to the reduced bandwidth.

Since the new circuit provides feedback to both inputs of the op amp, the common mode of the op amp is affected by a signal on either input. This alters the input voltage range of the circuit and it should therefore be evaluated to avoid overdriving the op amp. Also, since the noise gain has been increased, the spectral and peak-to-peak voltage noise at the output will also increase by that same factor. However, there is a negligible effect when the signal is referenced to the input. Lastly, the CMRR of the increased gain circuit is equal to the CMRR of the previous circuit assuming there is no additional common-mode error added from resistors R3, R4, and R5. Since R5 is implemented to correct the CMRR from the addition of R3 and R4, it is possible to tune the CMRR to be better than the original circuit using R5. However, this will require fine adjustments and you will be trading gain error for CMRR in the process.

This process can be utilized to take advantage of the benefits of the fixed-gain difference amplifier without being bounded by its fixed nature. Since the technique is generalized, it could be leveraged with many other difference amplifiers. Simply adding three resistors enables significant flexibility in the signal chain without adding any active components, which reduces cost, complexity, and board spacing.

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Understanding the Fundamentals of Earthquake Signal Sensing Networks

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Abstract
Earthquakes pose a major threat for condensed commercial and residential areas and for all types of structures. As these areas grow larger and as more buildings are constructed, seismic monitoring requires the implementation of a widespread sensor network. Traditional instruments are not viable due to high cost and complexity. The use of microelectromechanical system (MEMS) accelerometers and rugged small-sized geophones enable the development of a low cost Internet of Things (IoT) solution. Current technology in active components and converters allows these sensors to reach the modern instrument standards. Analog Devices provides a simple but reliable instrument design solution for seismic sensor network applications.

Introduction
As the world grows more interconnected and interdependent, moderate and large earthquakes have the potential to cause significant economic disruption and loss. A major earthquake in any vulnerable urban center will have a ripple effect on that center’s national economy and on the ability of its businesses to provide services and participate globally.1 Recognizing that earthquake risk is a global problem, improving seismic monitoring to mitigate this risk is a crucial responsibility.

One key factor to the improvement of seismic monitoring is the implementation of a seismic sensor network, which requires the widespread deployment and interconnection of seismic instruments.2 However, the cost and complexity of installing numerous traditional seismic instruments are high.3 Integrating IoT technology provides a low cost solution while maintaining standard seismic data quality.4 This article discusses the physics of earthquakes and ground motion sensors, the modern instrument standards followed and the features they extract. Furthermore, a system design using Analog Devices solutions is developed for different seismic sensor network applications.

Earthquake
An earthquake is an event that is caused by the movements and collisions of tectonic plates. The energy generated from the collisions propagates through and around the surface of the earth as seismic waves. These waves come in multiple directions and are categorized as body waves and surface waves.

There are two types of body waves: primary waves (P-waves) and secondary waves (S-waves). P-waves travel along the direction of propagation as a series of compressions and rarefactions. Due to their nature of propagation, they follow spherical divergence. Although they have the largest decay in wave energy among other types of waves, they are the fastest, having speeds in the range of 5 km/s to 8 km/s. The fast energy decay also makes them the least destructive type of wave. P-waves can travel not only through the surface, but also through water or fluids.

S-waves, also called shear waves, follow right after the arrival of P-waves. They travel along the surface of the earth at a rate of about 60% to 70% of P-waves. This type of wave travels orthogonally to the direction of propagation and the Earth’s surface. S-waves are more destructive than P-waves because of their lower energy decay. P-waves and S-waves are collectively known as body waves.
Compression
Undisturbed Medium
Dilation
Direction of Wave Propagation
(a)
Direction of Wave Propagation
(b)
Direction of Wave Propagation
(c)
Direction of Wave Propagation
(d)

Figure 1. Types of seismic waves: (a) primary waves; (b) secondary waves; (c) Love waves; (d) Rayleigh waves.5

Surface waves are 10% slower than body waves, but they are the most destructive. It is worth noting that the propagation velocity of seismic waves varies widely depending on the type of soil they are traveling in.6 Surface waves are composed of Rayleigh and Love waves. Rayleigh waves are a type of surface wave that propagate near the Earth’s surface as ripples and cause a rotation that can be either prograde (along the direction of propagation) or retrograde (against the direction of propagation). They are also called ground roll due to the nature of their movement. Love waves, on the other hand, travel orthogonally with the direction of propagation but parallel with the surface of the Earth. Figure 1 shows the different types of waves and their effect on the Earth's body.

Magnitude, Intensity, and Spectral Intensity

Earthquake magnitude and earthquake intensity are commonly mistaken for one another. They may be related, but they are measurements of two different earthquake parameters.

Earthquake Intensity

Earthquake intensity, or simply intensity, is highly dependent on the properties of the location where the measurement was taken. It describes the effect of an earthquake on a specific area and has been traditionally used worldwide as a method for quantifying the shaking pattern and the extent of the damage. Hence, earthquake intensity does not have one true value. Earthquake intensity values follow either the Modified Mercalli Intensity Scale (1 to 12) or the Rossi-Forel Scale (1 to 10). However, the Modified Mercalli Intensity (MMI) Scale is now dominantly used worldwide. Table 1 shows intensity values with their corresponding descriptive effect in the modified Mercalli scale given by the United States Geological Survey (USGS).

Table 1. Abbreviated Modified Mercalli Intensity Scale

<table>
<thead>
<tr>
<th>MMI</th>
<th>Descriptive Effect</th>
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<tbody>
<tr>
<td>I</td>
<td>Not felt except by a very few under especially favorable conditions.</td>
</tr>
<tr>
<td>II</td>
<td>Felt only by a few people at rest, especially on upper floors of buildings.</td>
</tr>
<tr>
<td>III</td>
<td>Felt quite noticeably by people indoors, especially on upper floors of buildings. Many people do not recognize it as an earthquake. Standing motor cars may rock slightly. Vibrations similar to the passing of a truck. Duration estimated.</td>
</tr>
<tr>
<td>IV</td>
<td>Felt indoors by many, outdoors by few during the day. At night, some awakened. Dishes, windows, doors disturbed; walls make cracking sound. Sensation like heavy truck striking building. Standing motor cars rock noticeably.</td>
</tr>
<tr>
<td>V</td>
<td>Felt by nearly everyone; many awakened. Some dishes, windows broken. Unstable objects overturned. Pendulum clocks may stop.</td>
</tr>
<tr>
<td>VI</td>
<td>Felt by all, many frightened. Some heavy furniture moved; a few instances of fallen plaster. Damage slight.</td>
</tr>
<tr>
<td>VII</td>
<td>Damage negligible in buildings of good design and construction; slight to moderate damage in well-built ordinary structures; considerable damage in poorly built or badly designed structures; some chimneys broken.</td>
</tr>
<tr>
<td>VIII</td>
<td>Damage slight in specially designed structures; considerable damage in ordinary substantial buildings with partial collapse. Damage great in poorly built structures. Fall of chimneys, factory stacks, columns, monuments, and walls. Heavy furniture overturned.</td>
</tr>
<tr>
<td>IX</td>
<td>Damage considerable in specially designed structures; well-designed frame structures thrown out of plumb. Damage great in substantial buildings, with partial collapse. Buildings shifted off foundations.</td>
</tr>
<tr>
<td>X</td>
<td>Some well-built wooden structures destroyed; most masonry and frame structures destroyed with foundations. Rails bent.</td>
</tr>
<tr>
<td>XI</td>
<td>Few, if any, (masonry) structures remain standing. Bridges destroyed. Rails bent greatly.</td>
</tr>
<tr>
<td>XII</td>
<td>Total damage. Lines of sight and level are distorted. Objects thrown into the air.</td>
</tr>
</tbody>
</table>

There have been numerous methods to determine the intensity of an earthquake.7 These methods used data gathered from past earthquakes and created their own ground motion prediction equations (GMPEs) to predict the intensity values. The equations that were derived use at least one, or a combination of, ground motion parameters—namely peak ground displacement (PGD), peak ground velocity (PGV), and peak ground acceleration (PGA). Earlier equations were primarily based on PGA with a few cases that used PGV and PGD. Even though the GMPEs used data from multiple databases to develop the correlation, the values obtained by different models still vary significantly. For example, a PGA value of 10 cm/s² using Wald’s GMPE results in an MMI value of 3.2. Alternatively, Hershberger’s GMPE categorizes a 10 cm/s² PGA value to an MMI value of 4.43. Note that the majority of the GMPEs observe the power law, so an exponential increase in PGA value is required for a step increase in MMI value. Equation 1 shows the correlation equations created by Wald and Hershberger.
Earthquake Spectral Intensity

While an earthquake’s intensity is dependent on its effect as felt on a certain location, spectral intensity (SI) is a measure of the magnitude of destructive energy imposed by the earthquake on a specific structure. The SI value is calculated from the velocity response spectrum using the equation shown in Equation 3. Highly rigid structures have a velocity normal period of 1.5 s to 2.5 s. Since the SI value operates over the shaking velocity spectrum, it can easily distinguish seismic activities from earthquakes or from other sources. Thus, the SI value can be used as a standard of earthquake effect on a building’s structural health. Furthermore, compared to the JMA seismic intensity, the SI value involves a less complex computation, which makes it more suitable for low power applications.

Seismic Sensing

Seismic sensing is the process of measuring and analyzing seismic waves. Seismic waves do not only refer to the motions generated by earthquakes; any force applied to the ground, even as light as walking, can cause a disturbance enough to generate seismic waves. The range of ground motion that is of interest in earthquake monitoring applications is very large. Earthquakes can generate ground motions as thin as paper or as tall as a room.

Ground motion can be characterized by displacement, velocity, and acceleration. Ground displacement is measured by the distance traveled by the Earth’s surface. The change in position can be either horizontal or vertical. Ground velocity is how far the surface has been moved, whereas ground acceleration is how fast the ground velocity is changing with respect to time. Ground acceleration is the most important factor in determining the stress induced to structures during earthquakes. The relationship between magnitude, ground motion, and intensity is shown in a presentation by GeoSIG.

The devices used for seismic sensing are very application specific. Applications that involve seismic sensing can be categorized based on their frequency ranges. Instruments are therefore made with frequency response curves appropriate to their use case. An illustration of different seismic sensing applications and their covered frequencies is shown in a chart by GeoSIG.

Overview of Modern Seismometers and Ground Sensors

Seismic sensing devices, commonly called seismometers, have evolved from using the traditional pen and pendulum to the use of electronic and electromechanical sensors. Advances in the design of these sensors have resulted in instruments with varied operating frequency ranges, sensing mechanisms, and measured ground motion parameters.
Strain Seismometers

Historical seismic instruments can only record ground displacement. Technology advancements have made it possible for different mechanisms in measuring ground displacement. A strain seismometer or strain meter generally refers to instruments that record and measure the displacement between two ground points. 14 Traditional models used a solid rod buried or installed in a borehole. The rod is usually infused with quarts and other materials highly sensitive to changes in length and strain. The change in length is attributed to small displacements caused by ground motion.

Another type of implementation is called the volumetric strain meter, which uses a borehole-installed cylinder with a liquid-filled tube. 15 Deformations of the container volume causes changes in the liquid level, which is translated by voltage displacement transducers to ground displacement. Without the need for special materials required by traditional models, the volumetric strain meter is more widely used in the field.

Current advances in laser technology has produced the laser interferometer, which greatly extends the accuracy of strain meters in general. This type of strain meter uses the same principle of an unequal arm length Michelson interferometer, where one point is the sensor, laser source, and short arm; and the other point is a reflector situated a measuring distance away. The device translates the change in the interference fringes caused by the movement of the reflector to ground displacement. The sensitivity and accuracy of the displacement measurement by this approach is directly proportional to the length of the measuring distance. Thus, laser strain meters require very deep underground installations.

The precision of strain meters can reach up to one part per billion. As such, these devices are usually used to measure the deformation of the Earth or crustal movement due to fault movement and volcanic activities. They can measure seismic wave signals at very low frequencies. However, differential ground movement is very small when compared to the motion of a suspended mass relative to the ground. Thus, strain meters are not recommended for sensing ground motions caused by earthquakes. 3

Inertial Seismometers

The inertial seismometer determines ground motion parameters with respect to an inertial reference, which is typically a suspended mass.3 Specifically, ground motion parameters refer to the linear velocity and displacement of the suspended mass. Although resultant ground motion is composed of both its linear and angular components, the rotational effect from a seismic wave has been found to be negligible. These velocity and displacement values are obtained from transducers, which convert the movement of the suspended mass into electrical signals. The mechanical suspension that governs the movement is dependent on the inertial force acting on the suspended mass. The velocity and displacement transducers, and the mechanical suspension are the two main components of inertial seismometers. The development of precision instruments for these two components are the main design principles of modern inertial seismometers.

Force-Balanced Accelerometers

The mechanical suspension requires a small restoring force for sensitivity such that small accelerations can still produce significant displacements on the suspended mass. However, when large accelerations from strong seismic motion are applied to the suspended mass, a small restoring force will not be able to balance the resulting movement. Thus, a passive mechanical suspension is precise and sensitive only to a limited range of ground accelerations. The force-balanced accelerometer (FBA) removes this limitation by adding a negative feedback loop to the mechanical suspension.

A compensating force is generated by an electromagnetic transducer based on the position of the suspended mass. This position is converted by a displacement transducer to an electrical signal that passes an integrator block to produce an output voltage proportional to ground acceleration.

The dynamic range of an FBA is significantly greater than seismometers with passive mechanical suspensions. Thus, this device is commonly used for strong motion seismic applications. However, the delay caused by the feedback loop limits the bandwidth of the device.

Velocity Broadband (VBB) Seismometers

Seismic waves from vehicular movement and man-made disturbances, such as mining events, have high frequency ground acceleration. At very low frequencies, an imbalanced suspension, ground tilt, and thermal effects will dominate ground acceleration. Thus, the bandwidth for seismometers using ground acceleration is limited to a specific band-pass response. A band-pass response of ground acceleration is equivalent to a high-pass response of ground velocity. Thus, for wider seismometer bandwidth, seismic signals are recorded in terms of ground velocity. The VBB seismometer is based on an FBA, but instead of passing the acceleration of the suspended mass as feedback, its velocity and position are used. The response of this device is very similar to the theoretical response of a traditional inertial seismometer, but without the decrease in sensitivity and precision for a wider range of forces.

Geophones and Microelectromechanical System (MEMS) Accelerometers

The trend for the increasing number of seismic applications is directed toward the development of seismometer or seismic sensor networks and arrays, such as in earthquake monitoring, oil exploration, and structural health. Seismometer implementation, shielding, and installation are three common constraints for these applications. Mass production and rapid deployment of devices, which directly solve these three common constraints, require seismometers to be scaled down in size and cost. Currently, there are two types of sensor technologies capable of ground motion sensing, which are extremely small and low cost when compared to FBAs and VBBs.

Geophones

Geophones are ground velocity sensors that are lightweight, robust, and require no electrical power to operate. Modern geophones have a magnet fixed to the case and surrounded by a coil of wire.16 The coil of wire is suspended by springs that allow it to move across the magnet. The velocity of this movement relative to the magnet induces an output voltage signal.

Shown in Figure 3 is the simulated frequency response of a 4.5 Hz geophone. The frequency response of a geophone is flat in velocity for a range of frequencies above its resonant frequency and diminishing for frequencies below this. Small-sized and low cost geophones have resonant frequencies typically above 4.5 Hz.

![Figure 3. Simulated 4.5 Hz geophone frequency response with a damping factor of 0.56.](image-url)
An equivalent electrical model can be created from the mechanical specifications of the geophone. Figure 4 shows an electrical model using the mechanical parameters of a SM-6 4.5 Hz geophone.\textsuperscript{17}  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Mechanical Parameter</th>
<th>Electrical Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 = M</td>
<td>M = Body Mass in kg</td>
<td>0.0111 F</td>
</tr>
<tr>
<td>L1 = 1/k</td>
<td>k = Coil Spring Constant</td>
<td>112.8 mH</td>
</tr>
<tr>
<td>R1 = 1/d</td>
<td>d = System Damping Coefficient</td>
<td>2.85 Ω</td>
</tr>
<tr>
<td>Rg = RCOIL</td>
<td>RCOIL = Coil Resistance</td>
<td>375 Ω</td>
</tr>
<tr>
<td>T1 = 1/G</td>
<td>Geophone Sensitivity</td>
<td>1.29</td>
</tr>
</tbody>
</table>

Figure 4. Equivalent electrical model of a SM-6 4.5 Hz geophone using mechanical parameters from the product data sheet.\textsuperscript{17}

To extend the bandwidth to cover the lower frequencies applicable to seismic sensing, a period extender is used. The three most common methods of low frequency response extension are inverse filters, positive feedback, and negative feedback.\textsuperscript{18}

**Inverse Filters**

The inverse filter compensates the geophone’s roll-off at frequencies below the resonant frequency. An inverse filter can be constructed by cascading an inverted high-pass filter at the resonant frequency and a low-pass filter with a cutoff frequency at the desired lowered value. Figure 5 shows the response of the inverse filter, as well as the resulting transfer function when it is applied. This method has many disadvantages that give the overall result a low signal-to-noise ratio (SNR). Pink noise will be amplified by the inverse filter, and its thermal stability at low frequencies is poor.

**Positive Feedback**

Positive feedback is done by feeding an external current to the geophone coil that would exert a force on its suspended mass. This external current signal is derived from the geophone’s output signal through positive feedback filters, such as the integrating filter, and amplify the suspended mass movement at low frequencies. Stability of the design of the positive feedback filter is difficult in practical situations.

**Negative Feedback**

Negative feedback, as opposed to positive feedback, attenuates the suspended mass movement inside. One method would be to overdamp the current through the geophone coil by reducing the damping resistance. However, this is physically limited by the coil resistance. To reduce the damping resistance to values significantly lower than the coil resistance, a negative resistance is added. A negative resistor can be achieved through active devices as a negative impedance converter (NIC). This can be implemented using an operational amplifier (op amp) as shown in Figure 6. Band-pass filters and high gain filters can be added to shape and stabilize the frequency response.

**MEMS Accelerometers**

MEMS accelerometers are motion transducers in a single IC device package. The typical construction uses a pair of capacitors with a micromass of silicon with metal plates in the middle.\textsuperscript{19} Very thin regions of silicon suspend the mass in the middle. Changes in the position of the mass result in changes to the device capacitance that translate to a voltage signal proportional to the acceleration of the suspended mass. MEMS devices require a power supply to operate, and some MEMS accelerometers have a built-in digitizer to eliminate the unnecessary noise, as well as the need to match sensors and recorders. As shown in Figure 6, the frequency response of a MEMS accelerometer is like a low-pass filter with a cutoff at the resonant frequency.

Figure 5. Frequency response of an inverse filter transfer function and its effects on a simulated 4.5 Hz geophone frequency response.

Figure 6. Basic architecture of a negative impedance converter using an op amp.

Figure 7. Frequency response of a MEMS accelerometer (ADXL354) on its X-axis.\textsuperscript{20}

Due to offset drifts, MEMS accelerometers perform better at higher frequencies up until their resonant frequency.\textsuperscript{21} Conversely, geophones, due to their mechanical construction, perform better at lower frequencies that are still above resonance. A small, low cost seismometer can be implemented to utilize both geophones and MEMS accelerometers to achieve a higher device bandwidth. The sensor output of geophones and MEMS accelerometers can be converted to different ground motion parameters when convolved with the appropriate sensor transfer function. The paper “Seismic Sensing: Comparison of Geophones and Accelerometers Using Laboratory and Field Data” discusses the geophone and MEMS accelerometer sensor outputs for the same ground displacement Ricker wavelet based on the common transfer functions of each sensor.\textsuperscript{22}
Seismic Sensor Instrument Guidelines

Seismic signal analysis using seismometer arrays or seismic sensor networks requires, for repeatability and uniformity, a set of standards and specifications on the instruments used. The USGS has set a standard for instruments to be deployed in their Advanced National Seismic System (ANSS). This section discusses the different specifications required to achieve the desired device performance for a wide range of applications based on experience and technological trends noted by the USGS.

Data Acquisition System (DAS) Standards

Modern seismometers are classified by the USGS as data acquisition systems. In contrast to the traditional seismometer, standard DAS include the seismic sensor, the data acquisition unit, and the peripheral and communication hardware. They are categorized into Class A, B, C, and D instruments based on the device performance. Class A instruments are near state-of-the-art seismometers while Class D instruments are comparable to traditional seismometers. For a complete discussion of the specifications, see the Instrument Guidelines.

Instrument Bandwidth

The specified bandwidth and frequency response of seismic sensors differ for those measuring velocity and acceleration. The higher the instrument class, the wider the bandwidth and better the frequency response. Broadband sensors are all Class A instruments with a bandwidth of at least 0.01 Hz to 50 Hz. Their frequency response is flat for velocity in the frequency range of 0.033 Hz to 50 Hz.

Short period Class A sensors have low bandwidth at 0.2 Hz to 50 Hz. Their frequency response is flat for velocity only in the frequency range of 1 Hz to 35 Hz.

Class A accelerometers have a flat frequency response in the range of 0.02 Hz to 50 Hz, while Class B accelerometers have a flat frequency response in the range of 0.1 Hz to 35 Hz only.

Strong Motion, Weak Motion, and Broadband Sensors

Sensors used by DAS are classified by the amplitude and frequency range of the seismic signals they capture. Strong motion sensors measure large amplitude seismic signals and are usually accelerometers. Strong motion accelerometers can measure up to 3.5 g with a system noise level less than 1 μg/$\sqrt{\text{Hz}}$.

Weak motion sensors can measure very low amplitude seismic signals with a noise level of less than 1 ng/$\sqrt{\text{Hz}}$. However, broadband sensors are already capable of measuring low amplitude seismic signals; hence, weak motion sensors are rarely used.

Sensor Channels and Orientation

Linear ground motion components resulting from seismic waves are present in all three Cartesian axes. The traditional standard orientation for triaxial seismic sensors is toward the East, North, and upward direction. However, the construction of traditional and even some modern seismometers is different for horizontal and vertical sensors since vertical sensors must consider gravitational effects. The homogenous triaxial arrangement allows for similarly constructed sensors to be used to determine the linear ground motion components in the Cartesian axes. The sensors are positioned at three equally spaced points in a circle around the center of the instrument and inclined toward it at an angle of 54.7° from the vertical. The modified set of axes can be transformed back to the Cartesian axes using the equation shown in Equation 4.

Equation 4 demonstrates the transformation matrix to convert the homogenous triaxial arrangement to the Cartesian coordinate system.

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \frac{1}{\sqrt{6}} \begin{bmatrix} 1 & -2 & 1 \\ 1 & 0 & -3 \\ 3 & 3 & -2 \end{bmatrix} \begin{bmatrix} U \\ V \\ W \end{bmatrix}$$

Most modern sensors, however, are already packaged and constructed for triaxial measurements. These sensors have inherent cross-axis coupling at very small degrees. The instrument guidelines require cross-axis coupling to be less than –70 dB of the output signal.

Resolution and Sampling Rate

Ground motion resulting from earthquakes can have very small amplitudes at very low frequencies. Data loggers used for seismic instruments are capable of recording signals at various sampling rates at high resolutions. Broadband seismometers require at least 20-bit data resolution at sampling rates as low as 0.1 samples per second (SPS) up to 200 SPS. Short period velocity sensors and Class A accelerometers require at least 22-bit data resolution at sampling rates of 1 SPS to 200 SPS. Class B accelerometers have lower requirements for resolution of at least 16 bits of data.
The specifications for sampling rates take into consideration instruments with internal data storage. However, advanced seismometers are equipped with more memory space and have access to large network data spaces, such as cloud data services, and thus can support sampling rates that exceed the rated specification. This allows for more accurate data analysis and seismic research.

**Timing and Location Information**

Seismic signals are only relevant to the specific location and time of measurement. It is the standard for every seismic instrument to have time-stamped data with a known global location or position. It is a requirement for every seismic instrument to be able to affix its location for every recording, either through manual user input or through a global positioning system (GPS) device or service. Modern seismometers also have either a built-in real-time clock or can sync to an accurate reference time such as via an online network time protocol (NTP) server.

**Output Data Format**

There are two prominent data formats used by seismic instruments worldwide, SEG-Y and SEED. The SEG-Y format is an open standard developed by the Society of Exploration Geophysicists (SEG) to handle geophysical data such as three-dimensional seismic signals. Included in each record are the timestamps, sample intervals, and location in coordinates of the actual measurement. Details on the specifications of the format as well as the revisions can be viewed on the organizational website. It is also worth noting that there are various open-source software for seismic analysis that use the SEG-Y format, but most do not follow the exact specifications.

The Standard for the Exchange of Earthquake Data (SEED) format was designed for the ease and accuracy of the exchange of unprocessed seismic data between institutions and between instruments. Although it is primarily used for archiving seismic records, different versions of SEED, such as the miniSEED and dataless SEED, have been used for data analysis and processing. miniSEED contains only the waveform data, while the dataless SEED contains the information about the seismic instrument and station.

**Analog Devices System Design**

Changes in the traditional seismometer design are necessary for the rapid deployment and implementation of seismic networks, especially for urban and structural monitoring stations. Remote instruments need to comply with the current instrument guidelines so that the modern seismic signal measurements will conform and correlate to the established data standard. However, the cost and size of the implementation should be significantly smaller. The use of small-sized geophones and MEMS accelerometers as ground motion sensors coupled with a high performance ADC and digital signal processor (DSP) is a reasonable solution.

**Analog-to-Digital Converter (ADC) Considerations**

The primary design consideration of a data acquisition unit (DAU) for a DAS is the analog-to-digital converter (ADC). Traditionally, this was performed by a digital field system (DFS), which functions as a linear successive approximation register (SAR) ADC with an instantaneous floating-point (IFP) amplifier. Shown in Figure 8 is the block diagram of a traditional DFS.

The discrete implementation of the preamplifier (PA), low-cut (LC), high-pass filter, notch filter (NF), antialiasing (AA) high-pass filter, and the IFP amplifier will contribute to the system noise and add to the power consumption. The use of a multiplexer adds switching, cross-talk, and harmonic distortion. Most importantly, the quantization error due to the SAR ADC limits the dynamic range and resolution of the system. Thus, it is preferable to design a DAU using a different architecture with a different converter.

**Sigma-Delta (Σ-Δ) Converters**

The sigma-delta converter uses the change in the signal and adds it to the original. This reduces the quantization error inherent in SAR ADCs and can achieve higher resolutions and dynamic ranges. With modern sigma-delta ADCs, discrete implementations in the signal conditioning filters are no longer necessary. They feature extensive and configurable digital filters, which perform the functions of the traditional signal chain. This effectively lowers the system noise and design complexity. Furthermore, high-end precision sigma-delta ADCs are capable of simultaneous sensing of multiple channels with at least 24-bit resolution.

**Modern DAS Design Using Analog Devices Solutions**

A general block diagram for a low cost implementation of a seismic sensor node that is flexible for different applications is presented in Figure 9.
Low cost compact geophones sense only a single channel at a resonant frequency typically greater than 4.5 Hz and a sensitivity greater than 25 V/m/s. The homogenous triaxial arrangement allows for three similar single-channel geophones to be combined into a three-axis ground sensor. A period extender is required to extend the geophone bandwidth downward to achieve the standard instrument specification for broadband sensors. When designed for single-supply operation, the period extender also functions as a gain amplifier and sets the bias of the input signal to be at the center of the ADC range.

The inherent frequency response of MEMS accelerometers makes them vulnerable to offset drifts and high frequency noise. Band-pass filters improve the acceleration signal in the frequency range of interest to local seismology. Both the geophone period extender and the accelerometer band-pass filter require low noise, low offset voltage, and low input bias-current precision op amps such as the ADA4610-1.26

The power supply of the seismic sensor can be sourced from a wired dc power converter for installations with available power lines, such as in buildings and stations, or from a battery for remote and field installations. When sourcing from a wired dc power converter, low noise switching regulators and low noise, low dropout (LDO) regulators are suitable for the application. Analog Devices LDO regulators, such as the ADM717x series, offer high power supply rejection ratio (PSRR), low temperature drift, and low noise features.26 For battery-powered designs, a load efficient and low power charge controller and battery charger are required to sustain the operation of the instrument for long periods without maintenance. Moreover, it is better if the instrument is capable of energy harvesting from easily available sources such as solar and thermal power. The ADP5091 ultra low power energy harvester has maximum power point tracking and hysteresis modes, which ensure the highest possible efficiency in energy transfer.26 It has power path management features that can switch between the harvester, a rechargeable battery, or a primary cell battery, which makes it reliable for operating self-powered instruments.

The sigma-delta converter takes in three channel velocity signals from the period extender and another three channel acceleration signals if an analog output accelerometer is used. The design requires a converter with at least six input channels. Velocity and acceleration signals need to be sampled, if possible, simultaneously. For multichannel ADCs that switch between channels when sampling, the sampling rate would need to be higher. The maximum frequency of seismic signals of interest to earthquakes are at 100 Hz. The sampling frequency without aliasing for these signals should be at least 200 Hz or 5 ms per period. Each acceleration and velocity channel should be sampled with at least 1.2 kSPS sampling rate. The analysis of seismic signals promotes the oversampling of each channel. Therefore, the ADC should be chosen to have a sampling rate much higher than 1.2 kSPS. The AD7768 is an 8-channel, 24-bit sigma-delta ADC capable of simultaneous sampling, which removes the need for higher sampling rates.20 Its maximum sampling rate is 256 kSPS; however, it can scale down to low power mode up to 32 kSPS. It is flexible enough for different implementations and applications of this seismic instrument design and easily achieves the standard requirements for a Class A data acquisition unit.

The function of the low cost processor varies with the application. For remote nodes that use an external computing device for data analysis, the processor is a data logger that stores and packs the seismic data of all channels to the standard format (SEED or SEG-Y) and sends them to the computing device via a data interface. Since this application has a low processing requirement, it is possible to use a low power microcontroller. The ADuCCM4050 is an ultra low power ARM® Cortex®-M4 microcontroller recommended for IoT applications.21 It has low power modes at 650 nA for hibernate mode and 200 nA for a fast wake-up shutdown mode. Additionally, it has two real-time clock (RTC) peripherals for time-keeping and time-synchronized data sampling.

For standalone instruments with built-in data analysis, a DSP computes for seismic features and other parameters dependent on the application, such as building health indicators for structural health monitoring. Seismic data analysis requires the calculation of various mathematical and statistical functions. For example, the computation of seismic intensity requires logarithmic functions and a peak detection window for acceleration and velocity. Furthermore, the processing time should be low enough to perform continuous data sampling and processing. The ADSP-BF706 is a low cost, low power DSP with up to 400 MHz processing speed and is an industry leading choice of DSP for field instrument applications.22 It offers multiple glueless peripheral interfaces, which makes it easier to connect to external devices such as the data interface and ADC.

The instrument’s location data may either be extracted from a GPS module or manually set during installation. For the time data, the low cost DSP can use either its internal RTC peripheral or via NTP through the data interface. There are multiple options for the data interface depending on the type of installation. The instrument may use industrial RS-485 for wired communications, especially inside buildings, or an Ethernet interface to easily connect the device to an existing data network. For wireless communications, the instrument may use Wi-Fi devices or the Analog Devices SmartMesh® IP for full data reliability in dynamic environments.

Applications

The reliability of seismic data increases as the number of seismic sensors deployed at various locations increases. There is a lot of information that can be extracted from seismic data that is useful for a wide range of applications such as structural health monitoring, geophysical research, oil exploration, and even industrial and household safety. This section discusses general overviews of the three common applications of seismic sensor networks.

Remote Seismic Networks

Volcanology and seismology research deploy seismic sensors in difficult and sometimes dangerous terrain.34 Monitoring internal processes inside volcanoes requires ground motion to be monitored at multiple points. These locations may become dangerous after certain phases of volcanic activity, and render the seismic sensor to be irretrievable. Low cost, low power seismic sensors will decrease research cost and at the same time remain active for very long periods. Another similar case is the characterization of plate movement, which also requires a lot of seismic sensors deployed along the fault line.
Earthquake Early Warning System

S-waves and surface waves, which are the more destructive types of seismic waves that are part of an earthquake, propagate slower than the least destructive P-wave. Therefore, it is feasible to implement an earthquake early warning system by detecting the early signs of occurrence. This would give all types of systems a short moment to act and prevent devastating effects due to earthquake damage. Residential and commercial buildings will be able to shut off electrical systems and gas pipelines moments before intense ground shaking occurs. Using a seismic sensor network deployed at several locations around a protected area, help to increase the allowed reaction time. Also, false alarms caused by non-earthquake sources will be minimized. Figure 10 shows a possible setup for an earthquake early warning system protecting a specific area or structure.

The response time allowed by an early warning system is proportional to the radial distance of the seismic sensor from the protected structure, as described by Equation 5. Given that P-waves travel at 3.5 mi/s or 5.6 km/s and S-waves travel at 2.0 mi/s or 3.2 km/s, it can be calculated that one second of response time is added for every 7.51 km distance of the seismic sensor from the protected area. Furthermore, placing multiple seismic sensors at shorter intervals will provide more timing resolution for the response time.

Equation 5 demonstrates the relationship of early warning system response time and radial distance of seismic sensor from the protected area.

\[ t_{\text{response}} \times (7.51 \, \text{km/s}) = d_{\text{radial}} \]

where:

- \( t_{\text{response}} \) = Allowed Response Time in Seconds
- \( d_{\text{radial}} \) = Radial Distance of Seismic Sensor from the Protected Area

Structural Health Monitoring

Earthquake safety of buildings can be improved by monitoring and modeling its response through forced vibration testing. Installing seismic sensors in building will help in post-earthquake damage assessment, response, and recovery. In cases of widespread damage, a widespread seismic sensor network can locate structurally damaged areas, thereby decreasing the risk and cost of visual inspection. A research on strong motion instrumentation applied this to the Atwood building, a 20-story steel MRF building, using 32 accelerometer-based seismic sensors deployed on 10 levels to accurately monitor the structural health of the building.

Conclusion

Seismic sensor networks have a wide range of applications in industrial technology, seismological research, and structural health monitoring. The application demand has changed the sensor and system requirements of seismometers to favor remote systems and low operational costs. Modern, low cost ground sensing technology is now capable of measurements that are on par with traditional instruments. Using the wide range of Analog Devices products, a sensing device can be implemented to cater different seismic sensing applications.
References


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ADI ToF Depth Sensing Technology: New and Emerging Applications in Industrial, Automotive Markets, and More

Colm Slattery, Marketing Manager and Yuzo Shida, Product Marketing Manager

Time-of-flight (ToF) cameras have gained attention as the depth sensing method of choice for their smaller form factor, wide dynamic range of sensing, and their ability to operate in a variety of environments. Though ToF technology has been used for years in the scientific and military fields, it has become more prevalent starting in the early 2000s with advances in image sensing technology. This evolution in performance means that technologies such as ADI’s ToF technology will become more ubiquitously deployed beyond the consumer market, where it is currently being designed into smartphones, consumer devices, and gaming devices. As the technology matures, there will be opportunities to further leverage mainstream manufacturing processes to increase system efficiencies in the design, manufacturing, and transport of goods.

Logistics, quality inspection, navigation, robotics, facial recognition, security, surveillance, safety, healthcare, and driver monitoring are all application use cases that can leverage 3D depth sensing ToF technology to solve many problems that traditional 2D technology struggles with today. Combining high resolution depth data with powerful classification algorithms and AI will uncover new applications.

This article will examine the basics of, and the two dominant methods for, ToF depth sensing, as well as compare it to other prevalent depth sensing technologies. It will then provide a detailed introduction to ADI’s 3D depth sensing ToF technology—leveraging the ADDI9036 analog front end, a complete ToF signal processing device that integrates a depth processor that processes the raw image data from a VGA CCD sensor into depth/pixel data. We will also discuss how ADI can scale this technology to our broad market customer base through an ecosystem of hardware partners.

Figure 1. Time of flight (ToF): a technology to detect the distance to an object.
Basic Theory of Operation

A ToF camera measures distance by actively illuminating an object with a modulated light source (such as a laser or an LED), and a sensor that is sensitive to the laser’s wavelength captures the reflected light (Figure 2). The sensor measures the time delay $\Delta T$ between when the light is emitted and when the reflected light is received by the camera. The time delay is proportional to twice the distance between the camera and the object (round-trip); therefore the depth can be estimated as:

$$d = \frac{c \Delta T}{2}$$  \hspace{1cm} (1)

where $c$ is the speed of light. The goal of a ToF camera is to estimate the delay between the emitted signal and the return signal.

There are different methods for measuring $\Delta T$, of which two have become the most prevalent: the continuous-wave (CW) method and the pulse-based method.

Continuous-Wave Method

In the CW method, a periodic modulated signal is used for the active illumination (Figure 3), and the phase shift of the reflected light is measured by homodyne demodulation of the received signal.

For example, a sinusoidal modulation can be used, where the emitted signal is:

$$s(t) = A_s \cos(2\pi f_{mod} t) + B_s$$  \hspace{1cm} (2)

where

- $A_s$ is the amplitude of the signal
- $B_s$ is the offset of the signal
- $f_{mod}$ is the modulation frequency, $1/T_{mod}$, where $T_{mod}$ is the modulation period.

The received signal $r(t)$ is a delayed and attenuated version of the emitted signal:

$$r(t) = \alpha s(t - \Delta T)$$  \hspace{1cm} (3)

$0 \leq \alpha < 1$ is an attenuation coefficient that depends on the distance and the surface reflectivity, and $\Delta T$ is the delay of the return signal.

Continuous-wave time-of-flight sensors measure the distance at each pixel by sampling the correlation function between the received signal $r(t)$ and a demodulating signal $g(t)$ with the same frequency as $s(t)$. In the ideal case, the demodulating signal is also a sine wave:

$$g(t) = A_g \cos(2\pi f_{mod} t) + B_g$$  \hspace{1cm} (4)

The operation performed by the pixel is a correlation operation:

$$c(\tau) = \int_{0}^{T_{mod}} r(t)g(t - \tau)dt$$  \hspace{1cm} (5)

When both the emitted signal and the demodulating signal are sine waves, the correlation value as a function of the delay $\tau$ applied to the demodulating signal is:

$$c(\tau) = A \cos(2\pi f_{mod}(\Delta T - \tau)) + B$$  \hspace{1cm} (6)

where $A = A_g A_s \alpha$ and $B = A_B g B_s$.

The correlation function $c(\tau)$ is then sampled at four equal steps over one period (by changing the illumination phase shift in steps of 90°), as shown in Equation 3. The phase offset $\Phi = 2\pi f_{mod} \Delta T$ between the emitted signal and the demodulating signal can be estimated using Equation 7:

$$\Phi = \text{atan}\left(\frac{c(\frac{3T_{mod}}{4}) - c(\frac{T_{mod}}{4})}{c(0) - c(\frac{T_{mod}}{2})}\right)$$  \hspace{1cm} (7)

and the depth, which is proportional to the phase shift is:

$$d = \frac{c_4 \pi f_{mod} \Phi}{2\pi}$$  \hspace{1cm} (8)
Pulse-Based Method

In the pulse-based method, an illumination source emits a series of \( N \) short light pulses, which are reflected back to a sensor equipped with an electronic shutter that enables the capture of light in a series of short temporal windows. In Figure 5, three shutter windows, or pulses, are used to capture the reflected light pulse. The BG window captures the ambient light, which is then subtracted from the other measurements.

The ToF \( \Delta T \) is estimated from the measured values corresponding to the different shutter windows according to the following equation:

\[
\Delta T = \frac{S_1 - BG}{S_0 + S_1 - 2 \times BG}
\]

The distance can then be calculated by replacing \( \Delta T \) with the expression in Equation 9 in Equation 1, which gives us Equation 10.

\[
d = \frac{S_1 - BG}{S_0 + S_1 - 2 \times BG} \times \frac{c}{2}
\]

It should be noted that these equations are predicated on the assumption that the pulses are perfect rectangular pulses, which is impossible, considering the limitations of the hardware. Additionally, in practical situations, several hundred to several thousand illumination pulses need to be accumulated in order to get a sufficient signal-to-noise ratio (SNR) for measurement.

Advantages/Disadvantages of the CW and Pulsed ToF Technology Systems

Both approaches to ToF have their advantages and disadvantages relative to the application’s use case. Issues such as the distances being measured, the environment in which the system is being used, accuracy requirements, thermal/power dissipation restrictions, form factor, and power supply issues need to be considered. It should be noted that the vast majority of CW ToF systems that have been implemented and are currently on the market use CMOS sensors, while pulsed ToF systems use non-CMOS sensors (notably CCDs). For this reason, the advantages/disadvantages listed as follows will be based on those assumptions:

Advantages of Continuous-Wave Systems:

- For applications that do not have high precision requirements, a CW system may be easier to implement than a pulse-based system in that the light source does not have to be extremely short, with fast rising/falling edges, though it is difficult to reproduce a perfect sinusoidal wave in practice. However, if precision requirements become more stringent, higher frequency modulation signals will become necessary and may be difficult to implement in practice.
- Due to the periodicity of the illumination signal, any phase measurement from a CW system measurement will wrap around every \( 2\pi \), meaning that there will be an aliasing distance. For a system with only one modulation frequency, the aliasing distance will also be the maximum measurable distance. To counteract this limitation, multiple modulation frequencies can be used to perform phase unwrapping, wherein the true distance of an object can be determined if two (or more) phase measurements with different modulation frequencies agree on the estimated distance. This multiple modulation frequency scheme can also be useful in reducing multipath error, which occurs when the reflected light from an object hits another object (or reflects internally within the lens) before returning to the sensor, resulting in measurement errors.
- As in all CMOS imager systems, standard power supply rails (+5 V, +3.3 V, +1.2 V) can be used, unlike CCDs which may require higher negative (–9 V) and positive (+14 V) supply rails.
- Depending on their configuration, CMOS ToF imagers tend to have more flexibility and faster readout speed, so functions such as region-of-interest (RoI) output are possible.
- Calibrating a CW ToF system over temperature may be easier than that of a pulsed ToF system. As the temperature of a system increases, the demodulation signal and the illumination will shift with respect to each other because of the temperature variation, but this shift will only affect the measured distance with an offset error that is constant over the entire range, with the depth linearity remaining essentially stable.

Disadvantages of Continuous-Wave Systems:

- Though CMOS sensors have higher output data rates compared to that of other sensors, CW sensors require four samples of the correlation function at multiple modulation frequencies, as well as multiframe processing, to calculate depth. The longer exposure time can potentially limit the overall frame rate of the system, or can cause motion blur, which can limit its use to certain types of applications. This higher processing complexity can necessitate an external application processor, which may be beyond the application’s requirements.
- For longer distance measurements or environments with high levels of ambient light, higher continuous optical power (compared to that of pulsed ToF) will become necessary; this continuous illumination from the laser could cause thermal and reliability issues.
Advantages of Pulse-Based ToF Technology Systems:

- Pulse-based ToF technology systems often rely on high energy light pulses emitted in very short bursts during a short integration window. This offers the following advantages:
  - It makes it easier to design a system that is robust to ambient light, therefore more conducive to outdoor applications.
  - The shorter exposure time minimizes the effect of motion blur.
- The duty cycle of the illumination in a pulse-based ToF system is generally much lower than that of a comparable CW system, thereby offering the following benefits:
  - It lowers the overall power dissipation of the system in longer range applications.
  - It avoids interference from other pulsed ToF systems by placing the pulse bursts in a different location in the frame from that of the other systems. This can be done by coordinating the placement of the pulses in the frame of the various systems or by using an external photodetector to determine the location of the other system’s pulses. Another method is to dynamically randomize the location of the pulse bursts, which will eliminate the need to coordinate the timing between the various systems, but it will not completely eliminate the interference.
- Since the pulse timing and width do not need to be uniform, different timing schemes can be implemented to enable functions such as wider dynamic range and auto-exposure.

Disadvantages of Pulse-Based ToF Technology Systems:

- Since the pulse width of the transmitted light pulse and the shutter need to be the same, the timing control of the system needs to be highly precise, and a picosecond level of precision may be required depending on the application.
- For maximum efficiency, the illumination pulse width needs to be very short, but with very high power. For this reason, very fast rising/falling edges (<1 ns) are required from the laser driver.
- Temperature calibration may be more complicated, compared to that of CW systems since a variation in temperature will affect individual pulse widths, affecting not only the offset and gain, but also its linearity.
- As previously indicated, the majority of the pulsed systems do not use CMOS sensors. As such:
  - Pulsed ToF systems will almost always require an external analog front end that can digitize and output the depth data (though the CW system may also require an external processor, depending on the complexity of the back-end processing).
  - The system configuration—especially the power supply requirements of the ToF sensor—will require more components and power supply rails.

Other Depth Sensing Technologies

It is instructive to be familiar with other depth mapping technologies to understand the trade-offs; as previously mentioned, all depth detection systems have advantages and disadvantages depending on the use case and the application requirement.

Stereo Vision

Stereo vision for depth sensing works by using more than one camera separated by a certain amount of distance from one another (Figure 6). Like the human eye, a given reference point in space will be in separate positions in each camera, allowing the system to calculate that point’s position in space if the correspondence of that point is made between the two cameras. Determination of this correspondence involves computationally intense and complex algorithms.

Advantages

- No active illumination is needed.
- Generally cheaper because it only involves two cameras to acquire the data (though a sophisticated application processor may be required to find the corresponding point and develop a 3D image).

Disadvantages

- If there is no contrast to make the corresponding point between the two cameras, distance cannot be calculated. This is especially prevalent in white walls, where there is no contrast between what the two cameras are seeing, and in environments where there is insufficient ambient light.
- At longer distances, the two cameras need to be located farther apart in order for the corresponding point to be positioned in different locations in the two cameras. This has obvious form factor issues for applications that require the measurement of longer distances.

Structured Light

The structured light method works by projecting a known reference pattern of dots onto an object. The 3D object distorts this reference pattern, and a 2D camera captures this distortion. This distortion is then compared to the reference pattern that was projected, and then calculates a depth map based on the distortion level.
Advantages
- Able to achieve very high spatial resolution as well as very high accuracy at close distances (<2 m).

Disadvantages
- Several projections are necessary to extract one frame of information that may lead to slower frame rates, which makes it difficult to extract distance information from moving objects.
- At longer depth ranges, the camera would need to have its illumination source far from the lens, since the distortion of the pattern may not be discernible if the illumination source is near. This would not be practical to implement in an application that requires a small form factor. For this reason, structured light systems are not commonly used in depth measurement applications longer than 2 m.
- Outdoor ambient light may also interfere with the distorted pattern, which is the reason why it is better suited for indoor applications.

ADI Depth Sensing (ToF) Technology
ADI’s ToF technology is a pulse-based ToF CCD system (Figure 8) that utilizes a high performance ToF CCD and the ADDI9036, a complete ToF signal processing device that integrates a 12-bit ADC, the depth processor (that processes the raw image data from the CCD into depth/pixel data), as well as a high precision clock generator that generates the timing for both the CCD and the laser. The precision timing core of the timing generator allows the adjustment of clocks and LD output with approximately 174 ps resolution at a clock frequency of 45 MHz.

ADI’s ToF system differentiates itself from other solutions by:
- Utilizing a ToF sensor that is 640 × 480 resolution, which is a 4× higher resolution than most other ToF solutions in the market.
- Using a sensor that has high sensitivity to light at the wavelength of 940 nm. As previously mentioned, ambient light will significantly reduce the SNR of a reflected signal, especially in very high ambient light conditions. 940 nm lasers have become prevalent since this wavelength occupies a space in the spectrum of sunlight where the magnitude of the photon flux is relatively low (Figure 9). The ADI ToF system uses a ToF CCD that is sensitive to 940 nm light, allowing it to capture more data in outdoor environments or areas with strong ambient light.

A pseudo-randomization algorithm combined with special image processing integrated in the depth processor enables interference cancellation (as previously mentioned). This enables multiple ToF systems to operate in the same environment.

Figure 10 shows an example where three different depth measurement systems were used outdoors to measure distance. Note that while a CMOS ToF system that used an 850 nm light source has difficulty distinguishing both the person and the tripod, the ToF CCD system was able to distinguish both more clearly.
Which Applications Are Leveraging ToF Technology?

As mentioned in the introduction, the addition of depth information to a 2D image allows useful information to be extracted and can greatly improve the quality of scene information. For example, 2D sensing cannot distinguish between a real person and a photograph. Extracting depth information allows better classification of people, tracking both their facial and body features. ToF depth sensing can provide high quality and reliable face recognition for security authentication. The higher the resolution and depth accuracy, the better the classification algorithm. This can be used for simple functions such as allowing access to mobile devices/our personal home space, or for high end use cases such as secure door access control in commercially sensitive areas.

![Image](image1.jpg)

Figure 11. Digital face recognition.

As depth sensing technologies achieve higher resolutions and depth accuracies, the classification and tracking of people will become easier. The use of artificial intelligence will allow for classification with very high confidence, which in turn will create new and emerging application areas. One use case is for a commercial automatic door opening function, especially in areas of strong sunlight. Ensuring a door only opens for a person and not anything else can provide efficiencies in building management, as well as in security and safety.

![Image](image2.jpg)

Figure 12. People classification for automatic door opening.

As 3D algorithms mature further, data analytics will be leveraged to gather lots of meaningful information about people’s behavior. The first wave of this is likely to happen in building control applications such as door entry/exit systems for people-counting. The addition of depth information from a vertically mounted sensor means that people can be counted with very high accuracy. Another use case is a smart automatic door opening (Figure 13) where people can be classified and the door only opens when a real person is detected. ADI is developing software algorithms in the area of people-counting and classification.

![Image](image3.jpg)

Figure 13. People-tracking algorithm using depth sensing technology.

Depth information allows high accuracy classification of people under many challenging conditions, such as environments with low or no ambient light, in areas where there is a significant density of people, and where people are well camouflaged (for example, with hats, scarves, etc.). Most importantly, the false triggering of people-counting is virtually eliminated. Today, stereo cameras can be used for entry/exit detection, but due to the limitations of mechanical size (two sensors) and high processor needs, stereo tends to be expensive and of a large form factor. As the ADI ToF technology directly outputs a depth map and only has one sensor, both the form factor and processing needs are much reduced.

As 3D algorithms mature further, data analytics will be leveraged to gather lots of meaningful information about people’s behavior. The first wave of this is likely to happen in building control applications such as door entry/exit systems for people-counting. The addition of depth information from a vertically mounted sensor means that people can be counted with very high accuracy. Another use case is a smart automatic door opening (Figure 13) where people can be classified and the door only opens when a real person is detected. ADI is developing software algorithms in the area of people-counting and classification.

![Image](image4.jpg)

Figure 14. 3D dimensioning.

An important application of depth sensing will be in the industrial, manufacturing, and construction process. The ability to accurately dimension and classify objects in real time through a production process is not trivial. Accurate depth sensing can determine space utilization of warehouse bays. Products that come off a production line need to be dimensioned quickly for transfer. High resolution depth sensing will allow edges and lines of target objects to be determined in real time, and fast volume calculations made. A neural network approach is already being used in such volume determination.
The autonomous transfer of product within a factory continues to increase. Autonomous vehicles like autonomous guided vehicles (AGVs) will need to self-navigate faster through the factory and warehouse. High accuracy depth sensing technology will allow sensors to map out their environment in real time, localize themselves within that map, and then plot the most efficient navigation path. One of the biggest challenges with the deployment of such technology in factory automation is the interference from other sensors that may operate in the same area. ADI’s interference cancellation IP will allow many such sensors to operate directly in each other’s line of sight without affecting the performance.

How Can I Evaluate, Prototype, and Design with ToF Technology?

ADI has developed an optical sensor board (AD-96TOF1-EBZ) that is compatible with the Arrow 96 application processor platform. This 96TOF1 board’s optical specifications are listed in Table 1.

### Table 1. ADI’s 96TOF Optical Board Specifications

<table>
<thead>
<tr>
<th>Range</th>
<th>&lt;6 m</th>
</tr>
</thead>
<tbody>
<tr>
<td>FOV</td>
<td>90° × 69.2°</td>
</tr>
<tr>
<td>Wavelength</td>
<td>940 nm</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>30 fps maz</td>
</tr>
<tr>
<td>Resolution</td>
<td>640 × 480 pixels</td>
</tr>
</tbody>
</table>

This board can interface directly to Arrow’s 96Boards family. The 96Boards family is a range of hardware processor platforms that make the latest ARM®-based processors available to developers at a reasonable cost. Boards produced to the 96Boards specifications are suitable for rapid prototyping, Qualcomm® Snapdragon™, and NXP and NVIDIA® processors are all supported within the 96Boards platform.

ToF depth sensing is a complex technology. There is significant optical expertise needed to achieve the highest performance of the VGA sensor. Optical calibration, high speed pulse timing patterns, temperature drifts, and compensation will all affect depth accuracy. Design cycles can be long to achieve the desired performance. While ADI can support chip-down designs for qualified customer opportunities, many customers are looking for an easier, faster, and more efficient approach to get to market.

Many customers are interested in a simple demonstration module to first evaluate the performance of the technology, before moving forward with a real project. ADI has worked with various hardware partners to provide different levels of hardware offerings. The DCAM710 demonstration module, offered by one of our hardware partners (Pico) supports USB depth image streaming directly to a PC.

### DCAM710 Module Specifications

The specifications of the ToF camera DCAM710 module are:
- Based on ADI’s ToF signal chain products and technology
- Can output depth map and (710 version) ToF + RGB image (can disable)
- FOV: 70 × 54
- Depth camera support image size: up to 640 × 480 at 30 FPS
- RGB camera support image size: up to 1920 × 1080 at 30 FPS
- USB 2.0 interface
- Support OS: runs on Android®, Linux®, and Windows® 7/8/10
- Pico depth sensor SDK, sample code and tools (OpenNI SDK compatible)
- Sample application algorithms available from ADI in Python®

The Pico SDK software platform can support Windows and Linux operating systems and supports several software functions. A point cloud, which can generate a set of data points in space around an object, and which are often used to generate 3D models, is easily generated through the SDK.
ADI provides simple sample code in Python to support customer evaluations. The example below shows a screen shot of real-time Python source code being used to detect and classify a person, and then apply a depth measurement to determine where the person is relative to the sensor. Other algorithms that are available include edge detection, object tracking, and a 3D safety curtain.

![Image of people classification and range detection](image)

**Figure 20. People classification and range detection.**

**How Do I Go to Production with ToF?**

While the ADI 96TOF reference design is useful for customers doing a chip-down design and the DCAM710 demonstration platform is a cost efficient way to evaluate the technology, in many cases, customers may need a different or more customized solution when they go to production. For example, in AGV systems, a GigE or Ethernet output from an edge node sensing module is often desirable. This gives a robust method of sending high speed, raw depth data from an edge node sensing module to a centralized CPU/GPU controller.

In other applications, customers may want to implement some edge node processing and only send metadata back to the controller. In this case, having a small form factor depth node module with an integrated edge node processor supporting ARM or an FPGA is more desirable. ADI has developed a set of third-party ecosystem partners that can meet all customers’ requirements.

These third parties offer a range of capabilities, from complete camera products to small optical modules without external housing that can be integrated into bigger systems. The diagram below shows a tiny MIPI module without external housing that can easily be mechanically integrated into bigger systems. ADI’s partner network can also offer customization of hardware, optics, and application processors if needed. An example of the modules our partners offer today are USB, Ethernet, Wi-Fi, and MIPI, with a range of integrated edge node processors available.

Both ADI and our hardware partners also work with external software partners who bring algorithm expertise in depth processing at the application level.

![Image of depth sensing in industrial AGVs (navigation/collision avoidance)](image)

**Figure 21. Depth sensing in industrial AGVs (navigation/collision avoidance).**

**Conclusion**

The advantages of high resolution depth imaging to solve difficult and complex tasks in new and emerging application areas are forcing our customers to quickly drive its adoption. The fastest, lowest risk, and cheapest path to get to market is through affordable, small form factor, high precision modules that can be integrated into larger systems. ADI’s 96TOF reference design platform provides a complete embedded evaluation platform, enabling customers to immediately evaluate the technology and start developing application code. Please contact ADI for more information about ADI’s ToF technology, hardware, or our hardware partners.

**About the Author**

Colm Slattery graduated from the University of Limerick with a bachelor of electronics engineering degree. He joined ADI in 1998 and has held various roles including test development and product and system applications. Colm has also spent three years on assignment in a field role in China. Colm is currently a marketing manager in the Industrial Business Unit, focusing on new sensor technologies and new business models. He can be reached at colm.slattery@analog.com.

Yuzo Shida is a product marketing manager for ToF products in the Healthcare, Consumer, and Industrial Group at Analog Devices. After graduating from the University of Illinois Urbana-Champaign with an EE degree in 1990, Yuzo joined ADI, where he has been involved in the product and business development of a variety of consumer, automotive, and industrial products. He can be reached at yuzo.shida@analog.com.
Get Up and Running with LTspice

Gabino Alonso, Director of Strategic Marketing

The key to most circuit designs is the speed with which you can reach an understanding of your circuit, its correctness, and its limitations, so that you can refine your design and select components before going into the lab to prototype and test. LTspice® is Analog Devices’ high performance circuit simulation program, which allows you to draft, probe, and analyze the performance of your circuit design. LTspice contains an integrated schematic editor, waveform viewer, and advanced features that are easy to use once you learn some basic commands.

LTspice includes an extensive library of macromodels covering most of ADI’s power management and signal chain products, as well as a library of passive components. LTspice uses proprietary modeling techniques for its macromodels, resulting in fast, accurate simulation results. This is especially important for switch-mode power supply designs, an area where LTspice outperforms many other simulation tools and enables you to iterate your designs in minimal time. Successive simulations allow you to explore the circuit limitations and performance boundaries of your design through minor adjustments, helping to develop your circuit intuition.

LTspice is provided at no cost to our customers and to the engineering community. Do not let its free status dissuade you; it outperforms many simulation solutions in the market and is not hobbled by any arbitrary limits. Consequently, you can create, encapsulate, and abstract complex circuits with confidence that circuit size and hierarchy are only limited by your computer’s resources and your time.

Software Installation and Updates

LTspice software runs on Windows® and Mac® OS X operating systems. Downloadable installation files for LTspice are available at analog.com/LTspice. To keep your software updated with the latest models, software, and examples, it is important to synchronize your release of LTspice. Sync Release is available under the LTspice Tools menu (Figure 1).

Use an Existing Circuit

Drafting a circuit from scratch can be a daunting task when using a new tool. Instead of starting with a blank slate, it is far better to familiarize yourself with LTspice by exploring an existing schematic and reviewing its performance in a simulation. LTspice schematic files are saved with an .asc extension. There are three main sources of LTspice schematics:

- Demonstration circuits available from LTspice.
- Test fixtures installed with LTspice.
- Educational examples installed with LTspice.

Download a Demo Circuit

If you are interested in a specific solution, look through ADI’s extensive collection of LTspice examples in the Demo Circuits section. These examples can also be found through product and evaluation board webpages under Tools & Simulations. Demo circuits are reviewed by applications engineering and provide a solid starting point for most designs. Many are based on available hardware evaluation boards.

To Use an LTspice Demo Circuit:

Find the demo circuit through a product web page or by searching the Demo Circuit database for a part or application. Download the demo circuit .asc file to your local directory and open it.
If you cannot find a demo circuit for the product you are interested in, there is a test fixture that can act as a starting point for your design.

## Grab a Test Fixture

Most of Analog Devices’ power management and signal chain products that are modeled in LTspice have an associated predrafted test fixture available. These test fixtures, called jigs, are used by the ADI modeling teams for testing and evaluating device macromodels, and are offered as drafting starting points. Note that test fixtures are not recommended for production use. They have not necessarily been reviewed by factory applications engineers, and many are simplified; they use ideal passive components or they are focused on evaluating how the macromodel handles specific fault conditions. Nevertheless, as a starting point, test fixtures are often better than a blank slate.

### To Open a Jig File for a Device or Component:

- Open LTspice.
- Choose **File > New Schematic** or press **CTRL + N**. A blank schematic will appear.
- Choose **Edit > Component** or press **F2**. The component dialogue will appear.

### Start with an Educational Example

LTspice includes educational examples designed to help you explore simulations and circuit design. Educational examples are installed along with LTspice, located in `C:\Program Files\LTC\LTspiceXVII\examples\Educational`.

### Using the Schematic Editor

LTspice is designed to expedite schematic drafting, but all schematic editors have a learning curve. With LTspice, once you learn the basic menu and the shortcut keys, it is very easy to draft and edit your schematics. All schematic editing commands and components are available under the **Edit** menu or by right-clicking the schematic background.

Drafting a circuit from scratch using the schematic editor is not covered here, but is well documented. Available instructional videos are a good way to learn the basics of drafting a circuit from scratch in LTspice with a few listed in the Additional Resources section at the end of this article.

### Editing Component Attributes

In most cases, to modify an object’s attributes, right-click the object. Depending on the circuit element, an editor window will appear, where you can change component parameters.

---

**Figure 3.** Search the device you want by typing its name in the text field.

**Figure 4.** Schematic of a macromodel’s test fixture.

**Figure 5.** Educational examples are installed with LTspice.

**Figure 6.** Resistor component parameters.

Resistors, capacitors, inductors, beads, diodes, bipolar transistors, MOSFET transistors, and JFET transistor circuit components have an associated database of models from which to choose. This extensive library of models for passive components can be leveraged to quickly build or modify a schematic using realistic components. If you cannot find the exact model of a device, you can use a similarly specified model instead and later add a model of the specific device of interest to the component database.
Figure 7. Selecting a component from the library.

Some components feature advanced options. For instance, the voltage source’s basic attributes are shown in Figure 8.

Figure 8. Standard parameters for a voltage source.

Click Advanced to access the voltage source’s additional parametric options, as shown in Figure 9.

Figure 9. Advanced parametric options for a voltage source.

**Entering Units**

When you enter a parametric value in option field, LTspice follows standard notation with the exception of using MEG (or meg) to specify $10^6$. Capital M is used by LTspice as an alternative to m for $10^{-3}$ (milli). See Table 1. Be careful when typing 1F for 1 farad as it incorrectly indicates $1 \text{femtofarad}$. For 1 farad, just enter 1.

Table 1. Standard Unit Prefixes in LTspice

<table>
<thead>
<tr>
<th>Character</th>
<th>What It Means</th>
</tr>
</thead>
<tbody>
<tr>
<td>T or t</td>
<td>tera = $10^{12}$</td>
</tr>
<tr>
<td>G or g</td>
<td>giga = $10^9$</td>
</tr>
<tr>
<td>MEG or meg</td>
<td>Meg = $10^6$</td>
</tr>
<tr>
<td>K or k</td>
<td>kilo = $10^3$</td>
</tr>
<tr>
<td>M or m</td>
<td>milli = $10^{-3}$</td>
</tr>
<tr>
<td>U or u (LTspice replaces with µ)</td>
<td>micro = $10^{-6}$</td>
</tr>
<tr>
<td>N or n</td>
<td>nano = $10^{-9}$</td>
</tr>
<tr>
<td>P or p</td>
<td>pico = $10^{-12}$</td>
</tr>
<tr>
<td>F or f</td>
<td>femto = $10^{-15}$</td>
</tr>
</tbody>
</table>

**Navigate the Schematic**

To navigate the schematic editor, use the mouse and scroll wheel to pan, zoom in, and zoom out in your schematic or use the options under the View menu. Click and drag a schematic to pan. Press the space bar to jump back to a full screen view.

**Add Simulation Commands**

Simulation commands for demo circuits, jigs, and educational example files are already defined so that you can run the simulation with no additional editing. LTspice includes simulation commands for transient, linearized small signal ac, dc sweep, noise, dc operating point, and small signal dc transfer function analysis.

**To Insert or Edit a Simulation Command:**

Choose Edit Simulation Cmd from the Simulate menu. The Edit Simulation Command dialogue will appear (Figure 10). It includes tabs for each analysis and fields for the associated parameters. More information on these different types of analyses is available in the F1 help files, which can be accessed by pressing F1.

Figure 10. Editing a simulation.

**Run the Simulation**

Once you have selected or drafted a schematic, choose Run from the Simulate menu. This generates a netlist file from the schematic editor using the same file name, but with the .net extension. LTspice simulates this netlist. **To view the contents of a netlist, choose SPICE Netlist from the View menu.**
View Waveforms

Probing Your Schematic
To analyze your circuit, after executing the run command, you can use the cursor to probe the schematic directly or use the Add Trace (or Visible Trace) command under the Plot Settings. This results in the trace appearing in the waveform viewer.

To Plot Ground-Referenced Voltage:
Place the cursor on the wire or node of interest. The cursor image will change to a red voltage probe. Click the wire or node of interest. The voltage displayed is referenced to ground.

Figure 11. Voltage probe cursor.

Figure 12. Measurement with a voltage probe.

To Plot a Differential Voltage:
With the probe cursor showing, click and hold on the wire or node of interest and drag the cursor to the wire or node to which you want it referenced. Initially, the probe cursor will be red, but as you drag to it to a referenced voltage, it will change to black.

Release the mouse button. The differential voltage will appear.

Figure 13. Differential voltage measurement.

Navigate the Waveform Viewer

Zooming in the Waveform
In the waveform window, you can use the mouse to zoom in. To zoom into a specific region of the waveform window, drag a box around the region you wish to draw larger (Figure 17).

Figure 16. Zooming in the waveform viewer.

To Plot a Current
To plot the current through a component with 2-wire connections:

- Move the cursor over the body of the component.
- The cursor image will change to a current probe (Figure 14).
- Click the body of the component.

To plot the current into a pin of a component with more than two connection points:

- Place the cursor over the pin of interest.
- The cursor image will change to a current probe.
- Click the pin of interest.

Figure 14. Current probe cursor.

Figure 15. Measurement with a current probe.
Taking Quick Measurements
If you draw a box around an area of interest and hold the mouse button down, the size of the box (in the x and y units) is displayed on the lower left corner of the waveform viewer. This enables quick measurements. Minimize the box before releasing the mouse button to prevent zooming in.

Deleting Traces
To delete individual traces from the waveform viewer, right-click the label of the trace at the top of the waveform viewer that you want to delete and select Delete this Trace. Alternatively, you can click the waveform viewer to make sure it is the active window, and choose Delete Traces from the Plot Settings menu (or press F5). The cursor changes to an image of scissors. At the top of the waveform viewer, click the labels of any traces you want removed. Right-click or press Esc to end the delete function.

If you only want to focus on one trace, double-click the wire, node, component, or pin, and all other traces from the waveform viewer will be removed.

You can explore the additional features of the waveform viewer by clicking on the window to make it active and reviewing the options under the Plot Settings menu or by right-clicking the waveform viewer.

Additional Features
LTspice also features other advanced simulations including steady state detection, turn-on transient response, step response, efficiency/power computations, and other advanced analysis options. To learn more about the waveform viewer and/or advanced simulation techniques, please see the following Additional Resources section.

Figure 17. Taking a quick measurement.

About the Author
Gabino Alonso is currently the director of strategic marketing for the Power by Linear™ Group. Prior to joining ADI, Gabino held various positions in marketing, engineering, operations and education at Linear Technology, Texas Instruments, and California Polytechnic State University. He holds a Master of Science degree in electrical and computer engineering from University of California, Santa Barbara. He can be reached at gabino.alonso@analog.com.

Additional Resources
To learn more about LTspice, visit analog.com/LTspice for technical articles and videos. The following classic videos provide additional foundational learning on using a schematic editor and a waveform viewer.

Schematic Editor
Waveform Viewer
For all general LTspice questions, refer to the help file (press F1) for more details or one of the many online LTspice forums such as EngineerZone® or one of the many LTspice user groups, which provide discussion threads, tutorials, and simulation examples to explore. If you encounter a software bug or device model issues, please email LTspice@analog.com. However, if you have a specific question with regard to a simulation using an ADI device in your application, it would be best to reach out directly to your local field applications engineer for support.

Happy simulations!

References
RAQ Issue 172: Manipulating MCU SPI Interface to Access a Nonstandard SPI ADC

Steven Xie, Product Applications Engineer

Question:
Can I access a nonstandard SPI interface with my MCU?

Answer:
Yes, but it might take a little extra effort.

Introduction
Many current precision analog-to-digital converters (ADCs) have a serial peripheral interface (SPI) or some serial interface to communicate with controllers including a microcontroller unit (MCU), a DSP, or an FPGA. The controllers write or read ADC internal registers and read conversion codes. SPI is becoming more and more popular due to its simple printed circuit board (PCB) routing and a faster clock rate compared to parallel interface. And, it is easy to connect an ADC to the controller with a standard SPI.

Some new ADCs have an SPI, but others have a nonstandard 3-wire or 4-wire SPI as a slave because they want to achieve a faster throughput rate. For example, the AD7616, AD7606, and AD7606B families have two or four SDO lines for faster throughput rate in serial mode. The AD7768, AD7779, and AD7134 families have multiple SDO lines and they work as SPI masters. Users tend to encounter difficulties in designing microcontroller SPIs for ADC configuration and code reading.

Figure 1. AD7768 as a serial master with two data output pins (14001-193).

Standard MCU SPI Connection to an ADC
SPI is a synchronous, full-duplex, master/slave-based interface. The data from the master or the slave is synchronized on the rising or falling clock edge. Both master and slave can transmit data at the same time. Figure 2 shows a typical 4-wire MCU SPI interface connection.

Figure 2. Standard MCU SPI connection to an ADC slave.

To begin SPI communication, the controller must send the clock signal and select the ADC by enabling the CS signal, which is usually an active low signal. Since SPI is a full-duplex interface, both the controller and ADC can output data at the same time via the MOSI/DIN and MISO/DOUT lines, respectively. The controller SPI interface provides the user with flexibility to select the rising or falling edge of the clock to sample and/or shift the data. For reliable communication between the master and the slave, users must follow the digital interface timing specifications of both the microcontroller and the ADC chip.
If the microcontroller SPI and ADC serial interface have the standard SPI timing mode, it is not a problem for users to design the PCB routing and develop the drive firmware. But there are some new ADCs with a serial interface port that is not a typical SPI timing pattern. It does not seem possible for the MCU or the DSP to read data through the AD7768 serial port, a nonstandard timing SPI port, as shown in Figure 4.

This article will introduce approaches to manipulating the standard microcontroller SPI to interface with ADCs that have nonstandard SPI ports.

This article will cover four different solutions to read the ADC codes by serial interface:

- Solution 1: MCU as SPI slave interfacing to ADC as SPI master by one DOUT line.
- Solution 2: MCU as SPI slave interfacing to ADC as SPI master by two DOUT lines.
- Solution 3: MCU as SPI slave interfacing to ADC as SPI master through DMA.
- Solution 4: MCU as SPI master and SPI slave to read data on two DOUT lines.

Figure 3. Example SPI data clock timing diagram.

Figure 4. AD7768 FORMATx = 1× timing diagram output on DOUT0 only.
AD7768 Code Reading with STM32F429 Microcontroller SPI by One DOUT Line

As shown in Figure 4, when FORMATx = 11 or 10, Channel 0 to Channel 7 output data on DOUT0 only. In standard mode operation, the AD7768/AD7768-4 operate as the master and stream data to the MCU, DSP, or FPGA. The AD7768/AD7768-4 supply the data, the data clock (DCLK), and a falling edge framing signal (DRDY) to the slave device.

The STM32Fxxx family of microcontrollers are widely used in many different applications. The MCUs have several SPI ports, which can be configured as SPI master or slave with typical SPI timing modes. The methods introduced in the following session can also be applied on other microcontrollers with an 8-bit, a 16-bit, or a 32-bit frame.

The AD7768/AD7768-4 have 8-channels and 4-channels, simultaneous sampling sigma-delta (Σ-Δ) ADCs, respectively, with a sigma-delta modulator and digital filter per channel, enabling synchronized sampling of ac and dc signals. They achieve 108 dB dynamic range at a maximum input bandwidth of 110.8 kHz, combined with typical performance of ±2 ppm INL, ±50 μV offset error, and ±30 ppm gain error. The AD7768/AD7768-4 user can trade off input bandwidth, output data rate, and power dissipation, and select one of three power modes to optimize for noise targets and power consumption. The flexibility of the AD7768/AD7768-4 allow them to become reusable platforms for low power dc and high performance ac measurement modules.

Unfortunately, AD7768’s serial interface is not a typical SPI timing mode, and AD7768 works as the serial interface master. Generally, users must use FPGA/CPLD as its controller.

For example, 32F429IDISCOVERY and AD7768 eval boards are used. The workaround SPI wires are connected as shown in Figure 5. In this setup, all eight AD7768 channel data outputs on DOUT0 only.

Problems to be solved:
- AD7768 works as the SPI master, so the STM32F429I SPI must be configured as SPI slave.
- DRDY high pulse is just one cycle of DCLK duration that is not a typical CS.
- DCLK continuously outputs and DRDY is low when all the channel data bit output is finished.

Solution 1: MCU SPI as Slave Interfacing to SPI Master ADC by One DOUT Line
- Configure one of STM32F429 is SPI ports, like SPI4, as a slave to receive data bits on MOSI at DCLK.
- Connect AD7768 DRDY to the STM32F429 external interrupt input pin EXTI0 and NSS (SPI CS) pin. The rising edge of DRDY will trigger EXTI0 handler routine to enable the SPI slave to start to receive data bits from the first DCLK falling edge after DRDY goes to low. Timing design is critical here.
- After all the data from Channel 0 to Channel 7 are received, the SPI should be disabled to prevent reading in extra invalid data, since the DRDY makes SPI slave CS low and DCLK keeps toggling.
MCU Firmware Development Notes

With the software in interrupt mode, DCLK can run up to 4 MHz, and ODR 8 kSPS is achieved. The software should go into the interrupt handler to start SPI within one and a half DCLK period time (375 ns). To more easily enable the software to go into the interrupt routine, the MCU can read the data at the DCLK rising edge, which can give an additional half DCLK period time. But, since the t5 DCLK rise to the DOUTx invalid minimum is –3 ns (–4 ns for IOVDD = 1.8 V), a propagation delay (>\|t5\| + MCU hold time) on DOUTx should be added by PCB routing or buffer.

```c
/*## Configure the SPI4 peripheral ###*/
Spi4Handle.Instance = SPI4;//use STM32F429 SPI4
Spi4Handle.Init.Direction = SPI_DIRECTION_2LINES_RXONLY;
Spi4Handle.Init.CLKPhase = SPI_PHASE_1EDGE;//read at DCLK falling edge
Spi4Handle.Init.CLKPolarity = SPI_POLARITY_HIGH;//read at DCLK falling edge
Spi4Handle.Init.Datasize = SPI_DATASIZE_8BIT;//or 16BIT
Spi4Handle.Init.NSS = SPI_NSS_HARD_INPUT;//make /CS low active
Spi4Handle.Init.Mode = SPI_MODE_SLAVE;//MCU SPI4 as SPI Slave

/*## Enable EXTI0 and SPI4 to Receive AD7768 Data bits ###*/
// clear EXTI0 IT flag prior to enable external interrupt 0 !!!
__HAL_GPIO_EXTI_CLEAR_IT(KEY_BUTTON_PIN);
HAL_NVIC_EnableIRQ(EXTI0_IRQn);
// wait for EXTI0 interrupt (/DRDY rising edge) to prepare for reading last conversion data
if (EXTI0_Flag == SET) {
    EXTI0_Flag = RESET;//clear /DRDY rising edge flag variable
    // throw out the last byte/word captured in the previous ODR cycle !!!
    Rx_temp = *(__IO uint8_t *)&Spi4Handle.Instance->DR;
    // SPI4_CNVByteNum is the total data byte number to read in one conversion cycle
    while (SPI4_ByteCount < SPI4_CNVByteNum) {
        // Check the RXNE flag
        if (__HAL_SPI_GET_FLAG(&Spi4Handle, SPI_FLAG_RXNE)) {
            // transfer the received data from DR register to memory
            SPI_RxBuffer[RxBuf_Idn] = *(__IO uint8_t *)&Spi4Handle.Instance->DR;
            RxBuf_Idn++;
            SPI4_ByteCount++;
        }
    }
    // disable SPI4 to prevent read in extra data after all channel codes finished due to /DRDY
    // is low active and DCLK continuously pulses
    __HAL_SPI_DISABLE(&Spi4Handle);
    SPI4_CNVCount++;
    RxBuf_Idn = SPI4_CNVCount * SPI4_CNVByteNum;
    SPI4_ByteCount = 0;
} else {
    //*** other software jobs ***
    /*## handles External 0 interrupt request ###*/
    // EXTI0 rising edge triggered to leave more response time for going into EXTI0_IRQHandler !!!
    void EXTI0_IRQHandler(void) {
        if (__HAL_GPIO_EXTI_GET_IT(EXTI0) != RESET) {
            // enable SPI4 as soon as possible, and make sure before the first DCLK falling edge
            // after /DRDY falling !!!
            __HAL_SPI_ENABLE(&Spi4Handle);
            __HAL_GPIO_EXTI_CLEAR_IT(EXTI0);
            EXTI0_Flag = SET;
        }
    }
}
```

Figure 7. Configure the SPI4 peripheral.
Solution 2: MCU SPI as Slave Interfacing to SPI Master ADC by Two DOUT Lines

In the first solution, only DOUT0 is used to output all the 8-channel data. So, the data reading limits the ADC throughput rate to 8 kSPS. As shown in Figure 1, Channel 0 to Channel 3 output on DOUT0 and Channel 4 to Channel 7 output on DOUT1 can reduce the data transfer time. The serial wires are connected as shown in Figure 7. With such improvement, the ODR can easily go up to 16 kSPS at DCLK 4 MHz.

The firmware can use polling mode instead of the interrupt mode to reduce the time latency from the DRDY rising edge trigger to enable the SPI to receive the data. This can achieve ODR 32 kSPS at DCLK 8 MHz.

Solution 3: MCU SPI as Slave Interfacing to SPI Master ADC Through DMA

Direct memory access (DMA) is used in order to provide high speed data transfer between peripherals and memory, and between memory and memory. Data can be quickly moved by DMA without any MCU action. This keeps MCU resources free for other operations. Here are the design notes for an MCU SPI acting as slave to receive data through DMA.

Solution 4: MCU SPI as Master and Slave to Read Data on Two DOUT Lines

The high throughput or multichannel precision ADCs provide SPI ports with two, four, and even eight SDO lines for faster code reading time in serial mode. For microcontrollers with two or more SPI ports, they can concurrently run the SPI ports for faster code reading.

Figure 8. AD7768 output data on DOUT0 and DOUT1 to STM32F429 MCU SPI connection.

Figure 9. EXTI0 in polling mode and SPI4 & SPI5 to receive AD7768 data bits on DOUT0 and DOUT1.

```c
/*## EXTI0 in Polling Mode and SPI4 & SPI5 to Receive AD7768 Data bits on DOUT0 and DOUT1 ###*/

// Polling for EXTI0 (/DRDY) rising edge to start MCU SPI ports
while (__HAL_GPIO_EXTI_GET_IT(EXTI0) != SET) {
    __HAL_SPI_ENABLE(&Spi4Handle);
    __HAL_SPI_ENABLE(&Spi5Handle);
    __HAL_GPIO_EXTI_CLEAR_IT(EXTI0);
}

// throw out the last byte/word captured in the previous ODR cycle !!!
Rx_temp = *(__IO uint8_t *)&Spi4Handle.Instance->DR;
Rx_temp = *(__IO uint8_t *)&Spi5Handle.Instance->DR;
while (SPI4_ByteCount < SPI4_CNVByteNum) // total data byte number to read in one conversion cycle
{
    if (__HAL_SPI_GET_FLAG(Spi4Handle, SPI_FLAG_RXNE))//
    {
        SPI_RxBuffer[RxBuf_Idn] = *(__IO uint8_t *)&Spi4Handle.Instance->DR;
        SPI_RxBuffer[RxBuf_Idn+1] = *(__IO uint8_t *)&Spi5Handle.Instance->DR;
        RxBuf_Idn++;
        SPI4_ByteCount += 2;
    }
}
__HAL_SPI_DISABLE(Spi4Handle);
__HAL_SPI_DISABLE(Spi5Handle);

Figure 10. EXTI0 in polling mode and SPI4 and SPI5 to receive AD7768 data bits on DOUT0 and DOUT1.
In the following use case, 32F429IDISCOVERY uses SPI4 as SPI master and SPI5 as SPI slave to receive EVAL-AD7606B-FMCZ data on DOUTA and DOUTB as shown in Figure 8.

The AD7606B is a 16-bit, simultaneous sampling, analog-to-digital data acquisition system (DAS) with eight channels, each channel containing analog input clamp protection, a programmable gain amplifier (PGA), a low-pass filter, and a 16-bit successive approximation register (SAR) ADC. The AD7606B also contains a flexible digital filter, low drift, 2.5 V precision reference and reference buffer to drive the ADC and flexible parallel and serial interfaces. The AD7606B operates from a single 5 V supply and accommodates ±10 V, ±5 V, and ±2.5 V true bipolar input ranges when sampling at throughput rates of 800 kSPS for all channels.

![Figure 11. MCU SPIs used in master and slave mode to receive data on DOUTA and DOUTB.](image)

```c
/*## Configure the SPI4 as Master and SPI5 as Slave ###*/
Spi4Handle.Init.Direction = SPI_DIRECTION_2LINES;
Spi4Handle.Init.CLKPhase = SPI_PHASE_1EDGE;  // read at DCLK falling edge
Spi4Handle.Init.CLKPolarity = SPI_POLARITY_HIGH; // read at DCLK falling edge
Spi4Handle.Init.DataSize = SPI_DATASIZE_16BIT;
Spi4Handle.Init.NSS   = SPI_NSS_SOFT;       // NSS pin is configured as GPIO output for /CS
Spi4Handle.Init.Mode   = SPI_MODE_MASTER;  // SPI4 as SPI Master
Spi5Handle.Init.Direction = SPI_DIRECTION_2LINES_RXONLY; // only receive data
Spi5Handle.Init.NSS             = SPI_NSS_HARD_INPUT;
Spi5Handle.Init.Mode   = SPI_MODE_SLAVE;  // SPI5 as SPI Slave
/*## Enable SPI4 as Master and SPI5 as Slave to Receive AD7606B Codes ###*/
__HAL_SPI_ENABLE(&Spi4Handle);
__HAL_SPI_ENABLE(&Spi5Handle);
while (SPI4_CNVCount < SPI4_CNVNum) {
    CLR_CNV();
    SET_CNV(); // AD7606B conversion start
    // wait for conversion finish, BUSY goes from high to low. Polling or interrupt mode
    while (BUSY == SET) {;
        while (SPI4_WordCount < SPI4_CNVWordNum) // code number to read per conversion cycle
            {
            CLR_CS();
            *(volatile uint8_t *)&Spi4Handle.Instance->DR = 0;
            while (!__HAL_SPI_GET_FLAG(&Spi4Handle, SPI_FLAG_RXNE)) {};
            Delay_us(1); // need half SCLK cycle delay for slow SCLK rate < 10MHz
            SET_CS();
            SPI_RxBuffer[RxBuf_Idn] = *(volatile uint16_t *)&Spi4Handle.Instance->DR;
            SPI_RxBuffer[RxBuf_Idn+ADCSDO1_WordIdn] = *(volatile uint16_t *)
                &Spi4Handle.Instance->DR;
            RxBuf_Idn++;
            SPI4_WordCount += 2;
        }
        SPI4_CNVCount++;
        RxBuf_Idn = SPI4_CNVCount * SPI4_CNVWordNum;
        SPI4_WordCount = 0;
    }
} //while (SPI4_CNVCount < SPI4_CNVNum)
__HAL_SPI_DISABLE(&Spi4Handle);
__HAL_SPI_DISABLE(&Spi5Handle);

Figure 12. Configure the SPI4 as master and SPI5 as slave.
```
Figure 13 shows the AD7606B digital interface capture of BUSY, SCLK, DOUTA, and DOUB running at 240 kSPS.

Conclusion
This article discussed approaches to using a microcontroller SPI to access ADCs with nonstandard SPI interfaces. These approaches can be used directly or with slight adjustments to control the ADC SPI, which is working as an SPI master or with multiple DOUT lines for a faster throughput rate.

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References

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