Improved DAC Phase Noise Measurements Enable Ultralow Phase Noise DDS Applications

By **Peter Delos** and **Jarret Liner**

Introduction

In radar applications, phase noise is a critical performance metric for systems requiring high clutter attenuation. Phase noise is a concern for all radio systems, but radar in particular can require phase noise performance at frequency offsets much closer to the carrier than a communication system.

System designers in these high performance systems will choose ultralow phase noise oscillators and the objective of the signal chains, from a noise perspective, is to add minimal degradation to the oscillator phase noise profile. This requires residual or additive phase noise measurements of the varied components in the signal chain.

Recent product releases of high speed digital-to-analog converters (DACs) are extremely attractive for both waveform generation and frequency creation for any LOs needed in frequency conversion stages. The radar objectives, however, challenge the DAC phase noise performance.

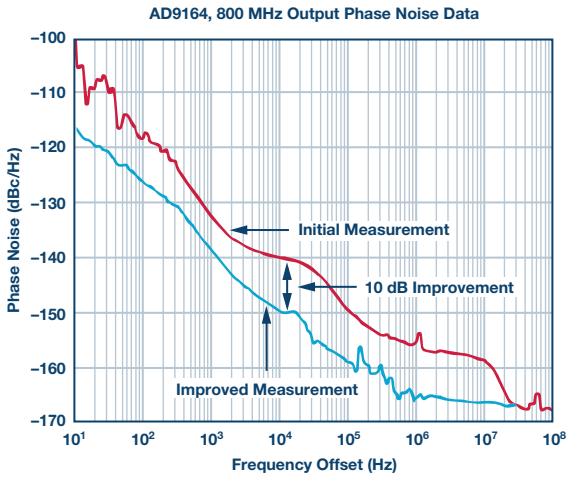

Figure 1. AD9164 phase noise improvements.

In this article we show measured improvements of over 10 dB at 10 kHz offsets using the AD9164 DAC. Figure 1 illustrates the improvement and we will discuss how the results were achieved through a combination of both power supply regulator selection and test setup improvements.

Phase Noise Definition

Phase noise is a measure of the deviation in the zero crossing of a periodic signal. Consider a cosine wave with phase fluctuations

$$x(t) = \cos(2\pi ft + \Phi(t))$$

f = instantaneous frequency

$\Phi(t)$ = randomly fluctuating phase in radians

Phase noise is determined from the power spectral density of the phase variations

$$S(f) = \frac{\Phi(t)^2_{RMS}}{BW} \text{ with units of } \frac{\text{rad}^2}{\text{Hz}}$$

In linear terms, the single sided phase noise is defined as

$$L(f) = \frac{S(f)}{2}$$

Phase noise is normally expressed in units of dBc/Hz from 10log(L(f)). Phase noise data is then plotted at offset frequencies relative to the RF carrier.

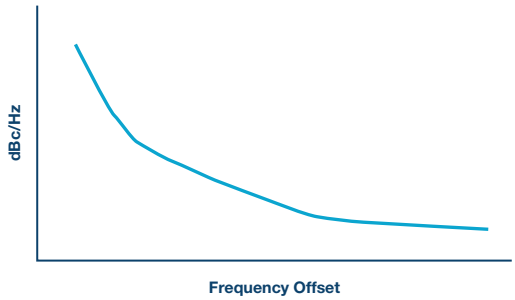

Figure 2. Phase noise plot method.

An important further definition of phase noise is absolute phase noise vs. residual phase noise. Absolute phase noise is the total phase noise measured in the system. Residual phase noise is the additive phase noise of the device under test. This distinction becomes critical in the test setups and in the process of determining component level phase noise contributions in a system.

DAC/DDS Phase Noise Measurement Methods

The figures in this section illustrate DDS phase noise test setups. For DAC phase noise measurements, it is assumed the DAC is used as part of a direct digital synthesizer (DDS) subsystem. A DDS is implemented with a digital sinewave pattern to a DAC that could be in a monolithic IC or an FPGA or ASIC communicating to a DAC. In modern DDS design, the digital phase errors can be made much less than the DAC errors, and DDS phase noise measurements are typically limited by the DAC performance.

The simplest and most common test setup is shown in Figure 3. A clock source is used for the DDS and the DDS output is fed to a cross correlation type phase noise analyzer. This is easy to implement since only a single DDS is required. However, with this test setup there is no method to extract the oscillator contribution to show only the DDS phase noise.

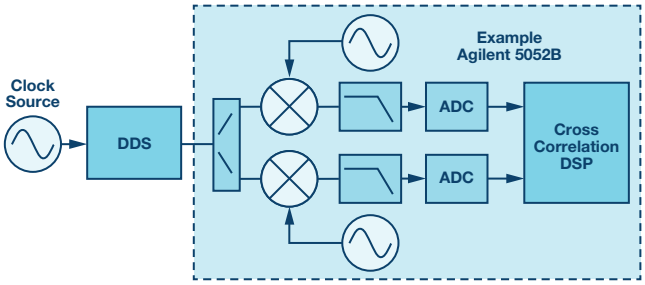

Figure 3. Absolute phase noise DDS test setup includes both DAC and oscillator noise.

Figure 4 shows two common methods to remove the oscillator phase noise from the measurement, providing a residual noise measurement. The drawback of the measurements is that additional DACs are required in the test setup. However, the benefit is a much better indicator of the DAC phase noise contribution that can be applied in system-level analysis budgets.

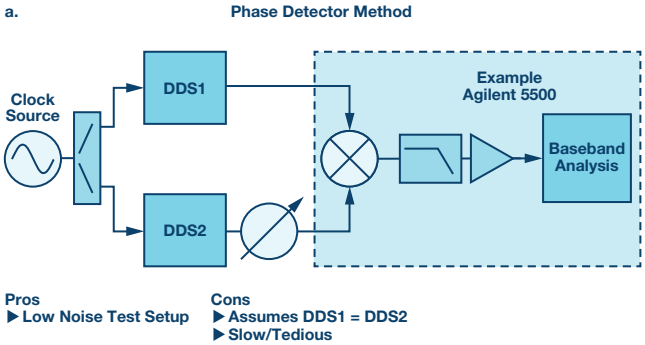

Figure 4a. DDS residual phase noise measurement using the phase detector method.

Figure 4a shows the phase detector method. In this case, two DACs are used and the oscillator contribution subtracts from both DUTs in the downconversion to dc.

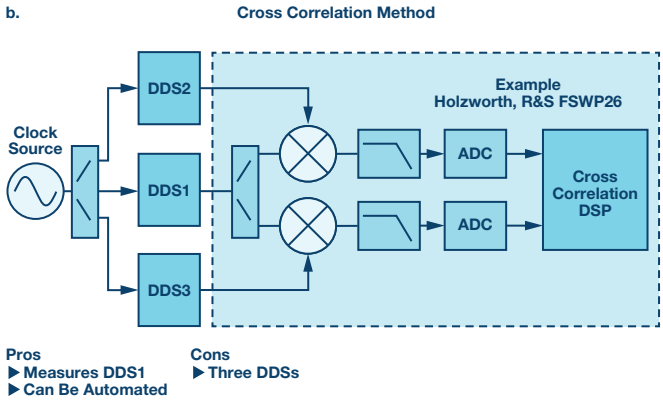

Figure 4b. DDS residual phase noise measurement using the cross correlation method.

Figure 4b shows a method using cross correlation phase noise analysis. In this case, DDS2 and DDS3 are used to translate the clock contribution to the LO ports of the measurement, their contribution is removed in the cross correlation algorithms, and the DDS1 residual phase noise is obtained in the measurement.

Power Supply Noise Contributions

In low noise analog and RF design, power supply noise is a well-known factor to consider. Power supply ripple that is periodic modulates onto the RF carrier and creates spurs on the RF carrier at frequency offsets equal to the ripple frequency. Regulator 1/f noise modulates onto the RF carrier also and contributes to the phase noise profile. Figure 5 illustrates the principles.

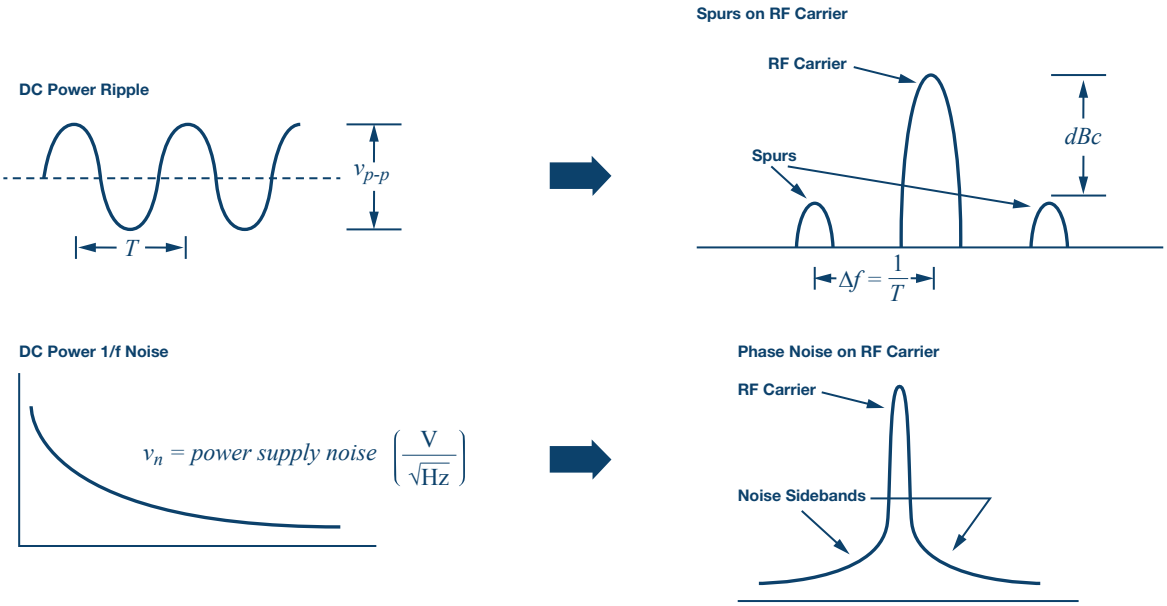

Figure 5. Power supply imperfections modulated on to the RF carrier.

Measured Results

During investigation of the true DAC phase noise performance, both the test setups and the regulator noise performance were considered.

The initial DAC evaluation board included the ADP1740 regulator for the analog and clock voltages. Noise spectral densities were compared with recently released ultralow noise regulators and the ADM7155 was chosen. Figure 6 illustrates the comparison of the noise densities as shown in the product data sheets. The power supply modification was merely to use the ADM7155 for both the AD9164 clock (data sheet pins VDD12_CLK) and the analog voltage (data sheet pins VDD12A).

Next, test setup options were considered for residual phase noise measurements. The cross correlation method was chosen with the Rohde & Schwarz FSWP primarily out of availability and convenience. The test setup used is shown in Figure 7.

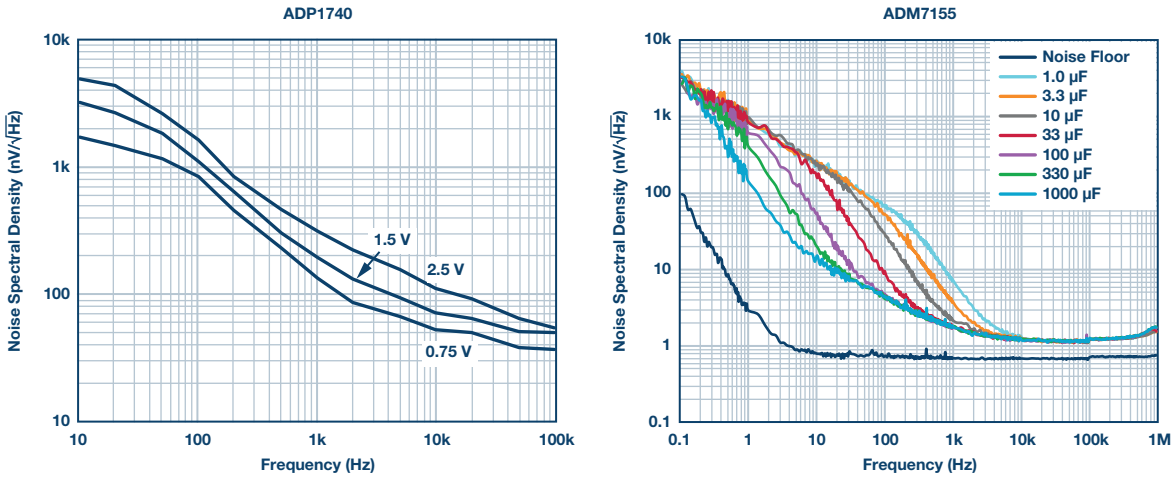

Figure 6. Regulator noise density comparison. Note the Y-axis units—the ADM7155 is an order of magnitude improved.

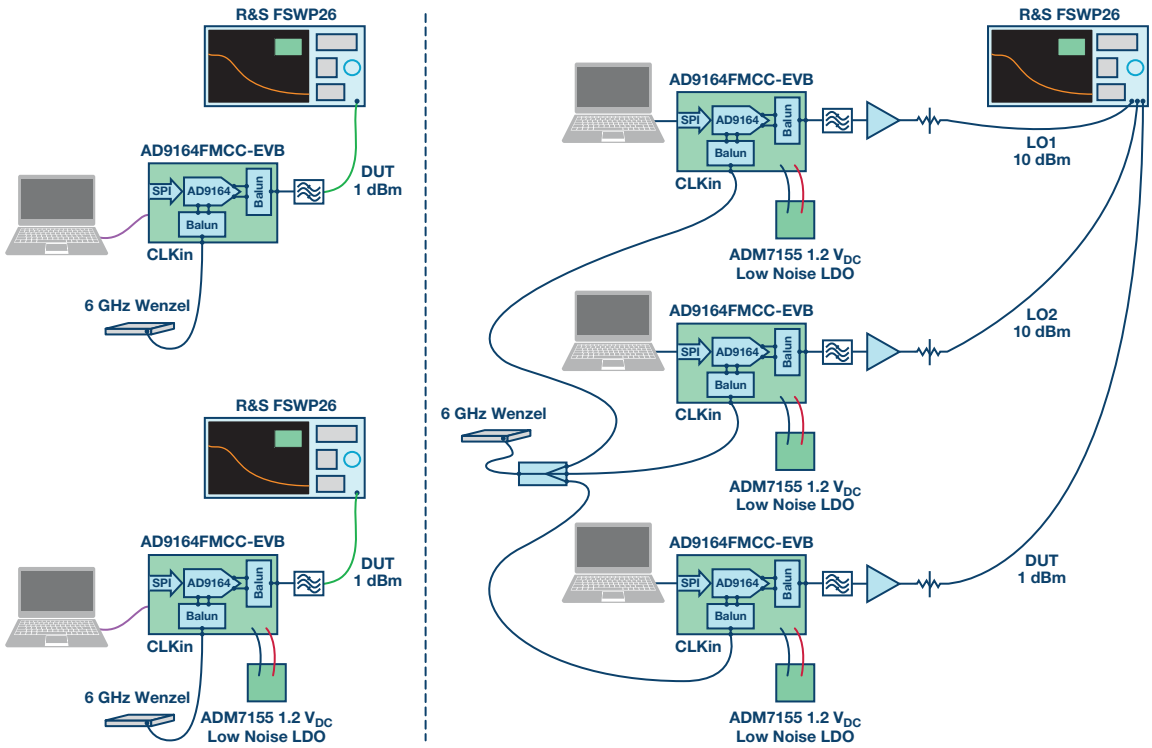

Figure 7. Test setups for AD9164 phase noise measurements.

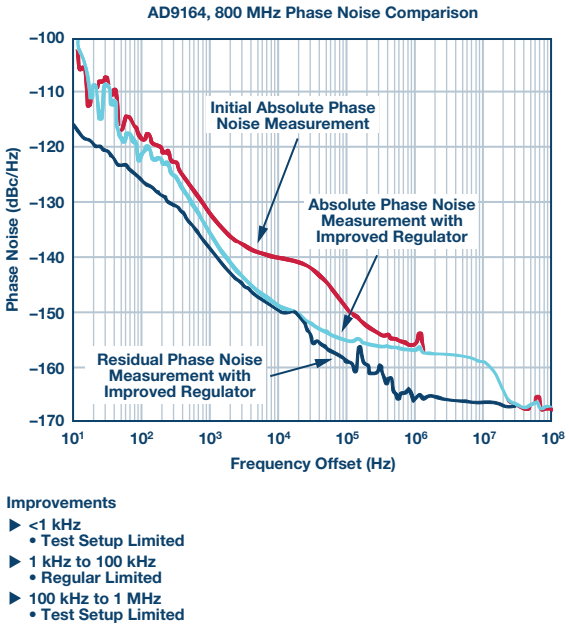

Figure 8. AD9164 800 MHz output phase noise comparisons.

Figure 8 is a measurement of three cases. The initial evaluation board measurement taken with an absolute phase noise approach is shown as the red curve. The light blue curve is also an absolute measurement but with the regulator improvement. The dark blue curve is a residual phase noise measurement that also includes the regulator improvement.

The measurement indicates three general regions of limitations in the initial measurement that were not obvious in the beginning of the investigation. Frequencies below 1 kHz were limited by the close in noise of the clock source. Frequencies from 1 kHz to 100 kHz were limited by the regulator selection. Frequencies above 100 kHz were limited by the clock source. The sharp drop off above 10 MHz is the clock source contribution as the clock used was a multiplied crystal oscillator to create 6 GHz and the roll-off is from the RF filters used in the multiplication stages.

Residual phase noise measurements with the regulator improvement were taken at additional DAC frequencies and several are summarized in Figure 9. The modifications were duplicated on several evaluation boards and all cases showed the same improved results.

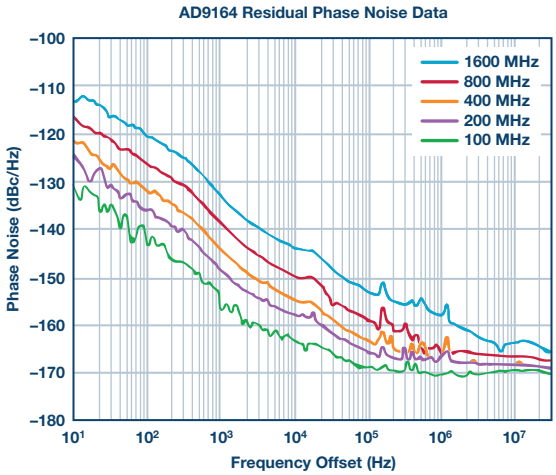

Figure 9. AD9164 residual phase noise measurements with low noise regulator improvement.

Table 1. Family of Regulators with State-of-the-Art Noise Density Performance

Part Number	V_{IN} Min (V)	VI_N Max (V)	V_{OUT} Options or Adj Range (V)	I_{OUT} (mA)	PSRR @ 1 nkHz	PSRR @ 1 MHZ (µV rms)[1]	RMS Noise 100 Hz to 100 kHz (nV/√Hz)	Noise Spectral Density 100 kHz (nV/√Hz)	Dropout @ Rated I_{OUT} Typ (mV)	Total Acuracy Max (±%)	Package
ADM7150	4.5	16	Fixed: 1.5 to 5.0	800	94	62	1	2	600	2	3 mm × 3 mm, 8-lead LFCSP, 8-lead SOIC
ADM7151	4.5	16	Adjustable: 1.5 to 5.1	800	94	62	1	2	600	2	3 mm × 3 mm, 8-lead LFCSP, 8-lead SOIC
ADM7154 *New*	2.3	5.5	Fixed: 1.2 to 3.3	600	90	58	1	1.2	120	2	3 mm × 3 mm, 8-lead LFCSP, 8-lead SOIC
ADM7155 *New*	2.3	5.5	Adjustable 1.2 to 3.3	600	90	58	1	1.2	120	2	3 mm × 3 mm, 8-lead LFCSP, 8-lead SOIC

[1] Noise independent at fixed output voltage.

The family of ultralow noise regulators with similar noise density is shown in Table 1. As demonstrated, the impact on the DAC phase noise is significant and these are also recommended for consideration for any areas of the RF system requiring optimum phase noise performance.

Summary

A phase noise review was provided for the fundamental definition, absolute vs. residual phase noise, DAC phase noise measurement test setups, and regulator noise contributions.

DAC phase noise improvements were demonstrated for including both residual phase noise test methods and optimum regulator selection. The end result is the AD9164 now is an enabler for ultralow phase noise, DDS-based applications when the analog voltages and clock voltages are powered from the Analog Devices family of low noise regulators.

References

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Peter Delos [peter.delos@analog.com] is a technical lead at Analog Devices, Inc., in the Aerospace and Defense Group. He received his B.S.E.E. from Virginia Tech in 1990 and M.S.E.E. from NJIT in 2004. He worked in the Naval Nuclear Power program from 1990 to 1997. This work included completion of the Naval Nuclear Power School Officer's Program, and work as an instructor in a Naval submarine facility and as a lead electrical field engineer on the Seawolf class Submarines in Groton, CT.

In 1997, he accepted a position with Lockheed Martin in Moorestown, NJ, and began a prolific career developing receivers/exciters and synthesizers for multiple radar and EW programs. This experience encompassed architecture definition, detailed design, rapid prototypes, manufacturing coverage, field installations, and coordination among many engineering disciplines. This work led the migration of phased array receiver/exciter electronics from centralized architectures to on-array digital beamforming systems.

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Jarrett Liner [jarret.liner@analog.com] is an RF systems application engineer with Analog Devices, Inc., in the Aerospace and Defense Group in Greensboro, NC. He has significant experience in the area of RF system and component design.

Formerly, Jarrett was an applications engineer for GaN on SiC amplifiers for the military and aerospace sector. His prior experience also includes design and test of RF IC WLAN power amplifier and front-end modules for 13 years. He served 6 years in the United States Navy as an electronics technician. Jarrett received his B.S.E.E. from North Carolina Agricultural and Technical State University located in Greensboro, NC, in 2004.

When Jarrett isn't simulating circuit solutions or taking data in the lab, he might be found mountain biking, teaching cycle class at the gym, running, or chasing his four kids around the yard.