Analyzing and Managing the Impact of Supply Noise and Clock Jitter on High Speed DAC Phase Noise

By **Jarrah Bergeron**

Out of all device properties, noise can be an especially challenging topic to grasp and design for. Such challenges often lead to hearsay design rules and trial-and-error development. In this article, phase noise will be tackled with the objective of making quantitative sense of how to design around the contributions of phase noise in high speed digital-to-analog converters. The goal is to obtain a methodology that neither over-designs nor under-designs the phase noise requirement, but, rather, gets it right the first time.

Starting from a blank slate, the DAC is first treated as a block box. Noise can be generated internally, as any real component will generate some noise, or the noise can come in from external sources. The entrance from external sources can occur through any of the DAC connections, which broadly include power, clocking, and digital interfaces. These possibilities are illustrated in Figure 1. Each of these possible noise suspects will be investigated individually to understand their importance.

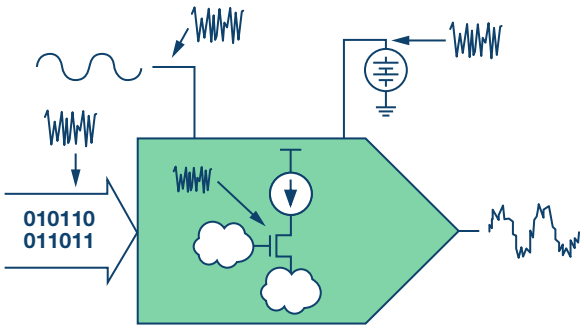

Figure 1. Sources of DAC phase noise.

The digital interface will be covered first and happens to be easiest to treat. The digital I/O is in charge of receiving samples to be outputted in the analog domain. As is commonly known, digital circuitry and the waveforms being received are noisy, as demonstrated by the eye diagrams. From this standpoint, the question that arises is: could all this noise and activity infiltrate into various regions inside the DAC and manifest itself as phase noise? Of course, the digital interface can cause noise elsewhere, but it is phase noise that is at issue here.

To prove out whether the I/O is a concern, the phase noise was compared with and without the digital interface on the AD9162 series of HSDAC parts. Without the interface, the device's NCO mode internally generates the waveform, effectively changing the DAC into a DDS generator. Figure 2 shows the experimental results.

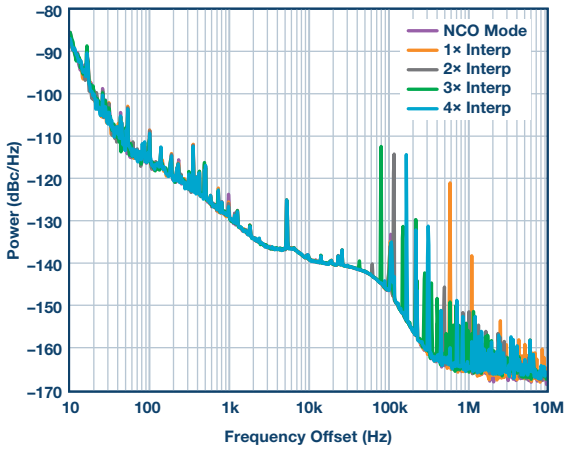

Figure 2. Phase noise at different interpolations.

Peaks do show up with the interface turned on and move around according to interface details. Now what is of interest is that the noise and all the curves are on top of each other. As a result, in this product line, the interface is not of concern, notwithstanding those spurs that may need attention depending on system requirements. Finding that the interface is of little concern leads into the next area of interest: clocking.

Clocking

Clocking is of prime concern for generating phase noise in DACs, namely the DAC clock. This clock dictates when the next sample will be sent, so any noise in the phase (or timing) directly affects the phase noise of the output, as shown in Figure 3. This process can be considered as the multiplication between each successive discrete value with a rectangular function whose timing is defined by the clock. Now, in the frequency domain, multiplication translates to the convolution operation. As a result, the desired spectrum gets smeared with the clock phase noise, as illustrated in Figure 4. The exact relationship, however, is not immediately obvious. A quick derivation follows.

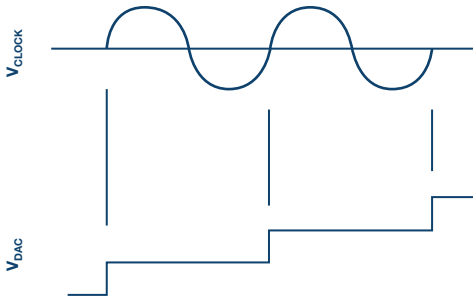

Figure 3. Clock to phase noise dependence.

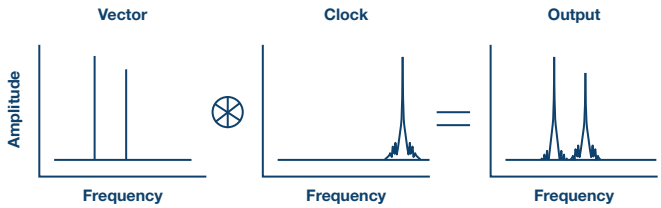

Figure 4. Phase noise convolution.

Taking a snapshot in time of the clock and output, an instance of the waveform is shown in Figure 5. The objective will be to find the ratios between the noise amplitudes of the clock and output shown as red arrows in Figure 6. Right triangles can be drawn and although none of the lengths are known, both triangles have a common horizontal side.

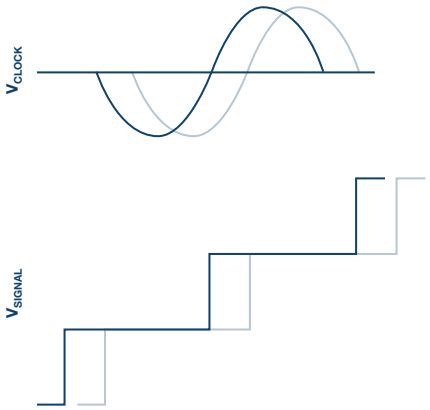

Figure 5. Waveform snapshot.

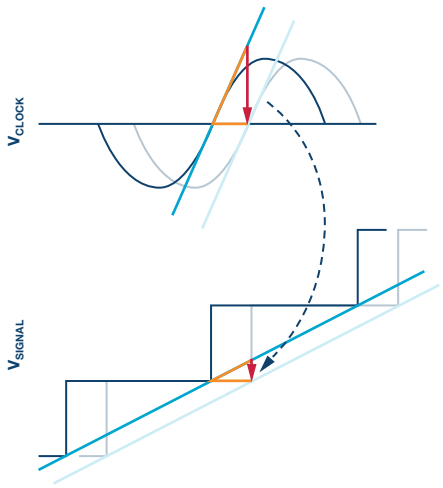

Figure 6. Phase noise relation.

Setting the slopes as derivatives of the respective waveforms, the geometry gives the following equation:

$$\frac{V_{CLK\_noise}}{\frac{\partial V_{CLK}}{\partial t}} = \frac{V_{SIG\_noise}}{\frac{\partial V_{SIG}}{\partial t}}$$

Rearranging for DAC noise yields the next equation:

$$V_{SIG\_noise} = V_{CLK\_noise} \frac{\frac{\partial V_{SIG}(t)}{\partial t}}{\frac{\partial V_{CLK}(t)}{\partial t}}$$

As we are often interested in sinusoid or near sinusoid waveforms for the DAC output and clock, the result can be simplified down. If this assumption doesn't hold, keep to the previous formulation.

$$V_{SIG\_noise} = V_{CLK\_noise}\left[\frac{V_{SIG}f_{SIG}}{V_{CLK}f_{CLK}}\right]$$

And then by reorganizing, we get this:

$$\frac{V_{SIG\_noise}}{V_{SIG}} = \frac{V_{CLK\_noise}}{V_{CLK}}\left[\frac{f_{SIG}}{f_{CLK}}\right]$$

Notice the noise relationship equates relative to the respective waveform amplitude, therefore, it is succinctly summarized relative to carrier. Also, by using logarithmic units, we arrive at the following equation:

$$N_{SIG} = N_{CLK} + 20\log_{10}\frac{f_{SIG}}{f_{CLK}}$$

The noise relative to the carrier is scaled up and down according to a ratio of the signal frequency to the clock frequency. Every halving of the signal frequency results in 6 dB improvement in noise. Examining the geometry, this makes sense as the triangle on the bottom would become more acute and shrink the vertical side. Also notice that increasing the clock amplitude doesn't improve phase noise if the noise increases at the same magnitude.

To prove this out, phase noise can be simulated by modulating the clock coming into the DAC. In Figure 7, the 5 GHz DAC clock is shown with light phase modulation at 100 kHz. Plotted on top are spectrums at 500 MHz and 1 GHz outputs. The tones do indeed follow this relationship. A 20 dB decrease is observed from the 5 GHz clock to the 500 MHz DAC output, and a 6 dB increase shows up from 500 MHz to the 1 GHz output.

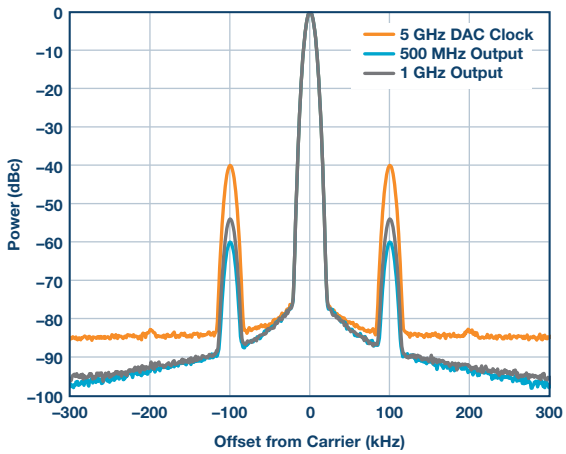

Figure 7. Clock output phase noise with 100 kHz phase modulation.

As nice as a well-controlled experiment is, real noise is of interest. Substituting the generator with the ADF4355 wideband synthesizer, Figure 8 shows the phase noise profile for the new clock source along with corresponding DAC outputs at ½ and ¼ clocking frequency. The noise behavior is preserved with 6 dB decreases each time. It should be noted that the PLL was not optimized for best phase noise. Perceptive readers will notice that some deviation from expectation occurs at small offsets, but this is expected due to differing reference sources.

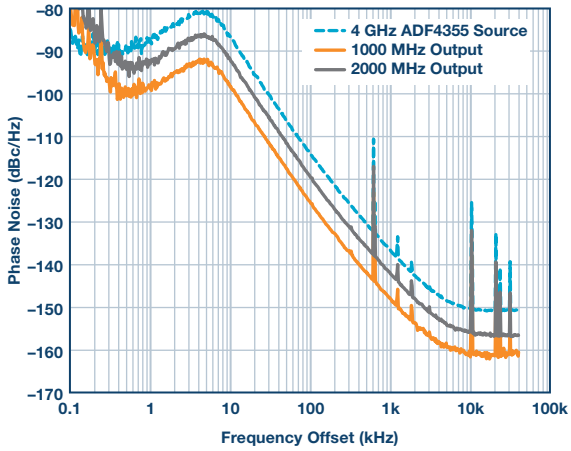

Figure 8. DAC output phase noise with wideband synthesizer clock source.

Another aspect to explore is the lack of dependency between input power and noise. It is only the difference between the noise power to the carrier that matters. This means that straight amplification of the clock yields no benefit. Figure 9 shows that this is indeed the case. The only change is a slight increase in the noise floor that is attributed to the signal generator. Now, this observation is only valid within reason; at a certain point, clocking will become so weak that other contributions such as clock receiver noise will start dominating.

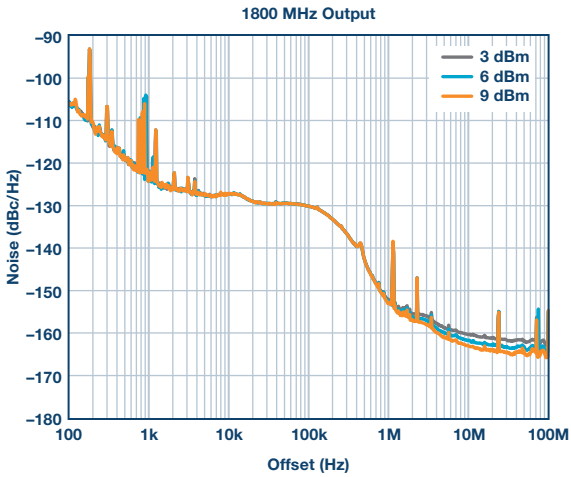

Figure 9. Phase noise vs. input power.

Lastly, the new sampling scheme, 2× NRZ, should be briefly mentioned. The AD9164 DAC series of parts introduces this new sampling mode that allows new sampled data on both the rising and falling edges of the clock. However, with these changes the phase noise characteristic stays the same. Figure 10 compares the original NRZ mode with this new mode. The curves show identical phase noise, though some noise floor rise is visible. This conclusion does assume the noise characteristics are the same on both the rising and falling edge, which is the case for most oscillators.

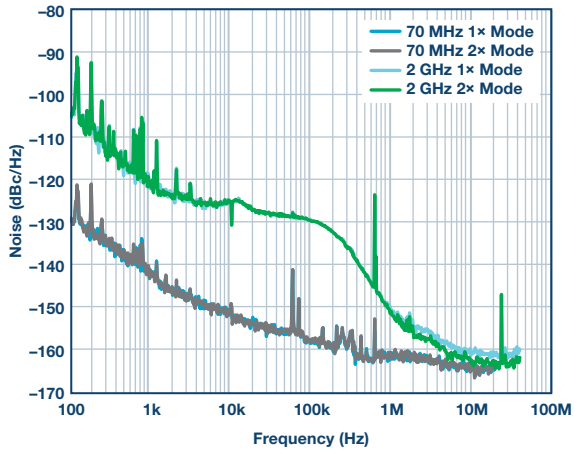

Figure 10. Phase noise and 2× NRZ.

Power Supply

The next possible point of entry for noise is through power. All of the circuitry on a die must be powered one way or another and this gives noise plenty of ways to propagate through to the output. The precise mechanism is circuit dependent but a few possibilities are highlighted below. The DAC output is typically composed of current sources with MOS switches to direct the current through either the positive or negative pin (Figure 11). As evidenced, the current source gets its power from an external supply and any noise will reflect as current fluctuations. The noise can pass through the switches to the output but that would only explain a direct coupling to baseband. To contribute to phase noise, this noise must be mixed up to the carrier frequency. This process is done by way of the switching MOSFETs, which act as a balanced mixer. Another path for noise is through the pull-up inductors. They set the dc bias from a rail and any noise present here flows to the transistors. Such fluctuations modify their operating conditions, such as source to drain voltage and current source load, leading to changes in current flow that once again gets mixed up to the RF signal. In general, any circuit is a vector for power supply noise to show up as phase noise, if switching is capable of mixing it up to the signal at hand.

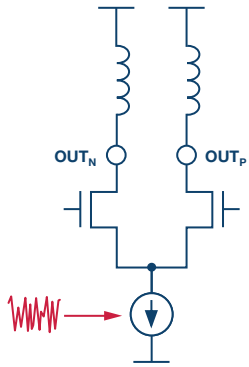

Figure 11. DAC current source.

With all of this circuitry and mixing phenomena, it gets unwieldy rather quickly to model all of this behavior. Instead, characterization of other analog blocks brings insight. In regulators, op amps, and other ICs, a power supply rejection ratio is specified. Supply rejection quantifies a load's sensitivity to supply changes and can be used here for phase noise analysis. Instead of rejection, however, a modulation ratio is used: power supply modulation ratio (PSMR). The traditional PSRR measure can still be useful in DACs in baseband applications but it is not of interest here. The next step is to obtain the data.

Measuring PSMR requires modulating the supply rail that is under investigation. A typical setup is shown in Figure 12. Supply modulation is obtained through a coupling circuit inserted between the regulator and the load, superimposing a sinusoid signal that is produced by a signal generator. The output of the coupling circuit is monitored with an oscilloscope to find the actual supply modulation. The resulting DAC output is fed to a spectrum analyzer. The PSMR is calculated by a ratio of the ac component of the supply as found from the oscilloscope to the modulated sideband voltage around the carrier.

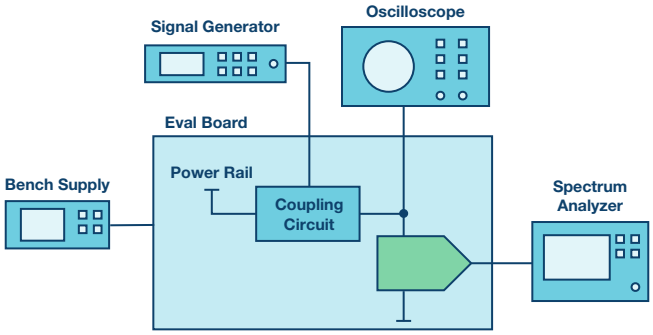

Figure 12. PSMR measurement.

Different coupling schemes are possible. Rob Reeder, Analog Devices applications engineer, provides a rundown of the use of LC circuits to measure PSMR of ADCs in the MS-2210 application note. Other options include a power op amp, transformer, or dedicated modulated power supply. The method used here was the transformer. A high turns ratio is recommended to lower the source impedance of the signal generator. A typical measurement is provided in Figure 14.

Using a 1:100 turns ratio current sense transformer and function generator, the 1.2 V clock supply was modulated at 500 kHz with a resulting peak-to-peak voltage of 38 mV. The DAC was clocked at 5 GSPS. The resulting output incurs sidebands on a full-scale, 1 GHz carrier at –35 dBm. Converting power to a voltage and then taking the ratio with the modulated supply voltage results in a PSMR of –11 dB.

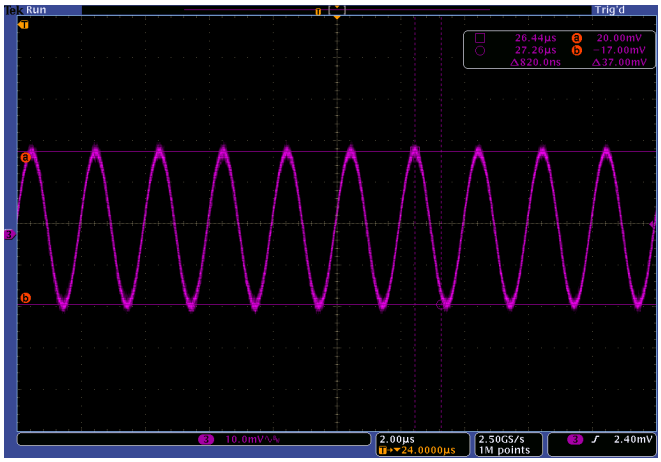

Figure 13. Clock supply modulation.

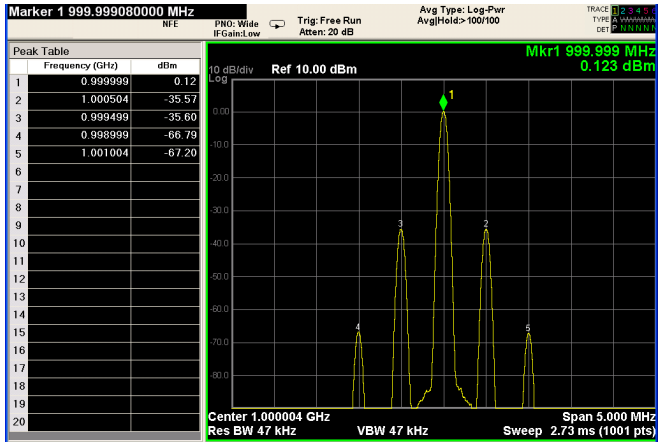

Figure 14. Modulated sidebands.

With a single data point performed, a sweep can be done over multiple frequencies. However, the AD9164 DAC includes a total of eight supplies. One option is to measure all the supplies, but the focus can be limited to the most sensitive supplies: AVDD12, AVDD25, VDDC12, and VNEG12. Some supplies, such as SERDES, aren't relevant for this analysis and therefore not included. Sweeping through multiple frequencies and supplies, the results are summarized in Figure 15.

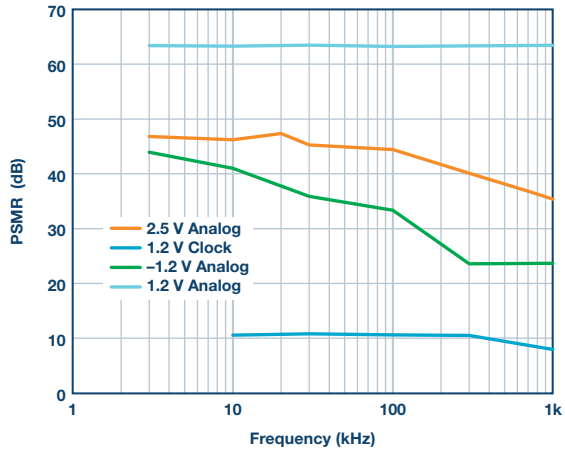

Figure 15. Supply PSMR measured over swept frequencies.

The clock supply is the most sensitive rail. The negative 1.2 V and 2.5 V analog supplies are next and then the 1.2 V analog supply, which is quite insensitive. Whereas the 1.2 V analog supply could, with appropriate consideration, be supplied by a switching regulator, the clock supply is on the complete opposite spectrum: it needs to be supplied by very low noise LDOs to obtain optimum performance.

PSMR could only be measured within a certain frequency range. On the low end, it's limited by weakening magnetic coupling. The selected transformer had a low frequency cutoff in the 10s of kHz. On the high end, decoupling caps lower the load impedance making the supply rail increasingly difficult to drive. Some caps can be removed for testing purposes as long as functionality isn't compromised.

Before using PSMR, a few aspects should be noted. Unlike PSRR, PSMR depends on the waveform power or, in the case of DACs, the digital back-off. The lower the waveform, the lower the sideband becomes, in a 1:1 ratio. However, backing off does not gain the designer anything as the sideband is constant relative to carrier. The second aspect is the dependency over carrier frequency. A sweep of the carrier indicates linear degradation at higher bands at various rates. Interestingly, the more sensitive the rail, the steeper the slope. For instance, the clock supply is sloped at –6.4 dB/octave, while the negative analog supply is at –4.5 dB/octave. The sampling rate also influences the PSMR. Finally, PSMR only provides an upper limit on phase noise contribution as it is not differentiated from amplitude noise that is also produced.

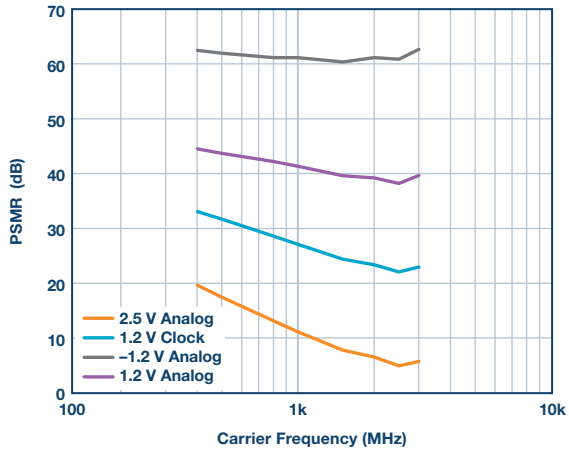

Figure 16. Supply PSMR over signal frequency.

Given these diverse noise requirements, it is helpful to look at a few powering options. The LDO is the tried and true regulator—especially for achieving utmost noise performance. However, not any LDO will do. The 15002C curve in Figure 17 demonstrates the phase noise of the initial AD9162 DAC evaluation board. The DAC output was set to 3.6 GHz, with the DAC being clocked at 4 GHz from the Wenzel source. The phase noise plateau between 1 kHz and 100 kHz was suspected to be dominated by the clock power supply noise: the ADP1740 LDO. Using this LDO's spectral noise density plots and the DAC PSMR measurements in Figure 16, the contribution can be calculated and plotted as shown in Figure 17, as well. Even though it does not precisely line up because of extrapolation, the calculated points line up reasonably to the measured noise, solidifying the clock supply effects on noise. In a redesign of the power solution, this LDO was replaced with the lower noise ADP1761. Noise was lowered by as much as 10 dB at certain offsets, approaching the clock contribution (15002D).

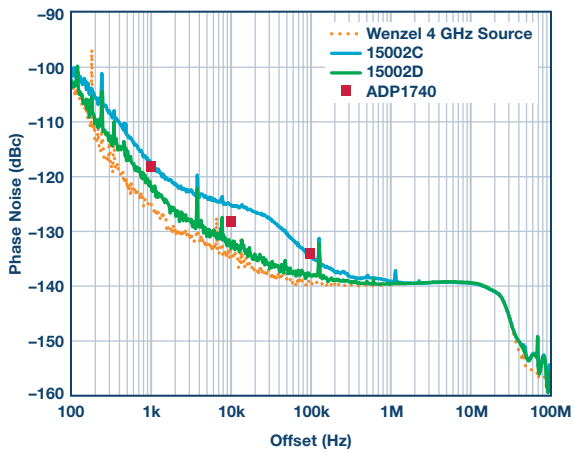

Figure 17. AD9162 evaluation board noises.

Not only does noise vary widely over various regulators, but it can also be influenced by output capacitors, output voltage, and load. Careful consideration of these factors should be taken into account, especially on sensitive rails. On the other hand, depending on the overall system requirements, LDOs are not necessarily required.

Switching regulators may provide power with appropriate LC filtering, simplifying the power solution. As with LDOs, start from the regulator NSD and design accordingly. However with LC filters, attention should be given to the series resonance. Not only can transients become unwieldly, but voltage gain in the vicinity of the resonance frequency can occur, increasing the power rail noise along with phase noise. The resonance can be tamed by de-Q-ing the circuit—that is, adding lossy elements to the circuit. The following figures show an example from another design featuring the AD9162 DAC.

In this design, the clock supply was also powered off an ADP1740 LDO but an LC filter followed it. The schematic shows the filter under consideration with an RL model for an inductor and an RC model for the main filter capacitor (C1+R1). The filter response is shown with a characteristic resonance in red on Figure 20. Not surprisingly, telltale signs of this filter show up in the phase noise response: the blue curve of Figure 21. A plateauing of the noise around 100 kHz and a steep drop off afterward from the filtering action. Fortunately, the LC filter peaking is not severe enough to cause a distinct peak but the filter can be improved nonetheless. One scheme, which is employed here is to add a second, larger cap with an appropriate series resistance to dissipate the energy. A series circuit of a 22 µF capacitor and a 100 mΩ resistor is shown that significantly dampers down the response (the blue curve). The end result is a phase noise improvement around this frequency offset: the yellow curve in Figure 21.

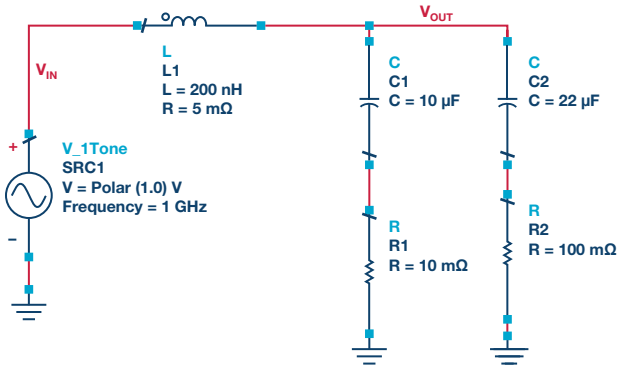

Figure 18. LC filter and de-Q network.

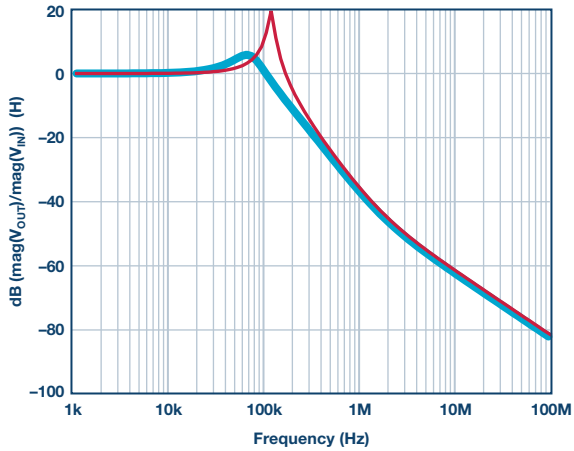

Figure 19. LC filter response.

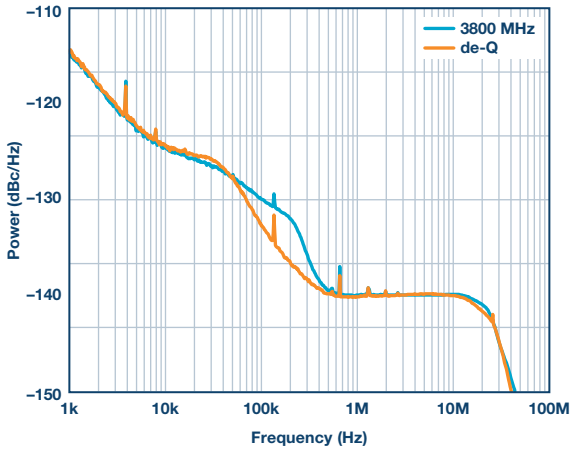

Figure 20. Phase noise response.

The final noise source to analyze is the phase noise of the part itself. The AD9164 DAC series of parts feature very low phase noise, which is challenging to quantify. By removing all the expected noise sources, the residual noise is from the DAC, as shown in Figure 22. The simulated phase noise is also plotted and aligns well with measurement. Clock phase noise still dominates in certain regions.

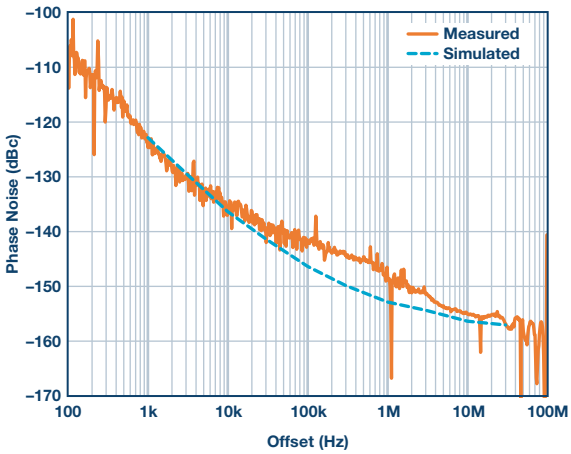

Figure 21. AD9162 phase noise.

Conclusion

Confronted with all of the previously discussed noise sources, the designer may become overwhelmed. The temptation is to follow a recommended solution; however, this approach will always be suboptimal for any particular design requirements. Analogous to RF signal chains and precision error budgets, a phase noise budget can be used in the design process. Using clock source phase noise, the PSMR results for each supply rail, LDO noise characteristics, and the DAC setup, the noise contributions from each source can be calculated and optimized. An example budget is shown in Figure 22. With all sources properly considered, phase noise can be analyzed and managed, and the signal chain designed right the first time.

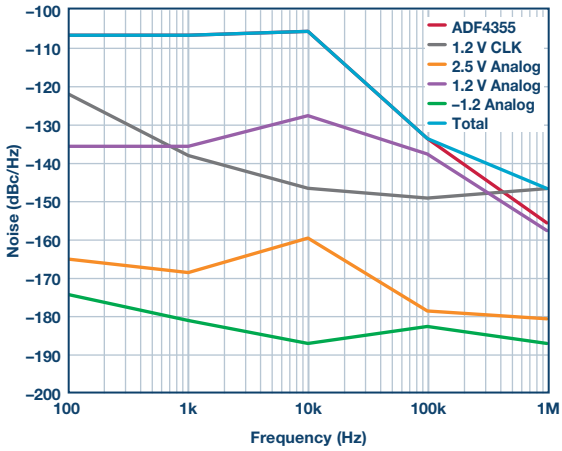

Figure 22. Example phase noise budget.

References

Brannon, Brad. Application Note AN-756, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*. Analog Devices, Inc., 2004.

Reeder, Rob. "Designing Power Supplies for High Speed ADC." Analog Devices, Inc., February 2012.

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