Improper Power Sequencing in Op Amps: Analyzing the Risks

By **David Guo**

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Introduction

In systems with multiple supply voltages, operational amplifier power supplies must be established simultaneously with or before any input signals are applied. If this doesn't happen, overvoltage and latch-up conditions can occur.

However, this can sometimes be a difficult requirement to meet in real-world applications. This article takes a look at the activity of op amps in different power sequence situations (see Table 2), analyzes possible issues, and presents some suggestions.

Power Sequencing Issues Can Vary

There are a number of different scenarios where power sequencing issues may arise. For example, in one customer application, an AD8616 can be configured as a buffer, the input is 0 V before power supplies are established (Figure 1), and the negative supply is powered on before the positive supply (negative power is present and positive power is absent).

Table 1 shows the results of all AD8616 pins in such conditions. Before V+ is applied, the voltage at the V+ pin and OUT pins is negative. This may not damage the op amp, but if these signals are connected to terminals on other chips that haven't been fully powered (for example, assuming the ADC uses the same V+, and its power pin normally tolerates only –0.3 V minimum voltage), the chips may suffer damage. A similar issue will happen if V+ is powered up before V–.

Table 2 highlights some possible situations in power sequencing.

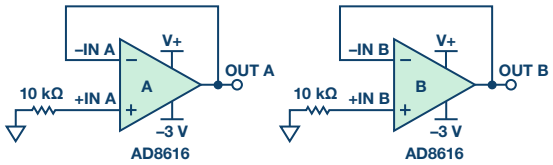

Figure 1. AD8616 test circuit with –3 V V– applied and V+ absent.

Table 1. AD8616 Pins' Voltage with –3 V V– Applied and V+ Absent

Pin1: OUTA	Pin2: –INA	Pin3: +INA	Pin4: V –	Pin5: +INB	Pin6: –INB	Pin7: OUTB	Pin8: V+
–1.627	–1.627	–0.959	–3.000	–0.959	–1.627	–1.627	–1.627

Table 2. Possible Situations in Power Sequencing

	IN	V+	V–	Amplifier Power with Load	Amplifier Out with Load
Case 1	Floating Floating	Present Absent	Absent Present	No No	No No
Case 2	0 V 0 V	Present Absent	Absent Present	No No	No No
Case 3	Positive or negative Positive or negative	Present Absent	Absent Present	No No	No No
Case 4	Positive or negative Positive or negative Positive or negative Positive or negative	Present Present Absent Absent	Absent Absent Present Present	Yes No Yes No	No Yes No Yes

Electrostatic Discharge (ESD) Diodes Within Op Amps

Electrostatic discharge can also result in an overvoltage event. Most op amps have an internal ESD diode to prevent electrostatic ESD events. ESD diodes can provide a key to analyzing activity when either V+ or V– is absent. Figure 2 is a simplified block diagram of the ADA4077/ADA4177. Table 3 shows the ADA4077-2/ADA4177-2's typical drop voltage of internal ESD diodes and back-to-back diodes. Notice that back-to-back diodes are placed between the two input terminals of the op amps to clamp the maximum differential input signal.

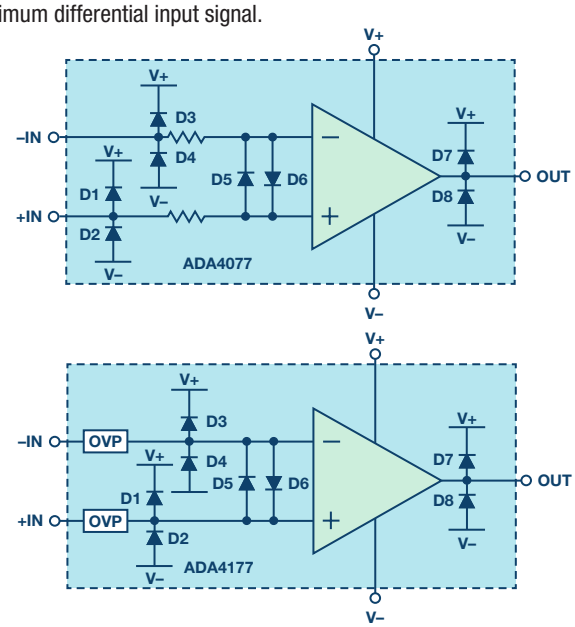

Figure 2. ADA4077/ADA4177 simplified block diagram.

Table 3. Internal Diode of an Op Amp

	ADA4077	ADA4177
D1	0.838	Unknown
D2	0.845	Unknown
D3	0.837	Unknown
D4	0.844	Unknown
D5	Unknown	Unknown
D6	Unknown	Unknown
D7	0.841	0.849
D8	0.842	0.849

Also note that when DMM is used to measure D5/D6 of the ADA4077-2, it shows no diode between the two input terminals. In fact, there are two series of resistors before the back-to-back diodes to limit input current smaller than ±10 mA. The internal resistors and back-to-back diodes limit the differential input voltage to ±Vs to prevent a base-emitter junction breakdown.

For the ADA4177, OVP cells are integrated for robustness. They are placed before the ESD diodes and back-to-back diodes, so it's hard to measure these diodes by DMM. The output ESD diodes of ADA4177 can be measured.

Evaluation Setup

Figure 3 is used to measure the activity of the op amp. Channel A and Channel B are each configured as a buffer, and the Channel B noninverting input is connected to the GND by a 100 kΩ resistor. By making V+ absent (V– present) or V+ present (V– absent), the input and power-related variables can be measured by the ampere and voltage meters. "By analyzing these variables, we can determine the current flow path.

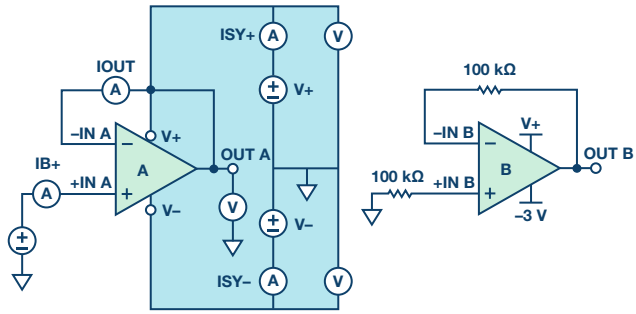

Figure 3. Setup for power sequencing test.

Case 1: Input Is Floating

Table 4 shows the results of a floating input and one absent supply. When V– is present and V+ is absent, there is a negative voltage at the V+ pin. When V+ is present and V– is absent, there is a positive voltage at the V– pin.

Testing the ADA4077-2 and ADA4177-2 reveals similar results. No large currents are observed at the input pins and power pins, and the op amp with floating input remains safe when a power rail is absent.

Case 2: Input Is Grounded

Table 5 shows the results when the input is grounded. Note for IB+, a negative value means the current flow out of the +IN terminal. For IOUT, a negative value means the current flow out of the –IN terminal.

Table 4. ADA4077-2/ADA4177-2 Results with Floating Input

	Condition	V+	V–	ISY+ (mA)	ISY– (mA)	IB+ (mA)	IOUT (mA)	IN (V)	OUT (V)
ADA4077-2	All power	15	–15	1.02	1.01	–0.00005	0.00007	0.001	–0.008
	V+ absent	–13.1	–15	0	0.12	–0.00001	0.001	–13.73	–14.42
	V– absent	15	13.06	0.15	0	–0.00001	0.001	12.93	13.62
ADA4177-2	All power	15	–15	0.98	0.96	–0.00001	0.00002	0	0.001
	V+ absent	–14.26	–15	0	0.14	–0.00002	0.00137	–13.77	–13.78
	V– absent	15	12.96	0.14	0	–0.00001	–0.00039	12.26	12.31

Table 5. ADA4077-2/ADA4177-2 Results with Grounded Input

	Condition	V+	V–	ISY+(mA)	ISY-(mA)	IB+(mA)	IOUT(mA)	IN(V)	OUT(V)
ADA4077-2	All power	15	–15	1.01	1	–0.00005	0.00001	0	-0.019
	V+ absent	–0.846	–15	0	2.30	2.300	-1.60	-0.017	–2.68
	V– absent	15	0.847	1.78	0	–1.758	1.064	0.012	2.116
ADA4177-2	All power	15	–15	0.98	0.96	–0.00001	0.00002	0	0
	V+ absent	–11.99	–15	0	9.3	9.300	–0.200	-0.068	–11.98
	V– absent	15	1.848	1.84	0	–1.823	0.067	0.013	1.851

Taking ADA4077-2 with V+ absent as an example, V+ is clamped to the VIN voltage by an ESD diode.

- VIN is connected to V+ via an ESD clamp diode, so when VIN is 0 V, V+ is –0.846 V.
- Current flow path loop: as the red path shown in Figure 4, 0.7 mA current flows from GND (+IN) to V+. 1.6 mA current flows from GND (+IN) through an internal resistor, D5 and the feedback path between –IN and OUT, then the current flow into output terminal. Finally the two currents (0.7 mA and 1.6 mA) combine to flow to –15 V, and the combined current flows back to GND (+IN).

Results are similar between the ADA4177-2 and ADA4077-2. Note that within the ADA4177-2, D1 is implemented by an emitter base of a lateral PNP transistor. The transistor routes the overvoltage current away from the V+ to the V–. The ADA4177 circuit in Figure 4 shows 9.1 mA current flow from V+ back to V– , and combined with 0.2 mA current in the feedback path, results in a 9.3 mA current flow to –15 V, then the current flows back to GND.

No large currents are observed at the input pins and power pins for either the ADA4077-2 or the ADA4177-2 (Table 5). These op amps can withstand any order of PU sequencings in a gain of +1 with +IN grounded.

Case 3: With Input

A positive or negative signal (+10 V or –10 V) is applied to the +IN terminal when one power is absent. Table 6 shows no large current, so these op amps can withstand any order of PU sequencings in a gain of +1 with +IN grounded for a short duration.

The current flow path analysis is similar with Case 2 (0 V input), refer to Figure 5.

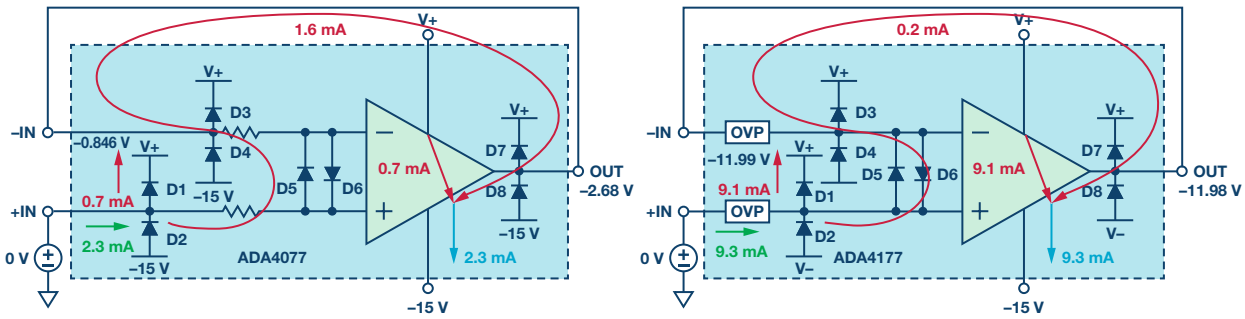

Figure 4. ADA4077/ADA4177 current path when V+ is absent (input grounded).

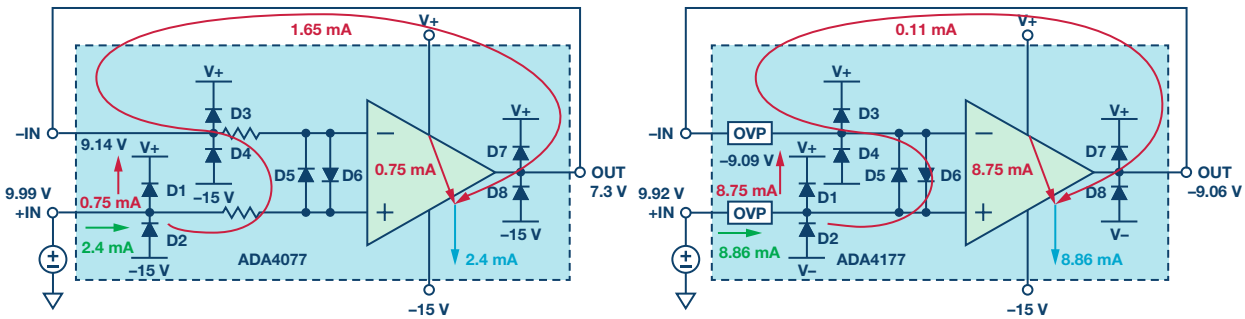

Figure 5. ADA4077/ADA4177 current path when V+ is absent (10 V input).

Table 6

	Condition	V+	V–	ISY+ (mA)	ISY– (mA)	IB+ (mA)	IOUT (mA)	IN (V)	OUT (V)
ADA4077-2	All power	15	–15	1.03	1.01	0.00098	–0.00003	10	9.97
	V+ absent and positive input	9.14	–15	0	2.4	2.396	–1.653	9.99	7.3
	V+ absent and negative input	–10.83	–15	0	2.41	2.308	–1.651	–10.02	–12.66
	V– absent and positive input	15	10.83	1.81	0	–1.689	1.055	10.02	12.09
	V– absent and negative input	15	–9.15	1.77	0	–1.759	1.031	–9.99	–7.88
ADA4177-2	All power	15	–15	1.02	1	–0.00099	–0.00009	9.99	9.97
	V+ absent and positive input	–9.09	–15	0	8.86	8.866	–0.113	9.92	–9.06
	V+ absent and negative input	–12.33	–15	0	4.31	4.18	–0.039	–10.02	–12.32
	V– absent and positive input	15	11.42	1.33	0	–1.2	0.056	9.99	11.43
	V– absent and negative input	15	–8.33	1.51	0	–1.492	0.062	–9.97	–8.32

Case 4: With Input and with Load at Power/Output

In a real application, the op amp circuit may work with another circuit. For example, the op amp's output may drive a load, or the op amp's power supply may also power other circuits. This can cause a problem.

In this test, a 47 Ω resistor is connected between the output and GND or the absent power pins and GND. Table 7 shows the test results for the ADA4077. Large currents are highlighted in red. Three possible situations can pose risks, assuming V+ is absent:

- Situation 1: When the input is 10 V and the load of OUT is 47 Ω, the output is 1.373 V. When there is a 23 mA current flow out of the op amp's output pin (refer to Figure 6) the current path is:
  - Input signal source supply 30.2 mA current
  - 24 mA current flow through D1 to V+, and 6.2 mA current flow through D5 and feedback path to OUT
  - 24 mA current from V+ is divided to 1 mA (to V–) and 23 mA (to OUT)
  - 29.2 mA current flow through 47 Ω load to GND

The current needs to be limited. By adding a 1 kΩ resistor at +IN, the input current is decreased to 6.8 mA.

- Situation 2: When the input is 10 V and the load of V+ is 47 Ω, 170 mA current flows into the ADA4077-2 and flows out of V+ pin to a 47 Ω power load. 170 mA current will burn the internal diode and damage the chip. By adding a 1 kΩ resistor at +IN, the input current is decreased to 8.9 mA. Figure 7 shows the current flow path.

Table 7. ADA4077 with Load at Output Pin or Absent Power Pin

ADA4077-2	Condition	IN (V)	V+	V–	ISY+ (mA)	ISY– (mA)	IB+ (mA)	IOUT (mA)	OUT (V)
V+ absent	Vo or V+ no load/positive input	9.99	9.14	–15	0	2.4	2.396	–1.653	7.3
	Vo 47 Ω to GND	9.98	8.77	–15	0	1.00	30.22	–6.174	1.373
	Vo 47 Ω to GND and 1 kΩ	9.98	2.389	–15	0	0.76	6.828	–2.104	0.284
	V+ 47 Ω to GND	9.59	8.01	–15	170	5.05	175	–5.0	6.06
	V+ 47 Ω to GND and 1 kΩ	9.94	0.295	–15	6.27	2.69	8.96	–2.69	–1.876
	Vo or V+ no load/negative input	–10.02	–10.83	–15	0	2.41	2.308	–1.651	–12.66
	Vo 47 Ω to GND	–9.97	–3.226	–15	0	48.6	–4.65	4.885	–2.501
	Vo 47 Ω to GND and 1 kΩ	–10.02	–10.83	–15	0	14.30	2.284	–1.629	–0.563

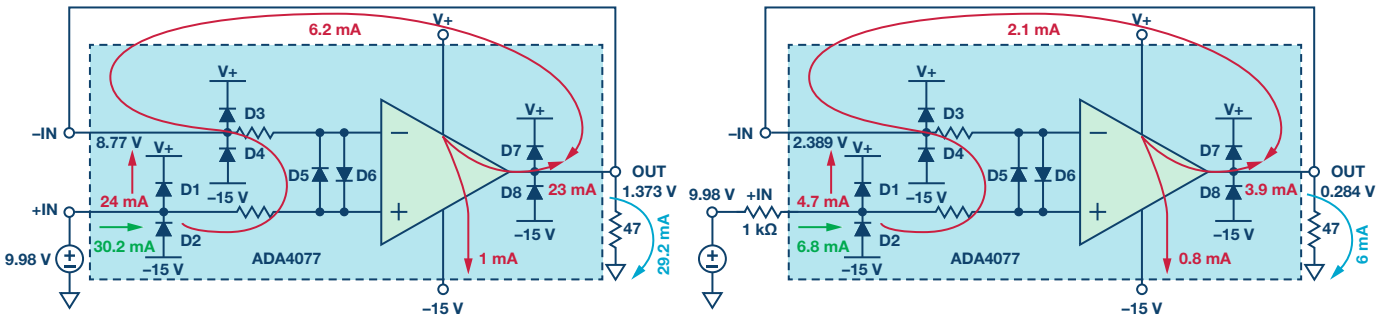

Figure 6. ADA4077 current path when V+ is absent (10 V input and 47 Ω output load).

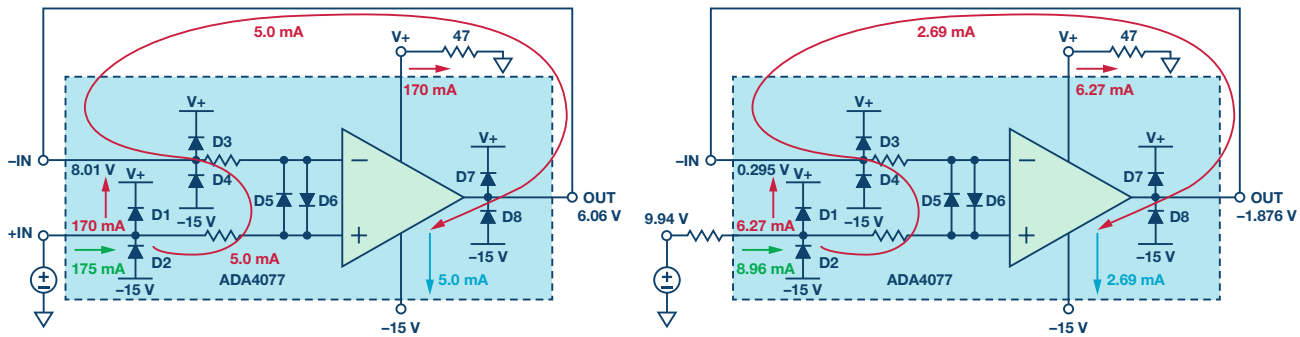

Figure 7. ADA4077 current path when V+ is absent (10 V Input and 47 Ω power load).

- Situation 3: When input is negative (–10 V) and the load of OUT is 47 Ω (refer to Figure 8), there is a 48 mA current that flows through the chip. This will generate a 48 mA × (–2.5 V + 15 V) = 0.6 W power dissipation. Considering the ADA4077-2's 158° C/W ΘJA , the junction temperature is 94.8° higher than the ambient temperature. If there are two channels or there is a heavier load, the junction temperature may be higher than 150°, and the chip may be damaged.
- Instead of adding a current-limiting resistor at the input, the resistor should be added at the output.
- When V+ is present and V– is absent, the same phenomena will happen. By adding external resistors to limit the current, the circuit can be more robust.

For ADA4177-2, only Situation 3 applies. When there is a large negative input and a heavy load at the output at the same time and when V+ is absent and there is 53 mA current flow through the chip, the power dissipation may be increased and the junction temperature is increased (refer to Figure 9). By adding a 1 kΩ resistor at the output, the risk can be avoided.

Of the two op amps, the ADA4177-2 is more robust than the ADA4077-2. It is a preferred choice for applications that require both precision and robustness.

Other Op Amp Activity in Power Sequencing

Among op amps, there are varying implementations of diodes, resistors, and OVP cells. Some op amps have no internal OVP cells, some have no back-to-back diodes. A different implementation will produce different results if one power supply is absent. In addition, different op amp designs can produce different results.

For example, the ADA4084-2 has no internal current-limiting resistor or OVP cells, and it has ESD diodes connected to the power supply and back-to-back diodes. Table 9 and Figure 10 show the results when V+ is absent and there is 10 V input. The ADA4084's activity and current path are similar to those of the ADA4077-2 and ADA4177-2 (discussed previously in Case 3). However, because the ADA4084 has no internal resistor or OVP cell to limit the current, 60 mA current will flow into the chip, which may cause damage.

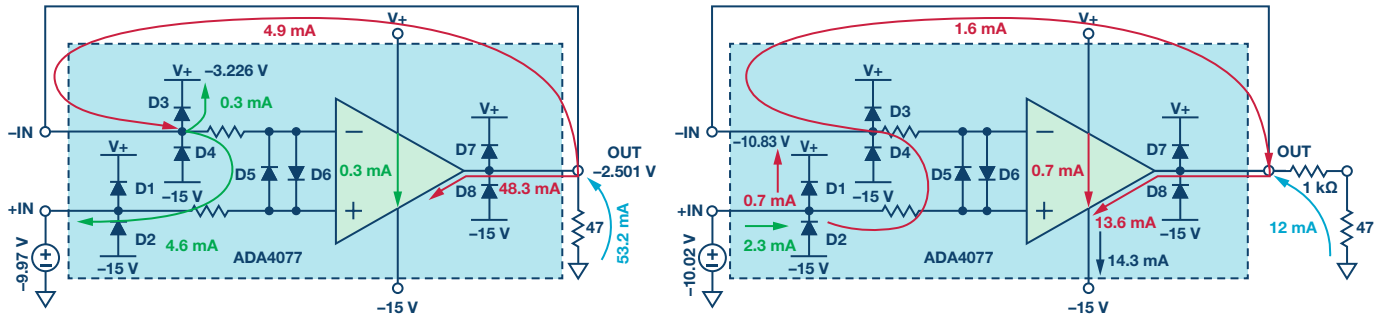

Figure 8. ADA4077 current path when V+ is absent (–10 V Input and 47 Ω output load).

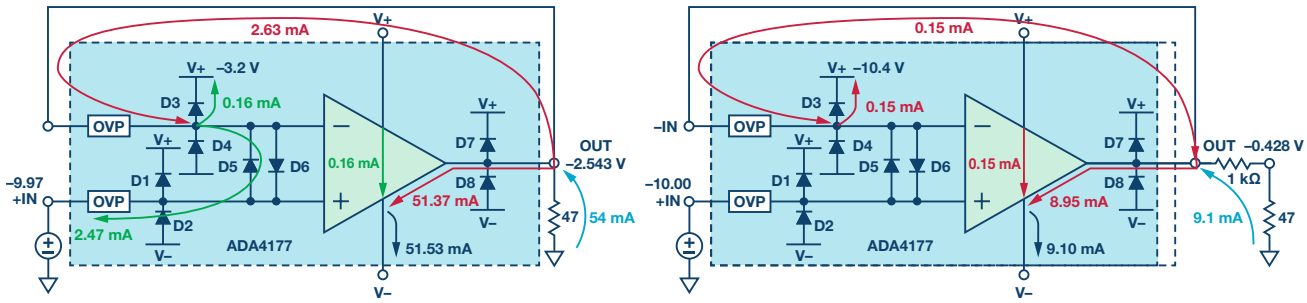

Figure 9. ADA4177 current path when V+ is absent (–10 V Input and 47 Ω output load).

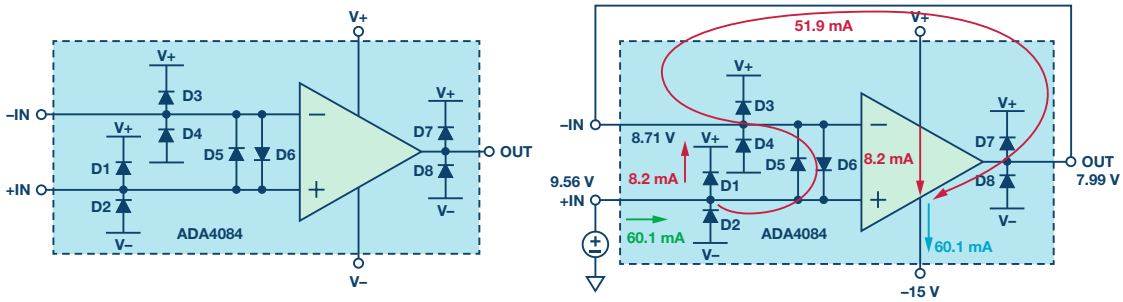

Figure 10. ADA4084 current path when V+ is absent (10 V input).

Table 8. ADA4177 with Load at Output Pin or Absent Power Pin

ADA4177-2	Condition	IN (V)	V+	V–	ISY+ (mA)	ISY– (mA)	IB+ (mA)	IOUT (mA)	OUT (V)
V+ absent	Vo or V+ is floating and negative input	–10.02	–12.33	– 15	0	4.31	4.18	–0.039	–12.32
	Vo 47 Ω to GND	–9.97	–3.218	– 15	0	51.53	–2.473	2.632	–2.543
	Vo 47 Ω to GND and 1 kΩ	– 10	–10.4	– 15	0	9.10	–0.003	0.147	–0.428

Table 9

ADA4084-2	Condition	V+	V–	I+ (mA)	I– (mA)	IB+ (mA)	IOUT (mA)	IN (V)	OUT (V)
	All power	15	–15	1.38	1.37	–0.001	–0.0001	10	9.98
	V+ absent and positive input	8.71	–15	0	60.1	60.102	–51.89	9.56	7.99

In system applications, different op amps, different topology (such as noninverting amplification, inverting amplification, and difference amplification), different load, and external connections can be implemented. If one power supply is absent, the risks need to be evaluated. This article can provide guidance on setting up the evaluation circuit (Figure 2), how to analyze the current path, and evaluate the potential risks.

Summary

To avoid overvoltage or latch-up situations, operational amplifier power supplies must be established simultaneously. General guidelines are:

- During the Power On sequence, turn on the supply first, then apply a signal at the input
- During the Power Off, turn off the input signal first, then turn off the power supply

In real-world applications, these guidelines may be difficult to adhere to. This can cause problems, especially when there is an input signal, and designers need to properly evaluate the risk. An effective solution is try to limit the input current of the op amp so it is within the spec in the data sheet. Adding a current-limiting resistor at the input and output can help in applications where power can't be supplied at the same time.

We tested three ADI op amps in a power supply absent application (ADA4084-2, ADA4077-2, and ADA4177-2). When integrated with internal resistors, the ADA4077-2 proved to be very robust. The ADA4177, when integrated with an OVP circuit, delivered the best robustness. In applications where the power may be absent, and external current-limiting resistors can't be added, the ADA4177 is recommended to avoid degrading the precision.

References

ADA4077. Analog Devices, Inc.

ADA4177. Analog Devices, Inc.

Arkin, Michael and Eric Modica. "Robust Amplifiers Provide Integrated Overvoltage Protection." *Analog Dialogue*, Volume 46, Number 1, 2012.

Blanchard, Paul and Brian Pelletier. "Using ESD Diodes as Voltage Clamps." *Analog Dialogue*, Volume 49, Number 10, 2015.

For more information on the ADA4177 and ADA4077, see the product pages and data sheets here: ADA4177 and ADA4077.

David Guo [david.guo@analog.com] is a product applications engineer for ADI's linear products. He started working in the China Central Application Center of ADI as an applications engineer in 2007 and transferred to the Precision Amplifier Group as an applications engineer in June, 2011. Since January 2013, David has worked as an application engineer in ADI's Linear Product Department, where he is responsible for the technical support of products including precision amplifiers, instrumentation amplifiers, high speed amplifiers, current sense amplifiers, multipliers, references, and rms-to-dc products. David earned his bachelor's and master's degree in mechano-electronic engineering from Beijing Institute of Technology.

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