

Successive-Approximation ADCs: Ensuring a Valid First Conversion

By Steven Xie

Introduction

Successive-approximation analog-to-digital converters (ADCs) with up to 18-bit resolution and 10-MSPS sample rates meet the demands of many data-acquisition applications, including portable, industrial, medical, and communications. This article shows how to initialize a successive-approximation ADC to get valid conversions.

Successive-Approximation Architecture

Successive-approximation ADCs comprise four main subcircuits: the sample-and-hold amplifier (SHA), analog comparator, reference digital-to-analog converter (DAC), and successive-approximation register (SAR). Because the SAR controls the converter's operation, successive-approximation converters are often called SAR ADCs.

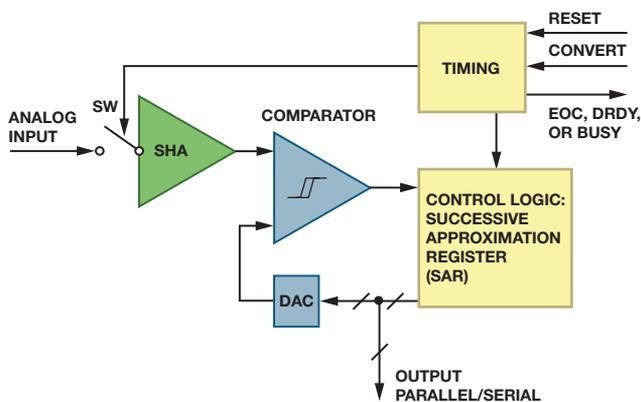


Figure 1. Basic SAR ADC architecture.

After power-up and initialization, a signal on CONVERT starts the conversion cycle. The switch closes, connecting the analog input to the SHA, which acquires the input voltage. When the switch opens, the comparator determines whether the analog input, which is now stored on the hold capacitor, is greater than or less than the DAC voltage. To start, the most significant bit (MSB) is on, setting the DAC output voltage to midscale. After the comparator output has settled, the successive-approximation register turns off the MSB if the DAC output was larger than the analog input, or keeps it on if the output was smaller. The process repeats with the next most significant bit, turning it off if the comparator determines that the DAC output is larger than the analog input, or keeping it on if the output was smaller. This binary search continues until every bit in the register is tested. The resulting DAC input is a digital approximation of the sampled input voltage, and is output by the ADC at the end of the conversion.

Factors Related To SAR Conversion Code

This article discusses the following factors as they relate to valid first conversions:

- Power Supply Sequence (AD765x-1)
- Access Control (AD7367)
- RESET (AD765x-1/AD7606)

- REF_{IN}/REF_{OUT} (AD765x-1)
- Analog Input Settling Time (AD7606)
- Analog Input Range (AD7960)
- Power-Down/Standby Mode (AD760x)
- Latency Delay (AD7682/AD7689, AD7766/AD7767)
- Digital Interfacing Timing

Power Supply Sequencing

Some ADCs that operate with multiple supplies have well-defined power-up sequences. The AN-932 Application Note, [Power Supply Sequencing](#), provides a good reference for designing power supplies for these ADCs. Special attention should be paid to the analog and reference inputs, as these typically should not exceed the analog supply voltage by more than 0.3 V. Thus, $AGND - 0.3 V < V_{IN} < V_{DD} + 0.3 V$ and $AGND - 0.3 V < V_{REF} < V_{DD} + 0.3 V$. The analog supplies should be turned on before the analog input or reference voltage, or the analog core could power up in a latched-up state. In a similar fashion, the digital inputs should be between $DGND - 0.3 V$ and $V_{IO} + 0.3 V$. The I/O supply must be turned on before (or at the same time as) the interface circuitry, or ESD diodes on these pins could become forward-biased and power up the digital core in an unknown state.

Data Access During Power Supply Ramp

Do not access the ADC before the power supplies are stable, as this may put it into an unknown state. Figure 2 shows an example where the host FPGA is trying to read data from an AD7367 while DV_{CC} is ramping up, which may put the ADC into an unknown state.

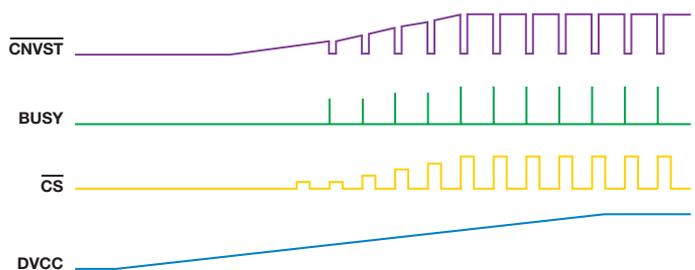


Figure 2. Reading data during DV_{CC} ramp-up.

SAR ADC Initialization with Reset

Many SAR ADCs, such as the AD760x and the AD765x-1, require a RESET for initialization after power-up. After all power supplies are stable, a specified RESET pulse should be applied to guarantee that the ADC starts in the intended state, with digital logic control in the default state and the conversion data register cleared. Upon power up, voltage starts to build up on the REF_{IN}/REF_{OUT} pin, the ADC is put into acquisition mode, and the user-specified mode is configured. Once fully powered up, the AD760x should see a rising edge RESET to configure it for normal operation. The RESET high pulse should typically be 50 ns wide.

Establishing the Reference Voltage

The ADC converts the analog input voltage to a digital code referred to the reference voltage, so the reference voltage must be stable before the first conversion. Many SAR ADCs have a REF_{IN}/REF_{OUT} pin and a REF or REFCAP pin. An external reference can overdrive the internal reference via the REF_{IN}/REF_{OUT} pin or the internal reference can drive the buffer

directly. A capacitor on the REFCAP pin decouples the internal buffer output, which is the reference voltage used for conversion. Figure 3 shows a reference circuit example from the AD765x-1 data sheet.

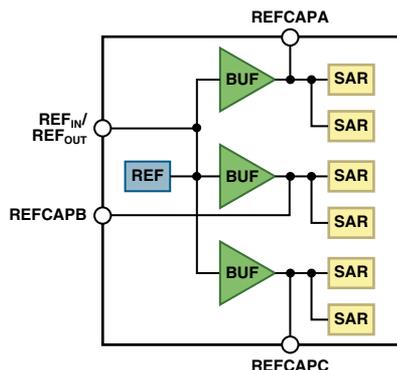


Figure 3. AD765x-1 reference circuit.

Make sure that the voltage on REF or REFCAP has settled before the first conversion. The slew rate and settling time varies for different reservoir capacitors, as shown in Figure 4.

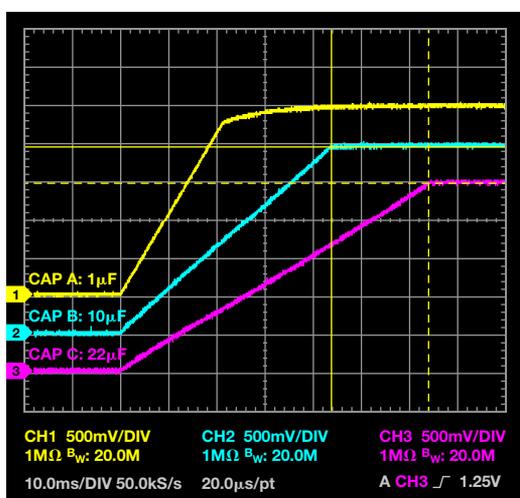


Figure 4. Voltage ramp on AD7656-1 REFCAPA/B/C pins with different capacitors.

In addition, a poorly designed reference circuit can cause serious conversion errors. The most common manifestation of a reference problem is “stuck” codes, which may be caused by the size and placement of the reservoir capacitor, insufficient drive strength, or a large amount of noise on the input. [Voltage Reference Design for Precision Successive-Approximation ADCs](#) by Alan Walsh (*Analog Dialogue* Volume 47, Number 2, 2013) provides details regarding reference design for SAR ADCs.

Analog Input Settling Time

For multichannel, multiplexed applications, the driver amplifier and the ADC’s analog input circuitry must settle to the 16-bit level (0.00076%) for a full-scale step on the internal capacitor array. Unfortunately, amplifier data sheets typically specify settling to a 0.1% or 0.01% level. The specified settling time could differ significantly from the settling time at a 16-bit level, so verification is required prior to driver selection.

Pay special attention to settling time in multiplexed applications. After the multiplexer switches, make sure to allow enough time for the analog input to settle to the specified accuracy before the conversion starts. When using the [AD7606](#) with a multiplexer, allow at least 80 μ s for the ± 10 -V input range and 88 μ s for the

± 5 -V range to give the selected channel enough time to settle to 16-bit resolution. [Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter](#) by Alan Walsh (*Analog Dialogue* Volume 46, Number 4, 2012) provides additional details regarding amplifier selection.

Analog Input Range

Make sure the analog input is within the specified input range, taking special care of differential input ranges with a specified common-mode voltage, as shown in Figure 5.

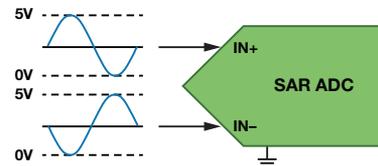


Figure 5. Fully differential input with common-mode voltage.

For example, the [AD7960](#) 18-bit, 5-MSPS SAR ADC’s differential input range is $-V_{REF}$ to $+V_{REF}$, but both V_{IN+} and V_{IN-} referred to ground should be in the -0.1 V to $V_{REF} + 0.1$ V range, and the common-mode voltage should be around $V_{REF}/2$, as shown in Table 1.

Table 1. Analog Input Specifications for the AD7960

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to GND	-0.1		$V_{REF} + 0.1$	V
Common-Mode Input Range		$V_{REF}/2 - 0.05$	$V_{REF}/2$	$V_{REF}/2 + 0.05$	V

Bringing the SAR ADC Out of Power-Down or Standby Mode

To conserve power, some SAR ADCs go into power-down or standby mode when they are idle. Make sure that the ADC comes out of this low-power mode before the first conversion starts. For example, the AD7606 family offers two power-saving modes: full shutdown and standby. These modes are controlled by GPIO pins STBY and RANGE.

Figure 6 shows that when \overline{STBY} and RANGE return high, the AD7606 goes from full shutdown mode into normal mode and is configured for the ± 10 -V range. At this point, the REGCAPA, REGCAPB, and REGCAP pins power up to the correct voltages as outlined in the data sheet. When placed in standby mode, the power-up time is approximately 100 μ s, but it takes approximately 13 ms in external reference mode. When powered up from shutdown mode, a RESET signal must be applied after the required power-up time has elapsed. The data sheet specifies the time required between power-up and a rising edge on RESET as $t_{WAKE-UP SHUTDOWN}$.

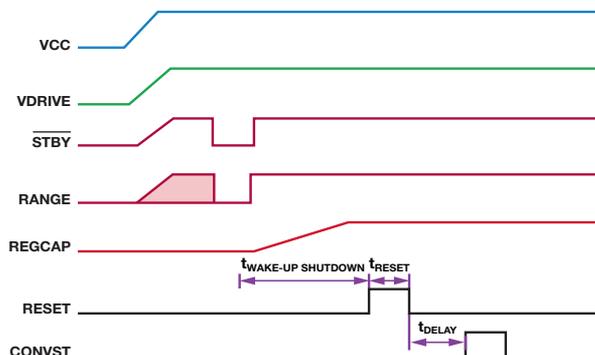


Figure 6. AD7606 initialization timing.

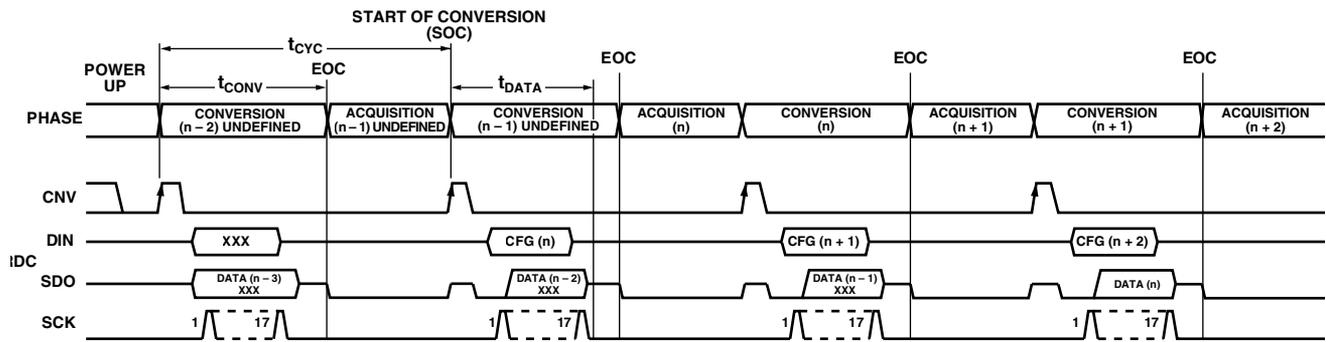


Figure 7. General timing for AD7682/AD7689.

SAR ADCs with Latency Delay

A common belief is that SAR ADCs have no latency delay, but some SAR ADCs have a latency delay for configuration updates, so the first valid conversion code may be undefined until the latency delay—which may be several conversion periods—has passed.

For example, the [AD7985](#) features two conversion modes of operation: turbo and normal. Turbo mode, which allows the fastest conversion rate of up to 2.5 MSPS, does not power down between conversions. The first conversion in turbo mode contains meaningless data, and should be ignored. In normal mode, on the other hand, the first conversion is meaningful.

For the [AD7682/AD7689](#), the first three conversion results after power-up are undefined, as a valid configuration does not take place until after the second EOC. Therefore, two dummy conversions are required, as shown in Figure 7.

When using the AD765x-1 in hardware mode, the logic state of the RANGE pin is sampled on the falling edge of the BUSY signal to determine the range for the next simultaneous conversion. After a valid RESET pulse, the AD765x-1 defaults to operating in the $\pm 4 \times V_{REF}$ range, with no latency problem. If, however, the AD765x-1 operates in $\pm 2 \times V_{REF}$ range, one dummy conversion cycle must be used to select the range at the first falling edge of BUSY.

In addition, some SAR ADCs, such as the [AD7766/AD7767](#) oversampled SAR ADC, have postdigital filters that cause additional latency delay. When multiplexing analog inputs to this type of ADC, the host must wait the full digital filter settling time before a valid conversion result can be achieved; the channel can be switched after this settling time.

As shown in Table 2, the latency of the AD7766/AD7767 is 74 divided by the output data rate (74/ODR). When running at the maximum output data rate of 128 kHz, the AD7766/AD7767 allows a 1.729-kHz multiplexer switching rate.

Table 2. Digital Filter Latency of AD7766/AD7767

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Group Delay			37/ODR		μ s
Settling Time (Latency)	Complete settling		74/ODR		μ s

Digital Interfacing Timing

Last, but not least, the host can access the conversion results from SAR ADCs through some common interface options, such as parallel, parallel BYTE, IIC, SPI, and SPI in daisy-chain mode. To get valid conversion data, make sure to follow the digital interfacing timing specifications in the data sheet.

Conclusion

To get a first valid conversion code from SAR ADCs, please follow the recommendations discussed in this article. Other specific configuration support may be needed; consult the target SAR ADC data sheet or application note for initialization before the first conversion cycle starts.

References

- Kester, Walt. [Data Converter Support Circuits](#). Chapter 7, *Data Converter Handbook*.
- Kester, Walt. “Which ADC Architecture Is Right for Your Application?” *Analog Dialogue*, Volume 39, Number 2, 2005.
- Walsh, Alan. “Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter.” *Analog Dialogue*, Volume 46, Number 4, 2012.

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