Low-Noise, Gain-Selectable Amplifier

By Nathan Carter and Chilann Chan

Data acquisition, sensor signal conditioning, and other applications with input signals that vary over a wide range require gain-selectable amplifiers. Traditional gain-selectable amplifiers use switches in the feedback loop to connect resistors to the inverting input, but the switch resistance degrades the noise performance of the amplifier, adds significant capacitance on the inverting input, and contributes to nonlinear gain error. The additional noise and capacitance are especially bothersome when working with low-noise amplifiers, and the nonlinear gain error is problematic in precision applications.

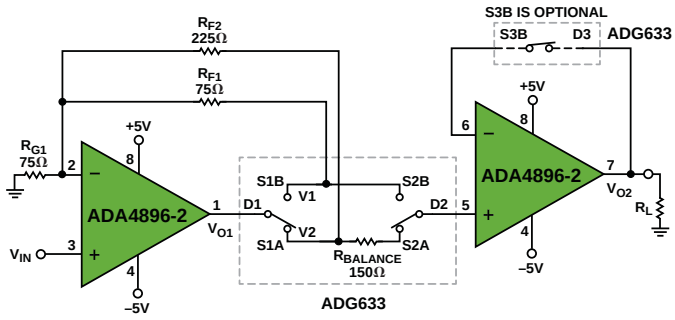

Figure 1. Using the ADA4896-2 and the ADG633 to construct a low-noise, gain-selectable amplifier to drive a low-resistance load.

The gain-selectable amplifier shown in Figure 1 uses an innovative switching technique that preserves the 1-nV/√Hz noise performance of the ADA4896-2 while reducing the nonlinear gain error. With this technique, the user can choose switches with minimal capacitance to maximize the bandwidth of the circuit.

The switches, implemented with an ADG633 triple SPDT CMOS switch, are configured such that either S1A and S2A are on, or S1B and S2B are on. Switch S1 connects to the output end of the feedback resistors, and Switch S2 samples at a point (V1 or V2) where the nonlinear switch resistance does not affect the gain. This reduces the gain error while preserving the noise performance. With the values shown, the first stage amplifier gain is 4 V/V when the "A" switches are on or 2 V/V when the "B" switches are on. The number of switched gains can be extended with additional switch packages or by using a multiplexer such as the 4:1 ADG659 or 8:1 ADG658.

Note that an offset is created by the input bias current of the output buffer flowing through the nonlinear on resistance of the S2 sampling switch. To compensate for this offset, place the unused switch (S3B) in the feedback path of the output buffer.

In addition, the bias current of the input amplifier causes a gain-dependent offset. Because the input amplifier and output buffer are built on the same chip, the relative matching of their bias currents can be used to cancel out the varying offset. Placing a resistor equal to the difference between R_{F2} and R_{F1}, in series with Switch S2A, results in less offset-voltage variation.

The following derivation shows that sampling at V1 yields the desired signal gain without gain error. R_S denotes the switch resistance. V2 can be derived using the same method.

$$V_{O1} = V_{IN} \times \left(1 + \frac{R_{F1} + R_{S1}}{R_{G1}}\right) \quad (1)$$

$$V_1 = V_{O1} \times \left(\frac{R_{F1} + R_{G1}}{R_{F1} + R_{G1} + R_{S1}}\right) \quad (2)$$

Substituting Equation 1 into Equation 2,

$$V_1 = V_{IN} \times \left(1 + \frac{R_{F1}}{R_{G1}}\right) \quad (3)$$

Note that if V_{O1} yields the desired signal gain without gain error, the buffered output, V_{O2}, will also be free from gain error. Figure 2 shows the normalized frequency response of the circuit at V_{O2}.

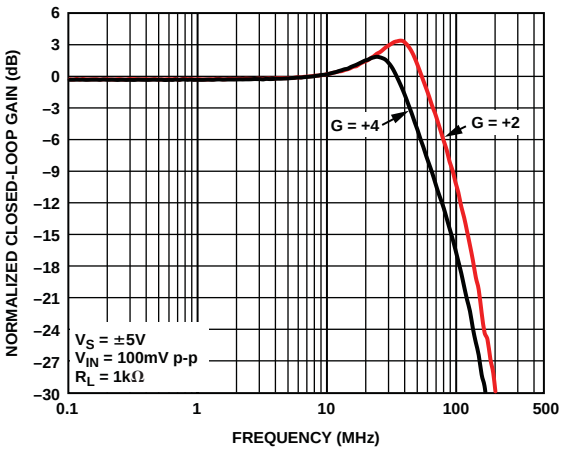

Figure 2. Frequency response of V_{O2}/V_{IN}.

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